Keysight D9021HDMC HDMI HEAC Compliance Application

KEYSIGHT

PROGRAMMER'S REFERENCE

Notices

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In This Book

This book is your guide to programming the Keysight Technologies D9021HDMC HDMI HEAC Compliance Application.

- Chapter 1, “Introduction to Programming,” starting on page 7, describes compliance application programming basics.
- Chapter 2, “Configuration Variables and Values,” starting on page 9, Chapter 3, “Test Names and IDs,” starting on page 39, and Chapter 4, “Instruments,” starting on page 71 provide information specific to programming the D9021HDMC HDMI HEAC Compliance Application.

How to Use This Book

Programmers who are new to compliance application programming should read all of the chapters in order. Programmers who are already familiar with this may review chapters 2, 3, and 4 for changes.

Contents

1 Introduction to Programming

Remote Programming Toolkit / 8

This chapter introduces the basics for remote programming a compliance/test application. The programming commands provide the means of remote control. Basic operations that you can do remotely with a computer and a compliance/test app running on an oscilloscope include:

- Launching and closing the application.
- Configuring the options.
- Running tests.
- Getting results.
- Controlling when and were dialogs get displayed
- Saving and loading projects.

You can accomplish other tasks by combining these functions.

Remote Programming Toolkit

The majority of remote interface features are common across all the Keysight Technologies, Inc. family of compliance/test applications. Information on those features is provided in the N5452A Compliance Application Remote Programming Toolkit available for download from Keysight here: www.keysight.com/find/rpi. The D9021HDMC HDMI HEAC Compliance Application uses Remote Interface Revision 7.2.20. The help files provided with the toolkit indicate which features are supported in this version.

In the toolkit, various documents refer to "application-specific configuration variables, test information, and instrument information". These are provided in Chapters 2, 3, and 4 of this document, and are also available directly from the application's user interface when the remote interface is enabled (View>Preferences::Remote tab::Show remote interface hints). See the toolkit for more information.

2 Configuration Variables and Values

The following table contains a description of each of the D9021HDMC HDMI HEAC Compliance Application options that you may query or set remotely using the appropriate remote interface method. The columns contain this information:

- GUI Location – Describes which graphical user interface tab contains the control used to change the value.
- Label – Describes which graphical user interface control is used to change the value.
- Variable – The name to use with the SetConfig method.
- Values – The values to use with the SetConfig method.
- Description – The purpose or function of the variable.

For example, if the graphical user interface contains this control on the **Set Up** tab:

- Enable Advanced Features

then you would expect to see something like this in the table below:

Table 1 Example Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Set Up	Enable Advanced Features	EnableAdvanced	True, False	Enables a set of optional features.

and you would set the variable remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SetConfig 'EnableAdvanced' 'True'"

C# syntax
```

```
---------
remoteAte.SetConfig("EnableAdvanced", "True");
```

Here are the actual configuration variables and values used by this application:

NOTE Some of the values presented in the table below may not be available in certain configurations. Always perform a "test run" of your remote script using the application's graphical user interface to ensure the combinations of values in your program are valid.

NOTE The file, "ConfigInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 2 Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Configure	# Data-Data Edges	NumEdgeSkew	(Accepts user-defined text), 1, 2, 3, 4, 5, 6, 7, 8, 9, 10	Specifies the number of edges to use when performing the Data Data Inter-Pair Skew measurements. Increasing # Edges will increase run time but will improve repeatability.
Configure	ARC Clock Frequency, Mhz	ARCFrequency	(Accepts user-defined text), 0, 4.096, 5.6448, 6.144	Specify the frequency for Audio Return Channel in Mhz.
Configure	ARC Clock Recovery Loop Bandwitdth, HZ	ARCCRLoopBandwidth	(Accepts user-defined text), 700, 1500, 3000	Specify the loop bandwith required to recover clock of ARC signals.
Configure	ARC Jitter Length, ms	ARCJitterLength	(Accepts user-defined text), 1, 25, 100, 1000	Specify the minimum waveform length in miliseconds for ARC jitter measurements.
Configure	ARC Memory Depth	ARCMemoryDepth	(Accepts user-defined text), 10.00E+6, 8.00E+6, 2.05E+6, 1.025E+6, 524.288E+3, 262.144E+3, 32.768E+3	Define the memory depth for ARC tests.
Configure	ARC Rise/Fall Time Edges	ARCRiseFallEdges	(Accepts user-defined text), 1000, 500, 100	Specifies minimum number of edges required for transition time measurement of ARC signals.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	ARC Sample Rate, MSa/s	ARCSRate	(Accepts user-defined text), 1000, 500, 250, 200	Specify the sample rate for ARC Tests in MSa/s.
Configure	ARC Sampling Rate for Rise/FallTime, MSa/s	ARCRiseFallSamplingRate	(Accepts user-defined text), 1000, 5000, 10000, 20000	Specify the sampling rate required to measure rise/fall time.
Configure	Additional Guard Band Pattern	GuardBandpattern	(Accepts user-defined text), Auto, 1101010100, 0010101011	This field allows you to enter additional Guard Band pattern to search, besides the default pattern. You can only enter digit 0 and 1 here. It needs to be 10 bits. 6 of these bits must consist of alternating 1s and 0s .The application use the default pattern only when None is selected. If you have more than one pattern to enter use ',' to separate them (example 0101010100,1010101011).
Configure	Additional Sync Pattern	pattern	(Accepts user-defined text), Auto, 1101010100, 0010101011	This field allows you to enter additional pattern to search, besides the default pattern. You can only enter digit 0 and 1 here. It needs to be 10 bits. 6 of these bits must consist of alternating 1s and 0s .The application use the default pattern only when None is selected. If you have more than one pattern to enter use ',' to separate them (example 0101010100,1010101011).
Configure	Allow TP2 eye tests with skew for differential probing	AllowTP2EyeDiff	true, false	Specify whether to allow TP2 eye tests with skew when user chooses differential probing configuration. Note this is not allowed for compliance testing which is why it is under Debug status.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Cable Eye Measurement Setup Steps	SkipCableEyeSteps	false, true	Allows user to skip steps that perform signal autoscale, mask loading etc and go straight to mask test. User must perform a full mask test at least once in order to skip steps in subsequent runs.
Configure	Cable Test Acquisition Points (Eye)	AcqPointCable	(Accepts user-defined text), 1000000, 8000000, 10000000, 16000000	Specifies the number of accumulate points to measure in the data eye pattern test. Note that increasing the number of points has a negative impact on the run time of the data eye pattern tests and peak-to-peak jitter.
Configure	Cable Test Mask Movement	MovementTypeCable	FINDPASS, FIXED, FINDMARGIN, FINDHORIZMARGIN, MANUAL	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs. (2) Fixed Mask will not be moving, it only report Pass or Fail upon test. (3) Find Margin will search +/-0.5 UI horizontally and vertically to find the maximum margin of non-violation mask. (4) Find Horizontal Margin only will search +/-0.5 UI horizontally to find the maximum margin of non-violation mask. (5) Manual mode will allow the user to move the mask manually during the eye test.
Configure	Cable Test Mask Rev	MaskRevCable	RevB, RevA	Select revision of mask to test with the eye. Rev-A is used for HDMI CTS 1.2. Rev-B is used for HDMI CTS 1.3 (Cable Test)
Configure	Cable Test Mask Type	MaskFileCable	HDMI-TP2.msk, HDMI-TP3.msk, HDMI-TP5.msk	Select type of mask to use in Eye Test.(Cable Test)

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Cable/Receiver Test Equalize Mode	EqCable	manual, IR_Seq_typeE_02_225, IR_Seq_typeE_05_225, IR_Seq_typeE_10_225, IR_EQ_2.3_742.5M, off	Specify the equalizer mode to use.(Cable Test)
Configure	Check Diff Probe	CheckDiffProbe	True, False	Turn off check on differential probing. For Debug purpose.
Configure	Check Measured TMDS character rate	CheckTMDSRate	true, false	Checks that the TMDS character rate measured is close to the TMDS character rate entered in Device Definition. Will raise a warning to user if measured TMDS character rate has high mismatch.
Configure	Clock Check Max Std. Deviation (Mhz)	ClockCheckMaxStdDv	(Accepts user-defined text), 4.0, 2.0, 1.0	Set the maximum standard deviation tolerance for clock signal verification
Configure	Clock Duty Cycle Edges	NumEdgeClockDutyCycle	(Accepts user-defined text), 400, 1000, 10000	Specifies the number of edges to use when performing the Clock Duty Cycle measurements. Increasing # Edges will increase run time but will improve repeatability.
Configure	Clock Jitter Acquisition Points	NumEgdeJitter	(Accepts user-defined text), 5000000, 10000000, 16000000	Specifies the number of accumulate points to use when performing the Clock Jitter measurements. Increasing # points will increase run time but will improve repeatability.
Configure	Clock Jitter Histogram Std Dev Multiplier	ClockJitterStdDevMultiplier	1, 2, 3, 4, 5, 6, 7, 8, 9, 10	If method '2' is chosen to calculate total clock jitter, select multiplier to multiply histogram std dev.
Configure	Clock Jitter Measurement Setup Steps	SkipJitterSteps	false, true	Allows user to skip steps that perform signal autoscale and go straight to clock jitter test. User must perform a full clock jitter test at least once in order to skip steps in subsequent runs.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Clock Jitter Multiplier	ClkJitterMultiplier	AUTO, 1, 5	Determines the type of multiplier method used in recover clock for clock rates < 55MHz.
Configure	Clock Jitter Multplier (Cable)	ClkJitterMultiplierCable	AUTO, 1, 5, EDGE	Determines the type of multiplier method used in recover clock.(Cable Test)
Configure	Clock Jitter Multplier (Receiver)	ClkJitterMultiplierReceiver	AUTO, 1, 5, EDGE	Determines the type of multiplier method used in recover clock.(Receiver Test)
Configure	Clock Multiplier	ClkMultiplier	Auto, 10, 40	Select clock multiplier to use.
Configure	Clock frequency measurement method	ClockFreqMethod	MODE, MEAN	Choose whether to use the histogram mode value or mean value when measuring clock frequency.
Configure	Clock frequency measurement method	ClockFreqMethod	MODE, MEAN	Choose whether to use the histogram mode value or mean value when measuring clock frequency.
Configure	Consider all edges for FRL Inter-pair Skew	FRLInterPairAllEdges	All, FirstSSB	Select whether to detect SSB occurrences throughout the entire acquisition and use the mean value for pass/fail criteria or just just first detected SSB edge for pass/fail criteria .
Configure	D+ Channel	CableDataP	CHAN1, CHAN2, CHAN3, CHAN4	Identifies the oscilloscope channel that is probing +ve Intra-Pair Data Lane.
Configure	D- Channel	CableDataN	CHAN1, CHAN2, CHAN3, CHAN4	Identifies the oscilloscope channel that is probing -ve Intra-Pair Data Lane.
Configure	DFE Equalization Location	FRLDFELocation	Equalize in place, Display as function	Select whether to equalize in-place or display as function.
Configure	DUT supports clock rates > 165MHz	SupportHighRates	true, false	Specifies whether the DUT supports clock rates > 165MHz. Lower limit for test ID 7-2 will be set to 2.7V if DUT does not support clock rates > 165MHz. Otherwise the VL lower limit will be set to 2.6V.
Configure	Data Lane A	RptDataLane1	D0, D1, D2	Identifies the target data lane for measurement and reporting.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Data Lane A Channel	Data1Cable	CHAN1, CHAN2, CHAN3, CHAN4	Identifies the oscilloscope channel that is probing Data Lane A.(2 Channels Connection Model)
Configure	Data Lane B	RptDataLane2	D0, D1, D2	Identifies the target data lane for measurement and reporting. This field is used for Inter-Pair Skew - Data Lane A/Data Lane B only.
Configure	Data Lane B Channel	Data2Cable	CHAN1, CHAN2, CHAN3, CHAN4	Identifies the oscilloscope channel that is probing Data Lane B.(2 Channels Connection Model)
Configure	Data Rate For Clock Recovery	DataRateForClkRecovery	(Accepts user-defined text), 3400000000	Sets the custom data rate for clock recovery. This value will only be used when "Enabled Data Rate For Clock Recovery" option is set to true.
Configure	Data rate measurement method	DataRateMeasMethod	1, 2	Choose the method to measure the data rate of the signal. For method 1, data rate is measured using ":MEASure:DATarate" with histogram turned on. The mode of the histogram is taken as the measured data rate. For method 2, data rate is measured using ":MEASure:CDRRATE". The clock recovery used in method 2 is "Constant Frequency, Semi-Automatic" where the nominal data rate is taken from the TMDS character rate set in the "Device Definition Setup" dialog. This method works better for signals with lots of ISI.
Configure	Decode Signal Batch Size	DecodeBatSize	(Accepts user-defined text), 50.00E+6, 40.00E+6, 30.00E+6, 20.00E+6, 10.00E+6, 5.00E+6	Define the memory depth for Inter Pair Skew tests. For method 2 only.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Decode Signal Memory Depth	DecodePairMemDepth	(Accepts user-defined text), 10.00E+6, 50.00E+6, 100E+6, 150E+6, 200E+6, 500E+6	Define the memory depth for Inter Pair Skew tests. For method 2 only.
Configure	Delay Lane 0	DelayTimeD0	(Accepts user-defined text), 0, 5e-12, 10e-12, 15e-12, 20e-12, 25e-12, 30e-12, 35e-12, 40e-12, -5e-12, -10e-12, -15e-12, -20e-12, -25e-12, -30e-12, -35e-12, -40e-12	Delay the signal on lane 0.
Configure	Delay Lane 1	DelayTimeD1	(Accepts user-defined text), 0, 5e-12, 10e-12, 15e-12, 20e-12, 25e-12, 30e-12, 35e-12, 40e-12, -5e-12, -10e-12, -15e-12, -20e-12, -25e-12, -30e-12, -35e-12, -40e-12	Delay the signal on lane 1.
Configure	Delay Lane 2	DelayTimeD2	(Accepts user-defined text), 0, 5e-12, 10e-12, 15e-12, 20e-12, 25e-12, 30e-12, 35e-12, 40e-12, -5e-12, -10e-12, -15e-12, -20e-12, -25e-12, -30e-12, -35e-12, -40e-12	Delay the signal on lane 2.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Delay Lane 3	DelayTimeD3	(Accepts user-defined text), 0, 5e-12, 10e-12, 15e-12, 20e-12, 25e-12, 30e-12, 35e-12, 40e-12, -5e-12, -10e-12, -15e-12, -20e-12, -25e-12, -30e-12, -35e-12, -40e-12	Delay the signal on lane 3.
Configure	Enabled Data Rate For Clock Recovery	EnabledDataRateForClkRecovery	true, false	Enable or disable custom data rate for clock recovery. Please set the data rate in the "Data Rate For Clock Recovery" option.
Configure	Enhanced Bandwidth	bwreduction	AUTO, 4E9, 6E9, 8E9, 12E9, 13E9, 14E9, 15E9, 16E9, 17E9, 18E9, 19E9, 20E9, 21E9, 22E9, 23E9, 24E9, 25E9, 26E9, 27E9, 28E9, 29E9, 30E9, 31E9, 32E9	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available with Enhance Bandwidth or Noise Reduction options.
Configure	External Triggering	EXTTRIGGER	NO, CHAN4, AUX	Specify if to use trigger from ParBERT.(Receiver Test)
Configure	External Triggering	EXTTRIGGERCable	NO, CHAN4, AUX	Specify if to use trigger from ParBERT.(Cable Test)
Configure	Eye Diagram Acquisition Points	AcqPoint	(Accepts user-defined text), 1000000, 10000000, 16000000, 100000000	Specifies the number of accumulate points to measure in the data eye pattern test. Note that increasing the number of points has a negative impact on the run time of the data eye pattern tests and peak-to-peak jitter.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Eye Diagram Mask Movement	MovementType	FINDPASS, FIXED, FINDMARGIN, FINDHORIZMARGIN, MANUAL	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs. (2) Fixed Mask will not be moving, it only report Pass or Fail upon test. (3) Find Margin will search +/-0.5 UI horizontally and vertically to find the maximum margin of non-violation mask. (4) Find Horizontal Margin only will search +/-0.5 UI horizontally to find the maximum margin of non-violation mask. (5) Manual mode will allow the user to move the mask manually during the eye test.
Configure	Eye Height Measurement Location	EyeHeightLocation	CenterEye, EntireEye	Select whether to measure eye height on center of eye or the entire eye. When measuring eye height on entire eye, the largest eye opening accross the entire eye is reported. This is mostly useful when the eye is not symmetrical. When measuring eye height at center of eye, the eye height opening reported is at the center of the eye only. This is mostly used for a symmetrical eye.
Configure	Eye Measurement Setup Steps	SkipEyeSteps	false, true	Allows user to skip steps that perform signal autoscale, mask loading etc and go straight to mask test. User must perform a full mask test at least once in order to skip steps in subsequent runs.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	FRL AC Common Mode Bandwidth Limit	FRLACCommonModeBWLimit	HalfDataRate, 1.5E9, 2E9, 4E9, 6E9, 8E9, 12E9, 13E9, 14E9, 15E9, 16E9, 17E9, 18E9, 19E9, 20E9, 21E9, 22E9, 23E9, 24E9, 25E9, 26E9, 27E9, 28E9, 29E9, 30E9, 31E9, 32E9	Specifies the low pass filter cut-off frequency to be applied for AC common mode test.
Configure	FRL Enhanced Bandwidth	FRLBWLimit	AUTO, 4E9, 6E9, 8E9, 12E9, 13E9, 14E9, 15E9, 16E9, 17E9, 18E9, 19E9, 20E9, 21E9, 22E9, 23E9, 24E9, 25E9, 26E9, 27E9, 28E9, 29E9, 30E9, 31E9, 32E9	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available with Enhance Bandwidth or Noise Reduction options.
Configure	FRL FFE Test Method	FFEMethod	1, 2	Select whether to use method 1 or method 2 for FRL FFE tests as described by the FRL test specification.
Configure	FRL InterPair Skew Sample Rate	FRLInterPairSampleRate	40.0E+9, 64.0E+9	Specifies the sample rate of the oscilloscope for FRL tests.
Configure	FRL Interpair Skew Target	InterpairSkewTarget	Tx, Cable	Choose between TX and Cable threshold levels for the test pass/fail criteria.
Configure	FRL Sample Rate	FRLSampleRate	80.0E+9, 40.0E+9, 128.0E+9, 64.0E+9	Specifies the sample rate of the oscilloscope for FRL tests.
Configure	Force non-tested lane to go quiet.	FRLForceNonTestedLanesQuiet	Yes, No	Whether to prompt user to force other lanes to transmit LTP2 (or go quiet) when waveform is being captured for one lane.
Configure	HEAC Single-Ended Lane+	HEACSingleEndedLanePlus	CHAN1, CHAN2, CHAN3, CHAN4	Define scope channel for HEC differential lane.
Configure	HEAC Single-Ended Lane-	HEACSingleEndedLaneMinus	CHAN1, CHAN2, CHAN3, CHAN4	Define scope channel for HEC differential lane.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	HEC Base Center Margin	HECBaseCenterMargin	(Accepts user-defined text), 15, 15	Specifies the maximum margin allowed to estimate of position base/center voltage in percentage to peak-to-peak voltage ratio .
Configure	HEC Clock Recovery Loop Bandwidth, Khz	HECLoopBandwitdh	(Accepts user-defined text), 75, 1000	Specify loop bandwith for clock recovery.
Configure	HEC Cycle Time Count	HECCycleTimeUI	(Accepts user-defined text), 10, 100, 1000	Specifies the number of measurements taken for cycle time tests.
Configure	HEC Differential Lane	HECDifferentialLane	CHAN1, CHAN2, CHAN3, CHAN4	Define scope channel for HEC differential lane.
Configure	HEC Eye Diagram Minimum UI	HECEyeMinUI	(Accepts user-defined text), 4000, 100000, 500000, 1000000	Specifies the number of accumulate points to measure in the data eye pattern test for HEC eye diagram test. Note that increasing the number of points has a negative impact on the run time of the data eye pattern tests and peak-to-peak jitter.
Configure	HEC Jitter Cross Line	HECJitterCrossLine	(Accepts user-defined text), Auto, Manual	Auto/Manual setting of the cross line of HEC jitter test.
Configure	HEC Level Measurements Count	HECLevelMeasurementCount	(Accepts user-defined text), 1, 10, 50, 100	Specifies number of measurement to be taken for High, Center and Low Level Test.
Configure	HEC Memory Depth	HECMemoryDepth	(Accepts user-defined text), 2.05E+6, 1.025E+6, 524.288E+3, 262.144E+3, 32.768E+3	Define the memory depth for HEC tests.
Configure	HEC Operating Voltage Count	HECOperatingVoltageCount	(Accepts user-defined text), 100, 50, 10	Specifies the number of measurements taken for operating voltage test.
Configure	HEC Rise/Fall Time Edges	HECRiseFallEdges	(Accepts user-defined text), 10, 50, 100	Specifies minimum number of edges required for transition time measurement .

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	HEC Sample Rate, GSa/s	HECSRate	(Accepts user-defined text), 40, 20, 10, 5	(Limited availability*) Specify the sample rate for HEC Differential Tests in GSa/s.
Configure	HEC Top Center Margin	HECTopCenterMargin	(Accepts user-defined text), 15, 15	Specifies the maximum margin allowed to estimate of position top/center voltage in percentage to peak-to-peak voltage ratio.
Configure	HEC Trigger Duration, UI	HECTriggerDuration	(Accepts user-defined text), 9, 10, 11, 12	Specifies the minimum duration for stable signals for High, Center and Low Level Test.
Configure	HEC Window Trigger Method	HECWindowTriggerMethod	Hardware, Software	Define window trigger method for high, level and center level test. Hardware method improves speed performance but might not be fully supported in some scopes.
Configure	Heart beat Trigger Level	eARCHeartBeatTriggerLevel	(Accepts user-defined text), 4.15, 0	Specify trigger level for eARC heartbeat.
Configure	Hide Informative Tests	HideInformativeTests	1.0, 0.0	Hides or shows informative test
Configure	Hysteresis(+-mV)	CableMeasHys	(Accepts user-defined text), 10	Sets the threashold hysteresis.(Cable Test)
Configure	InfiniiSim Bandwidth	FRLInfiniiSimBandwidth	12E9, 13E9, 14E9, 15E9, 16E9, 17E9, 18E9, 19E9, 20E9, 21E9, 22E9, 23E9, 24E9, 25E9, 26E9, 27E9, 28E9, 29E9, 30E9, 31E9, 32E9	Specify bandwidth to set for cable model application.
Configure	InfiniiSim Time Span (Crosstalk)	FRLInfiniiSimTimeSpanCrosstalk	1e-9, 5e-9, 10e-9, 20e-9, 30e-9, 40e-9, 50e-9	Specify time span to set for cable model application.
Configure	InfiniiSim Time Span (Insertion Loss)	FRLInfiniiSimTimeSpanInsertionLoss	1e-9, 5e-9, 10e-9, 20e-9, 30e-9, 40e-9, 50e-9	Specify time span to set for cable model application.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Inter-Pair Measurement Trigger Wait (ms)	InterPairTriggerWait	(Accepts user-defined text), 3000, 5000, 7000, 10000, 30000, 50000, 70000, 100000, 150000, 200000, 300000, 500000	Defines wait time for inter-pair trigger.
Configure	Inter-Pair Skew Method HDMI 1.4	InterpairMethod14	1, 2	Choose the method to measure inter-pair skew. For method 1, InfiniiScan is used to trigger on required pattern. For method 2, a large acquisition will be captured, then the required SYNC patterns will be searched throughout captured pattern.
Configure	Inter-Pair Skew Method HDMI 2.0	InterpairMethod	1, 2	Choose the method to measure inter-pair skew. For method 1, InfiniiScan is used to trigger on required pattern. For method 2, a large acquisition will be captured, then the required SYNC patterns will be searched throughout captured pattern.
Configure	Inter-Pair Skew Reference Channel	InterPairReferenceChannel	Clk, D2	Define the inter-pair skew reference channel when switch matrix is enabled.
Configure	Inter-pair Skew Batch Size	InterPairBatSize	(Accepts user-defined text), 20.00E+6, 10.00E+6, 5.00E+6	Define the memory depth for Inter Pair Skew tests. For method 2 only.
Configure	Inter-pair Skew Memory Depth	InterPairMemDepth	(Accepts user-defined text), 10.00E+6, 50.00E+6, 100E+6, 150E+6, 200E+6, 500E+6	Define the memory depth for Inter Pair Skew tests. For method 2 only.
Configure	InterPair Skew Trigger Length	TriggerLength	20, 10	This field allow user to select 10 bits or 20 bits trigger pattern for inter-pair skew test.
Configure	Intra-Pair Data Lane	CableIntraPairRptDataLane	D0, D1, D2	Identifies the target data lane for measurement and reporting.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Intra-Pair Skew Crossing Reference	IntraPairCrossingRef	LaneP, LaneN	Specifies the crossing-point reference for intra-pair skew test.
Configure	Intra-Pair Skew Edges	NumEdgeIntraSkew	(Accepts user-defined text), 100, 1000, 10000	Specifies the number of edges to use when performing the Intra-Pair Skew measurements. Increasing # Edges will increase run time but will improve repeatability.
Configure	Intra-Pair Skew Histogram Offset	IntraHistogramOffset	0, 1, 5, 10, 20, 30	Specifies the offset of Histogram threshold (in mV) for Skew measurement.
Configure	Intra-Pair Skew Interpolation	IntraPairInterpolation	OFF, ON	Enabling or Disabling Interpolation.
Configure	Log GPIB Commands	LogIO	true, false	Logs GPIB traffic into log directory.
Configure	Mask Type	MaskFile	HDMI-TP1.msk, HDMI-TP1.msk, HDMI-TP2.msk, HDMI-TP5.msk, HDMI-DP++.msk	Select type of mask to use in HDMI 1.4b Eye Test.
Configure	Maximum Tries	Maxtries	(Accepts user-defined text), 3, 5, 10, 50, 100	Specifies the maximum tries before timeout. This setting needed to be increase when testing at lower pixel rate. The is only applicable for Standard mode: Capture and analyze live waveform.
Configure	Measure FRL RJ at TP2	MeasureRJAtTP2	Yes, No	Select whether measure RJ at TP2 or TP1.
Configure	Measurement Threshold(V)	CableMeasThres	(Accepts user-defined text), 0	Sets the measurement threashold.(Cable Test)
Configure	Number of LookUp Bits for FRL Inter-pair Skew	FRLInterPairNumLookUpBits	1, 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30	Specify number of bits (front and back) to search for SSB pattern on second lane once SSB pattern is found on first lane.
Configure	Number of UIs to capture for FRL Eye Measurement.	FRLEyeMeasCaptureLength	500e3, 700e3, 1.0e6, 1.5e6, 1.7e6, 2e6	Specifies the low pass filter cut-off frequency to be applied for AC common mode test.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Number of UIs to capture for FRL RJ Measurement	FRLRJMeasCaptureLength	1e6, 2e6, 3e6, 4e6, 5e6, 6e6, 7e6, 8e6, 9e6, 10e6	Select the number of UIs to capture for FRL RJ measurement.
Configure	Number of waveforms to save	NumWaveformsToSave	1, 2, 3, 4, 5, 6	Specify number of waveforms to save for Capture and Process later mode.
Configure	Pattern Lane A	LaneAPatt	(Accepts user-defined text), Auto, 0010101011001010101011, 0010101010001010101010, 0010101011001010101011/0010101010001010101010, 0010101011001010101011/0010101010001010101010/1101010100110101010100	For HDMI 2.0 inter-pair skew only. Specify the pattern to use to trigger Lane A for method '1' or pattern to search for method '2'. If there are multiple patterns to try out, just use the '/' separator.
Configure	Pattern Lane B	LaneBPatt	(Accepts user-defined text), Auto, 0010101011001010101011, 0010101011001010101011/0010101010001010101010, 0010101011001010101011/0010101010001010101010/1101010100110101010100	For HDMI 2.0 inter-pair skew only. Specify the pattern to search for in Lane B. Once the oscilloscope triggers on Lane A, the software will search Lane B for specified pattern. If there are multiple patterns to try out, just use the '/' separator.
Configure	Perform pattern check.	PerformFRLPatternCheck	Yes, No	Specify whether to perform pattern checking during signal capture.
Configure	Pixel Clock(MHz)	CablePixClk	(Accepts user-defined text), 74.25, 340	Sets the pixel clock rate according to cable category.(Cable Test)
Configure	Probe Check	ProbeCheck	Enable, Disable	Enable or disable probe check.
Configure	RJDJ Bandwidth type	FRLRJDJBWType	NARROW, WIDE	Select BW type for RJDJ breakdown when measuring RJ.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	RJDJ RJ method	FRLRJDJMethod	SPECTRAL, BOTH	Select RJ method to use when measuring RJ.
Configure	Raw Clock Frequency	RawClockFreq	(Accepts user-defined text), auto, 222750000	Specify the raw clock frequency send by the transmitter.(Receiver Test)
Configure	Raw Clock Frequency	RawClockFreqCable	(Accepts user-defined text), auto, 222750000	Specify the raw clock frequency send by the transmitter.(Cable Test)
Configure	Receiver Eye Measurement Setup Steps	SkipReceiverEyeSteps	false, true	Allows user to skip steps that perform signal autoscale, mask loading etc and go straight to mask test. User must perform a full mask test at least once in order to skip steps in subsequent runs.
Configure	Receiver Test Acquisition Points (Eye)	AcqPointReceiver	(Accepts user-defined text), 1000000, 10000000, 16000000	Specifies the number of accumulate points to measure in the data eye pattern test. Note that increasing the number of points has a negative impact on the run time of the data eye pattern tests and peak-to-peak jitter.
Configure	Receiver Test Clock Channel	ClkChan	CHAN1, CHAN2, CHAN3, CHAN4	The scope channel used to probe transmitted clock from the DUT.(Receiver Test)
Configure	Receiver Test Data Channel	DataChan	CHAN1, CHAN2, CHAN3, CHAN4	The scope channel used to probe transmitted Data from the DUT.(Receiver Test)
Configure	Rise/fall time method	RiseFallMethod	1, 0	Specifies the method used when performing the Rise/Fall Time measurements for data lanes. 0 (default) will measure based on any edge. 1 will measure based on triggering on 0001/1110 edge.
Configure	Run All Selected Data Rate	RunAllSelDataRate	true, false	Run All Selected Data Rate.
Configure	Save waveforms for Inter-pair skew measurement	SaveInterPairWaveform	true, false	Saves the waveforms for both lanes for inter-pair skew measurement.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Set termination voltage for N5444A or N7010A probe head	EnableN5444Termination	True, False	If using N5444A or N7010A probe head, select whether to let the application set the 3.3V termination automatically. If set to "false", the application will not set the internal termination voltage.
Configure	Skip Connection PopUp	SkipConnectionPopUp	true, false	Turn On/Off Offline mode.
Configure	Store Detected Bits	StoreDetectedBits	No, Yes	Select whether to store detected bits for Lanes A and B. Bits will be stored in CSV format.
Configure	Termination Voltage	TerminationVoltage	(Accepts user-defined text), 3.3	Set termination voltage when infiniMax III probes are used.
Configure	Test Pattern for FRL Data Rate Measurement	FRLDataRateMeasurementPattern	LTP5, LTP3	Select test pattern to use for FRL Data Rate measurement.
Configure	Test Pattern for FRL Eye Measurement	FRLEyeMeasurementPattern	LTP5, LTP5AllLanes	Select test pattern to use for FRL Eye measurement.
Configure	Test Pattern for FRL Inter-pair skew Measurement	FRLInterPairSkewMeasurementPattern	LTP4, LTP5	Select test pattern to use for FRL Inter-Pair Skew measurement.
Configure	Test Pattern for FRL RJ Measurement	FRLRJMeasurementPattern	LTP5, LTP3	Select test pattern to use for FRL RJ measurement.
Configure	Test Pattern for FRL Transition Time Measurement	FRLTransitionTimeMeasurementPattern	LTP5, LTP4	Select test pattern to use for FRL transition time measurement.
Configure	Time Delay after TMDS VIC Configuration Setting (seconds)	DelayAfterVicSet	(Accepts user-defined text), 0, 5, 10, 30	When Timing Control Automation is enabled, this setting introduces a time delay (seconds) in between the TMDS VIC configuration set and start of test.
Configure	Time out duration (seconds)	TimeoutDuration	30000, 50000, 100000, 150000, 200000, 250000, 300000, 350000, 400000, 450000, 500000	Specify the time out duration in seconds to be used across all tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Total Clock Jitter Measurement Method	TotalClockJitterMethod	1, 2	Allows user to select method to determine total clock jitter. Method '1' uses histogram peak-peak reading as total clock jitter. Method '2' multiplies the histogram std dev by a factor to determine total clock jitter.
Configure	Transition Time Converter Mode	TTCCable	SWTTCAUTO, SWTTCOFF, SWTTCMANUAL, TTC1, TTC2, TTC3, TTC4, TTC5, TTC6	Specify the Transition Time Converter mode to use. TTC Auto will automatically select the desired filter based on the channel frequency; TTC Off will disable the feature; TTC Manual allow user to determine the equ file manually during the test; TTC Model 1 will select 1200ps rise time, it should be chosen for freq <= 27Mhz; TTC Model 2 will select 450ps rise time, it should be chosen for freq = 74.25Mhz; TTC Model 3 will select 220ps rise time, it should be chosen for Freq = 148.5Mhz; TTC Model 4 will select 200ps rise time, it should be chosen for freq = 165Mhz; TTC Model 5 will select 150ps rise time, it should be chosen for freq = 222.25Mhz;TTC Model 6 will select 60ps rise time, it should be chosen for Freq > 222.75Mhz.
Configure	Transmitter Sample Rate, GSa/s	TMDSSRate	40.0E+9, 20.0E+9, 64.0E+9, 32.0E+9	(Limited availability*) Specify the sample rate for Transmitter Tests in GSa/s.
Configure	Turn On Equalization for FRL Inter-pair Skew	FRLInterPairTurnOnEqualization	On, Off	Whether to turn on equalization for inter-pair skew test.
Configure	Turn off VTerm after probe offset calibration or when application exits	TurnOffVTermFinish	true, false	Specify whether to turn off VTerm for N7010A and N5444A probe heads after completing probe offset calibration or when user terminates the application.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Turn on DFE for 12G FRL eye measurement	FRLTurnOnDFEMeasurement	Yes, No	Select whether to turn on DFE for 12G FRL eye measurement.
Configure	Turn on Interpolation for FRL Inter-pair Skew	FRLInterPairTurnOnInterpolation	OFF, INT2, INT4	Whether to turn on interpolation for inter-pair skew test.
Configure	Turn on Interpolation for FRL Tests	FRLTurnOnInterpolation	OFF, INT2, INT4	Whether to turn on interpolation for FRL tests.
Configure	Use GBit Serial Trigger Mode	UseHWST	Yes, No	This only applies to DSOV 90000 series scope that has N2119AU hardware serial trigger accessory card installed. If this option is not detected the default method used for inter-pair skew measurement will follow the configuration selection of "Inter-Pair Skew Method HDMI 2.0". User may also choose to use the interpair-skew method in "Inter-Pair Skew Method HDMI 2.0" by choosing "No".
Configure	User Defined RJ RMS (ps)	FRLUserRJRMSMeasurement	(Accepts user-defined text), 0, 0.1, 1, 10	Enter user defined RJ RMS value in ps. This will overwrite measured RJ RMS value unless value is set to 0s.
Configure	VL Edges	NumEdgeVL	(Accepts user-defined text), 100, 1000, 10000	Specifies the number of edges to use when performing the VL measurements. Increasing # Edges will increase run time but will improve repeatability.
Configure	VL measurement method	VLMethod	1, 0	Specifies the method used when performing the VL measurements. 0 (default) will measure based on the any edge. 1 will measure based on triggering on 0001/1110 edge.
Configure	VSYNC Acquisition Points	VsyncAcqPoint	50.00E+6, 100.00E+6, 200.00E+6, 500.00E+6, 1.00E+9, 2.00E+9	Define the memory depth for HF1-87 tests only.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Vswing Measure	VSwingCount	(Accepts user-defined text), 50, 100, 500, 1000	Specifies the number of Edges to use when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves repeatability of the measurement.
Configure	Wait time to change FFE Level	FFELevelChangeWait	(Accepts user-defined text), 500, 1000, 2000, 5000	Specify wait time (in ms) after changing FFE Level with SCDC controller.
Configure	Wait time to change FFE Type	FFETypeChangeWait	(Accepts user-defined text), 500, 1000, 2000, 5000	Specify wait time (in ms) after changing FFE Type with SCDC controller.
Configure	Wait time to change data rate	DataRateChangeWait	(Accepts user-defined text), 1000, 2000, 5000	Specify wait time (in ms) after changing data rate with SCDC controller.
Configure	Wait time to change pattern	PatternChangeWait	(Accepts user-defined text), 1000, 2000, 5000	Specify wait time (in ms) after changing test pattern with SCDC controller.
Configure	eARC Termination Supply Voltage	eARCTerminationVoltage	(Accepts user-defined text), 4, 3.6, 4.4	Specify the eARC termination supply voltage.
Run Tests	Event	RunEvent	(None), Fail, Margin < N, Pass	Names of events that can be used with the StoreMode=Event or RunUntil RunEventAction options
Run Tests	RunEvent=Margin < N: Minimum required margin %	RunEvent_Margin < N_MinPercent	Any integer in range: 0 <= value <= 99	Specify N using the 'Minimum required margin %' control.
Set Up	10G	10G	0.0, 1.0	Select 10G data rate for FRL testing
Set Up	12G	12G	0.0, 1.0	Select 12G data rate for FRL testing
Set Up	3G	3G	0.0, 1.0	Select 3G data rate for FRL testing
Set Up	6G_3Lanes	6G_3Lanes	0.0, 1.0	Select 6G_3Lanes data rate for FRL testing

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	6G_4Lanes	6G_4Lanes	0.0, 1.0	Select 6G_4Lanes data rate for FRL testing
Set Up	8G	8G	0.0, 1.0	Select 8G data rate for FRL testing
Set Up	Add Waveform	AddWaveform	0.0, 1.0	Set to true to add waveform
Set Up	BtnAllTiming	BtnAllTiming	Check All, Uncheck All	Check/Uncheck all the selected video timing
Set Up	CableEmbedFile	CableEmbedFile	Reference Cable with skew, Reference Cable without skew, Other	Set the cable embed file for TMDS.
Set Up	CableEmbedShortD0D0Text	CableEmbedShortD0D0Text	(Accepts user-defined text)	D0D0 Cable embed s-parameter path
Set Up	CableEmbedShortD0D1Text	CableEmbedShortD0D1Text	(Accepts user-defined text)	D0D1 Cable embed s-parameter path
Set Up	CableEmbedShortD0D2Text	CableEmbedShortD0D2Text	(Accepts user-defined text)	D0D2 Cable embed s-parameter path
Set Up	CableEmbedShortD0D3Text	CableEmbedShortD0D3Text	(Accepts user-defined text)	D0D3 Cable embed s-parameter path
Set Up	CableEmbedShortD1D0Text	CableEmbedShortD1D0Text	(Accepts user-defined text)	D1D0 Cable embed s-parameter path
Set Up	CableEmbedShortD1D1Text	CableEmbedShortD1D1Text	(Accepts user-defined text)	D1D1 Cable embed s-parameter path
Set Up	CableEmbedShortD1D2Text	CableEmbedShortD1D2Text	(Accepts user-defined text)	D1D2 Cable embed s-parameter path
Set Up	CableEmbedShortD2D0Text	CableEmbedShortD2D0Text	(Accepts user-defined text)	D2D0 Cable embed s-parameter path
Set Up	CableEmbedShortD2D1Text	CableEmbedShortD2D1Text	(Accepts user-defined text)	D2D1 Cable embed s-parameter path
Set Up	CableEmbedShortD2D2Text	CableEmbedShortD2D2Text	(Accepts user-defined text)	D2D2 Cable embed s-parameter path
Set Up	CableEmbedShortD2D3Text	CableEmbedShortD2D3Text	(Accepts user-defined text)	D2D3 Cable embed s-parameter path
Set Up	CableEmbedShortD3D0Text	CableEmbedShortD3D0Text	(Accepts user-defined text)	D3D0 Cable embed s-parameter path
Set Up	CableEmbedShortD3D1Text	CableEmbedShortD3D1Text	(Accepts user-defined text)	D3D1 Cable embed s-parameter path

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	CableEmbedShortD3D2Text	CableEmbedShortD3D2Text	(Accepts user-defined text)	D3D2 Cable embed s-parameter path
Set Up	CableEmbedShortD3D3Text	CableEmbedShortD3D3Text	(Accepts user-defined text)	D3D3 Cable embed s-parameter path
Set Up	CableEmbedText	CableEmbed	(Accepts user-defined text)	Cable embed s-parameter file path for TMDS.
Set Up	CableEmbedType21	CableEmbedType21	Worst, Short	Set the cable embed type for FRL.
Set Up	ConnectionChoice	ConnectionChoice	2 Probes, 4 Probes	ConnectionChoice
Set Up	D0+ Waveform Path	D0PWaveform	(Accepts user-defined text)	D0+ Waveform Path
Set Up	D0- Waveform Path	D0NWaveform	(Accepts user-defined text)	D0- Waveform Path
Set Up	D1+ Waveform Path	D1PWaveform	(Accepts user-defined text)	D1+ Waveform Path
Set Up	D1- Waveform Path	D1NWaveform	(Accepts user-defined text)	D1- Waveform Path
Set Up	D2+ Waveform Path	D2PWaveform	(Accepts user-defined text)	D2+ Waveform Path
Set Up	D2- Waveform Path	D2NWaveform	(Accepts user-defined text)	D2- Waveform Path
Set Up	D3+ Waveform Path	D3PWaveform	(Accepts user-defined text)	D3+ Waveform Path
Set Up	D3- Waveform Path	D3NWaveform	(Accepts user-defined text)	D3- Waveform Path
Set Up	DNModule	DNModule	(Accepts user-defined text)	Module number for SP4T D-.
Set Up	DPModule	DPModule	(Accepts user-defined text)	Module number for SP4T D+.
Set Up	DUTTimingPath	DUTTimingPath	(Accepts user-defined text)	Enter the CDF/template file path.
Set Up	DUTTimingSelection	DUTTimingSelection	Load from CDF, Load from Template, Manual Select	DUTTimingSelection
Set Up	DeEmbedFixtureTP1FRL	DeEmbedTP121	0.0, 1.0	DeEmbed TP1 tests for FRL.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	DeEmbedFixtureTextBox	FixtureDembed	(Accepts user-defined text)	Fixture de-embed s-parameter file path for TMDS.
Set Up	DeEmbedFixtureTextBox21	FixtureDembed21	(Accepts user-defined text)	Fixture de-embed s-parameter path for FRL.
Set Up	DeEmbedFixtureType	DeEmbedFixtureType	N1080H04, Wilder HDMI TPA-P, Wilder HDMI2 TPA-P 6 inch, Wilder HDMI2 TPA-P 12 inch, Wilder HDMI2.1 TPA-P, Other	Set the fixture de-embedding file for TMDS.
Set Up	DeEmbedFixtureType21	DeEmbedFixtureType21	Wilder HDMI2.1 TPA-P, BIT-1010-0400-0 HDMI 2.1 Type A Plug, Luxshare TPA-P, Wilder HDMI2.1 TPA-R, BIT-1010-0400-0 HDMI 2.1 TPA-R, Luxshare TPA-R, Other	Set the fixture de-embedding file for FRL.
Set Up	DeEmbedTP1	DeEmbedTP1	0.0, 1.0	DeEmbed TP1 tests for TMDS
Set Up	DeviceID	DeviceID	Transmitter, Receiver, Cable	DeviceID

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	DeviceToAnalyze	DeviceToAnalyze	Device1, FRL_SQ4.6_MX0024A_A, FRL_SQ4.6_MX0024A_AX, FRL_SQ4.6_MX0024A_W, FRL_SQ4.6_MX0025A_A, FRL_SQ4.6_MX0025A_AX, FRL_SQ4.6_MX0025A_AX_Cap, FRL_SQ4.6_MX0025A_W, FRL_SQ4.6_N2803A_A, FRL_SQ4.6_N2803A_AX, FRL_SQ4.6_N2803A_W, FRL_SQ4.6_N7003A_A, FRL_SQ4.6_N7003A_AX, FRL_SQ4.6_N7010A_12G, FRL_SQ4.6_N7010A_A, FRL_SQ4.6_N7010A_AX, FRL_SQ4.6_N7010A_AX_12G, FRL_SQ4.6_N7010A_AX_Switch, FRL_SQ4.6_N7010A_A_Switch, FRL_SQ4.6_N7010A_W, FRL_SQ4.6_N7010A_W_Switch, FRL_Switch_W,Old, Test, TMDS_SQ4.6_1169B_AX_HF1-87, TMDS_SQ4.6_1169B_W_Diff,	DeviceToAnalyze

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	DeviceToAnalyze	DeviceToAnalyze (cont'd)	TMDS_SQ4.6_MX0 024A_A, TMDS_SQ4.6_MX0 024A_AX, TMDS_SQ4.6_MX0 024A_AX_16, 97, TMDS_SQ4.6_MX0 024A_W, TMDS_SQ4.6_MX0 025A_A, TMDS_SQ4.6_MX0 025A_AX, TMDS_SQ4.6_MX0 025A_AX_16, 17, TMDS_SQ4.6_MX0 025A_W, TMDS_SQ4.6_N280 3A_AX_Diff, TMDS_SQ4.6_N701 0A_AX	DeviceToAnalyze
Set Up	EqualizerATextBox	EQAParam	(Accepts user-defined text)	Equalizer A value.
Set Up	EqualizerCableLeng th	EqualizerCableLength	2M, 5M, 7M, 10M	Set the equalizer cable length to use for TMDS.
Set Up	EqualizerEmbedTex tBox	EquSParam	(Accepts user-defined text)	Equalizer s-paramater file path for TMDS.
Set Up	EqualizerF0TextBox	EQfoParam	(Accepts user-defined text)	Equalizer F0 value
Set Up	EqualizerInputType	EqualizerInputType	Reference Equalizer, Load s-parameter file	Select equalizer type for TMDS.
Set Up	EqualizerShortCabl eLength21	EqualizerShortCableLength2 1	1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB	Set the equalizer gain for Short cable model for FRL.
Set Up	EqualizerWorstCabl eLength21	EqualizerWorstCableLength 21	1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB	Set the equalizer gain for worst cable model for FRL.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	FixtureType	FixtureType	N1080H04, Wilder HDMI TPA-P, Wilder HDMI2 TPA-P 6 inch, Wilder HDMI2 TPA-P 12 inch, Wilder HDMI2.1 TPA-P, Other	FixtureType
Set Up	Generate TMDS TP2 Waveforms	GenerateTMDSTP2Waveforms	0.0, 1.0	Generate TP2 Waveforms
Set Up	HDMIConnectionType	HDMIConnectionType	1 Data Lane, 3 Data Lanes	HDMIConnectionType
Set Up	HDMITMDSWaveformLane	HDMITMDSWaveformLane	D0, D1, D2	Select the TMDS lane to load waveform.
Set Up	HDMITestType	HDMITestType	TMDS Physical Layer, FRL Physical Layer, HEAC, Direct Attach	Determine the HDMI Test Type.
Set Up	HDMIWaveformDataRate	HDMIWaveformDataRate	3G, 6G_3Lanes, 6G_4Lanes, 8G, 10G, 12G	Set the imported waveform FRL data rate.
Set Up	HDMIWaveformPattern	HDMIWaveformPattern	LTP3, LTP4, LTP5, LTP5 (All lanes transmit)	Set the imported waveform FRL test pattern.
Set Up	HDMIWaveformType	HDMIWaveformType	TMDS Physical Layer, FRL Physical Layer	Select TMDS Physical Layer or FRL Physical Layer
Set Up	HEAC Test Mode	HEACTestMode	ARC (Common Mode), ARC (Single Mode)	Set the HEAC Test Mode.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	ProbeHeadType	ProbeHeadType	N5380X/1169X*, N5444A/N280XA, N5444A/N700XA, N7010A, MX0105A/MX0021A (BETA), MX0105A/MX0022A (BETA), MX0105A/MX0023A*, MX0105A/MX0024A (BETA), MX0105A/MX0025A (BETA)	ProbeHeadType
Set Up	SPDT6XModule	SPDT6XModule	(Accepts user-defined text)	Module number for 6x SPDT.
Set Up	SkewTextBox	WorstCaseSkew	(Accepts user-defined text)	Enter skew value to insert for TMDS.
Set Up	TurnOnCableEmbeddingCheckBox	TurnOnCableEmbedding	0.0, 1.0	Enable cable embed for TMDS.
Set Up	TurnOnCableEmbeddingCheckBox21	TurnOnCableEmbedding21	0.0, 1.0	Enable cable embed for FRL.
Set Up	TurnOnFixtureDeEmbedCheckBox21	TurnOnFixtureDeEmbed21	0.0, 1.0	Enable fixture de-embed for FRL.
Set Up	TurnOnHDMIEqualizerCheckBox	TurnOnFixtureDeEmbed	0.0, 1.0	Enable fixture de-embed for TMDS.
Set Up	TurnOnHDMIEqualizerCheckBox	TurnOnHDMIEqualizer	0.0, 1.0	Enable equalizer for TMDS.
Set Up	TurnOnHDMIEqualizerCheckBox21	TurnOnHDMIEqualizer21	0.0, 1.0	Enable equalizer for FRL.
Set Up	TurnOnWorstCaseSkewCheckBox	TurnOnWorstCaseSkew	0.0, 1.0	Enable skew insertion for TMDS.
Set Up	Waveform VIC	WaveformVIC	(Accepts user-defined text)	Enter VIC number.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	WaveformCaptureOption	WaveformCaptureOption	Standard mode: Capture and analyze live waveform, Capture mode: Acquire and store waveforms only, Analyze mode: Analyze stored waveforms, Capture and analyze stored waveforms	Determine method of capture and run.
Set Up	WaveformYCbCrEncoding	WaveformYCbCrEncoding	24-bit 4:4:4/RGB, 30-bit 4:4:4, 36-bit 4:4:4, 48-bit 4:4:4, 24-bit 4:2:0, 30-bit 4:2:0, 36-bit 4:2:0, 48-bit 4:2:0	Select the YCbCrEncoding type
Set Up	cmb1	cmb1	Channel1, Channel2	Channel number for Clk+/DX1+
Set Up	cmb2	cmb2	Channel1, Channel2	Channel number for DX2+
Set Up	cmb3	cmb3	Channel3, Channel4	Channel number for Clk-/DX1-
Set Up	cmb4	cmb4	Channel3, Channel4	Channel number for DX2-
*Limited availability: Availability of this setting depends upon the oscilloscope model and installed license options.				

3 Test Names and IDs

The following table shows the mapping between each test's numeric ID and name. The numeric ID is required by various remote interface methods.

- Name – The name of the test as it appears on the user interface **Select Tests** tab.
- Test ID – The number to use with the RunTests method.
- Description – The description of the test as it appears on the user interface **Select Tests** tab.

For example, if the graphical user interface displays this tree in the **Select Tests** tab:

- All Tests
  - Rise Time
  - Fall Time

then you would expect to see something like this in the table below:

Table 3 Example Test Names and IDs

Name	Test ID	Description
Fall Time	110	Measures clock fall time.
Rise Time	100	Measures clock rise time.

and you would run these tests remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SelectedTests '100,110'"
arsl -a ipaddress -c "Run"

C# syntax
---------
remoteAte.SelectedTests = new int[]{100,110};
remoteAte.Run();
```

Here are the actual Test names and IDs used by this application. Listed at the end, you may also find:

- Deprecated IDs and their replacements.
- Macro IDs which may be used to select multiple related tests at the same time.

NOTE The file, "TestInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 4 Test IDs and Names

Name	TestID	Description
(Beta) Save Lane CLK and D0 Waveform (TP2/TP2_EQ with Worst Case Negative Skew) triggered by VSYNC	88016	Saves waveforms for clock and D0 lanes.
(Beta) Save Lane CLK and D0 Waveform (TP2/TP2_EQ with Worst Case Positive Skew) triggered by VSYNC	88011	Saves waveforms for clock and D0 lanes.
(Beta) Save Lane CLK and D1 Waveform (TP2/TP2_EQ with Worst Case Negative Skew) triggered by VSYNC	88036	Saves waveforms for clock and D1 lanes.
(Beta) Save Lane CLK and D1 Waveform (TP2/TP2_EQ with Worst Case Positive Skew) triggered by VSYNC	88031	Saves waveforms for clock and D1 lanes.
(Beta) Save Lane CLK and D2 Waveform (TP2/TP2_EQ with Worst Case Negative Skew) triggered by VSYNC	88056	Saves waveforms for clock and D2 lanes.
(Beta) Save Lane CLK and D2 Waveform (TP2/TP2_EQ with Worst Case Positive Skew) triggered by VSYNC	88051	Saves waveforms for clock and D2 lanes.
1-1: VL Clock +	7030000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-1: VL Clock -	7040000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-1: VL D0+	7050000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-1: VL D0-	7060000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-1: VL D1+	7070000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-1: VL D1-	7080000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1-1: VL D2+	7090000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-1: VL D2-	7010000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-2: Clock Fall Time	2010000	2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-2: Clock Rise Time	2000000	2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-2: D0 Fall Time	2030000	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-2: D0 Rise Time	2020000	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-2: D1 Fall Time	2050000	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-2: D1 Rise Time	2040000	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-2: D2 Fall Time	2070000	Confirm that the rise times and fall times on the TMDS differential signals fall within the limits of the specification.
1-2: D2 Rise Time	2060000	Confirm that the rise times and fall times on the TMDS differential signals fall within the limits of the specification.
1-4: Intra-Pair Skew - Clock	6000000	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.
1-4: Intra-Pair Skew - Data Lane 0	6010000	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.
1-4: Intra-Pair Skew - Data Lane 1	6040000	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1-4: Intra-Pair Skew - Data Lane 2	6050000	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.
1-5: Clock Duty Cycle(Maximum)	5020000	2 Channels Connection Model:Confirm that the duty cycle of the differential TMDS clock does not exceed the limits allowed by the specification. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-5: Clock Duty Cycle(Minimum)	5010000	2 Channels Connection Model: Confirm that the duty cycle of the differential TMDS clock does not exceed the limits allowed by the specification. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-6: Clock Jitter	1200000	2 Channels Connection Model: TMDS differential clock jitter must not exceed 0.27*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output > 340MHz for testing.
1-7: D0 Mask Test (TP8_EQ with Worst Case Skew)	3200000	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
1-7: D0 Mask Test (TP8_EQ)	2200000	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
1-7: D1 Mask Test (TP8_EQ with Worst Case Skew)	3400000	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
1-7: D1 Mask Test (TP8_EQ)	2400000	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
1-7: D2 Mask Test (TP8_EQ with Worst Case Skew)	3600000	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
1-7: D2 Mask Test (TP8_EQ)	2600000	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
7-10: D0 Data Jitter (Required For All Pixel Rates)	3	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D0 Data Jitter Separation	9	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D0 Mask Test (Required For All Pixel Rates)	2	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
7-10: D0 Mask Test (TP2_EQ with Worst Case Negative Skew)	23	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D0 Mask Test (TP2_EQ with Worst Case Positive Skew)	22	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D1 Data Jitter (Required For All Pixel Rates)	5	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D1 Data Jitter Separation	10	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D1 Mask Test (Required For All Pixel Rates)	4	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D1 Mask Test (TP2_EQ with Worst Case Negative Skew)	25	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D1 Mask Test (TP2_EQ with Worst Case Positive Skew)	24	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D2 Data Jitter (Required For All Pixel Rates)	7	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D2 Data Jitter Separation	90	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D2 Mask Test (Required For All Pixel Rates)	6	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D2 Mask Test (TP2_EQ with Worst Case Negative Skew)	27	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D2 Mask Test (TP2_EQ with Worst Case Positive Skew)	26	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: Eye Pattern (Required For All Pixel Rates)	9004	

Table 4 Test IDs and Names (continued)

Name	TestID	Description
7-2: VL Clock +	703	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL Clock -	704	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D0+	705	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D0-	706	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D1+	707	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D1-	708	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D2+	709	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D2-	701	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-3: Voff Clock +	713	Confirm that a disabled TMDS link only allows leakage currents within specified limits.
7-3: Voff Clock -	714	Confirm that a disabled TMDS link only allows leakage currents within specified limits.
7-3: Voff D0+	715	Confirm that a disabled TMDS link only allows leakage currents within specified limits.
7-3: Voff D0-	716	Confirm that a disabled TMDS link only allows leakage currents within specified limits.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
7-3: Voff D1+	717	Confirm that a disabled TMDS link only allows leakage currents within specified limits.
7-3: Voff D1-	718	Confirm that a disabled TMDS link only allows leakage currents within specified limits.
7-3: Voff D2+	719	Confirm that a disabled TMDS link only allows leakage currents within specified limits.
7-3: Voff D2-	711	Confirm that a disabled TMDS link only allows leakage currents within specified limits.
7-4: Clock Fall Time	201	2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: Clock Rise Time	200	2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: D0 Fall Time	203	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: D0 Rise Time	202	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: D1 Fall Time	205	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: D1 Rise Time	204	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: D2 Fall Time	207	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: D2 Rise Time	206	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
7-4: Transition Time (Required For The Highest Supported Pixel Rate)	9005	
7-6: Inter-Pair Skew (Required For The Highest Supported Pixel Rate)	9009	
7-6: Inter-Pair Skew - D0/Clock	330	Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-6: Inter-Pair Skew - D0/D1	300	Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-6: Inter-Pair Skew - D0/D2	302	Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-6: Inter-Pair Skew - D1/Clock	331	Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-6: Inter-Pair Skew - D1/Clock	332	Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-6: Inter-Pair Skew - D1/D2	301	Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-6: Single Ended Test (Required For The Highest Supported Pixel Rate)	9008	
7-7: Intra-Pair Skew - Clock	600	Frequency > 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-7: Intra-Pair Skew - Data Lane 0	601	Frequency > 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
7-7: Intra-Pair Skew - Data Lane 1	604	Frequency > 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-7: Intra-Pair Skew - Data Lane 2	605	Frequency > 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-8: Clock Duty Cycle (Required For The Highest Supported Pixel Rate)	9007	
7-8: Clock Duty Cycle(Maximum)	502	2 Channels Connection Model: Clock duty cycle must be at least 40% and not more than 60%.The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-8: Clock Duty Cycle(Minimum)	501	2 Channels Connection Model: Clock duty cycle must be at least 40% and not more than 60%.The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-9: Clock Jitter	12	2 Channels Connection Model: TMDS differential clock jitter must not exceed 0.25*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output 27MHz(or 25MHz), 74.25MHz, 148.5MHz, and 222.75MHz for testing.
7-9: Clock Jitter (Required For All Pixel Rates)	9003	
Cable Clock Jitter	85	TMDS differential clock jitter must not exceed 0.25*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
Cable Clock Jitter	1085	TMDS differential clock jitter must not exceed 0.25*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
Cable Data Jitter	83	Eye diagram Data Jitter with equalized clock,data and Transition Time Converter using coefficients store in file
Cable Inter-Pair Skew	86	Cable Assembly Inter-Pair Skew should be no more than 2.42ns.
Cable Inter-Pair Skew - D0/D1	1086	Cable Assembly Inter-Pair Skew should be no more than 2.42ns.
Cable Inter-Pair Skew - D0/D2	1186	Cable Assembly Inter-Pair Skew should be no more than 2.42ns.
Cable Inter-Pair Skew - D1/D2	1286	Cable Assembly Inter-Pair Skew should be no more than 2.42ns.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Cable Intra-Pair Skew	87	Cable Assembly Intra-Pair Skew should be no more than 151ps.
Cable Mask Test	84	Eye diagram Mask Test with equalized clock,data and Transition Time Converter using coefficients store in file
Convert Signal into Digital 1s and 0s	88400	Convert Signal into Digital 1s and 0s.
D0 Cable Data Jitter	1083	Eye diagram Data Jitter with equalized clock,data and Transition Time Converter using coefficients store in file
D0 Cable Intra-Pair Skew	1087	Cable Assembly Intra-Pair Skew should be no more than 151ps.
D0 Cable Mask Test	1084	Eye diagram Mask Test with equalized clock,data and Transition Time Converter using coefficients store in file
D0 Data Jitter Separation (TP2_EQ with Worst Case Negative Skew)	400001	The Source shall have output levels at TP2, which meet the normalized eye diagram requirements.
D0 Data Jitter Separation (TP2_EQ with Worst Case Positive Skew)	400000	The Source shall have output levels at TP2, which meet the normalized eye diagram requirements.
D1 Cable Data Jitter	1183	Eye diagram Data Jitter with equalized clock,data and Transition Time Converter using coefficients store in file
D1 Cable Intra-Pair Skew	1187	Cable Assembly Intra-Pair Skew should be no more than 151ps.
D1 Cable Mask Test	1184	Eye diagram Mask Test with equalized clock,data and Transition Time Converter using coefficients store in file
D1 Data Jitter Separation (TP2_EQ with Worst Case Negative Skew)	400003	The Source shall have output levels at TP2, which meet the normalized eye diagram requirements.
D1 Data Jitter Separation (TP2_EQ with Worst Case Positive Skew)	400002	The Source shall have output levels at TP2, which meet the normalized eye diagram requirements.
D2 Cable Data Jitter	1283	Eye diagram Data Jitter with equalized clock,data and Transition Time Converter using coefficients store in file
D2 Cable Intra-Pair Skew	1287	Cable Assembly Intra-Pair Skew should be no more than 151ps.
D2 Cable Mask Test	1284	Eye diagram Mask Test with equalized clock,data and Transition Time Converter using coefficients store in file
D2 Data Jitter Separation (TP2_EQ with Worst Case Negative Skew)	400005	The Source shall have output levels at TP2, which meet the normalized eye diagram requirements.
D2 Data Jitter Separation (TP2_EQ with Worst Case Positive Skew)	400004	The Source shall have output levels at TP2, which meet the normalized eye diagram requirements.
HEC Eye Diagram Test (Differential Mode)	2010	To evaluate eye diagram of HEC differential signals.
HF1-1: Clock + VSwing	70301	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HF1-1: Clock - VSwing	70401	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: D0+ VSwing	70501	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: D0- VSwing	70601	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: D1+ VSwing	70701	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: D1- VSwing	70801	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: D2+ VSwing	70901	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: D2- VSwing	70101	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL Clock +	70300	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL Clock -	70400	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL D0+	70500	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL D0-	70600	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL D1+	70700	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL D1-	70800	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL D2+	70900	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL D2-	70100	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-2: Clock Fall Time	20100	2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-2: Clock Rise Time	20000	2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HF1-2: D0 Fall Time	20300	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-2: D0 Rise Time	20200	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-2: D1 Fall Time	20500	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-2: D1 Rise Time	20400	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-2: D2 Fall Time	20700	Confirm that the rise times and fall times on the TMDS differential signals fall within the limits of the specification.
HF1-2: D2 Rise Time	20600	Confirm that the rise times and fall times on the TMDS differential signals fall within the limits of the specification.
HF1-3: Inter-Pair Skew - D0/D1	30000	Confirm that any skew between the differential data pairs in the TMDS portion of the HDMI link does not exceed the limits in the specification.
HF1-3: Inter-Pair Skew - D0/D2	30200	Confirm that any skew between the differential data pairs in the TMDS portion of the HDMI link does not exceed the limits in the specification.
HF1-3: Inter-Pair Skew - D1/D2	30100	Confirm that any skew between the differential data pairs in the TMDS portion of the HDMI link does not exceed the limits in the specification.
HF1-4: Intra-Pair Skew - Clock	60000	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.
HF1-4: Intra-Pair Skew - Data Lane 0	60100	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.
HF1-4: Intra-Pair Skew - Data Lane 1	60400	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.
HF1-4: Intra-Pair Skew - Data Lane 2	60500	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HF1-5: D0 Maximum Differential Voltage	22000	Confirm that the differential signal on each TMDS differential data pair does not exceed Maximum/Minimum Differential Voltage.
HF1-5: D0 Minimum Differential Voltage	22001	Confirm that the differential signal on each TMDS differential data pair does not exceed Maximum/Minimum Differential Voltage.
HF1-5: D1 Maximum Differential Voltage	24000	Confirm that the differential signal on each TMDS differential data pair does not exceed Maximum/Minimum Differential Voltage.
HF1-5: D1 Minimum Differential Voltage	24001	Confirm that the differential signal on each TMDS differential data pair does not exceed Maximum/Minimum Differential Voltage.
HF1-5: D2 Maximum Differential Voltage	26000	Confirm that the differential signal on each TMDS differential data pair does not exceed Maximum/Minimum Differential Voltage.
HF1-5: D2 Minimum Differential Voltage	26001	Confirm that the differential signal on each TMDS differential data pair does not exceed Maximum/Minimum Differential Voltage.
HF1-6: Clock Duty Cycle(Maximum)	50200	Confirm that the duty cycle of the differential TMDS clock does not exceed the limits allowed by the specification. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-6: Clock Duty Cycle(Minimum)	50100	Confirm that the duty cycle of the differential TMDS clock does not exceed the limits allowed by the specification. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-6: Clock Rate	50300	Confirm that the clock rate of the differential TMDS clock does not exceed the limits allowed by the specification. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-7: Clock Jitter (TP2_EQ with Worst Case Negative Skew)	12001	2 Channels Connection Model: TMDS differential clock jitter must not exceed 0.3*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output > 340MHz for testing.
HF1-7: Clock Jitter (TP2_EQ with Worst Case Positive Skew)	12000	2 Channels Connection Model: TMDS differential clock jitter must not exceed 0.3*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output > 340MHz for testing.
HF1-7: Clock Jitter (TP2_EQ)	12002	2 Channels Connection Model: TMDS differential clock jitter must not exceed 0.3*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output > 340MHz for testing.
HF1-7: Differential Clock Voltage Swing, Vs (TP1)	12003	This is a subset of the clock jitter test where the differential voltage swing at TP1 must be > 400mV and < 1200mV.
HF1-87 (Beta): D0 Mask Test (TP2/TP2_EQ with Worst Case Negative Skew) triggered by VSYNC	32005	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP2/TP2_EQ, which meet the normalized eye diagram requirements.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HF1-87 (Beta): D0 Mask Test (TP2/TP2_EQ with Worst Case Positive Skew) triggered by VSYNC	32004	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP2/TP2_EQ, which meet the normalized eye diagram requirements.
HF1-87 (Beta): D1 Mask Test (TP2/TP2_EQ with Worst Case Negative Skew) triggered by VSYNC	34005	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP2/TP2_EQ, which meet the normalized eye diagram requirements.
HF1-87 (Beta): D1 Mask Test (TP2/TP2_EQ with Worst Case Positive Skew) triggered by VSYNC	34004	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP2/TP2_EQ, which meet the normalized eye diagram requirements.
HF1-87 (Beta): D2 Mask Test (TP2/TP2_EQ with Worst Case Negative Skew) triggered by VSYNC	36005	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP2/TP2_EQ, which meet the normalized eye diagram requirements.
HF1-87 (Beta): D2 Mask Test (TP2/TP2_EQ with Worst Case Positive Skew) triggered by VSYNC	36004	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP2/TP2_EQ, which meet the normalized eye diagram requirements.
HF1-8: D0 Mask Test (TP1)	32003	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D0 Mask Test (TP2_EQ with Worst Case Negative Skew)	32001	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D0 Mask Test (TP2_EQ with Worst Case Positive Skew)	32000	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D0 Mask Test (TP2_EQ)	32002	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D1 Mask Test (TP1)	34003	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D1 Mask Test (TP2_EQ with Worst Case Negative Skew)	34001	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D1 Mask Test (TP2_EQ with Worst Case Positive Skew)	34000	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D1 Mask Test (TP2_EQ)	34002	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HF1-8: D2 Mask Test (TP1)	36003	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D2 Mask Test (TP2_EQ with Worst Case Negative Skew)	36001	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D2 Mask Test (TP2_EQ with Worst Case Postive Skew)	36000	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D2 Mask Test (TP2_EQ)	36002	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HFR1-1: D0 DC Common Mode	5091	The Source shall meet the DC specifications in Table 6-20 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-1: D1 DC Common Mode	5092	The Source shall meet the DC specifications in Table 6-20 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-1: D2 DC Common Mode	5093	The Source shall meet the DC specifications in Table 6-20 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-1: D3 DC Common Mode	5090	The Source shall meet the DC specifications in Table 6-20 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Max D0+	5205	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Max D0-	5207	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Max D1+	5209	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Max D1-	5211	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Max D2+	5213	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HFR1-2: Vse Max D2-	5215	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Max D3+	5201	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Max D3-	5203	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Min D0+	5204	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Min D0-	5206	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Min D1+	5208	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Min D1-	5210	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Min D2+	5212	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Min D2-	5214	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Min D3+	5200	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-2: Vse Min D3-	5202	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-3: D0 Fall Time	5083	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D0 Rise Time	5082	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D0+ Fall Slew Rate	50930	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HFR1-3: D0+ Fall Time	50830	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D0+ Rise Slew Rate	50920	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D0+ Rise Time	50820	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D0- Fall Slew Rate	50931	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D0- Fall Time	50831	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D0- Rise Slew Rate	50921	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D0- Rise Time	50821	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D1 Fall Time	5085	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D1 Rise Time	5084	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D1+ Fall Slew Rate	50950	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D1+ Fall Time	50850	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D1+ Rise Slew Rate	50940	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D1+ Rise Time	50840	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D1- Fall Slew Rate	50951	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D1- Fall Time	50851	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D1- Rise Slew Rate	50941	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D1- Rise Time	50841	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D2 Fall Time	5087	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D2 Rise Time	5086	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HFR1-3: D2+ Fall Slew Rate	50970	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D2+ Fall Time	50870	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D2+ Rise Slew Rate	50960	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D2+ Rise Time	50860	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D2- Fall Slew Rate	50971	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D2- Fall Time	50871	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D2- Rise Slew Rate	50961	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D2- Rise Time	50861	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D3 Fall Time	5081	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D3 Rise Time	5080	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D3+ Fall Slew Rate	50910	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D3+ Fall Time	50810	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D3+ Rise Slew Rate	50900	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D3+ Rise Time	50800	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D3- Fall Slew Rate	50911	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D3- Fall Time	50811	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D3- Rise Slew Rate	50901	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.
HFR1-3: D3- Rise Time	50801	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HFR1-4: Inter-Pair Skew - D0/D1	5420	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-4: Inter-Pair Skew - D0/D2	5450	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-4: Inter-Pair Skew - D1/D2	5410	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-4: Inter-Pair Skew - D3/D0	5400	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-4: Inter-Pair Skew - D3/D1	5430	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-4: Inter-Pair Skew - D3/D2	5440	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-5: D0 Data Rate	5251	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-5: D1 Data Rate	5252	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-5: D2 Data Rate	5253	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-5: D3 Data Rate	5250	The Source shall meet the DC specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-6: D0 RJ Measurement Test	5032	Measures RMS random jitter.
HFR1-6: D0 RJ Measurement Test - Category 3 Short Cable Model (SCM3)	5033	Measures RMS random jitter.
HFR1-6: D1 RJ Measurement Test	5034	Measures RMS random jitter.
HFR1-6: D1 RJ Measurement Test - Category 3 Short Cable Model (SCM3)	5035	Measures RMS random jitter.
HFR1-6: D2 RJ Measurement Test	5036	Measures RMS random jitter.
HFR1-6: D2 RJ Measurement Test - Category 3 Short Cable Model (SCM3)	5037	Measures RMS random jitter.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HFR1-6: D3 RJ Measurement Test	5030	Measures RMS random jitter.
HFR1-6: D3 RJ Measurement Test - Category 3 Short Cable Model (SCM3)	5031	Measures RMS random jitter.
HFR1-7: D0 Eye Mask Test - Category 3 Short Cable Model (SCM3)	5060	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HFR1-7: D0 Eye Mask Test - Category 3 Worst Cable Model (WCM3)	5052	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HFR1-7: D1 Eye Mask Test - Category 3 Short Cable Model (SCM3)	5062	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HFR1-7: D1 Eye Mask Test - Category 3 Worst Cable Model (WCM3)	5054	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HFR1-7: D2 Eye Mask Test - Category 3 Short Cable Model (SCM3)	5064	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HFR1-7: D2 Eye Mask Test - Category 3 Worst Cable Model (WCM3)	5056	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HFR1-7: D3 Eye Mask Test - Category 3 Short Cable Model (SCM3)	5058	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HFR1-7: D3 Eye Mask Test - Category 3 Worst Cable Model (WCM3)	5050	Confirm that the differential signal on each FRL differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HFR1-8: D0 AC Common Mode Noise	5120	The Source shall meet the AC Common Mode Noise specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-8: D1 AC Common Mode Noise	5140	The Source shall meet the AC Common Mode Noise specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-8: D2 AC Common Mode Noise	5160	The Source shall meet the AC Common Mode Noise specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.
HFR1-8: D3 AC Common Mode Noise	5100	The Source shall meet the AC Common Mode Noise specifications in Table 6-21 for all operating conditions specified in H14b Table 4-22 when driving FRL data signals.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HFR1-9: D0 De-emphasis Delta of FFE0 and FFE1	5381	D0 De-emphasis Delta of FFE0 and FFE1.
HFR1-9: D0 De-emphasis Delta of FFE1 and FFE2	5382	D0 De-emphasis Delta of FFE1 and FFE2.
HFR1-9: D0 De-emphasis Delta of FFE2 and FFE3	5383	D0 De-emphasis Delta of FFE2 and FFE3.
HFR1-9: D0 De-emphasis FFE0 Measurement	5304	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D0 De-emphasis FFE1 Measurement	5320	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D0 De-emphasis FFE2 Measurement	5340	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D0 De-emphasis FFE3 Measurement	5344	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D0 FFE De-emphasis Monotonicity	5368	Confirms that TxFFE monotonically decreases de-emphasis level.
HFR1-9: D0 FFE Preshoot Monotonicity	5370	Confirms that TxFFE monotonically increases preshoot level.
HFR1-9: D0 Pre-shoot Delta of FFE0 and FFE1	5461	D0 Pre-shoot Delta of FFE0 and FFE1.
HFR1-9: D0 Pre-shoot Delta of FFE1 and FFE2	5462	D0 Pre-shoot Delta of FFE1 and FFE2.
HFR1-9: D0 Pre-shoot Delta of FFE2 and FFE3	5463	D0 Pre-shoot Delta of FFE2 and FFE3.
HFR1-9: D0 Pre-shoot FFE0 Measurement	5306	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D0 Pre-shoot FFE1 Measurement	5322	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D0 Pre-shoot FFE2 Measurement	5342	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D0 Pre-shoot FFE3 Measurement	5346	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D1 De-emphasis Delta of FFE0 and FFE1	5384	D1 De-emphasis Delta of FFE0 and FFE1.
HFR1-9: D1 De-emphasis Delta of FFE1 and FFE2	5385	D1 De-emphasis Delta of FFE1 and FFE2.
HFR1-9: D1 De-emphasis Delta of FFE2 and FFE3	5386	D1 De-emphasis Delta of FFE2 and FFE3.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HFR1-9: D1 De-emphasis FFE0 Measurement	5308	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D1 De-emphasis FFE1 Measurement	5324	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D1 De-emphasis FFE2 Measurement	5348	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D1 De-emphasis FFE3 Measurement	5352	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D1 FFE De-emphasis Monotonicity	5372	Confirms that TxFFE monotonically decreases de-emphasis level.
HFR1-9: D1 FFE Preshoot Monotonicity	5374	Confirms that TxFFE monotonically increases preshoot level.
HFR1-9: D1 Pre-shoot Delta of FFE0 and FFE1	5464	D1 Pre-shoot Delta of FFE0 and FFE1.
HFR1-9: D1 Pre-shoot Delta of FFE1 and FFE2	5465	D1 Pre-shoot Delta of FFE1 and FFE2.
HFR1-9: D1 Pre-shoot Delta of FFE2 and FFE3	5466	D1 Pre-shoot Delta of FFE2 and FFE3.
HFR1-9: D1 Pre-shoot FFE0 Measurement	5310	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D1 Pre-shoot FFE1 Measurement	5326	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D1 Pre-shoot FFE2 Measurement	5350	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D1 Pre-shoot FFE3 Measurement	5354	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D2 De-emphasis Delta of FFE0 and FFE1	5387	D2 De-emphasis Delta of FFE0 and FFE1.
HFR1-9: D2 De-emphasis Delta of FFE1 and FFE2	5388	D2 De-emphasis Delta of FFE1 and FFE2.
HFR1-9: D2 De-emphasis Delta of FFE2 and FFE3	5389	D2 De-emphasis Delta of FFE2 and FFE3.
HFR1-9: D2 De-emphasis FFE0 Measurement	5312	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D2 De-emphasis FFE1 Measurement	5328	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D2 De-emphasis FFE2 Measurement	5356	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HFR1-9: D2 De-emphasis FFE3 Measurement	5360	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D2 FFE De-emphasis Monotonicity	5376	Confirms that TxFFE monotonically decreases de-emphasis level.
HFR1-9: D2 FFE Preshoot Monotonicity	5378	Confirms that TxFFE monotonically increases preshoot level.
HFR1-9: D2 Pre-shoot Delta of FFE0 and FFE1	5467	D2 Pre-shoot Delta of FFE0 and FFE1.
HFR1-9: D2 Pre-shoot Delta of FFE1 and FFE2	5468	D2 Pre-shoot Delta of FFE1 and FFE2.
HFR1-9: D2 Pre-shoot Delta of FFE2 and FFE3	5469	D2 Pre-shoot Delta of FFE2 and FFE3.
HFR1-9: D2 Pre-shoot FFE0 Measurement	5314	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D2 Pre-shoot FFE1 Measurement	5330	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D2 Pre-shoot FFE2 Measurement	5358	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D2 Pre-shoot FFE3 Measurement	5362	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D3 De-emphasis Delta of FFE0 and FFE1	5390	D3 De-emphasis Delta of FFE0 and FFE1.
HFR1-9: D3 De-emphasis Delta of FFE1 and FFE2	5391	D3 De-emphasis Delta of FFE1 and FFE2.
HFR1-9: D3 De-emphasis Delta of FFE2 and FFE3	5392	D3 De-emphasis Delta of FFE2 and FFE3.
HFR1-9: D3 De-emphasis FFE0 Measurement	5300	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D3 De-emphasis FFE1 Measurement	5316	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D3 De-emphasis FFE2 Measurement	5332	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D3 De-emphasis FFE3 Measurement	5336	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D3 FFE De-emphasis Monotonicity	5364	Confirms that TxFFE monotonically decreases de-emphasis level.
HFR1-9: D3 FFE Preshoot Monotonicity	5366	Confirms that TxFFE monotonically increases preshoot level.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HFR1-9: D3 Pre-shoot Delta of FFE0 and FFE1	5471	D3 Pre-shoot Delta of FFE0 and FFE1.
HFR1-9: D3 Pre-shoot Delta of FFE1 and FFE2	5472	D3 Pre-shoot Delta of FFE1 and FFE2.
HFR1-9: D3 Pre-shoot Delta of FFE2 and FFE3	5473	D3 Pre-shoot Delta of FFE2 and FFE3.
HFR1-9: D3 Pre-shoot FFE0 Measurement	5302	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D3 Pre-shoot FFE1 Measurement	5318	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D3 Pre-shoot FFE2 Measurement	5334	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR1-9: D3 Pre-shoot FFE3 Measurement	5338	Confirms that TxFFE monotonically increases pre-shoot amplitude and monotonically decreases de-emphasis.
HFR5-1-10: eARC TX Common Mode Output Data Bit Time at TP2	5610	Confirm that the eARC Tx meets Common Mode Output Data Bit Time requirements.
HFR5-1-11: eARC TX Common Mode Output "1" Bit Toggle Time at TP2	5620	Confirm that the eARC Tx meets Common Mode Output "1" Bit Toggle Time requirements.
HFR5-1-12: eARC TX Common Mode Input Swing at TP2	5600	Confirm that the eARC Tx meets Common Mode Output Swing requirements.
HFR5-1-15: eARC TX Common Mode Output Fall Time (10% - 90%) at TP2	5640	Confirm that the eARC Tx meets Common Mode Output Rise/Fall Time requirements.
HFR5-1-15: eARC TX Common Mode Output Rise Time (10% - 90%) at TP2	5630	Confirm that the eARC Tx meets Common Mode Output Rise/Fall Time requirements.
HFR5-1-1: eARC TX Termination Supply Voltage at TP2 - eARC+	5625	Confirm that the eARC Tx meets Termination Supply Voltage requirements.
HFR5-1-1: eARC TX Termination Supply Voltage at TP2 - eARC-	5626	Confirm that the eARC Tx meets Termination Supply Voltage requirements.
HFR5-1-2: eARC TX Differential Mode Swing at TP2	5520	Confirm that the eARC Tx meets Differential Mode Swing requirements.
HFR5-1-4: eARC TX Differential Bit Rate Accuracy at TP2	5540	Confirm that the eARC Tx meets Differential Bit Rate requirements.
HFR5-1-4: eARC TX Differential Bit Rate at TP2	5530	Confirm that the eARC Tx meets Differential Bit Rate requirements.
HFR5-1-5: eARC TX Differential Mode Fall Time at TP2	5560	Confirm that the eARC Tx meets Differential Mode Rise/Fall Time requirements.
HFR5-1-5: eARC TX Differential Mode Rise Time at TP2	5550	Confirm that the eARC Tx meets Differential Mode Rise/Fall Time requirements.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HFR5-1-6: eARC TX Differential Mode Clock Jitter at TP2	5570	Confirm that the eARC Tx meets Differential Mode Clock Jitter requirements.
HFR5-1-7: Differential Mode Eye Diagram at TP1	5510	Confirm that the differential signal on eARC Tx output has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HFR5-1-8: eARC TX Differential Mode Duty Cycle (Maximum) at TP1	5590	Confirm that the eARC Tx meets Differential Mode Duty Cycle requirements.
HFR5-1-8: eARC TX Differential Mode Duty Cycle (Minimum) at TP1	5580	Confirm that the eARC Tx meets Differential Mode Duty Cycle requirements.
HFR5-1-9: eARC TX Differential to Common Mode Conversion at TP2 - DUT connected	5650	Confirm that the eARC Tx meets Differential to Common Mode Conversion requirements.
HFR5-1-9: eARC TX Differential to Common Mode Conversion at TP2 - DUT disconnected	5651	Confirm that the eARC Tx meets Differential to Common Mode Conversion requirements.
HFR5-2-10: eARC RX Common Mode Input Swing at TP1	5700	Confirm that the eARC RX meets Common Mode Output Swing requirements.
HFR5-2-12: eARC RX Common Mode Output Fall Time (10% - 90%) at TP1	5740	Confirm that the eARC Rx meets Common Mode Output Rise/Fall Time requirements.
HFR5-2-12: eARC RX Common Mode Output Rise Time (10% - 90%) at TP1	5730	Confirm that the eARC Rx meets Common Mode Output Rise/Fall Time requirements.
HFR5-2-7: eARC RX Common Mode Output Data Bit Time at TP1	5710	Confirm that the eARC Rx meets Common Mode Output Data Bit Time requirements.
HFR5-2-8: eARC RX Common Mode Output "1" Bit Toggle Time at TP1	5720	Confirm that the eARC Rx meets Common Mode Output "1" Bit Toggle Time requirements.
Receiver Clock Jitter	82	TMDS differential clock jitter must not exceed 0.25*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
Receiver Equalized Eye Diagram	80	Eye diagram with equalized clock and data using coefficients store in file.
Receiver Equalized Jitter Separation	81	Jitter Separation with equalized clock and data using coefficients store in file.
Save Lane CLK and D0 Waveform (TP1)	88000	Saves waveforms for clock and D0 lanes.
Save Lane CLK and D0 Waveform (TP2_EQ with Worst Case Negative Skew)	88015	Saves waveforms for clock lanes.
Save Lane CLK and D0 Waveform (TP2_EQ with Worst Case Positive Skew)	88010	Saves waveforms for clock lanes.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Save Lane CLK and D1 Waveform (TP1)	88020	Saves waveforms for clock and D1 lanes.
Save Lane CLK and D1 Waveform (TP2_EQ with Worst Case Negative Skew)	88035	Saves waveforms for clock lanes.
Save Lane CLK and D1 Waveform (TP2_EQ with Worst Case Positive Skew)	88030	Saves waveforms for clock lanes.
Save Lane CLK and D2 Waveform (TP1)	88040	Saves waveforms for clock and D2 lanes.
Save Lane CLK and D2 Waveform (TP2_EQ with Worst Case Negative Skew)	88055	Saves waveforms for clock lanes.
Save Lane CLK and D2 Waveform (TP2_EQ with Worst Case Positive Skew)	88050	Saves waveforms for clock lanes.
Save Lane D0 De-emphasis FFE0 Waveforms (TP1) (LTP4)	5803	Saves De-emphasis waveforms for D0 lane for pattern LTP4.
Save Lane D0 De-emphasis FFE1 Waveforms (TP1) (LTP4)	5815	Saves De-emphasis FFE1 waveforms for D0 lane for pattern LTP4.
Save Lane D0 De-emphasis FFE2 Waveforms (TP1) (LTP4)	5827	Saves De-emphasis FFE2 waveforms for D0 lane for pattern LTP4.
Save Lane D0 De-emphasis FFE3 Waveforms (TP1) (LTP4)	5839	Saves De-emphasis FFE3 waveforms for D0 lane for pattern LTP4.
Save Lane D0 No FFE0 Waveforms (TP1) (LTP4)	5849	Saves No FFE0 mode waveforms for D0 lane for pattern LTP4.
Save Lane D0 No FFE1 Waveforms (TP1) (LTP4)	5855	Saves No FFE1 mode waveforms for D0 lane for pattern LTP4.
Save Lane D0 No FFE2 Waveforms (TP1) (LTP4)	5856	Saves No FFE2 mode waveforms for D0 lane for pattern LTP4.
Save Lane D0 No FFE3 Waveforms (TP1) (LTP4)	5857	Saves No FFE3 mode waveforms for D0 lane for pattern LTP4.
Save Lane D0 Normal FFE0 Waveforms (TP1) (LTP4)	5801	Saves normal FFE0 waveforms for D0 lane for pattern LTP4.
Save Lane D0 Normal FFE1 Waveforms (TP1) (LTP4)	5813	Saves normal FFE1 waveforms for D0 lane for pattern LTP4.
Save Lane D0 Normal FFE2 Waveforms (TP1) (LTP4)	5825	Saves normal FFE2 waveforms for D0 lane for pattern LTP4.
Save Lane D0 Normal FFE3 Waveforms (TP1) (LTP4)	5837	Saves normal FFE3 waveforms for D0 lane for pattern LTP4.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Save Lane D0 Pre-shoot FFE0 Waveforms (TP1) (LTP4)	5805	Saves Pre-shoot waveforms for clock and D0 lane for pattern LTP4.
Save Lane D0 Pre-shoot FFE1 Waveforms (TP1) (LTP4)	5817	Saves Pre-shoot waveforms for D0 lane for pattern LTP4.
Save Lane D0 Pre-shoot FFE2 Waveforms (TP1) (LTP4)	5829	Saves Pre-shoot FFE2 waveforms for D0 lane for pattern LTP4.
Save Lane D0 Pre-shoot FFE3 Waveforms (TP1) (LTP4)	5841	Saves Pre-shoot FFE3 waveforms for D0 lane for pattern LTP4.
Save Lane D0 Waveform (TP1) (LTP3)	50013	Saves waveforms for D0 lane for pattern LTP3.
Save Lane D0 Waveform (TP1) (LTP4)	50014	Saves waveforms for D0 lane for pattern LTP4.
Save Lane D0 Waveform (TP1) (LTP5)	50011	Saves waveforms for D0 lane for pattern LTP5. Untested lanes must be set to LTP2.
Save Lane D0 Waveform (TP1) (LTP5) (All lanes transmit)	50012	Saves waveforms for D0 lane for pattern LTP8. All lanes transmit LTP5/6/7/8.
Save Lane D0 and D1 Waveform	5024	Saves waveforms for D0 and D1 lanes for interpair skew test.
Save Lane D0 and D1 Waveform for Inter-pair skew test	88100	Saves waveforms for D0/D1 lanes.
Save Lane D0 and D2 Waveform for Inter-pair skew test	88300	Saves waveforms for D0/D2 lanes.
Save Lane D1 De-emphasis FFE0 Waveforms (TP1) (LTP4)	5808	Saves De-emphasis waveforms for D1 lane for pattern LTP4.
Save Lane D1 De-emphasis FFE1 Waveforms (TP1) (LTP4)	5820	Saves De-emphasis FFE1 waveforms for D1 lane for pattern LTP4.
Save Lane D1 De-emphasis FFE2 Waveforms (TP1) (LTP4)	5832	Saves De-emphasis FFE2 waveforms for D1 lane for pattern LTP4.
Save Lane D1 De-emphasis FFE3 Waveforms (TP1) (LTP4)	5844	Saves De-emphasis FFE3 waveforms for D1 lane for pattern LTP4.
Save Lane D1 No FFE0 Waveforms (TP1) (LTP4)	5850	Saves No FFE0 mode waveforms for D1 lane for pattern LTP4.
Save Lane D1 No FFE1 Waveforms (TP1) (LTP4)	5858	Saves No FFE1 mode waveforms for D1 lane for pattern LTP4.
Save Lane D1 No FFE2 Waveforms (TP1) (LTP4)	5859	Saves No FFE2 mode waveforms for D1 lane for pattern LTP4.
Save Lane D1 No FFE3 Waveforms (TP1) (LTP4)	5860	Saves No FFE3 mode waveforms for D1 lane for pattern LTP4.
Save Lane D1 Pre-shoot FFE0 Waveforms (TP1) (LTP4)	5810	Saves Pre-shoot waveforms for D1 lane for pattern LTP4.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Save Lane D1 Pre-shoot FFE1 Waveforms (TP1) (LTP4)	5822	Saves Pre-shoot FFE1 waveforms for D1 lane for pattern LTP4.
Save Lane D1 Pre-shoot FFE2 Waveforms (TP1) (LTP4)	5834	Saves Pre-shoot FFE2 waveforms for D1 lane for pattern LTP4.
Save Lane D1 Pre-shoot FFE3 Waveforms (TP1) (LTP4)	5846	Saves Pre-shoot FFE3 waveforms for D1 lane for pattern LTP4.
Save Lane D1 Waveform (TP1) (LTP3)	50023	Saves waveforms for D1 lane for pattern LTP3.
Save Lane D1 Waveform (TP1) (LTP4)	50024	Saves waveforms for D1 lane for pattern LTP4.
Save Lane D1 Waveform (TP1) (LTP6)	50021	Saves waveforms for D1 lane for pattern LTP6. Untested lanes must be set to LTP2.
Save Lane D1 Waveform (TP1) (LTP6) (All lanes transmit)	50022	Saves waveforms for D1 lane for pattern LTP6. All lanes transmit LTP5/6/7/8.
Save Lane D1 and D2 Waveform	5022	Saves waveforms for D1 and D2 lanes for interpair skew test.
Save Lane D1 and D2 Waveform for Inter-pair skew test	88200	Saves waveforms for D1/D2 lanes.
Save Lane D1 normal FFE0 Waveforms (TP1) (LTP4)	5806	Saves normal FFE0 waveforms for D1 lane for pattern LTP4.
Save Lane D1 normal FFE1 Waveforms (TP1) (LTP4)	5818	Saves normal FFE1 waveforms for D1 lane for pattern LTP4.
Save Lane D1 normal FFE2 Waveforms (TP1) (LTP4)	5830	Saves normal FFE2 waveforms for D1 lane for pattern LTP4.
Save Lane D1 normal FFE3 Waveforms (TP1) (LTP4)	5842	Saves normal FFE3 waveforms for D1 lane for pattern LTP4.
Save Lane D2 De-emphasis FFE0 Waveforms (TP1) (LTP4)	5809	Saves De-emphasis waveforms for D2 lane for pattern LTP4.
Save Lane D2 De-emphasis FFE1 Waveforms (TP1) (LTP4)	5821	Saves De-emphasis FFE1 waveforms for D2 lane for pattern LTP4.
Save Lane D2 De-emphasis FFE2 Waveforms (TP1) (LTP4)	5833	Saves De-emphasis FFE2 waveforms for D2 lane for pattern LTP4.
Save Lane D2 De-emphasis FFE3 Waveforms (TP1) (LTP4)	5845	Saves De-emphasis FFE3 waveforms for D2 lane for pattern LTP4.
Save Lane D2 No FFE0 Waveforms (TP1) (LTP4)	5851	Saves No FFE0 mode waveforms for D2 lane for pattern LTP4.
Save Lane D2 No FFE1 Waveforms (TP1) (LTP4)	5861	Saves No FFE1 mode waveforms for D2 lane for pattern LTP4.
Save Lane D2 No FFE2 Waveforms (TP1) (LTP4)	5862	Saves No FFE2 mode waveforms for D2 lane for pattern LTP4.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Save Lane D2 No FFE3 Waveforms (TP1) (LTP4)	5863	Saves No FFE3 mode waveforms for D2 lane for pattern LTP4.
Save Lane D2 Pre-shoot FFE0 Waveforms (TP1) (LTP4)	5811	Saves Pre-shoot waveforms for D2 lane for pattern LTP4.
Save Lane D2 Pre-shoot FFE1 Waveforms (TP1) (LTP4)	5823	Saves Pre-shoot FFE1 waveforms for D2 lane for pattern LTP4.
Save Lane D2 Pre-shoot FFE2 Waveforms (TP1) (LTP4)	5835	Saves Pre-shoot FFE2 waveforms for D2 lane for pattern LTP4.
Save Lane D2 Pre-shoot FFE3 Waveforms (TP1) (LTP4)	5847	Saves Pre-shoot FFE3 waveforms for D2 lane for pattern LTP4.
Save Lane D2 Waveform (TP1) (LTP3)	50033	Saves waveforms for D2 lane for pattern LTP3.
Save Lane D2 Waveform (TP1) (LTP4)	50034	Saves waveforms for D2 lane for pattern LTP4.
Save Lane D2 Waveform (TP1) (LTP7)	50031	Saves waveforms for D2 lane for pattern LTP7. Untested lanes must be set to LTP2.
Save Lane D2 Waveform (TP1) (LTP7) (All lanes transmit)	50032	Saves waveforms for D2 lane for pattern LTP7. All lanes transmit LTP5/6/7/8.
Save Lane D2 normal FFE0 Waveforms (TP1) (LTP4)	5807	Saves normal FFE0 waveforms for D2 lane for pattern LTP4.
Save Lane D2 normal FFE1 Waveforms (TP1) (LTP4)	5819	Saves normal FFE1 waveforms for D2 lane for pattern LTP4.
Save Lane D2 normal FFE2 Waveforms (TP1) (LTP4)	5831	Saves normal FFE2 waveforms for D2 lane for pattern LTP4.
Save Lane D2 normal FFE3 Waveforms (TP1) (LTP4)	5843	Saves normal FFE3 waveforms for D2 lane for pattern LTP4.
Save Lane D3 De-emphasis FFE0 Waveforms (TP1) (LTP4)	5802	Saves De-emphasis waveforms for D3 lane for pattern LTP4.
Save Lane D3 De-emphasis FFE1 Waveforms (TP1) (LTP4)	5814	Saves De-emphasis FFE1 waveforms for D3 lane for pattern LTP4.
Save Lane D3 De-emphasis FFE2 Waveforms (TP1) (LTP4)	5826	Saves De-emphasis FFE2 waveforms for D3 lane for pattern LTP4.
Save Lane D3 De-emphasis FFE3 Waveforms (TP1) (LTP4)	5838	Saves De-emphasis FFE3 waveforms for D3 lane for pattern LTP4.
Save Lane D3 No FFE0 Waveforms (TP1) (LTP4)	5848	Saves No FFE0 mode waveforms for D3 lane for pattern LTP4.
Save Lane D3 No FFE1 Waveforms (TP1) (LTP4)	5852	Saves No FFE1 mode waveforms for D3 lane for pattern LTP4.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Save Lane D3 No FFE2 Waveforms (TP1) (LTP4)	5853	Saves No FFE2 mode waveforms for D3 lane for pattern LTP4.
Save Lane D3 No FFE3 Waveforms (TP1) (LTP4)	5854	Saves No FFE3 mode waveforms for D3 lane for pattern LTP4.
Save Lane D3 Normal FFE0 Waveforms (TP1) (LTP4)	5800	Saves normal FFE0 waveforms for D3 lane for pattern LTP4.
Save Lane D3 Normal FFE1 Waveforms (TP1) (LTP4)	5812	Saves normal FFE1 waveforms for D3 lane for pattern LTP4.
Save Lane D3 Normal FFE2 Waveforms (TP1) (LTP4)	5824	Saves normal FFE2 waveforms for D3 lane for pattern LTP4.
Save Lane D3 Normal FFE3 Waveforms (TP1) (LTP4)	5836	Saves normal FFE3 waveforms for D3 lane for pattern LTP4.
Save Lane D3 Pre-shoot FFE0 Waveforms (TP1) (LTP4)	5804	Saves Pre-shoot waveforms for clock and D3 lane for pattern LTP4.
Save Lane D3 Pre-shoot FFE1 Waveforms (TP1) (LTP4)	5816	Saves Pre-shoot waveforms for D3 lane for pattern LTP4.
Save Lane D3 Pre-shoot FFE2 Waveforms (TP1) (LTP4)	5828	Saves Pre-shoot FFE2 waveforms for D3 lane for pattern LTP4.
Save Lane D3 Pre-shoot FFE3 Waveforms (TP1) (LTP4)	5840	Saves Pre-shoot FFE3 waveforms for D3 lane for pattern LTP4.
Save Lane D3 Waveform (TP1) (LTP3)	50003	Saves waveforms for D3 lane for pattern LTP3.
Save Lane D3 Waveform (TP1) (LTP4)	50004	Saves waveforms for D3 lane for pattern LTP4.
Save Lane D3 Waveform (TP1) (LTP8)	50001	Saves waveforms for D3 lane for pattern LTP8. Untested lanes must be set to LTP2.
Save Lane D3 Waveform (TP1) (LTP8) (All lanes transmit)	50002	Saves waveforms for D3 lane for pattern LTP8. All lanes transmit LTP5/6/7/8.
Save Lane D3 and D0 Waveform	5020	Saves waveforms for D3 and D0 lanes for interpair skew test.
Save eARC Differential Waveform	5500	Saves eARC differential waveform.
Save eARC Single-Ended Waveform Rx	5705	Saves eARC single-ended waveform.
Save eARC Single-Ended Waveform Tx	5505	Saves eARC single-ended waveform.
Test ID 5-11: ARC Operating DC Voltage (Single Mode)	3950	To evaluate operating DC voltage of ARC Single Mode signals.
Test ID 5-12: ARC Signal Amplitude (Single Mode)	4000	To evaluate signal Amplitude of Single Mode ARC signals.
Test ID 5-13a: ARC Rise Time (Single Mode)	4014	To evaluate rise time of HDMI ARC Single Mode signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Test ID 5-13b: ARC Fall Time (Single Mode)	4015	To evaluate fall time of HDMI ARC Single Mode signal.
Test ID 5-14a: ARC Jitter Test(Single Mode)	4020	To evaluate total jitter of ARC signals.
Test ID 5-14b: ARC Clock Frequency (Single Mode)	4030	To evaluate clock frequency of HDMI ARC Single Mode signal.
Test ID 5-19: ARC Rx Operating DC Voltage(Common Mode)	3050	To evaluate operating DC voltage of ARC signals for receiver.
Test ID 5-1: HEC Operating DC Voltage	1900	To evaluate operating DC voltage of HEC differential signals.
Test ID 5-2 HEC Maximum Jitter Test (Differential Mode)	2011	To evaluate maximum jitter of HEC differential signals.
Test ID 5-20: ARC Operating DC Voltage For Receiver(Single Mode)	4050	To evaluate operating DC voltage of ARC Single Mode signals for receiver.
Test ID 5-3a: HEC Rise Time Test Top(Differential Mode)	2020	To evaluate rise time of top MLT-3 differential mode signal of HDMI HEC transmission.
Test ID 5-3b: HEC Fall Time Test Top(Differential Mode)	2021	To evaluate fall time of top MLT-3 differential mode signal of HDMI HEC transmission.
Test ID 5-3c:HEC Rise Time Test Bottom(Differential Mode)	2022	To evaluate rise time of Bottom MLT-3 differential mode signal of HDMI HEC transmission.
Test ID 5-3d:HEC Fall Time Test Bottom(Differential Mode)	2023	To evaluate fall time of bottom MLT-3 differential mode signal of HDMI HEC transmission.
Test ID 5-4a: HEC High Level Voltage (Differential Mode)	2000	To evaluate high level voltage of HEC differential signals.
Test ID 5-4b: HEC Low Level Voltage (Differential Mode)	2001	To evaluate low level voltage of HEC differential signals.
Test ID 5-4c: HEC Center Level Voltage (Differential Mode)	2002	To evaluate center level voltage of HEC differential signals.
Test ID 5-5a:HEC Cycle Time Top (Differential Mode)	2030	To evaluate cycle time of differential mode signal of HDMI HEC transmission.
Test ID 5-5b: HEC Cycle Time Bottom (Differential Mode)	2031	To evaluate cycle time of differential mode signal of HDMI HEC transmission.
Test ID 5-6: ARC Operating DC Voltage (Common Mode)	2950	To evaluate operating DC voltage of ARC signals.
Test ID 5-7a: ARC High Level Voltage (Common Mode)	3000	To evaluate high level voltage of ARC signals.
Test ID 5-7b: ARC Low Level Voltage (Common Mode)	3001	To evaluate low level voltage of ARC signals.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Test ID 5-8a: ARC Rise Time (Common Mode)	3014	To evaluate rise time of HDMI ARC Common mode signal.
Test ID 5-8b: ARC Fall Time (Common Mode)	3015	To evaluate fall time of HDMI ARC Common mode signal.
Test ID 5-8c: ARC Rise Time (Common Mode with HEC)	3016	To evaluate rise time of HDMI ARC Common mode signal when HEC accompanies ARC.
Test ID 5-8d: ARC Fall Time (Common Mode with HEC)	3017	To evaluate fall time of HDMI ARC Common mode signal when HEC accompanies ARC.
Test ID 5-9a: ARC Jitter Test(Common Mode)	3020	To evaluate total jitter of ARC signals.
Test ID 5-9b: ARC Clock Frequency (Common Mode)	3030	To evaluate clock frequency of HDMI ARC Common mode signal.

4 Instruments

The following table shows the instruments used by this application. The name is required by various remote interface methods.

- Instrument Name — The name to use as a parameter in remote interface commands.
- Description — The description of the instrument.

For example, if an application uses an oscilloscope and a pulse generator, then you would expect to see something like this in the table below:

Table 5 Example Instrument Information

Name	Description
scope	The primary oscilloscope.
Pulse	The pulse generator used for Gen 2 tests.

and you would be able to remotely control an instrument using:

```
ARSL syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
arsl -a ipaddress -c "SendScpiCommandCustom 'Command=[scpi
command];Timeout=100;Instrument=pulsegen'"

arsl -a ipaddress -c "SendScpiQueryCustom 'Command=[scpi
query];Timeout=100;Instrument=pulsegen'"


C# syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
SendScpiCommandOptions commandOptions = new SendScpiCommandOptions();
commandOptions.Command = "[scpi command]";
commandOptions.Instrument = "[instrument name]";
commandOptions.Timeout = [timeout];
remoteAte.SendScpiCommand(commandOptions);

SendScpiQueryOptions queryOptions = new SendScpiQueryOptions();
queryOptions.Query = "[scpi query]";
queryOptions.Instrument = "[instrument name]";
```

```
queryOptions.Timeout = [timeout];
remoteAte.SendScpiQuery(queryOptions);
```

Here are the actual instrument names used by this application:

NOTE The file, "InstrumentInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 6 Instrument Names

Instrument Name	Description
Infiniium	The primary oscilloscope.

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