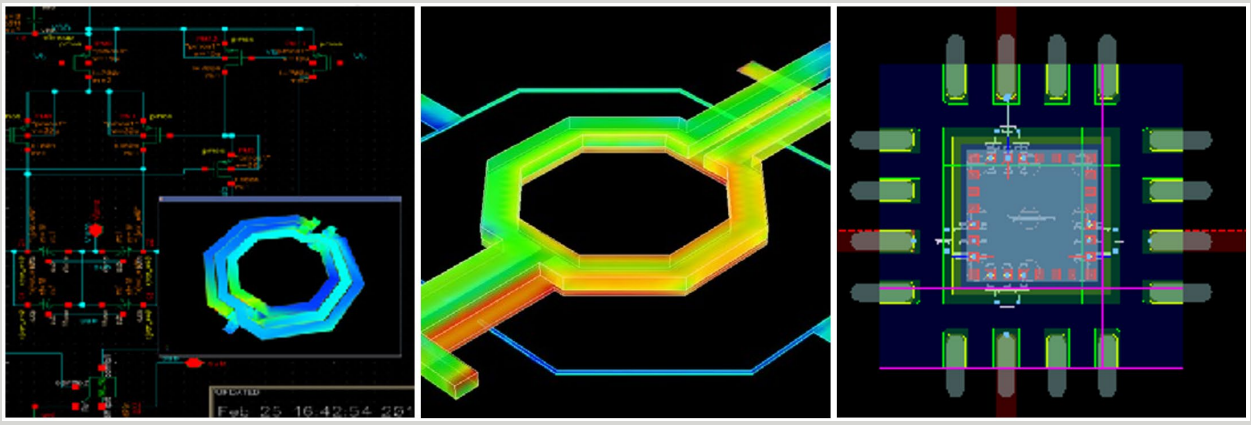

PathWave RFIC Design (GoldenGate) Solutions

The circuit simulation
for RFIC design and verification

KEYSIGHT

PATHWAVE

Overview

PathWave RFIC Design (GoldenGate) is the most trusted simulation, analysis, and verification solution available for integrated RF circuit design within Cadence Virtuoso and Synopsys Custom Compiler. It provides thorough circuit and statistical simulation along with verification against the latest industry wireless standards to eliminate the costly risk of re-spins and low yields.

For wireless front end RFIC and SoC designers working on 5G, automotive radars, WiFi and mmWave applications, it is an integral part of Keysight Silicon RFIC solution that also includes:

- PathWave Advanced Design System (ADS) for small-scale RFIC front-to-back implementation
- RFPro, Momentum and PathWave EM Design (EMPro) for on- and off-chip electromagnetic analysis
- PathWave System Design (SystemVue) Virtual Test Benches (VTB) for system-level co-design

This suite of products links the RF system, subsystem, and component-level design and analysis as part of a unique and comprehensive RFIC design offering.

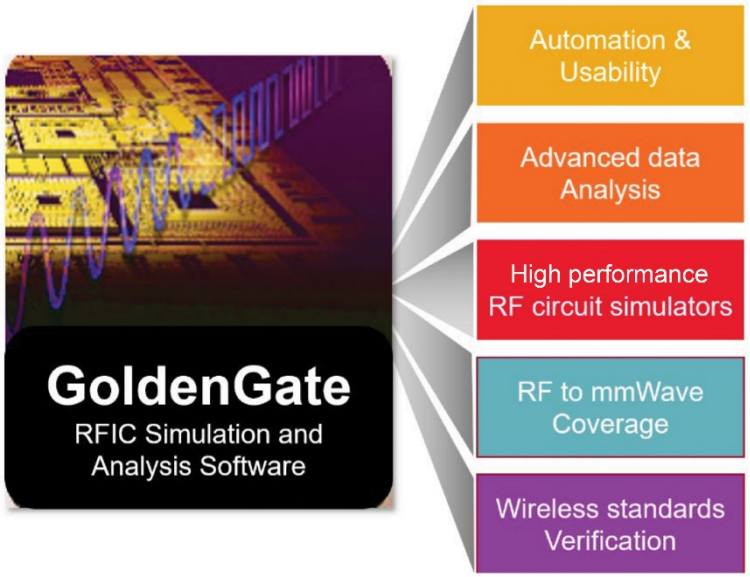

Figure 1. PathWave RFIC Design (GoldenGate) provides RF to mmWave circuit and statistical simulators along with wireless standards verification for RFIC and RF SoC designers. It eliminates the risk of costly re-spins and low yields. It enjoys broad foundry PDK support, such as TSMC's 79 GHz process.

PathWave RFIC Design (GoldenGate)

GoldenGate is a comprehensive RFIC Design and Verification solution that is seamlessly integrated in the Cadence Virtuoso and Synopsys Custom Compiler design environments. It offers unique simulation algorithms that enable full characterization of transceivers prior to tape-out. It includes the industry's most advanced set of steady-state and envelope circuit simulators allow design teams to confidently tackle even the most challenging RF integrated circuit designs.

Pathwave RFIC Design (GoldenGate) Solutions

Beyond providing the superior RF circuit simulators, PathWave RFIC Design (GoldenGate) Solutions come with powerful supporting capabilities.

- The RF circuit simulator provides advanced steady-state and envelope solvers for design and verification of RFICs within the Cadence Virtuoso and Synopsys Custom Compiler environments.
- Advanced analysis support offers a wide variety of capabilities to fully explore, analyze and optimize designs, before tape-out, minimizing the time and expense of re-spins.
- Automation and usability features accelerate design and verification by providing a number of tools on top of ADE-Explorer and ADE-Assembler.
- RF to mm-Wave design support provides optimal performance, capacity, and accuracy for RF to millimeter-wave (mm-Wave) applications.
- Wireless standard-compliant design capability couples the power of system- and circuit-level simulators with a comprehensive library of standard-based wireless verification intellectual property (IP) to accelerate the design of complex RFICs under real-life conditions.
- Broad foundry PDK support for RF processes such as TSMC N6RF and N16FFC reference flows for 28 GHz and 79 GHz designs.

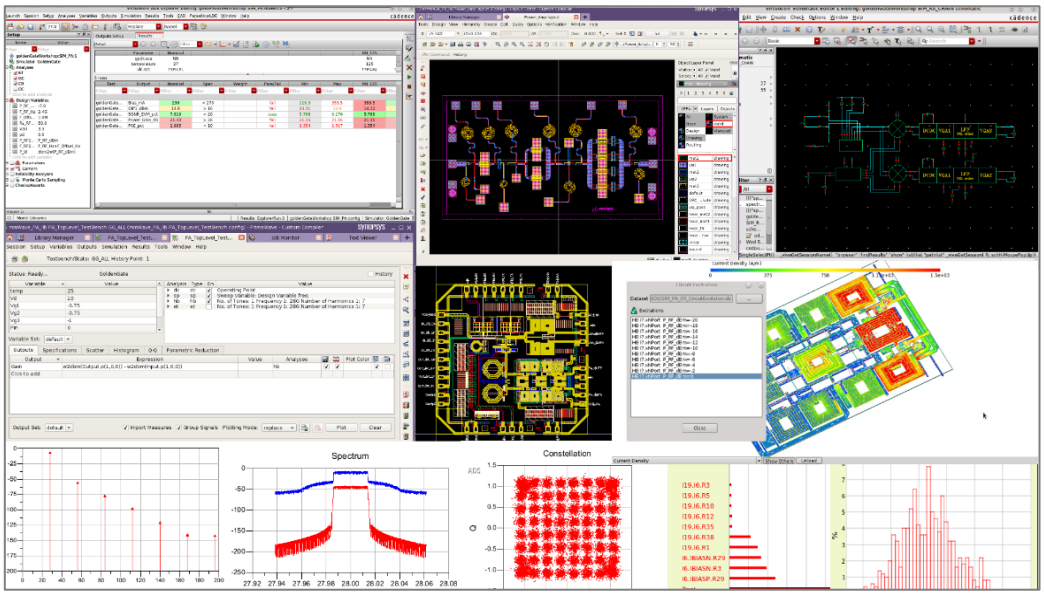

Figure 2. PathWave RFIC Design (GoldenGate) solutions provides an RF circuit simulators simulator, with advanced steady-state and envelope solvers for design and wireless standards verification of RF integrated circuits within the Cadence and Synopsys environments.

Leading the Way in RF Circuit Simulation

Widely known for its advanced steady-state and envelope solvers, GoldenGate also provides a full set of analog and application-specific analyses. Additionally, GoldenGate supports X-parameter* simulation and generation, which allows designers to capture the nonlinear behavior of active components in a standard format. X-parameters hide IP while enabling fast, accurate simulation within GoldenGate, ADS or SystemVue.

Keysight EDA works closely with RFIC Foundries to ensure GoldenGate covers all relevant models and is continually qualified against new and updated process nodes to ensure silicon-accurate results.

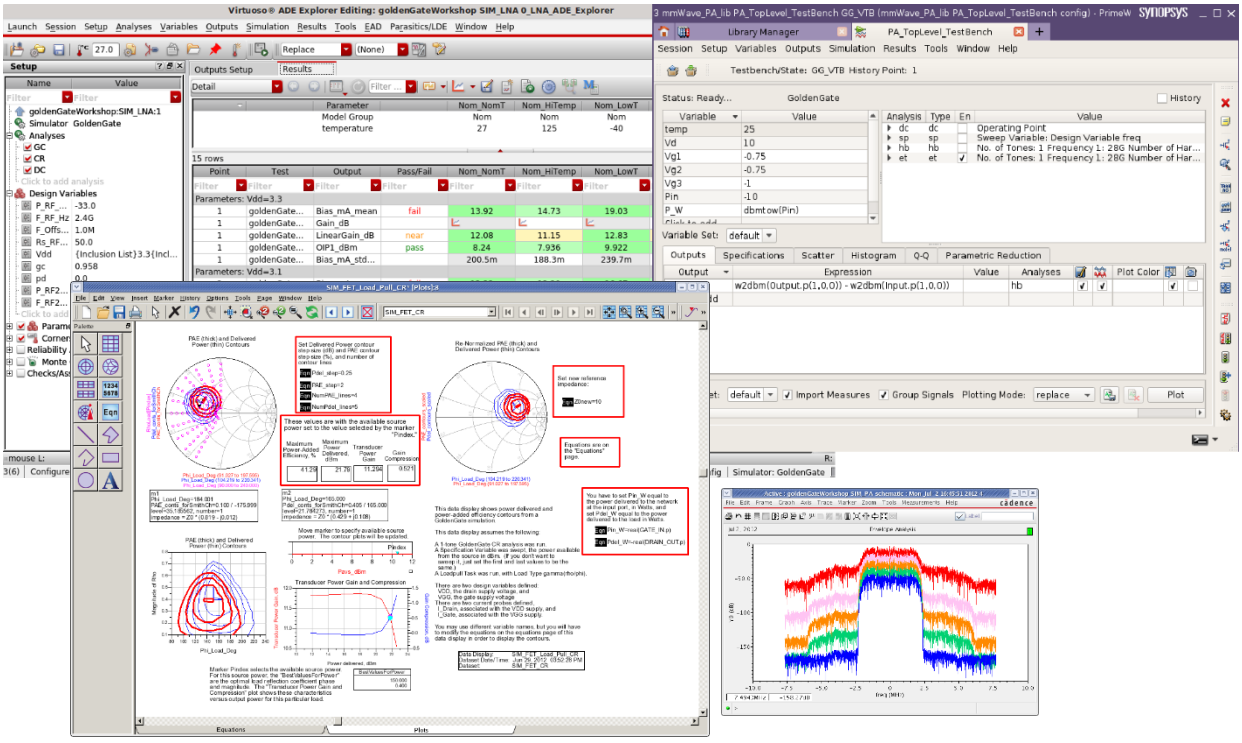

Figure 3. PathWave RFIC Design (GoldenGate) is directly integrated within the Cadence and Synopsys environments to provide standard functionality plus many unique RF capabilities.

RFIC Circuit Simulation Overview

- Unmatched Harmonic-Balance and Envelope-Transient analyses
  - Steady-state solvers include: Harmonic Balance, time balance, time shooting, and hybrid solvers
  - Envelope hybrid time-/frequency- domain nonlinear simulator
  - Fast Envelope algorithm that reduces runtimes by orders of magnitude while keeping memory effects
- Comprehensive set of analyses
  - DC, AC, noise, S-parameters, transient
  - Large-scale S-parameters, transient noise, sensitivity, as well as Bode, Nyquist and eigenvalue stability analyses
  - Intermodulation distortion and gain compression
- Keysight X-parameter nonlinear behavioral model generation and simulation

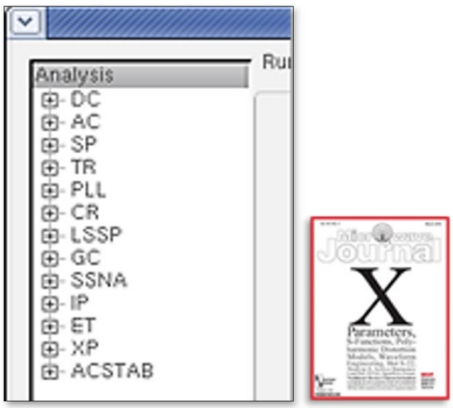

Figure 4. PathWave RFIC Design (GoldenGate) provides thorough circuit analyses, including Keysight X-parameter nonlinear behavioral model generation and simulation.

Making Designs More Robust

GoldenGate features a suite of automation tools that enable design teams to quickly analyze and diagnose problem areas early in the design cycle, and fully optimize circuit performance before tapeout. It also tightly integrates easy-to-use tools such as multi-dimensional sweeps, optimization and load-pull analysis.

GoldenGate's broad range of powerful, easy-to-use statistical tools helps pinpoint problems during the design phase.

Advanced Monte Carlo algorithms speed trials while reducing the number required.

Yield sensitivity histograms help identify critical design components. This information allows designers to make the design adjustments necessary to improve manufacturing yield.

Sensitivity analysis quickly allows insights on what parameters most strongly affect critical performances.

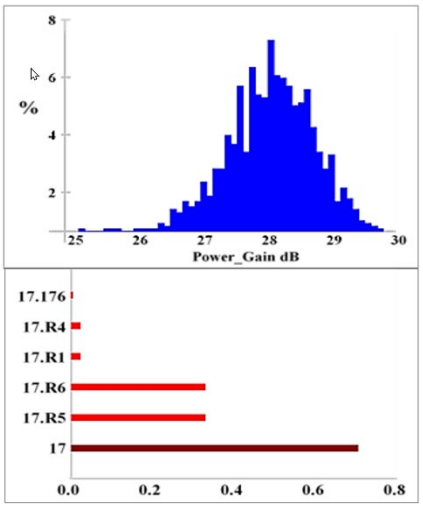

Figure 5. PathWave RFIC Design (GoldenGate) provides advanced statistical analyses to identify components causing performance variations before tapeout.

Advanced Analysis Overview

- Multi-dimensional sweeps with unmatched speed and convergence
- Fast yield and mismatch analyses for DC, AC, SP, SSNA, and CR with full contribution summary table
- Sensitivity analysis for CR, SSNA and DC analyses including sensitivity summary table
- Extensive load-pull setup and plotting capabilities
- Advanced Monte Carlo sampling algorithms
- Latin Hypercube
- Hammersley Sequence Sampling
- Boundary Mode and Orthogonal Arrays
- Fast yield and mismatch analyses for DC, AC, SP, SSNA, and CR
- Full contribution table
- Powerful optimization engine
- Digital state sweeping for operational mode performance, calibration and control sequences
- EVM fast computation through Keysight Compact Test Signals and Distortion EVM
- Digital Pre-Distortion (DPD) tests

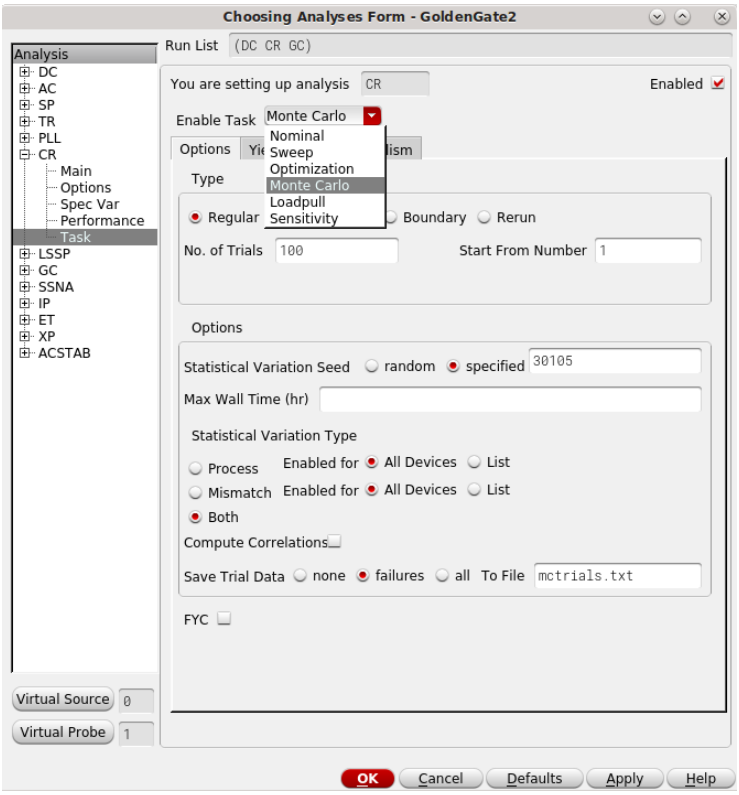

Figure 6. GoldenGate simulation UI simplifies the setup of advanced analyses.to access multiple-run simulations including Monte Carlo analysis. Fast Yield Contributor (FYC) analysis is a unique capability which enables very fast computation of device-level contributions within Monte Carlo analysis.

Automation Tools to Accelerate Your Design Cycle

Design verification of today's RFICs can be tedious and time-consuming. GoldenGate accelerates this task with several powerful tools that allow designers to set up and run distributed simulations. These tools enable the quick analysis and display of massive amounts of data, and can be used within Virtuoso, operated separately or integrated with other third-party products.

GoldenGate offers a variety of post-processing solutions and functionality beyond support of the Cadence ADE plotting capabilities. The Performance Editor and ADS Data Display include large repositories of built-in expressions. Data Display's flexibility enables designers to create advanced plots (e.g., load-pull contours, gain circles or eye diagrams) or even write their own functions.

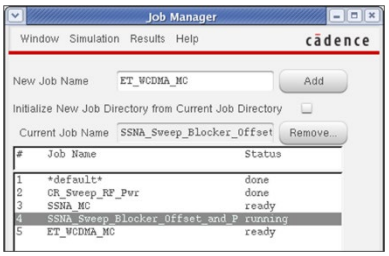

Figure 7. Job Manager enables designers to launch and monitor multiple ADE states at one time.

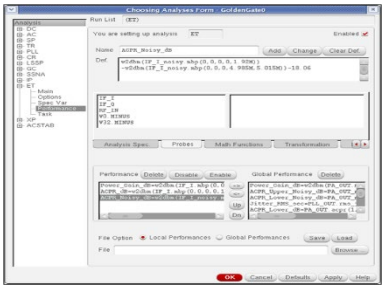

Figure 8. Performance Editor built-in functions automates calculating important figures-of-merit.

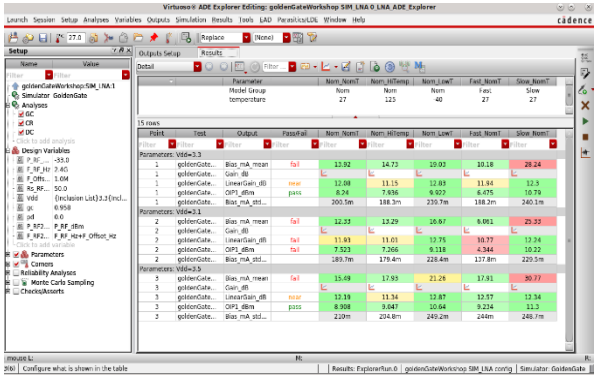

Figure 9. GoldenGate supports the ADE-Explorer and Assembler cockpits to provide a variety of tools to set up, launch and analyze parallel verification runs including corners.

Automation and Usability Overview

- Choosing Analyses Form – Simplified setup plus direct access to multi- dimensional sweeps, optimization, Monte Carlo, or load-pull
- Job Manager – Launch and monitor multiple ADE states simultaneously
- Sim Manager – Environment beyond ADE to run multiple simulations
- Monte Carlo, PVT corners
- Parallel sweeps on different machines
- Performance Editor – Easily represent significant circuit metrics
- ADS Data Display – Comprehensive plotting environment for wireless and wireline applications
- Automated Simulations – Calculate EVM, ACPR, gain compression, IPN, and load-pull contours
- Virtuoso Integration – Supports ADE-Assembler and ADE-Explorer setup and post- processing capabilities
- Synopsys PrimeWave integration
- Results Browser, Calculator
- ViVa & Ocean

Optimizing RFICs from RF to mm-Wave

By leveraging the powerful ADS model library, GoldenGate accurately models the effects of integrating microwave components with silicon RFICs within the Cadence Virtuoso environment. Its transient and envelope-transient engines handle very large S-parameter blocks, beyond the frequency-domain, using multi-threaded convolution techniques.

Tight links to the ADS common Open Access database allow designers to include IC content within the complete module design inside ADS or to perform more complete package characterization.

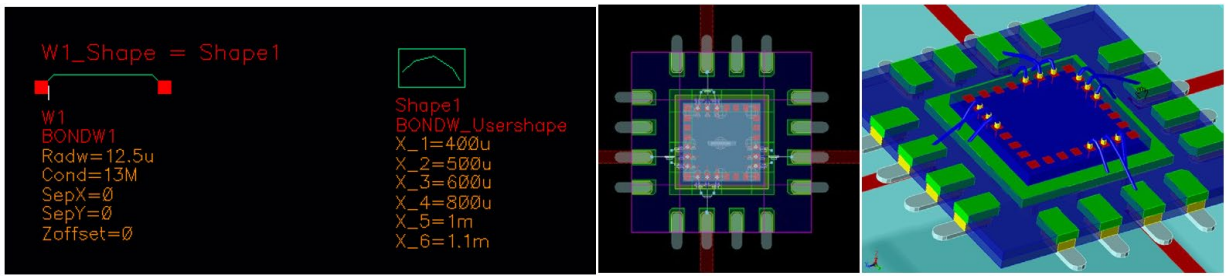

Figure 10. GoldenGate provides access from within Virtuoso to over 150 passive and distributed circuit models. Virtuoso layout can be viewed in 3D within the ADS platform to also include packaging effects for end-to-end EM verification. The ADS QFN designer automates the packaging design.

RF to mm-Wave Design Overview

- Accurately model the effects of microwave components and parasitic interconnections on silicon or SiGe chips
- RFPro enables silicon-accurate 3D planar EM simulation at nanometer scales
- Over 150 ADS models:
- Lines, bends, tees, and more, bond wires with coupling
- RF passive elements
- Tight links into ADS provide easy access to go beyond the IC
- ADS Data Display provides extensive plotting options
- Robust convolution engine ensures accurate results when using frequency-dependent components in a transient engine

Integrated with RFPro (FEM full 3DEM and Momentum 3D Planar Simulators)

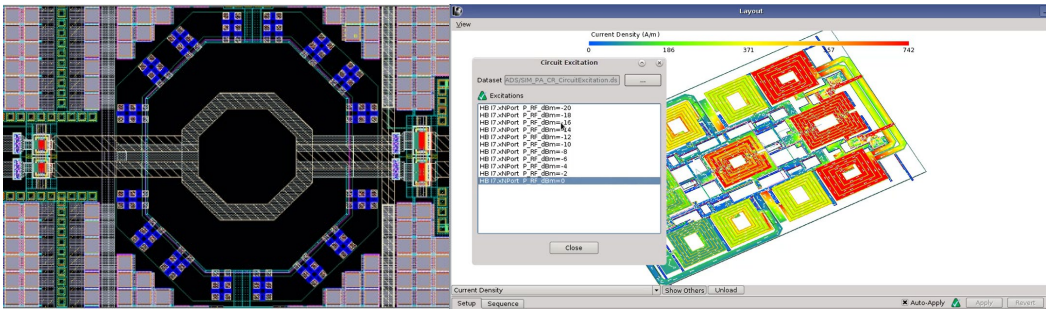

Figure 11. RFPro EM integration with Virtuoso extends 3D visualization and full 3D EM simulation of foundry PDK components, supported by broad foundry partners. This enables off-chip packaging to be included in simulation.

RFPro (FEM full 3D and Momentum planar 3DEM simulator):

- No expert setup
- No removing active devices and placing pins & ports
- No reconnecting schematics to S-parameter files

Silicon-accurate nanometer RFIC process support:

- Automated defeaturing (via merging/dummy removal/hatched planes…)
- Dummy metal fill and process scaling support
- Can read GoldenGate circuit simulations to show the EM behavior under real conditions

Main integrations:

- Same user interface for ADS/ Cadence Virtuoso/ Synopsys Custom Compiler
- Sweeping capabilities
- Broad foundry PDK support for Momentum stack-up files
- 3D Viewer with embedded visualization of surface currents or radiated fields

Going beyond 3D planar:

- Access to the Finite Element Method directly in Virtuoso and Custom Compiler
- Through Silicon Via modeling support

Assuring Circuit-Level Compliance to System-Level Wireless-Standards

GoldenGate features links to system-level analysis — from architectural exploration up to full co-simulation with data flow engines — for verification of the complex measurements required by today's wireless standards. These scalable links support various levels of interaction ranging from simple input/output file exchange to powerful integration with Keysight test equipment, and SystemVue.

GoldenGate integrates with SystemVue through easy-to-use Virtual Test Benches (VTBs). Such flexibility makes it ideal for a range of uses, whether performing architectural exploration, block-level specification refinement or complete standard-compliant system tests (e.g., EVM or BER).

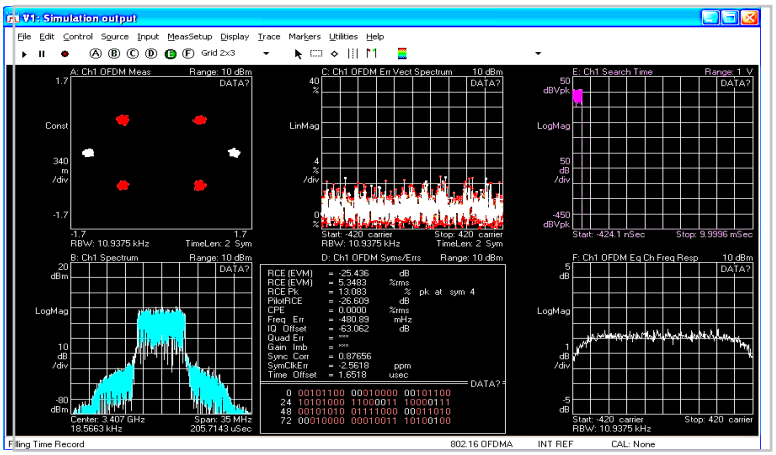

Figure 12. Links with SystemVue provide access to Keysight's powerful VSA instrument software

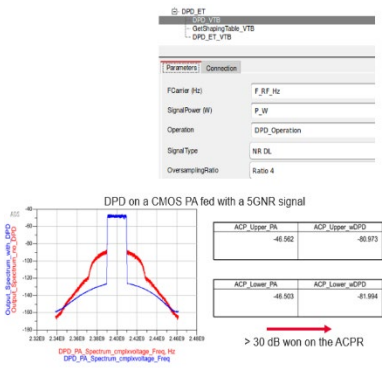

Figure 13. GoldenGate helps designers investigate the impact of circuits on system-level metrics directly in Virtuoso or Custom Compiler.

Wireless Standard Compliance Overview

- Full radio functionality verification using Keysight's extensive standard-compliant wireless libraries through scalable links to test equipment and ESL platforms
- Multiple links with SystemVue
- Fast Circuit-Envelope (FCE) model export to SystemVue
- Full GoldenGate – SystemVue co-simulation
- Pre-configured standard-compliant Virtual Test Benches (VTBs)
- Links to Keysight test equipment
- Stimuli creation through Signal Studio
- Standard-compliant post-processing in Keysight's Vector Signal Analyzer (VSA) software
- Avoid overdesigning RFICs
- Impairments of "as designed" RFICs visible to system engineer
- Low barrier for RF verification engineer to access standard-compliant modulated signals
- Access to the latest standard of communications (5GNR, WLAN11be,…)
- Digital Pre-Distortion examples

PathWave RFIC Design (GoldenGate) Configurations

GoldenGate Bundles For Virtuoso and Custom Compiler Design Flow

PathWave RFIC Design (GoldenGate)	W5500E
PathWave RFIC Design Quad (GoldenGate)	W5501E
PathWave RFIC Design (GoldenGate) + VTB Engine + Complete VTBs	W5802B
PathWave RFIC Design (GoldenGate) + RFPro	W5803B
PathWave RFIC Design (GoldenGate) + VTB Engine + Complete VTBs + RFPro	W5804B

ADS Packaging and Virtuoso / Custom Compiler Flow Bundles

PathWave ADS Core + EM Design Core + RFIC Design (GoldenGate) + RF Circuit Sim	W3611B
PathWave ADS Core + EM Design Core + RFIC Design (GoldenGate) + RF Circuit Sim + VTB Engine + VTB Complete	W3612B
PathWave ADS Core + EM Design Core + RFIC Design (GoldenGate) + RF Circuit Sim + Layout + RFPro	W3613B
PathWave ADS Core + EM Design Core + RFIC Design (GoldenGate) + RF Circuit Sim + Layout + RFPro + VTB Engine + Complete VTBs	W3614B
PathWave ADS Core, EM Design, RFIC Design Quad (GoldenGate), Layout, RFPro, RF Ckt Sim, Sys-Ckt Verif, VTBs	W3609B

GoldenGate Co-Simulation Elements

GoldenGate	
PathWave RFIC Design (GoldenGate)	W5500E
PathWave RFIC Design Quad (GoldenGate)	W5501E
Design Environments	
PathWave ADS Core & EM Design Core	W3600B
PathWave EM Design Core (excl. EM simulator)	W4300B
ADS Layout	
PathWave ADS Layout	W3010E
Circuit Simulation	
PathWave RF Circuit Simulation (incl. HB, CE, T/C, X-Param Gen)	W3020E
PathWave RFIC Design (GG) Parallel Corners / Monte Carlo	W5529E
Electromagnetic Simulation	
PathWave RFPro (incl. Momentum & FEM Simulators)	W3030E
PathWave Momentum	W3031E
Pathwave FEM (including RFPro UI)	W3032E
PathWave EM HPC 1-pack	W3039E
System-Circuit Verification Simulator and VTBs	
PathWave Sys-Ckt Verification Simulator (incl. Ptolemy & VTB Engine)	W3040E
PathWave VTB Engine	W3048E
PathWave Radar VTB	W3041E
PathWave 5G and Cellular VTB	W3042E
PathWave WiFi and Connectivity VTB	W3043E
PathWave WiMedia, WVAN and DTV VTB	W3046E
PathWave Complete VTBs	W3049E
Electrothermal Simulation	
PathWave Electro-Thermal Simulator	W3050E
PathWave Electro-Thermal Dynamic Model Generator	W3051E

Keysight enables innovators to push the boundaries of engineering by quickly solving design, emulation, and test challenges to create the best product experiences. Start your innovation journey at www.keysight.com.

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