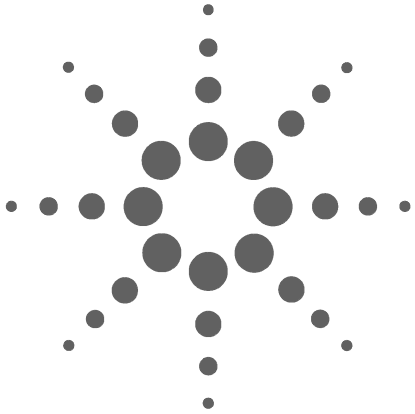

Agilent 35670A
Dynamic Signal Analyzer

Supplement to Installation, Service and Operator's Guide

Agilent Technologies

Notices

Manual Part Number

35670-90067

Edition

Third Edition. August 2006

Printed in Malaysia

Agilent Technologies, Inc.
3501 Stevens Creek Blvd.
Santa Clara, CA 95052 USA

Software Revision

This guide is valid for the firmware that was installed in the instrument at the time of manufacture.

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CAUTION

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WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

In This Supplement

Purpose

The purpose of this supplement is to describe changes to the display of the Agilent 35670A. These changes apply only to instruments with a serial number higher than MY42506200 made after December 2002.

Most users of the Agilent 35670A will see few or no changes in the operation of the instrument. The changes apply to specific sections of the *Agilent 35670A Operator's Guide*, the *Agilent 35670A Installation and Verification Guide*, and the *Agilent 35670A Service Guide*.

How to Use This Supplement

You may use these supplement pages to mark up your other guides or you may place supplement pages in the appropriate locations in those guides. Each segment of this document indicates which section of the original guide is affected by the changes. Only content which has changed is presented here in order to avoid confusion.

Declaration of Conformity

According to ISO/IEC Guide 22 and EN 45014

Manufacture's name:	Agilent Technologies
Manufacture's address:	Lake Stevens Site 8600 Soper Hill Road Everett, Washington 98205-1209

declares that this product

Product Name:	Dynamic Signal Analyzer
Model Number:	Agilent 35670A

conforms to the following specifications, except as noted in the Product Specifications:

Safety:	IEC 1010-1 (1990)+A1/EN61010-1 (1993)
EMC:	CISPR 11:1990/EN55011 (1991):Group 1, Class A IEC 801-2:1991/EN50082-1 (1992): 4kV-CD, 8kV-AD IEC 801-3:1984/EN50082-1 (1992): 3V/m (1) IEC 801-4:1988/EN50082-1 (1992): 1kV

Supplementary Information:
The product herewith complies with the requirements of Low Voltage Directive 72/23/EEC and the EMC Directive 89/336/EEC and carries the "CE " mark accordingly.

(1) In a 3V/m, field, some degradation of the product performance occurs.

Everett, Washington - May 5, 2000

Kevin Johnson, Manufacturing Engineering Manager

Contents

1 Overview

The changes to the Agilent 35670A Dynamic Signal Analyzer will not be noticeable to most users. The changes covered in the supplement include:

- new display
- new CPU board that also incorporates the memory and NVRAM boards
- memory options are now standard
- new external monitor interface which supports XGA resolution.
- DC-DC converter has been replaced by a power inverter

Summary of Changes

Display

Changes in the display will be imperceptible to most users. The changes are mainly at the assembly level and are addressed in the Service Guide.

Rear panel

The illustration below shows the new rear panel. The only change is in the location of the external monitor connection. This is the only place in this supplement that shows the new rear panel unless a detailed illustration is required.

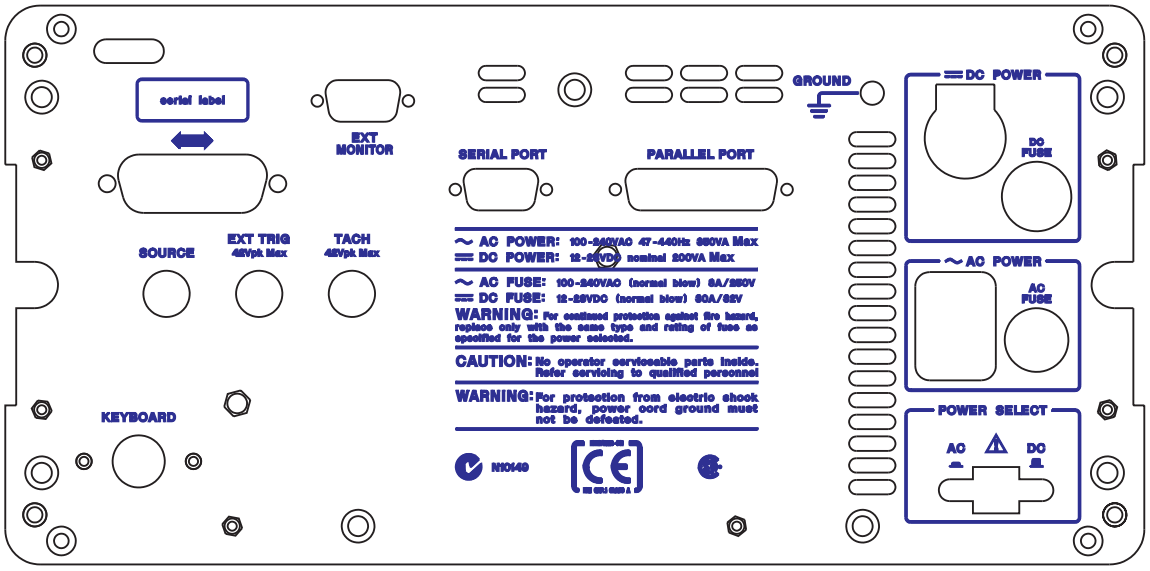

Figure 1 Rear panel

Board revisions

Throughout this supplement please note that the following is true for all instances of the following board numbers:

- A7 (CPU) is now A17
- A8 (memory) in now incorporated into A17
- A9 (NVRAM) in now incorporated into A17 and is no longer an option

These are global changes and will not be noted in each instance to avoid a large number of insignificant changes.

2
Installation and Verification Guide

The Agilent 35670A has incorporated a standard VGA monitor output and is now compatible with most monitors.

Preparing the Analyzer for Use

Page in original guide 2-13

To connect the analyzer to an external monitor

The External Monitor is a standard 15-pin miniature connector that can interface with an external monitor. The monitor must be compatible with the 49.74 kHz line rate, 61.6 Hz frame rate, analog RGB signals, and TTL sync signals provided by the Agilent 35670A.

1 Set the analyzer's power switch to on (|).

2 Set the monitor's power switch to on.

3 Connect the external monitor's input cable to the analyzer's rear panel EXT MONITOR connector.

4 Press the following keys to enable external display mode:

[**Disp Format**]
[MORE]
[MORE]
[EXT MON **ON** OFF]

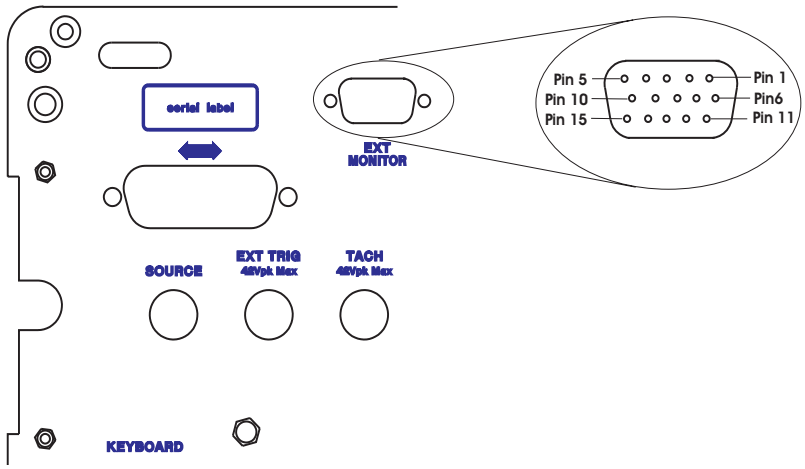

Figure 2 Rear panel showing external monitor connector

Pin Number	Signal Name
1	red analog output
2	green analog output
3	blue analog output
4	not connected
5	Ground
6	Ground
7	Ground
8	Ground
9	Not connected
10	Ground
11	Not connected
12	Not connected
13	TTL Horizontal Sync
14	TTL Vertical Sync
15	Not connected

3
Operator's Guide

Changes in this guide include display attributes (resolution, size, brightness) and external monitor connections.

Formatting the Display

To control the screen

Page in original guide 2-4

Disregard item 2. Display brightness is no longer adjustable.

4
Service Guide

The CPU board has a new number (A17) and is a consolidation of the original CPU assembly (A7), memory assembly (A8) and the Non-Volatile RAM option board (A9). Memory options are now standard.

There is a new higher resolution display, and a power inverter to replace the dc-dc converter. The external monitor port is now a standard VGA interface with XGA output resolution.

Preparing the Analyzer for Use

AC Power Cable and Grounding Requirements

Page in original guide 2-4

New power cable illustration shows new number for United Kingdom Option 900 cable.

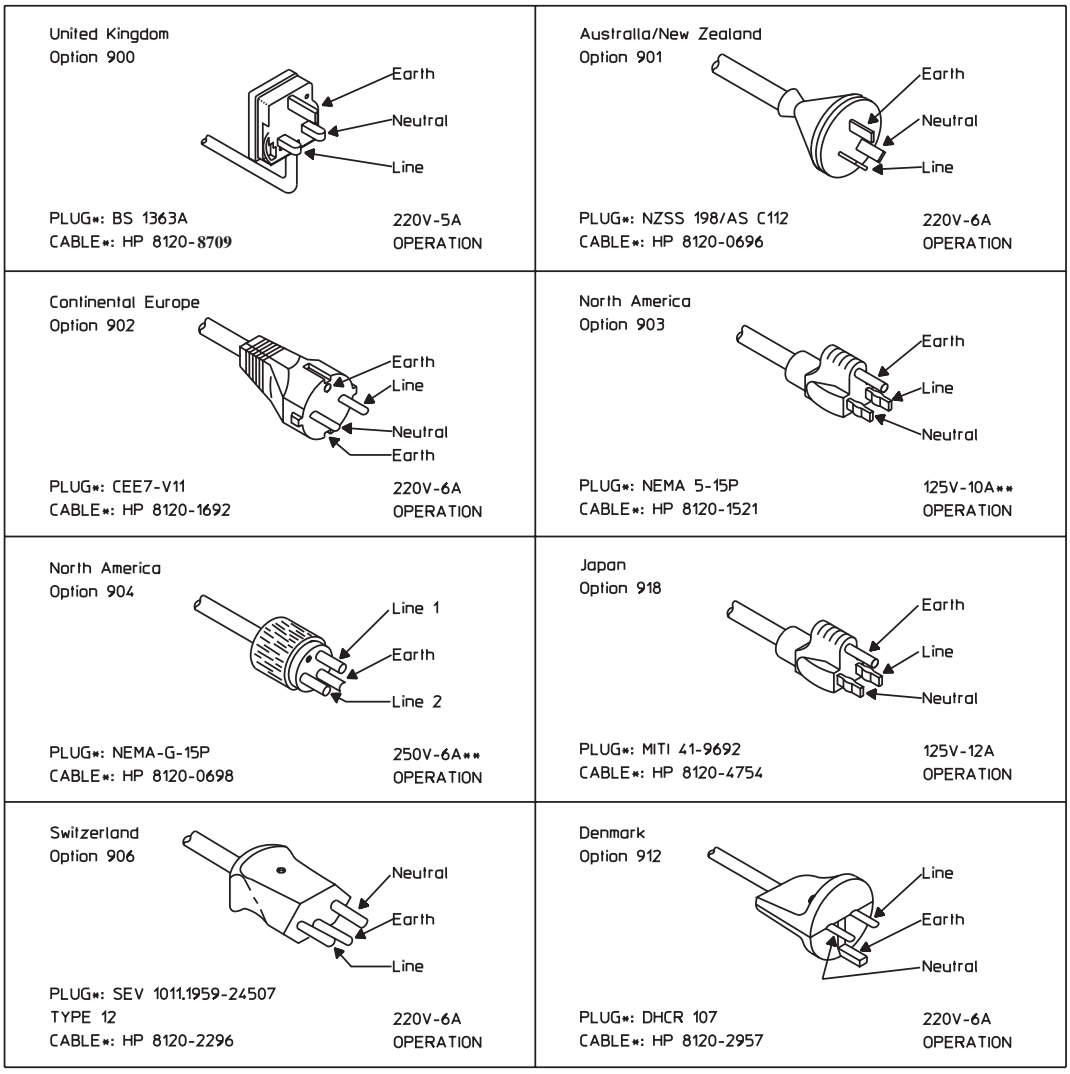

Figure 3 Power cables

To connect the analyzer to an external monitor

Page in original guide 2-13

The External Monitor is a standard 15-pin miniature connector that can interface with an external monitor. The monitor must be compatible with the 49.74 kHz line rate, 61.6 Hz frame rate, analog RGB signals, and TTL sync signals provided by the Agilent 35670A.

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[**Disp Format**]
[MORE]
[MORE]
[EXT MON **ON** OFF]

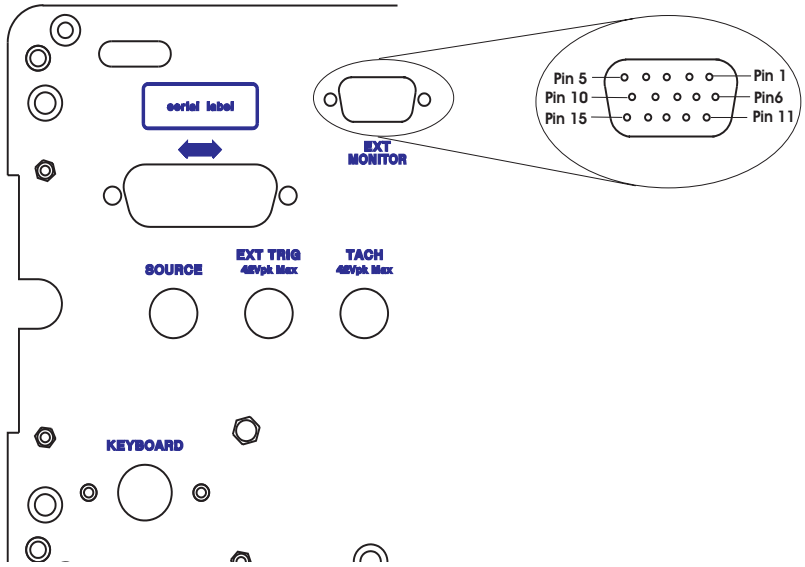

Figure 4 Rear panel showing external monitor connector

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
1	red analog output	6	Ground	11	Not connected
2	green analog output	7	Ground	12	Not connected
3	blue analog output	8	Ground	13	TTL Horizontal Sync
4	not connected	9	Not connected	14	TTL Vertical Sync
5	Ground	10	Ground	15	Not connected

Troubleshooting the Analyzer

To perform initial verification

Page in original guide 4-5

New illustrations for component locators show new test points and new connector locations:

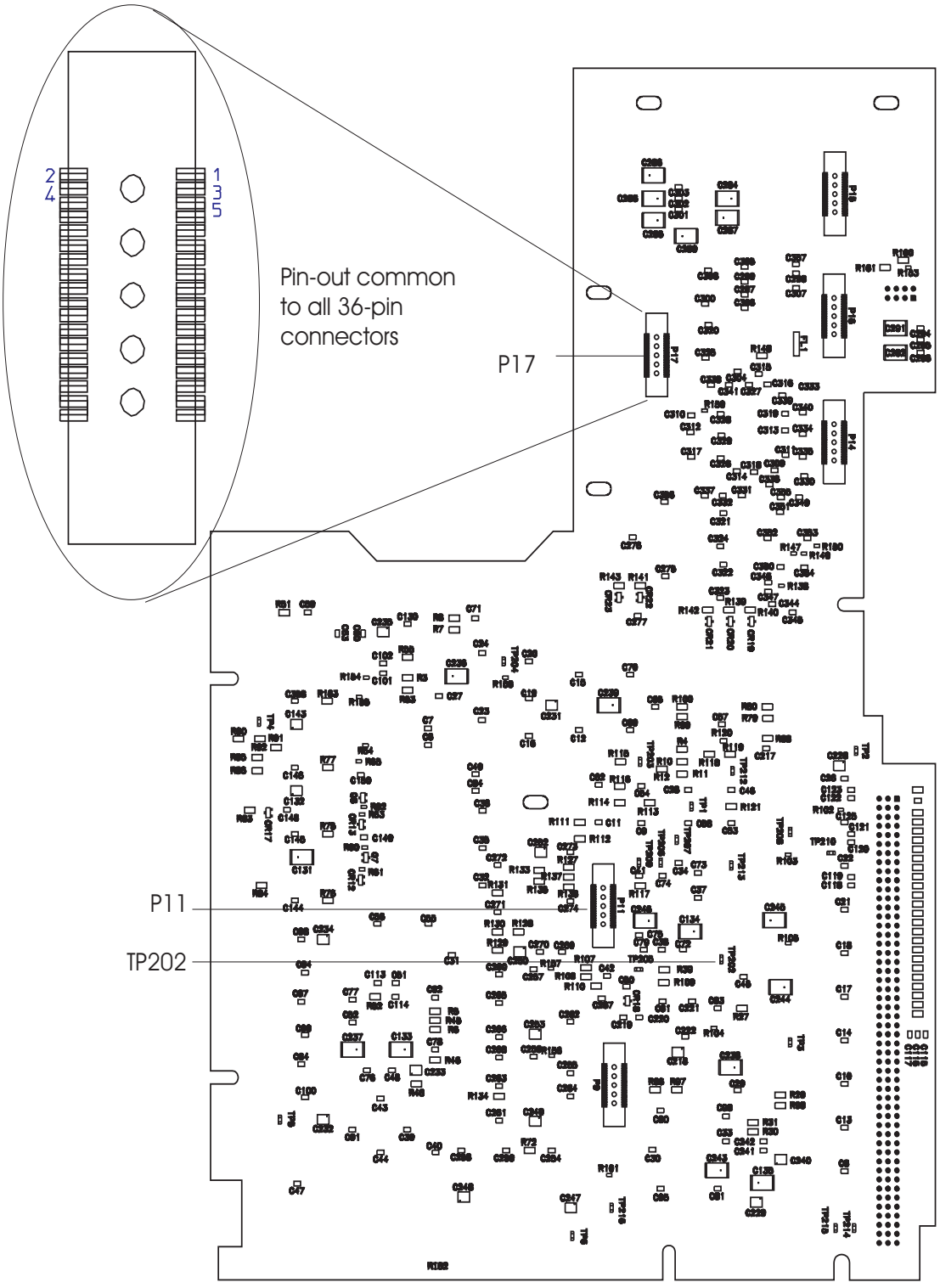

Figure 5 A17 CPU board test point locator

Replace Step 7: Check signals required for power up.

- Using a logic probe, check the following signals.

Signal Name	Test Location	TTL State	Probable Faulty Assembly
PVALID	TP202-1	High	A98 Power Supply
RSTn	P11-32	High	A17 CPU
ASn	P17-27	Toggling	A17 CPU
+5V	A17 TP212	High	A98 Power Supply
+3.3V	A17 TP 216	High	A17
C20MHz	A17 TP1	Toggling	A17
PASn	TP205	Toggling	A17
DSACK1n	TP207	Toggling	A17
DSACK0n	TP206	Toggling	A17
PRW	TP210	Toggling	A17
PDSn	TP209	Toggling	A17

- Using a logic probe, check that A17 P10 pin B20 (SCL) and A17 P10 pin C11 (SDA) toggle TTL states at least twice just after power up.
- If the signals are correct, go to page 4-15, “To troubleshoot power-up failures.”

To troubleshoot the power supply

Page in original guide 4-13

Step 5: Replace the bullet concerning reconnecting assemblies:

- Reconnect one assembly at a time in the following order:
  1. A17 CPU (A17 P10 to A99 J7)
  2. A102 Power Inverter (cable to A17 P13)
  3. A11 Keyboard Controller (Cable to A17 P1)
  4. A100 Disk Drive (cable to A17 P3)

The illustration for component locator shows new connector locations.

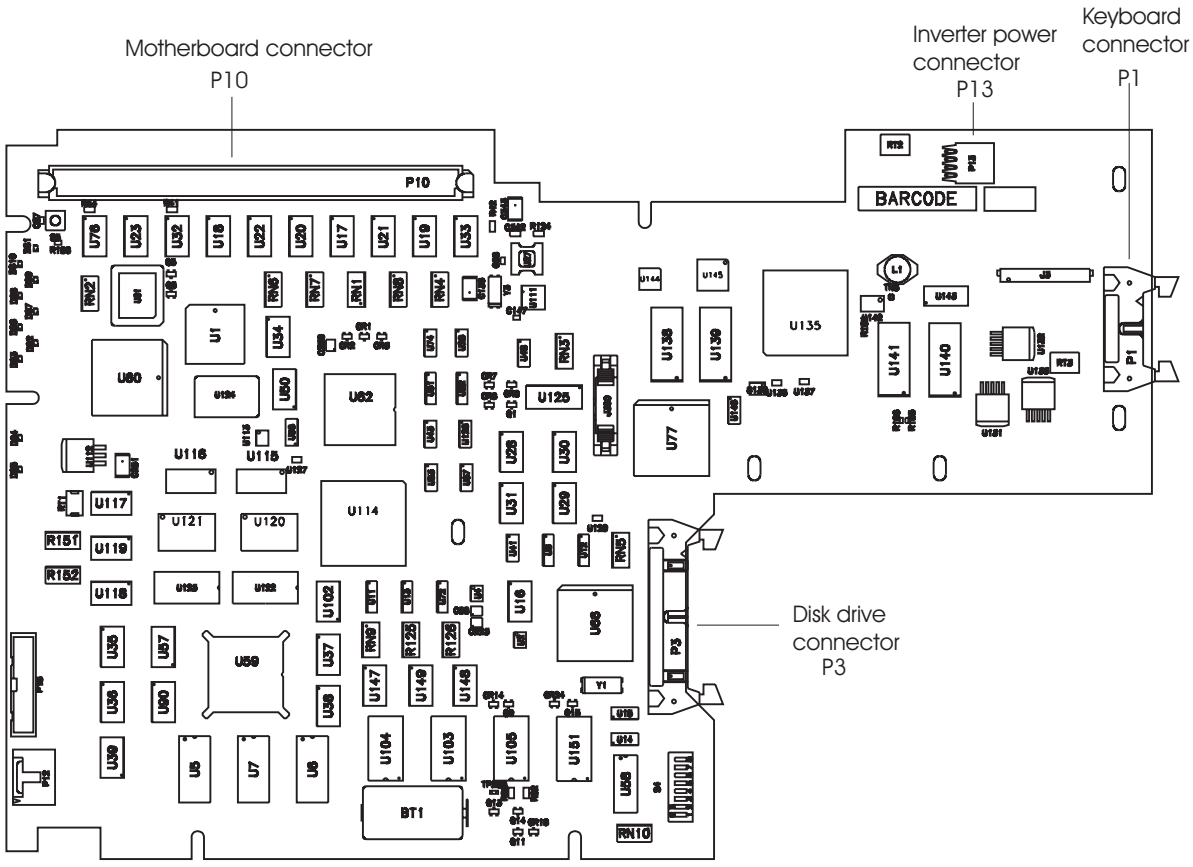

Figure 6 A17 CPU board connector locator, component side

To troubleshoot power-up failures

Page in original guide 4-15

Replace the first five rows of the table:

Failing Power-up Message	Probable Faulty Assembly or Next Test
LEDs MC68030 Processor MC68882 Coprocessor Bootrom Display	A17 CPU
Main RAM ProgramROM	A17 CPU
DSP	A17 CPU
Fast bus	A17 CPU
MFP	A17 CPU

To troubleshoot CPU, memory and buses failures

Page in original guide 4-19

Step 1: Disregard references to Memory Assembly and incorporate the related information into A17 CPU.

Step2: Illustration for component locator shows new connector locations

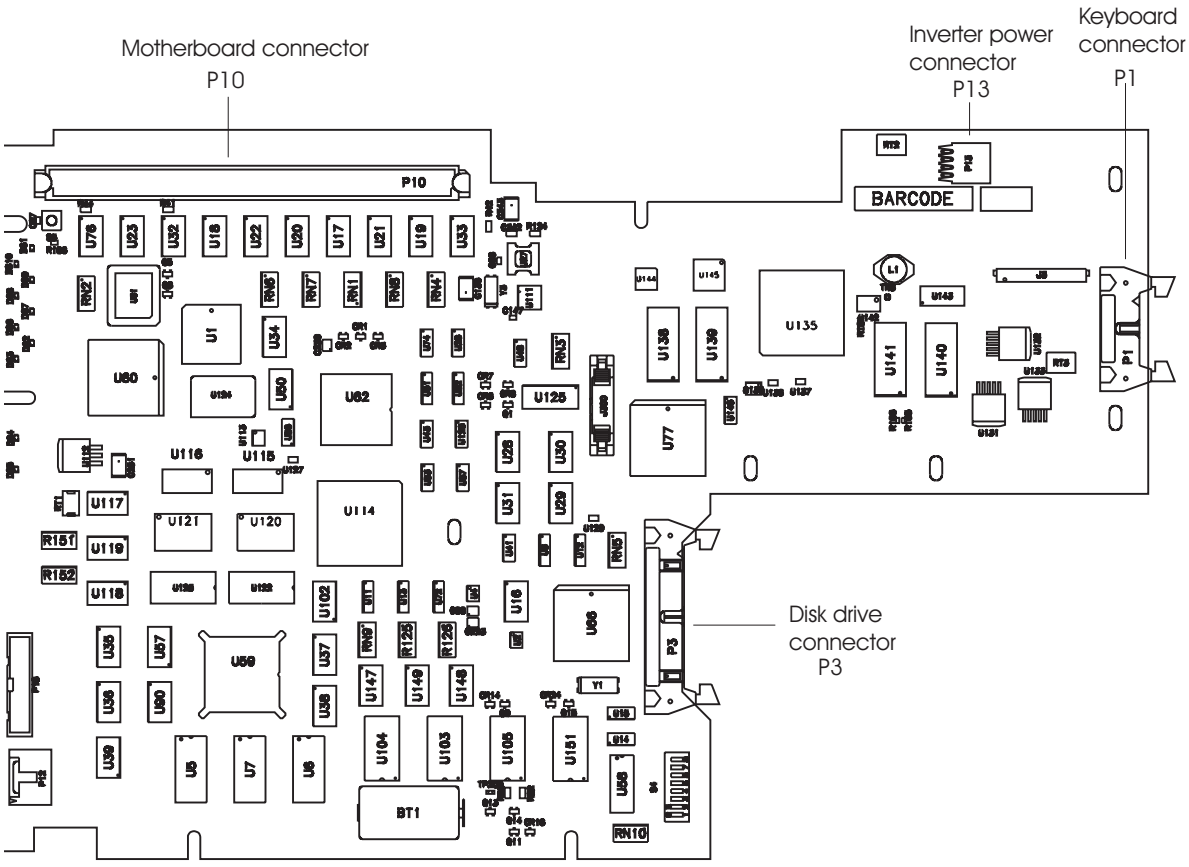

Figure 7 A17 CPU board connector locator, component side

To troubleshoot display failures

Page in original guide 4-23

Replace entire section

Use this test to isolate display failures to the A101 Display assembly, A102 assembly, or the A17 CPU assembly

✔ Step 1. Check the power inverter assembly.

- Set the power switch to off (O).
- Remove the cable connected to P13 on the A17 assembly.
- Set the power switch to on (|)
- Measure voltage at P13 pin 1 on A17 assembly.
- If voltage is not +5Vdc the A17 board may be faulty.
- Set the power switch to off (O).
- Reconnect the cable to P13.
- Set the power switch to on (|).
- Measure voltage at A17 P13 pin 1.
- If voltage is not +5Vdc the power inverter assembly may be faulty.
- If display backlight lamps do not light up, one or both of the lamps may be faulty.
- If lamps are replaced and still do not light up, the power inverter may be faulty.

✔ Step 2. Check the CPU signals on the Display assembly.

- Set the power switch to on (|).
- Using a logic probe check that the following TTL signals are toggling:

Test Location	Signal Name	In/Out
P14-31	VSYNCLCD	A17 Out
P14-33	HSYNCLCD	A17 Out
P14-24	CLK_LCD	A17 Out

- If the signals are incorrect the A17 board may be faulty.

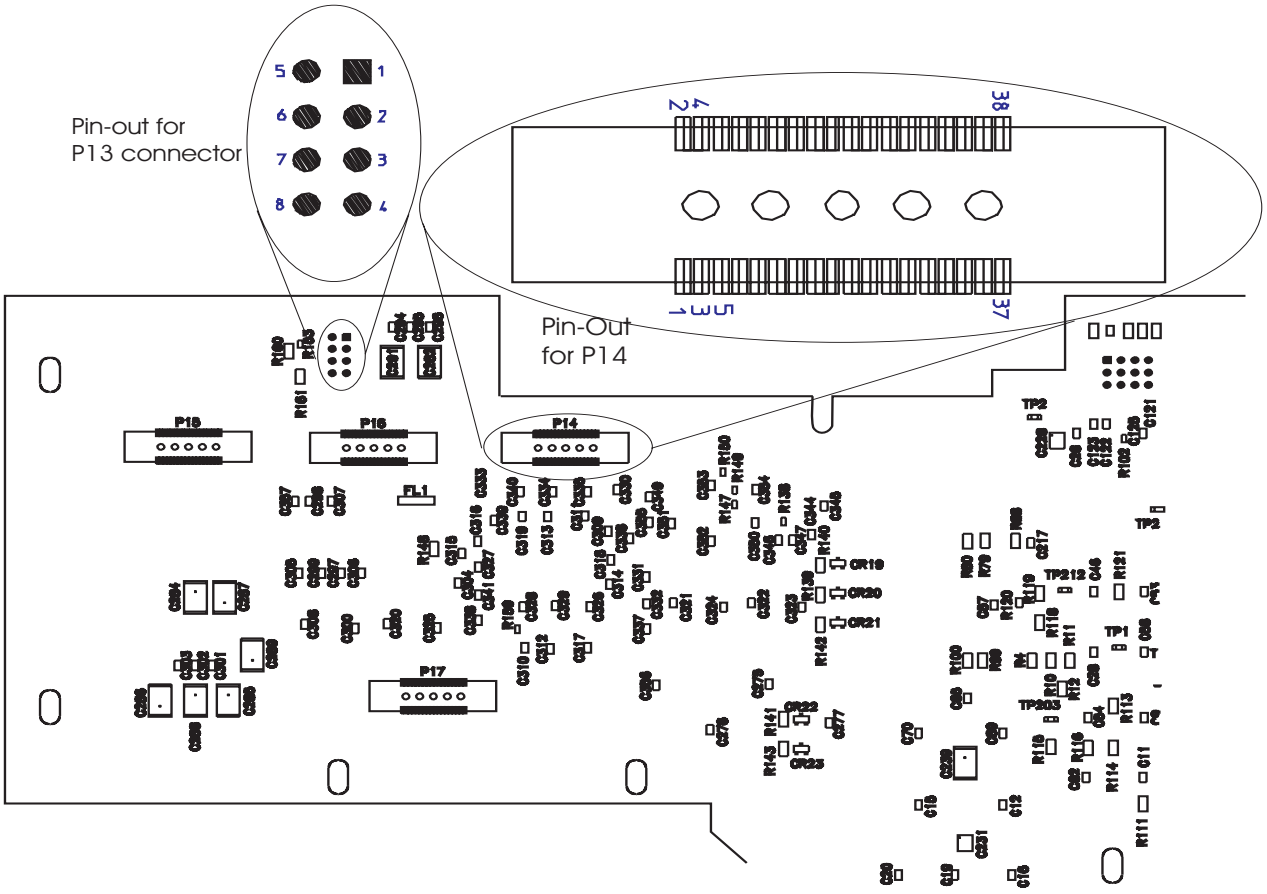

Figure 8 A17 CPU board connector locator, circuit side

✔ Step 3. Determine the probable faulty assembly by comparing the analyzer's symptoms to the following table.

Symptom	Probable Faulty Assembly
Vertical and horizontal scanning is occurring Part of information is missing, for example only half letters Blocks of information are missing Information on the screen is scrambled or mixed up Vertical or horizontal stripes appear across the screen	CPU
Screen is blank	Display, Power inverter, Display backlights, cables
Screen is tilted, compressed, or distorted Line across the screen	Display, A17

To troubleshoot IIC bus failures

Page in original guide 4-26,27

A new illustration above step 2 shows new connector pin-outs:

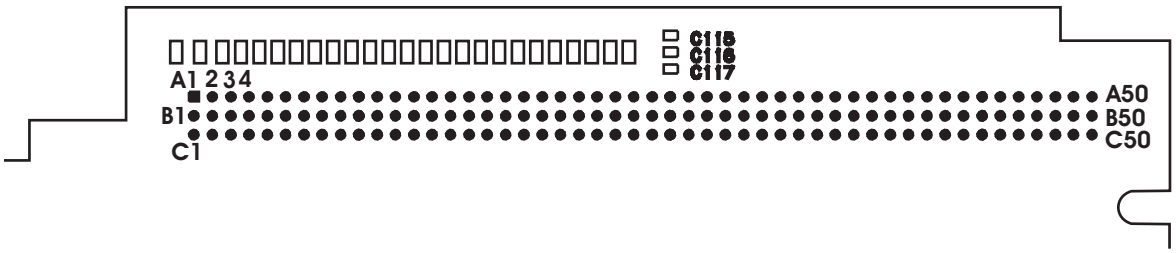

Figure 9 A17 CPU motherboard (P10) connector pin locations

✔ Step 2. Check the serial clock (SCL).

- Attach a logic probe to A17 P1-15 (SCL) or P10 pin B10.
- Set the power switch to on (|).
- Press S5 (reset switch) while monitoring A17 P10 pin B10 (SCL), the power-on LEDs, and the display.

NOTE **S5 (reset switch) is a normally open momentary switch. A press of the switch, S5, can be simulated by temporarily shorting TP214(RESET INn) to TP215 (DCOM).**

The TTL logic level of the SCL signal should toggle continuously while **Booting System** is displayed. The following failure message should be displayed after **Booting System** and the display grid should appear about two minutes after power up.

Front Panel failure information:
keyboard IIC chip fails:
IIC: No Device Acknowledge
Key stuck: 32

A power-on test has failed. Refer servicing to qualified personnel.

Press Start key to attempt to continue Power-up.

- If the SCL signal does not toggle after S5 is pressed, the A17 CPU assembly is probably faulty

- If no error messages are displayed after **Booting System** or A17 DS101 (green run LED) is off, go to page 4-29, "To troubleshoot fast bus failures."

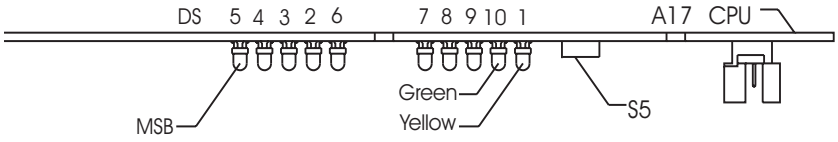

Figure 10 Power-on LEDs and reset switch

✔ Step 3. Check the serial data line (SDA).

- Attach the logic probe to A17 P10 pin C11 (SDA).
- Press S5 while monitoring A17 P10 pin C11 (SDA), the power on LEDs and the display.

The TTL logic level of the SCL signal should toggle continuously while **Booting System** is displayed. The following failure message should be displayed after **Booting System** and the display grid should appear about two minutes after power up.

Front Panel failure information:
keyboard IIC chip fails:
IIC: No Device Acknowledge
Key stuck: 32

A power-on test has failed. Refer servicing to qualified personnel.

Press Start key to attempt to continue Power-up.

- If the SCL signal does not toggle after S5 is pressed or the failure message is not displayed, the A17 CPU assembly is probably faulty.

To troubleshoot fast bus failures

Page in original guide 4-30

New table:

A17 P10 Pin	Signal Name	TTL Logic State in Test Mode
B14, C14, B15, C15, B16	FA1 to FA5	Toggling
B22	ECLK	Toggling
B24	FSELAn	Toggling
C12	BRESETn	Low
C19	FRW	Toggling
C23	FIFOENn	High
C24	FSELSn	Toggling

New illustration showing location of motherboard connector pins.

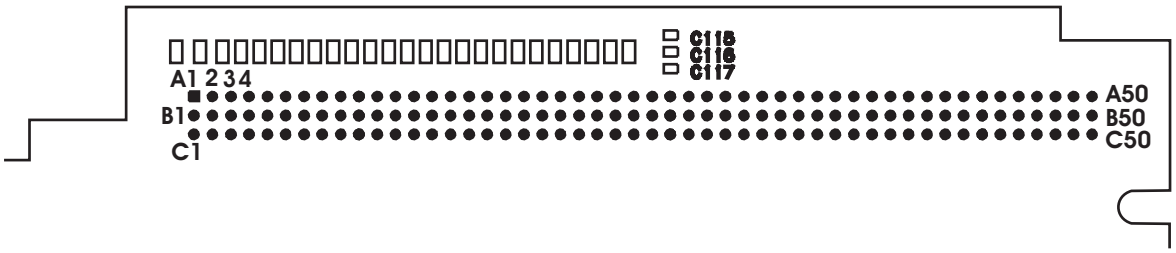

Figure 11 A17 CPU motherboard (P10) connector pin locations

To troubleshoot memory or battery failures

Page in original guide 4-67,68

Replace the last five bulleted items:

- If the date is 01-01-01, the battery-backed-up memory is functioning correctly. Enter the current date. Go to page 4-13, “To perform self tests,” to continue troubleshooting.
- Set power switch to off (O)
- Check that the voltage at TP200 is 2.6Vdc to 3.1Vdc.
- If the voltage is correct, the memory is probably faulty.
- If the voltage is incorrect, replace the battery BT1.

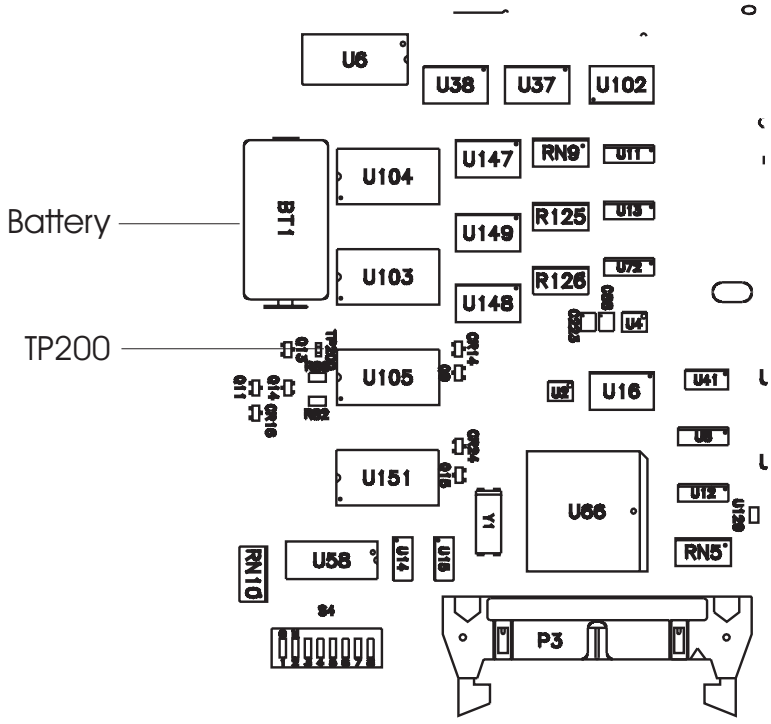

Figure 12 Battery location

Adjusting the Analyzer

Adjusting the analyzer

Page in original guide 5-2

Delete the first row of the table referring to frequency reference. The frequency is no longer adjustable.

To adjust the frequency reference

Page in original guide 5-5

Disregard this section. The frequency reference is not adjustable.

To adjust the display voltage

Page in original guide 5-21,22

Disregard this section. The display voltage is not adjustable.

Replacing Assemblies

What to do before replacing the CPU assembly

Page in original guide 6-3

The EEPROM is now U111 on the A17 CPU assembly.

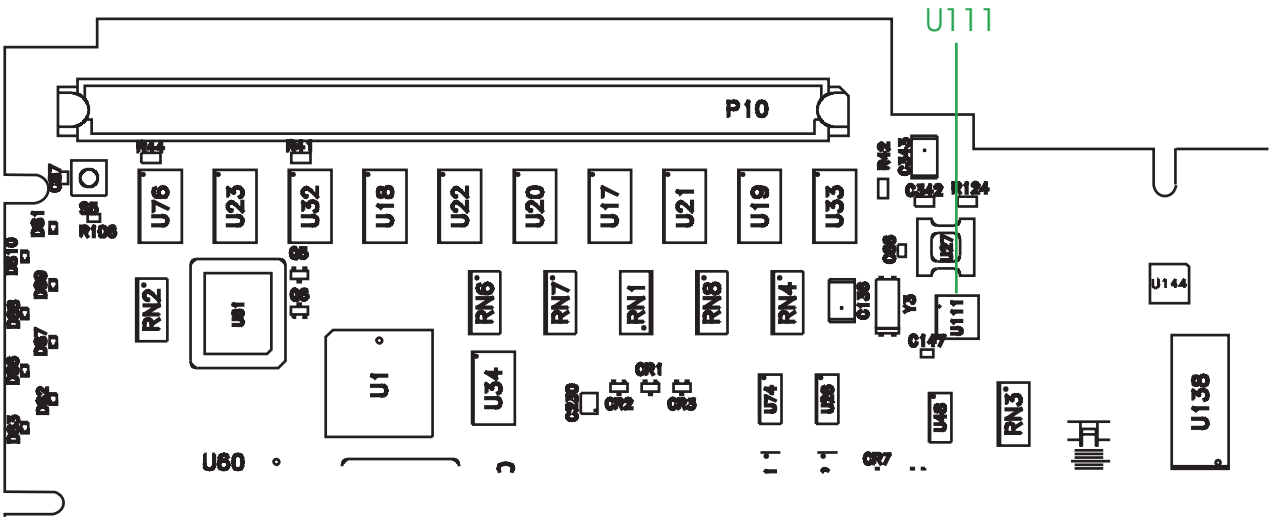

Figure 13 Location of U111

What to do after replacing an assembly

Page in original guide 6-5

The rows referring to A7 CPU, A8 Memory, and A9 NVRAM are replaced with:

Assembly Replaced	Required Adjustment	Required Performance Test
A17 CPU	No	No

Note that the frequency adjustment is no longer needed.

Disregard the last two rows of the table referring to adjustments of the Display and the DC-DC Converter (now a Power Inverter). There are no adjustments for these items.

To remove CPU

Page in original guide 6-11

New illustration in step 3 showing an additional cable:

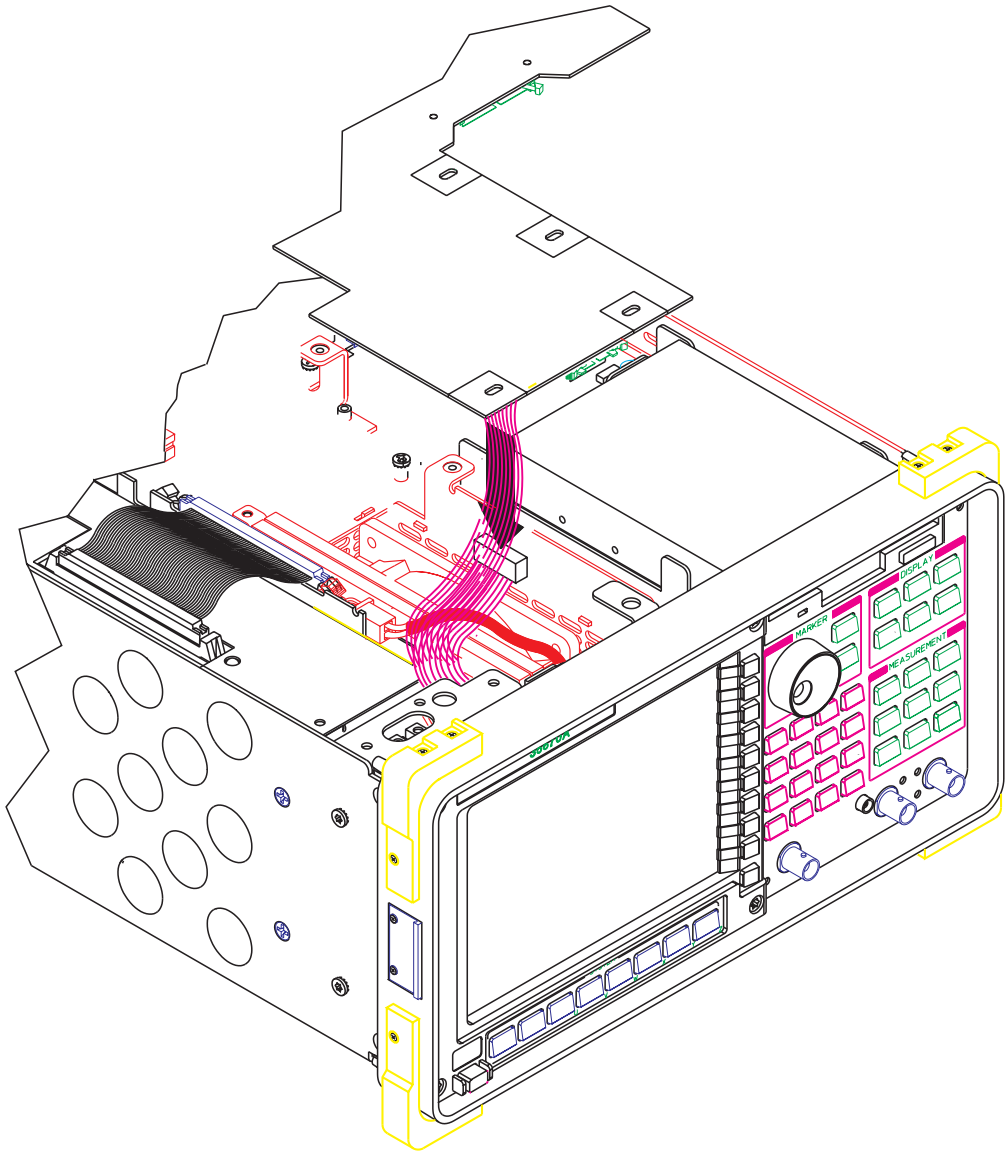

Figure 14 Disconnect the cables from A17

To remove NVRAM

Page in original guide 6-12

Disregard this section. The NVRAM is now on the CPU board.

To remove memory

Page in original guide 6-13

Disregard this section. The memory in now on the CPU board.

To remove motherboard

Page in original guide 6-17

Disregard step 5.

Replaceable Parts

Assemblies

Page in original guide 7-4

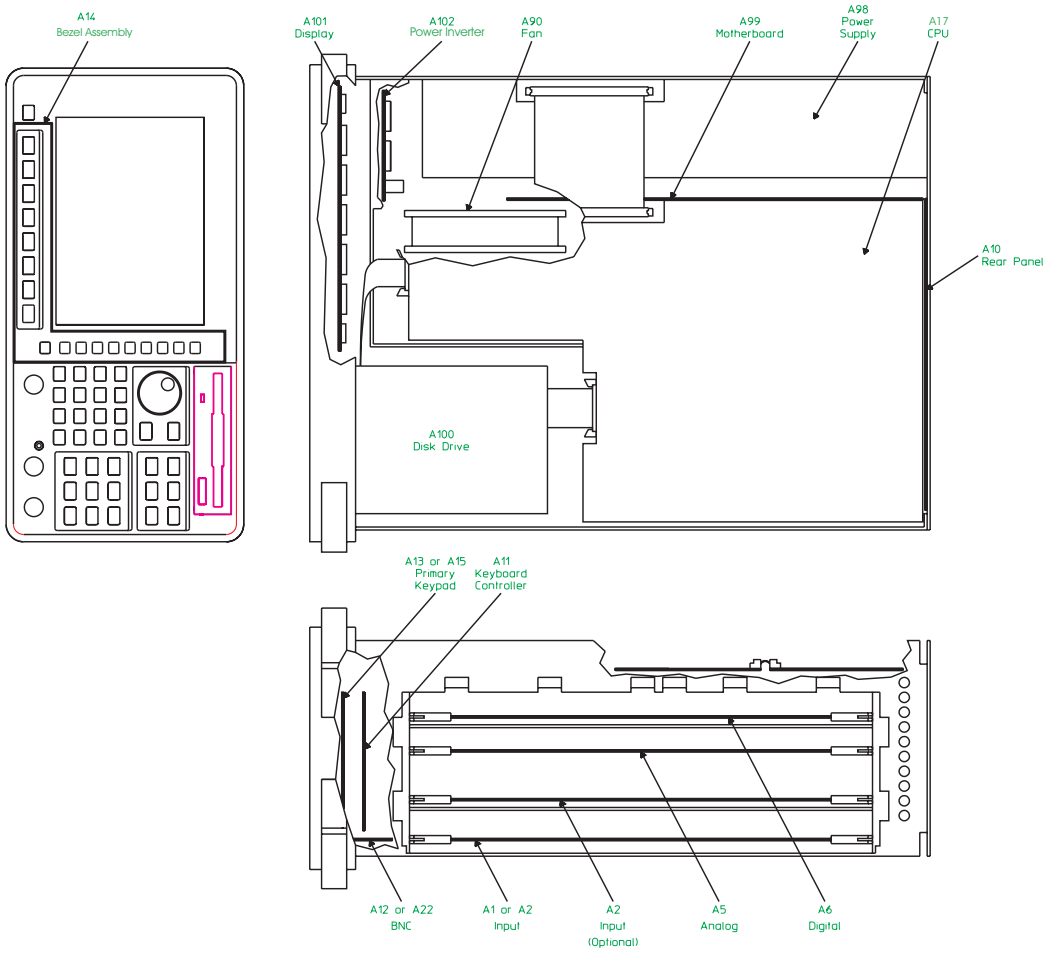

Figure 15 Assemblies

Reference designator A17 replaces A7, A8 and A9. There is also a replacement motherboard, bezel assembly, display assembly and DC-DC converter assembly.

Ref Des	Agilent Part Number	Description
A17	35670-66517	CPU ASSEMBY
A99	35670-66598	MOTHERBOARD
A14	35670-64320	BEZEL ASSEMBLY
A101	2090-0881	VGA DISPLAY ASSEMBLY
A102	35670-66525	INVERTER ASSEMBLY

Cables

Page in original guide 7-6

Disregard Memory and NVRAM sections of block diagram.

Four new cables have been added:

Agilent Part Number	Description
35670-61626	EXTERNAL MONITOR CABLE
35670-61627	INVERTER CABLE
3670-61628	EXTENDER CABLE FOR CCFL TUBES
3670-61624	DISPLAY CABLE

Instrument Covers and Handles

Page in original guide 7-7

Two parts have been replaced:

Ref Des	Agilent Part Number	Description
MP1	35670-64101	SHTF ASSY-COVER ALV
MP4	5063-5523	MOLD BUMPER SET 4PC FF CORNRS

Front Panel Parts

Page in original guide 7-9

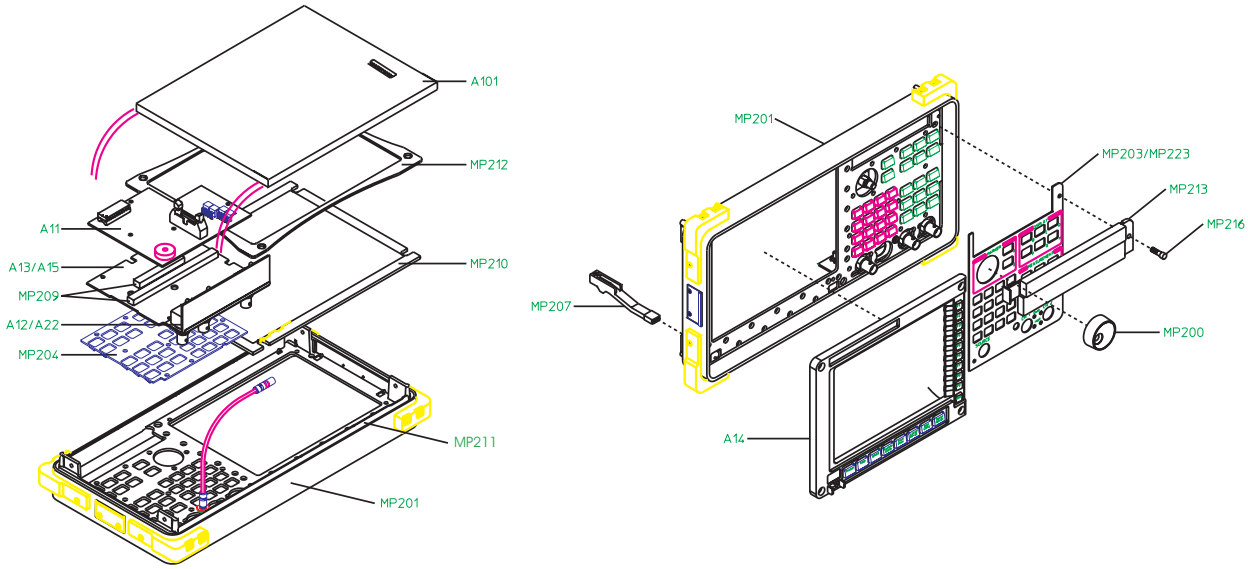

Figure 16 Front panel parts

Three parts have been replaced and a new one added:

Ref Des	Agilent Part Number	Description
MP201	35670-22021	CSTG-FRT FRAME MACH&PAINTED
MP210	35670-29321	LNZ-FLTR RFI/OPTICAL
MP212	35670-44723	DISPLAY GASKET
MP211	8160-1502	4 RFI ELASTOMER STRIPS

Rear Panel Parts

Page in original guide 7-10

One part has been replaced:

Ref Des	Agilent Part Number	Description
MP300	35670-00221	SHTF REAR PANEL W/SILKSCREEN

Chassis Parts

Page in original guide 7-11

Two parts have been replaced:

Ref Des	Agilent Part Number	Description
MP400	35670-00122	SHTF-CHASSIS ASSY
MP401	35670-00123	SHTF WALL ASSY FRONT

Miscellaneous Parts

Page in original guide 7-12

One part has been replaced and a new part has been added:

Ref Des	Qty	Agilent Part Number	Description	Mfr Code	Mfr Part Number
A17BT1	1	1420-0338	BATTERY - 3V LITIUM	08709	BR2/3EAE2P
	2	2090-0896	Backlight (CCFL) lamps	NEC	63LHS01

Circuit Descriptions

Overall Block Diagram

Page in original guide 8-4,5

The Memory and NVRAM assemblies are now incorporated into the CPU assembly. The additional NVRAM option assembly is now standard and consolidated onto the CPU assembly.

The DC-DC Converter has been replaced with a Power Inverter which generates the display backlight voltage.

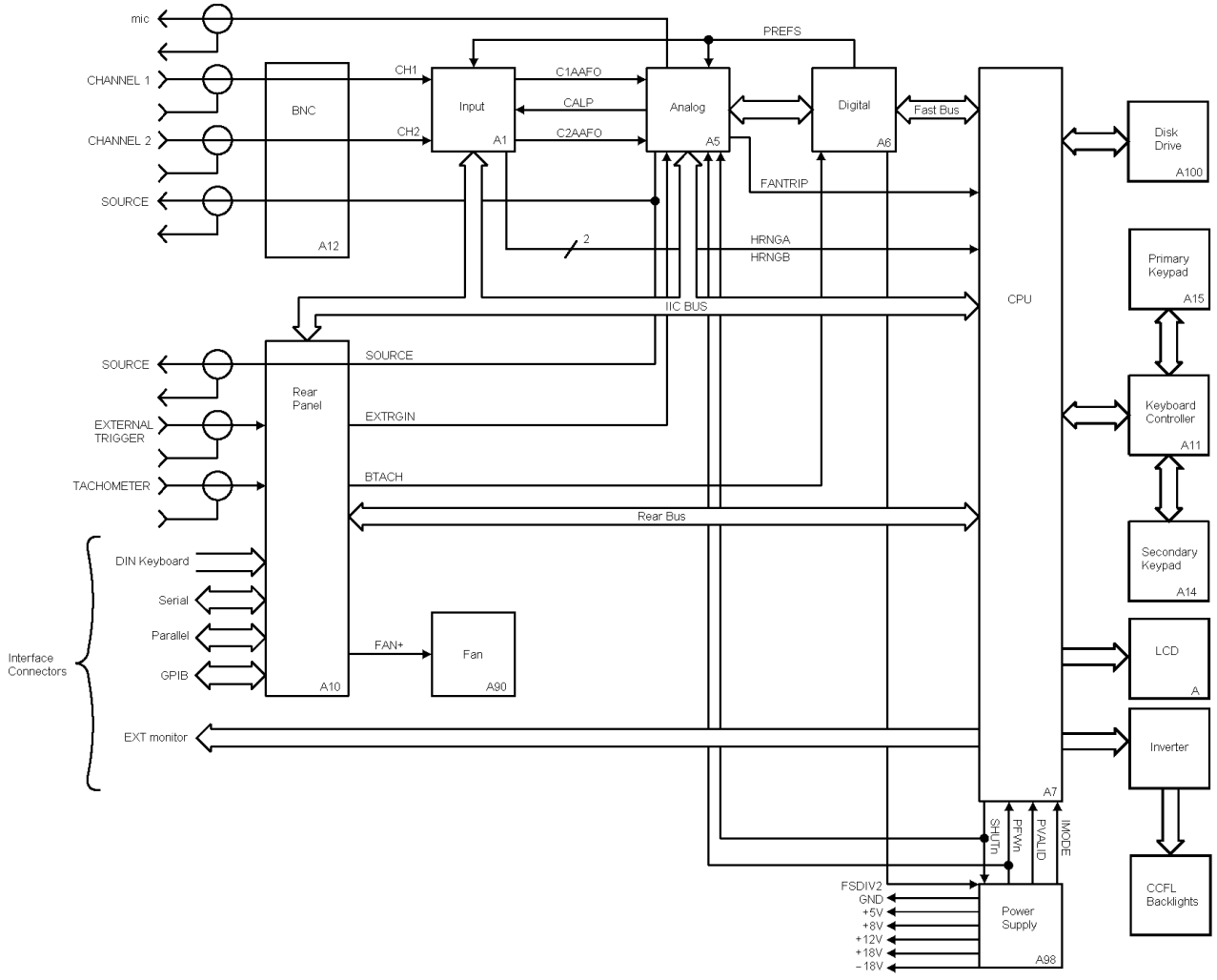

Figure 17 Two channel overall block diagram

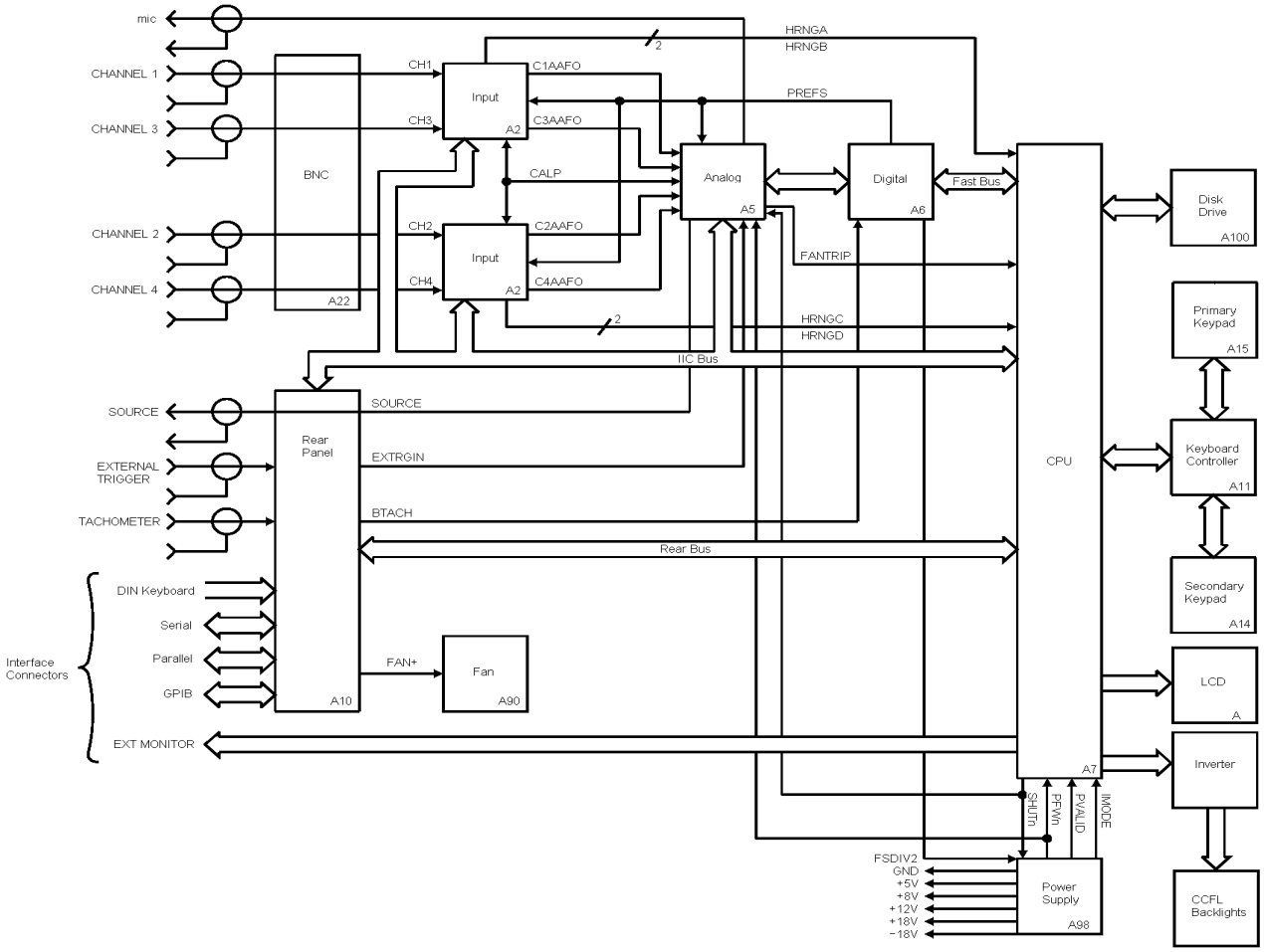

Figure 18 Four channel overall block diagram

A7 CPU

Page in original guide 8-26 through 29

This is now the A17 CPU. Delete all references to A8 memory and A9 NVRAM as separate assemblies since they are now incorporated on the CPU board.

The A17 board now includes Non-Volatile Memory Storage operations among its tasks.

The Math Co-processor is 20 MHz rather than 40 MHz (error in previous documentation).

The 40 MHz oscillator is now a precision clock oscillator and is no longer adjustable.

Clock Circuits Provide the clocks for the CPU assembly and all other assemblies.

New block diagrams:

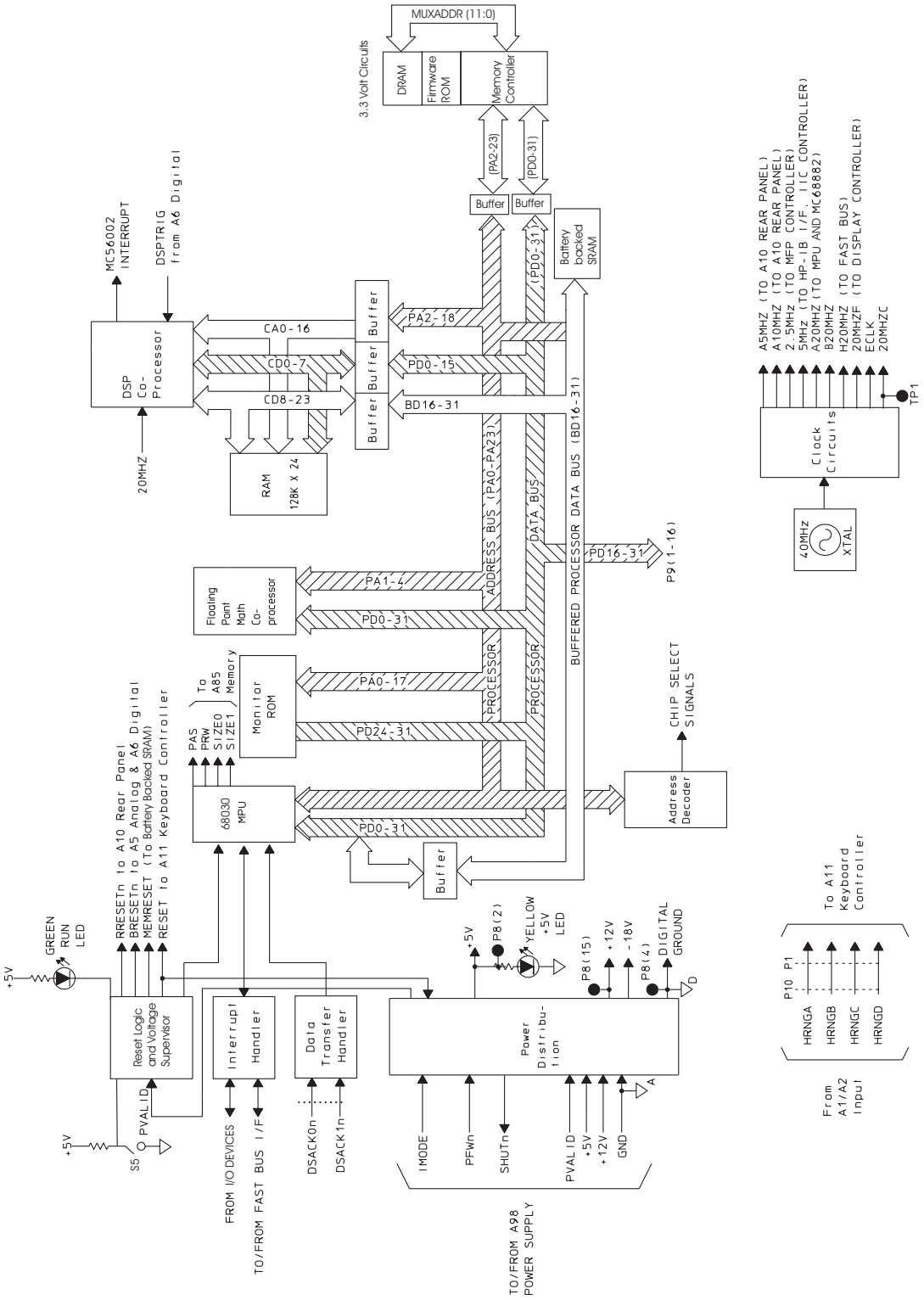

Figure 19 A17 CPU Block Diagram

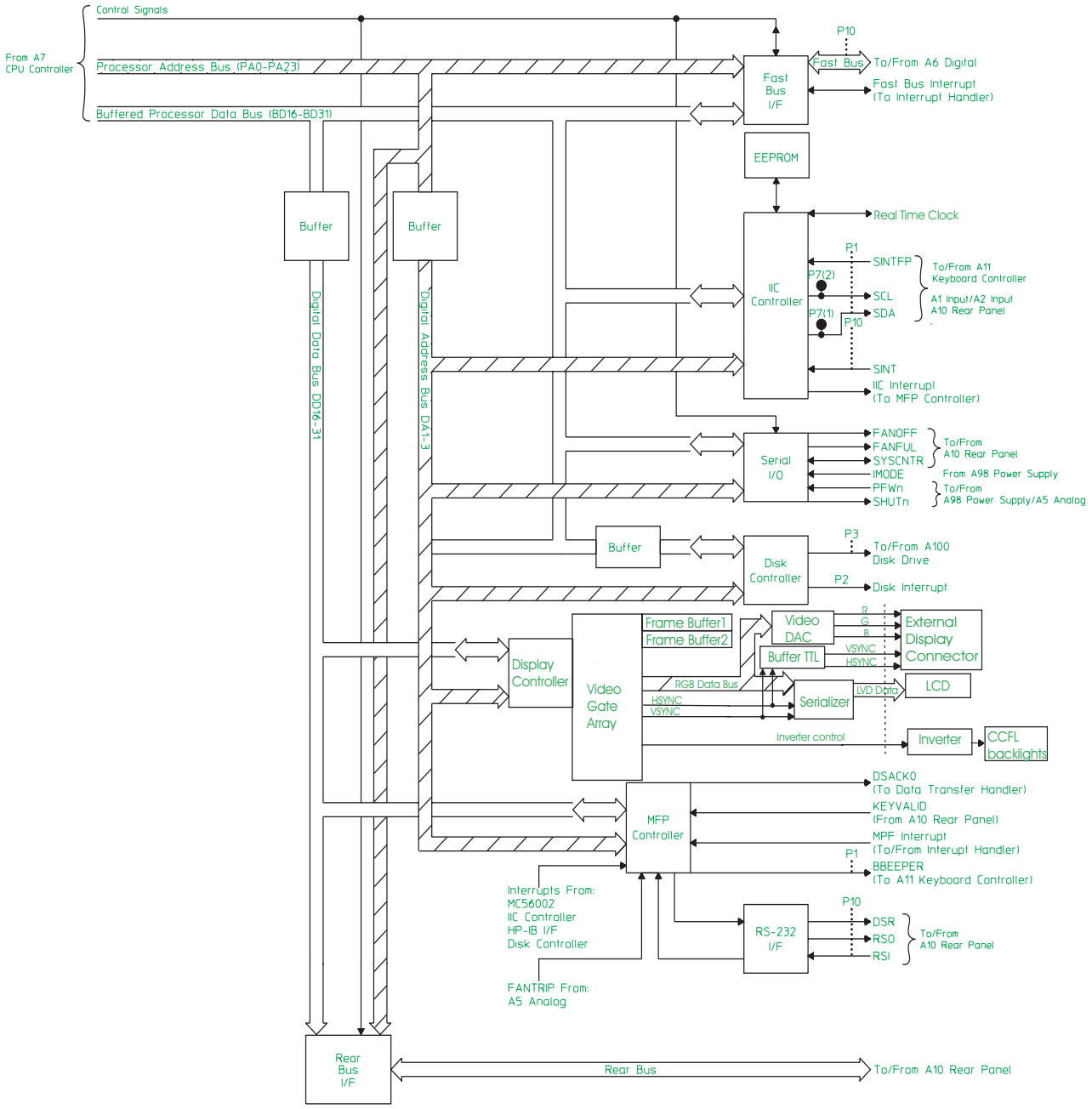

Figure 20 CPU Block Diagram: Interface

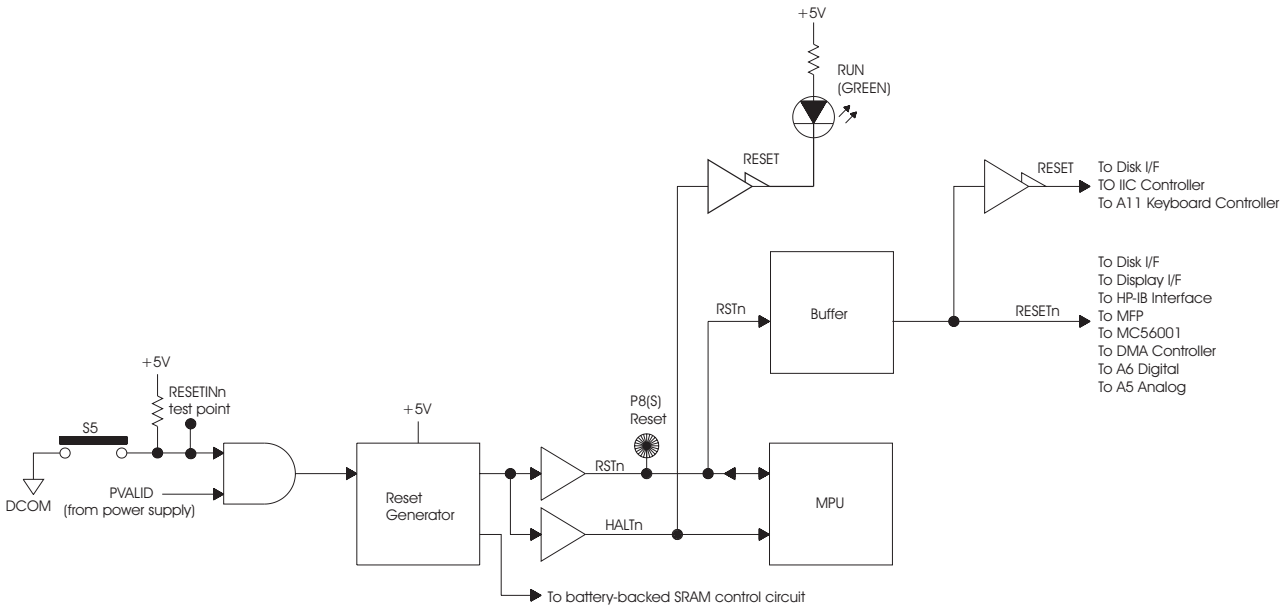

Figure 21 Reset logic

Reset logic all references to S2 are changed to S5 and there is a new block diagram.

IIC (Inter_IC) controller the bullet referring to A8 memory is replaced:

- A17 CPU (Real time clock, EEPROM)

Disk Controller Disregard the final sentence referring to reversed operation.

Frame Memory Consists of four SRAM chips.

A8 Memory

Page in original guide 8-30,31

The memory has been incorporated into the CPU board. Therefore, the information in the sections on Memory Controller and FLASH ROM, DRAM, and SRAM is now added to the section on the A17 CPU. Disregard the rest of this section

A9 NVRAM

Page in original guide 8-32

The NVRAM has been incorporated into the CPU board. Disregard this section.

A102 DC-DC Converter

Page in original guide 8-39

This is now a power inverter assembly which supplies the voltage for the LCD display backlights (CCFL).

Voltages and Signals

Voltages and Signals

Voltages and Signals

Page in original guide 9-2

The references in the table to A8 Memory and A9 NVRAM are deleted since the circuits are now consolidated onto the A17 CPU board.

Assembly Locations and Connections

Page in original guide 9-3,4,5

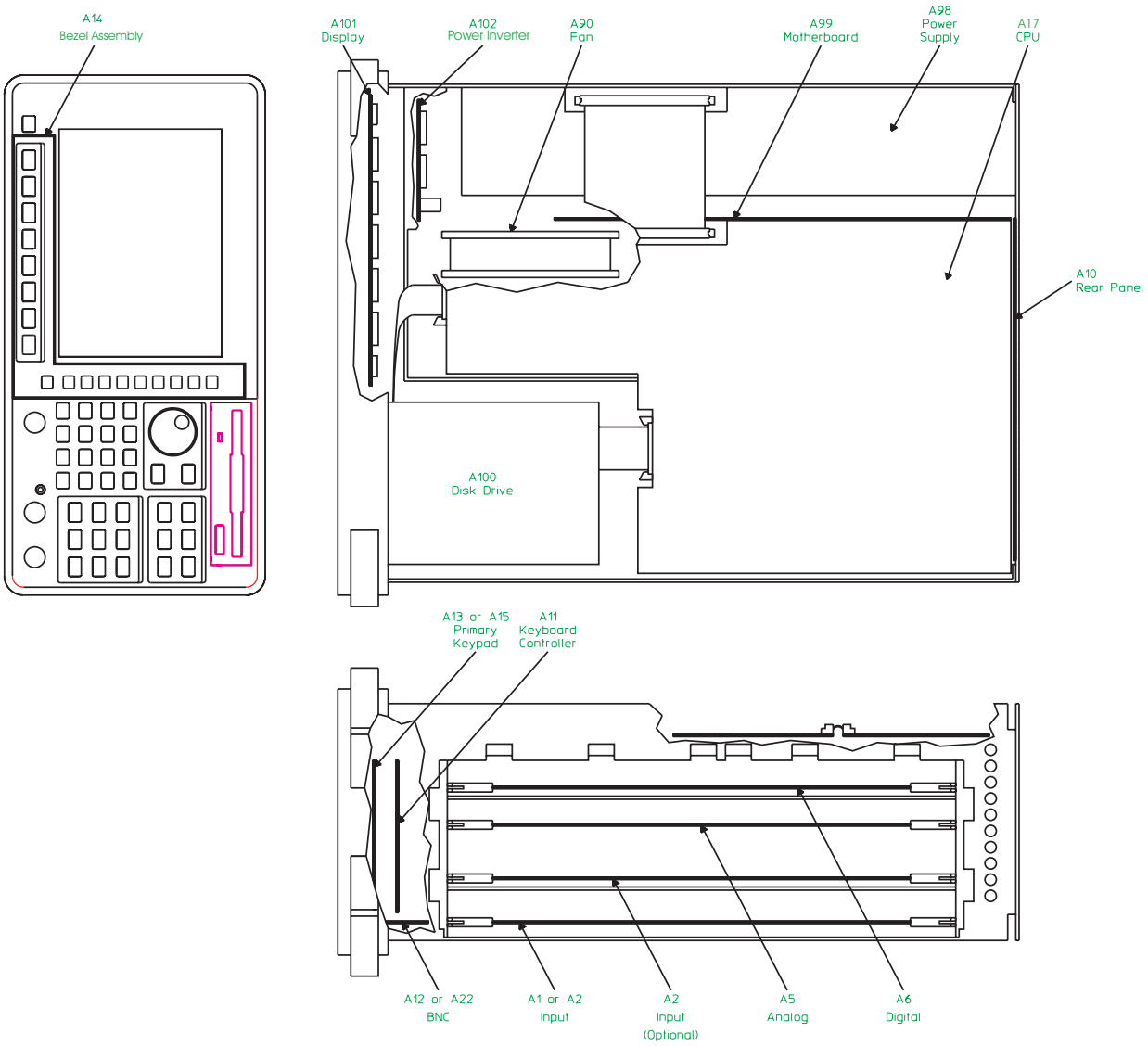

Figure 22 Assembly locations

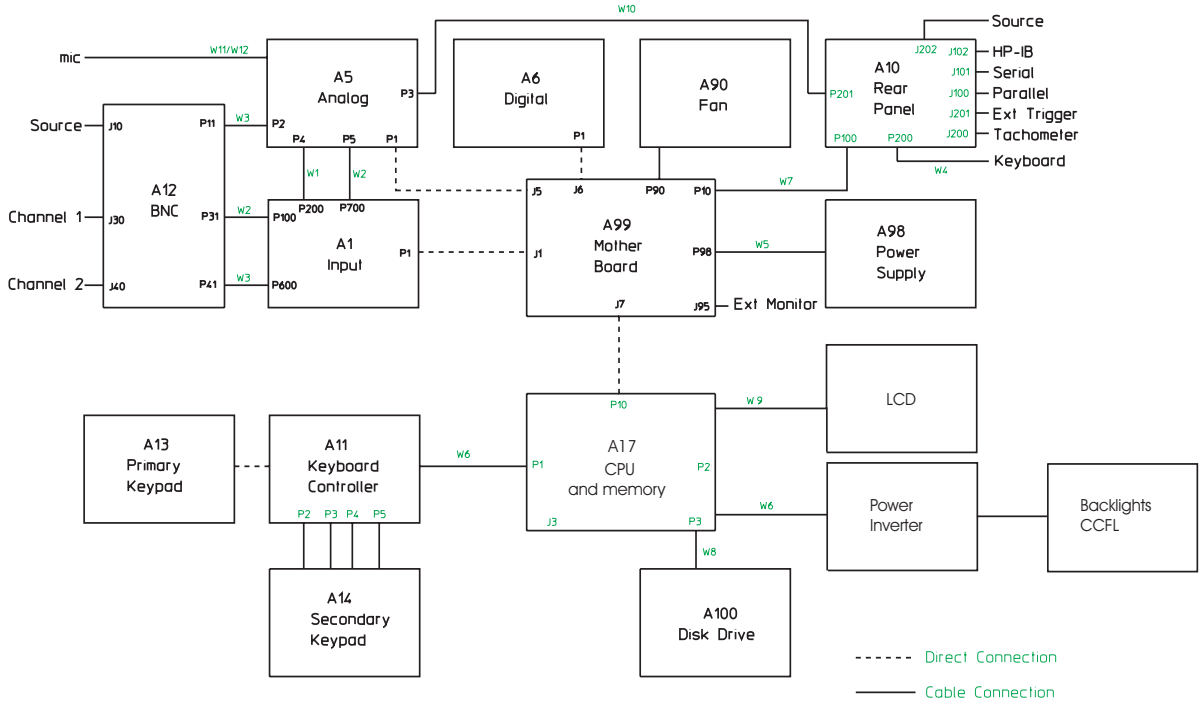

Figure 23 Assembly connections for two-channel analyzer

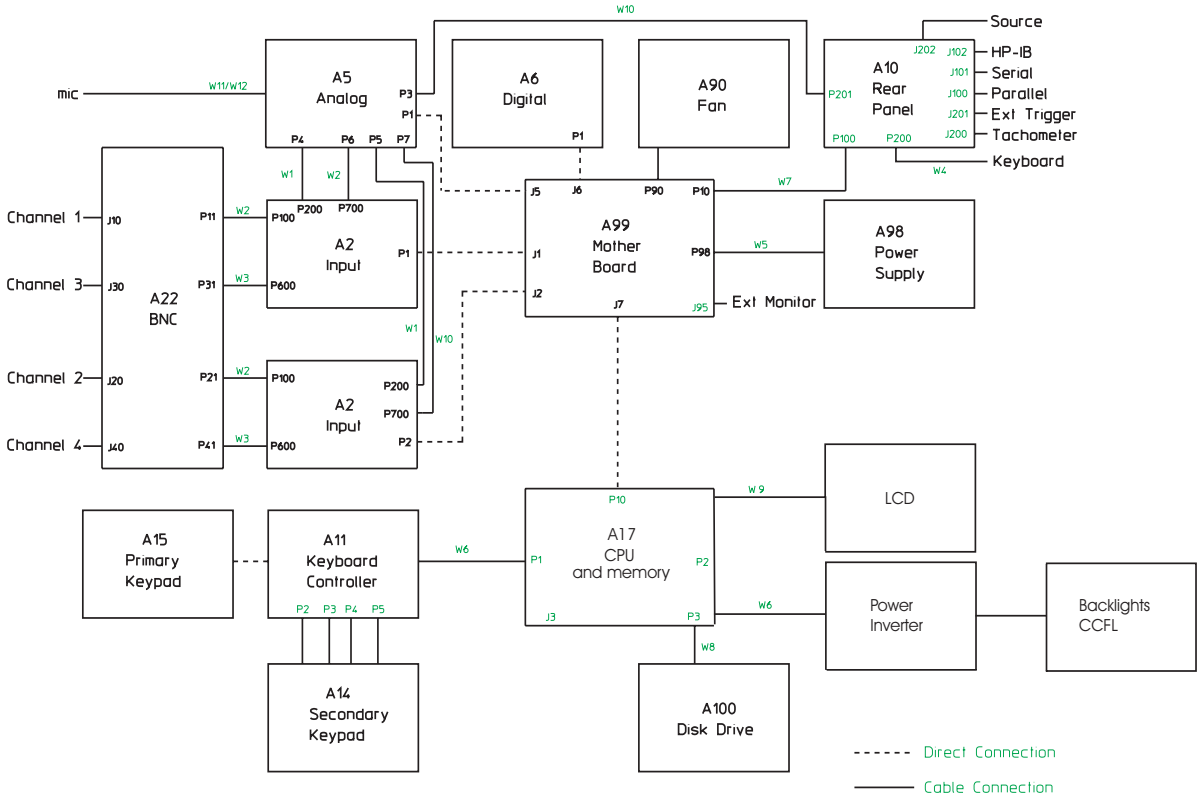

Figure 24 Assembly connections for four-channel analyzer

Power Supply Voltage Distribution

Page in original guide 9-6

In the table the references to paths to the A8 and A9 boards is deleted since the circuits are now on the A17 CPU board.

A8 Memory

Page in original guide 9-8 through 9-11

The memory is in now incorporated into the A17 CPU board and the following information should be transferred to the A17 signal descriptions:

BD16-31	Buffered Data Bus–This is the buffered processor data bus from the A17 CPU assembly. This bus is further buffered on the A17 CPU assembly to create the Device Data bus.
DSACK0n—DSACK1n	Data Strobe Acknowledge–During a write cycle, DSACK signals are set low when the device being addressed is ready to end the memory access cycle. When DSACK0n goes low and DSACK1n is low, 32 bits of data are valid. When DSACK0n goes low and DSACK1n is high, 8 bits of data are valid.
PA0—PA26	Processor Address Bus–This is the processor address bus from the CPU. PA0 and PA1 also operate with SIZE0 and SIZE1 to specify the alignment of the operand.
PASn	Processor Address Strobe–A low on this line starts a memory access cycle. This line pulses low when a valid address is on the processor address bus.
PD0—15	Processor Data Bus–This is the processor data bus.
PRW	Processor Read/Write–This line is high when the current memory cycle is a read, and low when the current memory cycle is a write.
SCL	Serial Clock–This is the serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock to synchronize the transfer of data on the IIC bus.
SDA	Serial Data–This is the IIC bus bidirectional data line.

Everything else in the section should be disregarded.

A9 NVRAM

Page in original guide 9-12, 13

The NVRAM is in now incorporated into the A17 CPU board and the following information should be transferred to the A17 signal descriptions:

PROTCTn	Protect–A low on this line disables the battery-backed static RAM. This line is low during power-up and power-down, when the CPU assembly's microprocessor is externally reset, and when +5 volts is too low.
VBATT	Battery Voltage–This line provides the power to the battery-backed static RAM and real time clock. When the analyzer is on, the +5 volts provides the power for this line. When the analyzer is off, the battery on the A17 board provides the power for this line. Since power is applied to the static RAM even when the analyzer is off, the static RAM is non-volatile.

Everything else in the section should be disregarded.

A99 Motherboard

Page in original guide 9-31,33

Disregard the sections on HSYNC, VDATA, and VSYNC

A101 Display

Page in original guide 9-36

The following table lists signals routed between the A17 board and the LCD display assembly. All signals are generated on the A17 board and are used by the display assembly. A description of each signal follows the table. All data lines are LVDS.

CLK +	6
CLK –	7
Pixel Data 2 +	9
Pixel Data 2 –	10
Pixel Data 1 +	12
Pixel Data 1 –	13
Pixel Data 0 +	15
Pixel Data 0 –	16
VCC	19,20
Gnd	1,2,3,4,5,8,11,14,17,18

CLK: LVDS pair carrying the 66.660MHz clock signal used by the LCD screen

Pixel Data 2: LVDS pair carrying blue pixel bits 4 to 7, Hsync, Vsync, and Data enable signals

Pixel Data 1: LVDS pair carrying green pixel bits 3 to 7, and blue pixels bits 2 to 3

Pixel Data 0: LVDS pair carrying red pixel bits 2 to 7, and green pixels bit 2.

VCC: 3.3 Volts.

A102 DC-DC Converter

Page in original guide 9-37

This assembly is now a Power Inverter.

The following table lists signals routed between the A17 board and the A102 Power Inverter. A description of each signal follows the table:

VCC	1,2
Gnd	3,4,7,8
BLight_ON	5

VCC: 5 Volts

BLight_ON: Generated by U135 to turn on and off the display backlights for power saver mode.