Release Notes

Keysight Logic and Protocol Analyzer Software (64-bit Application)

Version 6.71 – November 2020

Operating System Compatibility

Version 6.71 of the Keysight Logic and Protocol Analyzer software is a 64-bit application and therefore it is only supported for use with 64-bit operating systems.

Recommended operating systems:

- Windows® 10
- Windows® 8.1
- Windows® 8
- Windows® 7
- Windows® Server 2012 R2
- Windows® Server 2012
- Windows® Server 2008 R2
- Windows® Server 2008
- Windows® Vista 64-bit (SP2)

Notes:

- Keysight recommends you install the latest service pack offered for your operating system. In addition, apply all critical operating system updates.
- Each OS variant places a different limit to the amount of physical memory supported to the system. Users should consult their system's documentation to determine how much memory their specific operating system variant will support. For optimum performance of the Logic and Protocol Analyzer software, Keysight recommends installing more than the minimum required system memory.
- Version 6.00 or higher of the Logic and Protocol Analyzer software is **not** compatible with 32-bit operating systems. Version 5.90 or lower of the Logic and Protocol Analyzer software is supported for use with 32-bit operating systems.

KEYSIGHT TECHNOLOGIES

Hardware Prerequisites

Keysight 16860A and 16850A Series Portable Logic Analyzers and the Keysight M9537A and M9536A embedded controllers for AXIe modular systems are fully compatible with the Logic and Protocol Analyzer software.

The following recommendations are for M950xA AXIe modular systems with an external host PC (desktop or laptop) running the Logic and Protocol Analyzer software.

- The minimum CPU, memory, and graphics specified for your chosen operating system
- Increase RAM to 4 GB minimum, or more (e.g. 8 GB is recommended for a multiple module logic and protocol analysis system)
- Increase CPU performance to a minimum of 2 GHz dual core processing
- 80 GB minimum hard drive, SSD recommended for loading/storing configurations and acquired data

Additionally, for an external host PC (desktop or laptop) connected to an M9502A or M9505A AXIe chassis or a U4002A AMP chassis, the appropriate IO support for the chassis is required.

- Cabled PCIe is the recommended IO option

Supported Instruments

If you do not see your specific logic or protocol analyzer listed here, please refer to www.keysight.com/find/la-sw-download to determine the correct software to use for your instrument.

- 16860A Series Portable Logic Analyzers
- 16850A Series Portable Logic Analyzers
- U4164A Logic Analyzer Module
- U4154B Logic Analyzer Module
- U4154A Logic Analyzer Module
- U4301B Protocol Analyzer Module for PCIe 8 Gbps
- U4301A Protocol Analyzer Module for PCIe 8 Gbps
- U4421A Protocol test module for MIPI D-PHY
- U4331A protocol test module for MIPI M-PHY

How to Download

- Click the download button, select file and save.

How to Install

The Logic and Protocol Analyzer software install directory is:

"C:\Program Files\Keysight Technologies\Logic Analyzer\".

Licenses for options to the U4154A, U4301A, and U4421A modules, as well as licenses for software add-ins and features released prior to version 6.00, are installed in the following directory:

"C:\Program Files (x86)\Agilent Technologies\Logic Analyzer\License"

Licensing

- The Logic and Protocol Analyzer application software does not require a license.
- Some hardware and software features and options are licensed. See the appropriate product data sheet for more information.

Supporting Documentation

- See Logic and Protocol Analyzer Readme (version 6.71.0000)
- See Logic and Protocol Analyzer Online Help Files (Version 6.71.0000)
- See Logic and Protocol Analyzer Online Help – PDF Version (Version 6.71.0000)

Add-On Software / Utilities

See www.keysight.com/find/lpa-sw-download for the most up-to-date list of software applications supported by version 6.00 and higher.

- B4621B DDR2/3/4 Bus Decoder
- B4622B DDR2/3/4, LPDDR2/3/4 Protocol Compliance and Analysis Tool
- B4623B LPDDR2/3/4 Bus Decoder
- B4661A Memory Analysis Software for Logic Analyzers
- DDR/LPDDR Memory Support Tools
- B4655A FPGA Dynamic Probe for Xilinx
- B4656A FPGA Dynamic Probe for Altera
- E9528A ARM Cortex ETM Trace Decoder
- E9529A ARM Cortex PTM Trace Decoder
- Analysis AddIn Wizard – Create custom plug-ins for the Logic and Protocol Analyzer
- B4641A Protocol Development Toolkit – Create custom protocol decoders
- License Server – Administer floating licenses shared within an organization
- COM Automation – Use the Logic and Protocol Analyzer COM interface from a PC or a laptop where the application has not been installed

The following add-on software products have been discontinued. The last software update for these tools occurred with software version 6.10.0000. The B462xB tools have been replaced by the B4661A Memory Analysis Software.

- B4621B DDR2/3/4 Bus Decoder
- B4622B DDR2/3/4, LPDDR2/3/4 Protocol Compliance and Analysis Tool
- B4623B LPDDR2/3/4 Bus Decoder
- DDR/LPDDR Memory Support Tools

Start the application software

1. Double click the Keysight LPA icon  located on your desktop.

   Or type “Analyzer” into the Search box in the Windows 7 start menu.

Release Contents

Logic and Protocol Analyzer Software Version 6.71.0000 (November 2020)

Additions

- New transaction decode filtering feature for Memory Analysis Viewer and ONFi Analysis Viewer
- External Scope support for Keysight Infiniium MXR-Series and EXR-Series Oscilloscopes
- New “pass” count feature for DDR4, DDR5, and LPDDR5 measurements in Real-Time Compliance Tool
- Configuration and DDR Setup Assistant support for FP-FS2601, FP-FS2602, FP-FS2608, and FP-FS2609 interposers

Modifications

- Updated DDR4, DDR5, and LPDDR5 support to keep up with the latest JEDEC changes, added new measurement support, and improved performance
- Fixed CSG-28310 – LTSSM Overview display problem for U4301B
- Fixed CSG-29743 – U4301B file save issue
- Various other minor bug fixes and feature enhancements

Logic and Protocol Analyzer Software Version 6.70.0002 (April 24, 2020)

Modifications

- Measurement updates for DDR/LPDDR Post-process Compliance Tool and Real-time Compliance Tool

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Logic and Protocol Analyzer Software Version 6.70.0001 (April 5, 2020)

Modifications

- Fixed a defect in DDR/LPDDR Post-process Compliance Tool

Logic and Protocol Analyzer Software Version 6.70.0000 (March 2020)

Additions

- GDDR6 support in Memory Analysis Viewer
- Added software support for W5643A DDR5 BGA interposer
- Added software support for Futureplus FP-FS2521 DDR4 SO-DIMM interposer

Modifications

- Updates to DDR5 and LPDDR5 support to keep up with the latest JEDEC changes

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Logic and Protocol Analyzer Software Version 6.60.0001 (October 2019)

Additions

- Additional LPDDR5 support in Memory Analysis Viewer and compliance tools
  - Additional compliance tests in both Post Process and Real-time Compliance tools
  - Handling of system clock speed changes in Memory Analysis Viewer and Post Process Compliance Tool
  - Updates to be current with the official release of LPDDR5 specifications
- ONFi Viewer enhancements:
  - Support for new training-related commands in ONFi 4.1
  - New LUN-related features:
    - Grouping of commands by LUN in the ONFi Viewer overview table
    - Ability to define custom command sequences as LUN-level or target-level commands
    - Ability to define custom command sequences that select a LUN
    - Option to substitute “LUN” with a different term (e.g., “Chip” or “Die”)
- Updates to DDR5 support to match the evolving draft specifications
- Updates to Viewscope to support UXR-series oscilloscopes

Modifications

- Fixed problems with the waveform window rows getting out of sync when scrolling with the mouse wheel. (WIT564909)
- Fixed the issue with no back-to-back trigger in DDR Eyescan and DDR Setup Assistant in the case of DDR4 geardown mode. (WIT566244)
- Fixed an exception that occurred when exporting the Timing Zoom data through the COM interface command *ExportEx* method. (WIT577276)

Logic and Protocol Analyzer Software Version 6.50.0001 (December 2018)

Modifications

- Updated PCI Express transaction protocol definition for Secondary PCIE Extended Capability which was causing Transaction Decode output to terminate early without displaying any results. (WIT563217)

Logic and Protocol Analyzer Software Version 6.50.0000 (December 2018)

Additions

- DDR5 and LPDDR5 support in Memory Analysis Viewer, DDR/LPDDR Post Process Compliance Tool, and Real-Time Compliance Tool.
- Ability to set limit/parameter values based on DUT properties in DDR/LPDDR Post Process Compliance Tool and Real-Time Compliance Tool.
- LPDDR4X support.
- Improved “Mode Registers Overview” tab in Memory Analysis Viewer.
- Export feature in Memory Analysis Viewer.

- Support for DDR4 Geardown mode in Memory Analysis Viewer, DDR/LPDDR Post Process Compliance Tool, and Real-Time Compliance Tool.
- ONFi Analysis Viewer enhancements:
    - Additional customization options.
    - Support for using one Logic Analyzer module to capture and analyze multiple ONFi busses.
    - SDR mode decode
    - Export of Payload data

Modifications

- Added missing DDR4 compliance tests *tMRD_L* and *tMRD_L2*. (WIT549808)
- Fixed potential hang when computing ONFi trace in ONFi Analysis Viewer. (WIT550165)
- Fixed "e-mail on trigger" feature. (WIT506323, WIT506596)
- Fixed the problem with protocol viewer lockstep feature with .NET 4.6 or greater. (WIT533193)
- Fixed address conversion and physical address trigger handling for DDR4. (WIT528305)
- Fixed the issue with saving a subset of bus/signals to an ALB file when saving automatically after an acquisition. (WIT525288)

Logic and Protocol Analyzer Software Version 6.40.0004 (November 2017)

Modifications

- Fixed problems with saving an ALB file on each run of repetitive run
- Fixed issues with the Address Conversion Trigger tool in DDR Decoder
- Fixed problems with the lockstep windows feature that would appear when .NET 4.6 or greater is installed

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Logic and Protocol Analyzer Software Version 6.40.0001 (August 2017)

Modifications

- Updated configuration files for the W6602A LPDDR4 BGA Interposer
- Added new 2-card configuration files for the FS2520 DDR4 interposer
- Fixed an issue where DDR4 traces may not compute correctly on first compute

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Logic and Protocol Analyzer Software Version 6.40.0000 (June 2017)

Additions

- B4661A Memory Analysis Software - DDR3/4 and LPDDR2/3/4 Performance Analysis (including ONFi Analysis Viewer) options 4FP/4NP/4TP
    - Ability to customize how vendor-specific commands and command sequences are decoded
    - New Timeline View, which graphically renders all ONFi transactions in a time domain chart and separates them by NAND targets
    - ONFi-specific Export feature
- B4661A Memory Analysis Software - LPDDR Decoder, options 2FP/2NP/2TP
    - Added support for LPDDR4X

  - Added support for decoding of commands sent to multiple ranks simultaneously in LPDDR4 listing decoder and Memory Analysis Viewer

Modifications

- B4661A Memory Analysis Software
  - Fixed an issue with repetitive runs in the DDR Post Process Compliance Tool. (WIT 488435)
  - Modifications to configuration files for FS2520 DDR4 DIMM interposer. (WIT 493812)
- Triggering
  - Fixed the crash that would occur when selecting the Advanced Trigger radio button in serial protocol trigger dialog. (WIT 488289)
  - Fixed the problem with loading an ALA configuration file which contained a trigger condition that included a burst resource referencing a 1-bit label. (WIT 490334)
  - Fixed the crash that would occur on loading a PCIe configuration containing certain “Physical Layer Error” trigger setups. (WIT 514919)
- COM Interface
  - Modifications to return “Filling Memory” (instead of “Unknown”) from the RunningStatus property when module has triggered and is filling memory. (WIT 494354)
- Install Packages
  - Updated install package executables to use the newest Keysight code signing certificate
- Fixed a configuration file name typo for W6601A in DDR Setup Assistant. (WIT 495057)
- Corrected the decode for certain UFS 2.1 attributes for U4431 (MIPI M-PHY Analyzer) (WIT # 505399)
- Improvements in the behavior of U4431A (MPHY Packet Generator, Option 613)

Logic and Protocol Analyzer Software Version 6.30.1018 (December 2016)

Modifications

- Updated configuration files for FS2520 to include information on which signals are single-ended and which are differential.
- Fixed a quad sample mode threshold problem in which the quad sample thresholds could not be adjusted individually
- Fixed an issue with the spacing between rows in transaction decode with Windows 8 and 10. The different spacing would cause the markers in the left-hand margin to be off as these were moved down the page.
- Fixed a problem with loading an ALA configuration file using a burst resource that references a 1-bit label. The configuration file loading was incorrect, causing the trigger specification to work incorrectly. This fix is retroactive - that is, loading a configuration file that used to fail will now work without any changes to the configuration file itself.
- Updated to latest, more secure Keysight SHA256 code signing certificate to avoid "signature is corrupt or invalid" given by some browsers
- Fixed an issue with loading certain DDR/LPDDR configurations where the details window in the Memory Analysis viewer was displayed immediately upon load

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Logic and Protocol Analyzer Software Version 6.30.1011 (October 2016)

Modifications

- Additional Windows 10 support - Adjustments to install drivers correctly on standalone instruments migrated to Windows 10
- Fixed the issue where a Memory Access Overview chart in the Memory Analysis Viewer would not update after being drawn once
- Corrected the version number displayed in the DDR/LPDDR Post Process Compliance tool
- Fixed errors in the configuration file for FS2510AB DDR4 interposer for double-edge clocking setup
- Fixed the issue where the DDR/LPDDR Post Process Compliance tool was displaying incorrect results during repetitive runs
- Fixed an exception that occurred when selecting the "Advanced Trigger" option in the Trigger dialog for all serial analyzers

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Logic and Protocol Analyzer Software Version 6.30.0000 (September 2016)

Additions

- 16860A Series Portable Logic Analyzers – The 16860A Series Portable Logic Analyzers is the industry's highest performance portable logic analyzer.

Feature	16861A	16862A	16863A	16864A
Logic analyzer channels	34	68	102	136
Maximum timing sample rate (full/half channel)	2.5 GHz / 5 GHz			
Maximum timing sample rate (quarter channel)	--	10 GHz	--	10 GHz
High-speed Timing Zoom	12.5 GHz (80 ps) with 256 K depth			
Maximum state clock rate	350 MHz standard, 700 MHz with Option 700			
Maximum state data rate	700 Mb/s standard, 1400 Mb/s with Option 700			
Maximum memory depth	2 Mb standard; 4 Mb, 8 Mb, 16 Mb, 32 Mb, 64 Mb, 128 Mb optional			

- ONFi (Open NAND Flash Interface) support – ONFi memory analysis support has been added to B4661A DDR3/4 and LPDDR2/3/4 Performance Analysis option (4FP/4NP/4TP).
- Multiple clock mode has been added to the U4164A – In addition, the minimum clock frequency for the U4164A is now 0 Hz.
- B4661A Memory Analysis Software Additions
    - Added the Mode Registers Overview tab to the DDR/LPDDR Memory Analysis window. The new tab provides detailed information on mode register settings that are visible in the trace.
    - Added support for Quad-rank Encoded Chip select to the B4661A Memory Analysis tool. (WIT 337444)
    - Added support for DDR4 3DS to the triggering, decode, and both compliance tools. (WIT 451421)
    - Added DDR4 DBI decode to the listing and Transaction tracker. (WIT 478787)

- Added the rank as well as "long" vs. "short" to the fields for ZQCal in the transaction decoder. The listing decoder was already correctly reporting those fields. (WIT 479024)

Modifications

- Logic and Protocol Analyzer (LPS) software platform
  - Retention of eye scan settings was being impacted by the version of .NET that was installed. The conflict with .NET has been resolved and eye scan settings will be retained.
  - The U4203A, U4204A, and U4205A direct connect probe files are once again available. (WIT 471665)
- B4610A Data Import Tool
  - Due to a change in buses/signals naming for dual threshold support, sometimes not all buses/signals would be imported when using the Data Import Tool. This issue has been resolved and all buses/signals will be imported. (WIT 470722)

- B4661A Memory Analysis Software
  - B4661A properly identifies entry and exit of Self Refresh. (WIT 461444)
  - The DDR4 decoder and compliance tools now correctly recognize and report MPR reads/writes. (WIT 480130)
  - The Real Time Compliance tool has been updated to decouple tRCD and tRP for 3DS. (WIT 463266)
  - DDR setup assistant correctly sets single edge clocking for DQ tuning over 2500 (WIT 459443)

- U4154A/B Logic Analyzer Module
  - If you encounter a triggering issue when transferring .ala files between different model analyzers, save the setup file as an xml file before transferring to a different model analyzer. (WIT 468799)
- U4301B PCIe Protocol Analyzer
  - CSV export now exports data in Little Endian as well as Big Endian. (WIT 471343)
  - The link width setting is retained when saving/loading configurations. (WIT 457647)

- U4421A MIPI D-PHY
  - A defect has been fixed in interpreting RGB color information. (WIT 379960)
  - The correct color is now displayed when extracted in non-command mode. (WIT 449953)

- U4431A MIPI M-PHY
  - UniPro/UFS Protocol Analyzer (Option 712) now supports JESD220C UFS 2.1. (WIT 462563)
  - In the UniPro Packet Generator, sometimes PACP_GET_req would have '0's instead of FLR after its CRC. Now the packet generator PACP_GET_req frame will contain FLR instead of '0' in TxPaPacpReq module. (WIT 449849)
  - The UniPro Protocol Analyzer has capture improvements under the following scenarios:
    - Preemption scenarios leading to CRC errors
    - Burst scenarios leading to missing packets

Logic and Protocol Analyzer Software Version 6.20.0000 (December 2015)

Additions

- U4164A Logic Analyzer module support. The U4164A is being introduced in conjunction with version 6.20 of the Logic and Protocol Analyzer software. Enhanced capabilities over previous logic analyzers include:

  - 350 MHz, 700 MHz, 1.4 Gb, and 2.4 Gb state speed options: purchase the level of state speed capture capability you need initially and upgrade as your state speed needs increase. The U4164A allows you to capture the highest speeds for DDR/LPRDD memory systems.
  - 400 Mb (sample) memory depth option: capture more system activity so you can debug complex problems when the symptom and root cause are widely separated in time.
  - 10 GHz ¼ channel conventional and transitional timing mode: identify timing problems in deep traces with high sample resolution. Enabled with either option -01G or -02G.
  - Clock Hysteresis: capture State traces through power down entry/exit and initialization events where the differential clock is turning off and on.
  - Dual Sample mode with dual threshold: provides separate thresholds so you can separate DDR memory Read/Write data.
  - Quad sample State mode: capture DDR4 and LPDDR4 data (Read rising/falling and Write rising/falling) at data rates over 2500 Mb/s through a single probe connection per signal. This mode provides four samples at two different thresholds, less loading on the system under test and better signal integrity.
  - Software de-skew tool for use with timing modes.

- B4661A Memory Analysis Software for Logic Analyzers support.

  With the B4661A memory analysis software, users can monitor DDR3/4 or LPDDR2/3/4 systems to perform debug, optimize performance, and validate protocol compliance. Powerful traffic overviews, multiple viewing choices, and real-time compliance violation triggering help identify elusive DDR/LPDDR system violations.

  The Keysight B4661A memory analysis software provides four standard software features and four licensed memory analysis options.

  Standard software features:
  - Default configurations for DDR and LPDDR probing solutions
  - DDR setup assistant
  - DDR eye finder / eye scan
  - DDR configuration creator

  Software Licensed options:
  - DDR decoder with physical address trigger tool
  - LPDDR decoder with physical address trigger tool for LPDDR/2/3
  - DDR and LPDDR Post-process and Real-time compliance violation analysis
  - DDR3/4 and LPDDR2/3/4 performance analysis

Modifications

- Logic and Protocol (LPA) SW Platform
  - Removed an Online Help reference to a Split Analyzer dialog topic (WIT 429499)

- U4154A/B and 16850 Series Logic Analyzers
  - Added a large system Configuration Utility into the LPA 6.XX series software (WIT 439310)
  - Resolved an issue where ‘burst trigger only’ added an unexpected burst to the 1st level of triggers (WIT 443929)

- U4301A/B PCIe Gen3 8 Gb/s Protocol Analyzer
  - Added support for drag and drop markers in Traffic and Performance charts

- U4421A MIPI D-PHY Protocol Analyzer
  - Resolved an image extraction issue specific to a particular Custom PPS setting, which won’t open properly unless you export/import PPS settings. The resolution requires that Mux mode settings

should be de-serialized properly while opening existing ala file with image list and PPS setting. (WIT 435729)
  - Fixed an issue where the extracted image was being displayed with bluish hue, when using same color order say RGB / BGR (WIT 435731)
  - Fixed an issue where the wrong Color in image was getting displayed when extracted, when using same color order say RGB / BGR (WIT 435731)
  - Added five missing API commands into the COM Automation Online Help and User Guide (WIT 435926)

- U4431A MIPI M-PHY Protocol Analyzer
  - Fixed an issue where HIBERNATE exit was not happening properly on DUT direction (WIT 418296)
  - Resolved a U4431A-613 issue where at PWM-G2 X1 with scrambling enabled, unknown bytes were attached with AFC0 frame (sent by Host) causing DUT to respond with a NAC. (WIT 421913)
  - Resolved a Unipro/UFS issue where Skip symbols in TC0 data packets were not handled correctly when 'enable preemption support' was selected.(WIT 429726)
  - Increased the 'PatternMatcher' count for Unipro, which caused the PACP_PWR_cnf packet to take 30 bytes of data. The incorrect packet was triggered when simple trigger is set on the field (after 9th byte) of the packet (WIT 429866)
  - Red Packets seen at HSG2 X2 in DUT direction has been resolved for a specific DUT (WIT 430365)
  - Problem at power mode change (PWM G1-HS G1A) has been resolved for a specific DUT. (WIT 430368)
  - Unknown packets in UFS will now be exported successfully for data having unknown packets. (WIT 446601)
  - 'Traffic Overview -> Compute' operation will now work on all Unknown packets having 0 packet bytes or 'less than' required bytes (WIT446606)

- B4620 Series Memory tools
  - The B4622B Post-processing tool glitch which displays N/A instead of trial which has a value has been addressed in the new B4661A Memory tool. (WIT 379887)
  - Improved text clarity in 'DDR decoder (Quad CS)' mode and also defaulted all 4 active CS signals to automatically select by default when this mode is chosen (WIT 337433)
  - Added a check to identify when the logic analyzer status contains the text 'slow or missing' while the test is waiting to trigger, at which time an error message is displayed and the test is exited (WIT 348174)

Logic and Protocol Analyzer Software Version 6.10.0000 (August 2015)

Additions

- Memory tool support:
  - B4621B DDR/2/3/4 Decoder enhanced to cover MRS decode of DDR4 RDIMM and LRDIMM.
  - W4630A series DDR4 BGA interposers default configurations and included into DDR setup assistant:
  - W4631A DDR4 x16 4-wing, 3.2Gb/s BGA interposer
  - W4636A DDR4 x16 2-wing, 2400Mb/s limited DQ BGA interposer
  - W4633A DDR4 x4/x8 3-wing, 3.2Gb/s BGA interposer

- B4610A Data Import Tool support: This tool allows you to import external data into the logic and protocol analyzer software and analyze it just like data acquired by logic analyzer modules. Data import modules read data from a module CSV file and make it available to tools and display windows. You can create module CSV files using external tools or by saving from any module using the main menu's *File>Export...* command. Data import modules are a licensed feature. You can evaluate the data import capability on imported data limited to 16 rows without a license.

  Data import modules appear in the Overview window like other logic analyzer modules. Because the data does not come from acquisition hardware in a logic analysis system frame, a virtual frame is created for data import modules. You can add tools and display windows to data import modules just like you add these to logic analyzer modules.

- SW Platform Enhancements.
  - Power Measurements are now possible in the Waveform viewer, through a GUI setup dialog, when connected to a scope.
  - Symbols that can be defined for Logic Analyzer labels can now be colorized in the Listing and Waveform views. When you select a symbol, the Edit button is enabled and you can select the color for the symbol. The symbol's color and font attributes are saved in the configuration file. (WIT 310776).
- U4301B PCIe Gen3 protocol analyzer module new features: These updates can also be applied to U4301A PCIe Gen3 analyzers that utilize a 64 bit OS and install the latest 6.0 or greater software.

  The following new capabilities apply to the U4301A/B PCIe Protocol Analyzer modules when operating under version 6.10 or higher.

  - L1 Substate with CLKREQ
  - Auto Lane Width detect
  - Auto Lane reversal
  - New trigger capability has been added, including:
    - Trigger on L1 Substate
    - Trigger on Error (Symbol Error, Disparity Error, Block Header Error, Idle Symbol Error)
    - Trigger on Speed change
    - Trigger on link width change
  - NVMe performance scatter chart
  - LTSSM decode updated for L1 Substates
  - Quick search / filter using traffic overview
  - Compact Training sequences
  - User ability to set Bi-directional traffic cut-off
  - Bi-directional trimming of data traffic
  - New GUI support for new interposers: M.2 and U.2 (SFF-8639)
  - New additions for PCIe 3.1 support
    - L1 substate
    - SRIS (Separate Refclk Independent SSC)
    - Readiness Notification
    - Precision Time Measurement
    - Change Root Complex
    - Enhanced DPC (Downstream Port Container)
    - Lightweight Notification
    - PASID (Process Address Space ID) translation
    - End to End TLP Prefix Changes for RCs

- U4431A MIPI M-PHY
    - **Unipro Packet Generator with Inbuilt Analyzer support**: Introduced Option 613 for the U4331A MIPI M-PHY protocol test modules to enable the UniPro Command Line Packet Generator with Inbuilt Analyzer (Full Rx, Half Tx). New Packet Generator option can be used in standalone way using Command Line tcl interface OR along with Keysight Partner product for UFS & UniPro conformance tests.

  The U4331A already supports the Protocol analysis for Unipro, UFS, SSIC, and CSI-3 MIPI M-PHY standards. The following new capabilities apply to the U4431A MIPI M-PHY Protocol Analyzer modules when operating under version 6.10 or higher.

    - SSIC
        - Store qualifier - Provides option to exclude DLPs, TLPs, Link Commands, and/or Ordered Sets from storing.
        - Transactional Decode
        - Device class CDC decodes with AMC, NCM, MBIM subclasses
        - Supported Device classes/sub-classes are automatically detected from device configuration response and decoded accordingly.
        - Test Assertions (15) - Provides seamless navigation with protocol viewer to analyze results.
        - LTSSM State viewer and analysis
        - Triggering support on Standard USB 3.0 Device Requests such as trigger on SET_DESCRIPTOR, GET_DESCRIPTOR etc.
    - MPCIe
        - Store qualifier - Provides option to exclude DLPs, TLPs, and/or Ordered Sets from storing.
        - Storage Transaction decode (NVMe, AHCI)
        - LTSSM State viewer and analysis
    - Compact view feature (applicable to M-PCIe, SSIC, and UniPro)

- **U4421A** MIPI D-PHY

  Additional feature enhancements included under version 6.1

    - DSI Image Inserter:
        - Image Inserter now supports compression of pixel data as per VESA DSC 1.1 for DSI protocol. This option is available for burst, non-burst and command mode operations.
        - Image inserter settings can be independently saved to/loaded from a '.imgc' XML file.
    - DSI Image extractor:
        - Decompression of compressed data packets as per VESA DSC 1.1 algorithm for DSI. This option is available for burst, non-burst and command mode operations.
        - Image extractor can automatically link to a PPS (if available) or a user can provide custom PPS settings in a user friendly dialog.
        - PPS attributes can be saved to/loaded from a '.ppsc' XML file independent of LA configuration file.

Modifications

- Logic and Protocol (LPA) SW Platform
    - Minor performance improvements due to 64-bit memory related optimization.

  - Work-around identified: When a CSV file reaches an inherent limitation within the LPA SW, the work around is to break the file into 2 distinct files (WIT 345096).
  - Probe definition files supporting the HW Setup drop-down choices has been updated to include the 16850 series logic analyzers (WIT 359195).
  - Usability improvements
    - The LPA application 'File > Open' dialog has been updated to enable resizing of the dialog (WIT 218240).
    - The zoom in/out/full keyboard short cuts now better align with industry standards (Ctl +/-/0 as opposed to Shift key combinations). Waveform and listing zoom can also now be performed by holding down CTRL and scrolling the mouse wheel (like you can with most applications and web browsers).

- U4154A/B and 16850 Series Logic Analyzers
  - Fixed an issue that caused repetitive Run speeds to slow down due to a recent GUI revision update (WIT 359204).
- U4301A/B PCIe Gen3 8 Gb/s Protocol Analyzer
  - Many ECN updates from the PCIe Standards committee have been addressed in the 6.10 release (see New Additions for PCIe 3.1 support above)
  - LED light architecture has been reverted back to the pre-6.0 release status to again show physical mapping rather than logical
  - PCIe Performance tools updated to add MSI-X to band chart Interrupt series (WIT 241814).
  - Eliminated corner case situation where a skew could be observed in single direction for Gen2 speed captures at x4 link width (WIT 375606).
  - Resolved a tuning issue that was triggered when a PC localization setting caused numbers to appear with a comma when a decimal point was expected (WIT 379042).
  - Improved the automatic link tuning process.
- U4421A MIPI D-PHY Protocol Analyzer
  - Exerciser now allows you to generate time accurate syncs for video mode testing at the expense of disabling certain features like 'Dynamic Data Insertion' at insertion bit. A new check box 'Ignore Insertion Bit' is added in the Exerciser Data tab of the setup dialog. If accurate sync times are desired, this checkbox must be checked before adding CSV files in the 'Run Sequence' list.(WIT 354339)o Image Inserter feature was enhanced to enable save/load of a specific GUI configuration (WIT 377328)
  - DSI Non-burst mode issue was addressed, where the timings of all VSync packets were delayed by >100ns as compared to all other HSync packets (WIT 377340)
  - DSI Non-burst mode was enhanced to include a read-only field in the GUI to display the time it takes the frame to restart when looping (WIT 354339)
  - DSI Non-burst mode has been improved in how the .csv files are generated with respect to blanking modes, which occasionally resulted in an unexpected transition to LP mode (WIT 354339)
  - DSI mode has been updated to address an issue where more than one symbol Jitter was observed at image loop-over, when playing at 720p 2X at 590.3 mbps (WIT 388324)
- U4431A MIPI M-PHY Protocol Analyzer
  - The overall analysis measurement jitter has been improved.
  - The MPHY Unipro exerciser choice in the drop-down list has been removed in LPA SW app.
  - In Track Mode of UniPro Analyzer, while exiting Hibern8 in HS mode analyzer mistakenly fall to PWM mode. (WIT 380647).
- B4620 Series Memory tools
  - Resolved a GUI issue where the LPDDR decoder dialog didn't allow for row/column value adjustment after set to the lowest values (WIT 376043)

Logic and Protocol Analyzer Software Version 6.03.1100 (March 2015)

Modifications

- U4301A/U4301B PCIe Gen3 8 Gb/s Protocol Analyzer
  - Updated the PCIe acquisition settings for more reliable data capture in some situations
  - Fixed an issue that was introduced in the 6.00 release which resulted in an incorrect computation of the TLP Digest (ECRC) (WIT 359429).

- U4421A MIPI D-PHY Protocol Analyzer
  - In the 6.03 release, an issue was introduced which resulted in the Image View sample number always being 0. The "Image View" Sample Number has been corrected to show the sample corresponding to the DSI frame start. (WIT 368805)
  - Fixed a CSV non-burst mode issue where LP11 state displayed for a longer duration between frames when multiple images are present (WIT 366514)

- Other
  - View Scope – added support for the Infiniium V-Series Oscilloscopes
  - The GP Probe definition file has been updated to include the following new probe choices. (WIT 359195)
    - U4203A Probe, 34 channel, flying lead, single-ended, 160-pin direct connect
    - U4204A Probe, 34 channel, Soft Touch Pro, single-ended, 160-pin direct connect
    - U4205A Probe, 34 channel, Mictor, single-ended, 160-pin direct connect
    - E5402A Probe, 34 channel SE right angle soft touch pro connectorless, connects to 90-pin LA cable
    - E5381B Probe, 17 channel differential flying leads, connects to 90-pin Logic Analyzer cable
    - E5382B Probe, 17 channel single-ended flying leads, connects to 90-pin Logic Analyzer cable

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Logic and Protocol Analyzer Software Version 6.03 (November 2014)

Modifications

- U4154A/B and 16850 Series Logic Analyzers
  - Added a field called “Trig out” in the Status dialog and updated the help to provide information on this field. After a run completes, the time between a Trigger Event at the Probe Tips and the Trigger Out pulse at the BNC is displayed in the Trig out field. (WIT 342857)
  - Resolved a timing zoom data correlation off-set issue that occurred under certain conditions in both timing and state modes (Wit 337415)
- U4301A PCIe Gen3 8 Gb/s Protocol Analyzer
  - Added support for the U4301U-GFP upgrade option that includes 8 GB Capture Buffer, LTSSM, Performance Summary, and Transaction Decode support. (WIT 349642)
- U4421A MIP D-PHY Protocol Analyzer
  - Made the following changes to the non-burst mode DSI signal inserter dialog and CSV to raw data translator (WIT 354339).
    - Fixed the calculation of times for LP-11 blanking
    - Fixed the translation of CSV for LP-11 No Clock blanking
    - Fixed a rounding error in the byte time conversions
    - Enabled fractional HS Bit Rates in the GUI

        - Fixed a defect in one of the blanking pulldowns that occasionally would not select the clicked option
        - Fixed the dialog to not clear all entered timings when various settings are changed
- I2C, SPI and CAN decode support
    - Added a chapter, *Extracting Slow Speed Serial Bus Data*, in the Signal Extractor help and user guide to provide detailed information on CAN, I2C, and SPI algorithm files and how to perform the required configuration in the Logic and Protocol Analyzer GUI. The extracted output for CAN, I2C, and SPI is also described with the extracted labels and errors. (WIT 350691)
- View Scope
    - Added U4301A/B to the supported analyzers for View Scope (WIT 358623)

Logic and Protocol Analyzer Software Version 6.0 (September 2014)

Additions

- Keysight Technologies: The Logic and Protocol Analyzer software has been re-branded with a new Keysight Technologies logo, splash screen and screen saver.
- 64-bit Application: The Logic and Protocol Analyzer software and the Add-in packages supported on Version 6.00 have been released as 64-bit applications.
- U4154B 4 Gb/s logic analyzer module support. The U4154B Logic Analyzer model is being introduced in conjunction with version 6.00 of the Logic and Protocol Analyzer software. Enhanced capabilities include the ability to combine 3 modules for higher channel count, and the addition of a clock qualifier.
- U4301B PCIe Gen3 protocol analyzer module support: The U4301B modular PCIe Protocol Analyzer model is being introduced in conjunction with version 6.00 of the Logic and Protocol Analyzer software. The U4301B has a memory depth of 8G. The LTSSM Overview, Performance Analysis, and Transaction Decode features are included standard.

  The following new capabilities apply to the U4301B and U4301A PCIe Protocol Analyzer modules when operating under version 6.00.

    - Compute
        - When checked, a “Compute All on Run” check box in the Protocol Viewer performs a compute in background after the data is captured for the Traffic Overview, LTSSM Overview, Performance Overview and Transaction Decode tabs. The result is lower compute times relative to running a compute for each tab individually after a trace is captured. Errors are included in the compute by default.
        - The Compute button in the Traffic Overview, LTSSM Overview, Performance Overview and the Transaction Decode tabs has been modified to select “Compute This” or “Compute All”. The modified button allows you to compute across all active tabs on data that was previously captured.
    - LTSSM Overview
        - Enhanced LTSSM analysis with new EQ selections (Compute EQ and Setup Organized by EQ) that provide more insight into Equalization negotiation that occurred during the trace.
        - When the Setup is organized by EQ, the File area of the display provides a table that summarizes the equalization changes in order over time.
        - Enables you to see the EQ handshake process so you can understand when settings have been accepted, rejected, etc. Clicking on a row in the EQ Overview takes to the particular packet in the Packet Viewer and LTSSM state.

        - The LTSSM state diagram has been updated to highlight which states have been visited for a given trace. This enables you to quickly identify not only which states have been visited but also see if states you expected to be visited did not occur.
    - Traffic Overview
        - Added a packet type band chart to the Traffic Overview tab.
    - Performance Overview
        - Added charting for Header Flow Control. In addition, sub-headings are now available under All Flow Control.
        - The Setup dialog has been updated to add controls for setting Header Flow Control Init values.
    - Transaction Decoder
        - Scatter Gather List (SGL) support has been added to the NVMe Transaction Decoder.
    - Filter
        - Added a Simple Packet Filter icon within the Protocol Viewer that provides an easy way to Show or Hide packets in the Protocol Viewer.
    - Search
        - Added Simple Packet Search to quickly find the most frequently requested packets. A new Search field within the Protocol Viewer includes an AutoComplete popup that provides both the Short Name and the Packet Type Name.
- LPDDR4 support: LPDDR4 support at speeds ≤ 2.5 Gb/s and > 2.5 Gb/s has been added to:
    - the B4623B LPDDR2/3/4 Decoder
    - the Post Process Compliance Tool, Real-time Compliance Tool, and Performance Tool of the B4622B DDR2/3/4, LPDDR2/3/4 Protocol Compliance and Analysis Tool
    - and the DDR Setup Assistant and the Configuration Creator Tool of the DDR/LPDDR Memory Support Tools
- DDR4 support: Added support for RDIMM/LRDIMM for DDR4 in the B4621B DDR2/3/4 Bus Decoder
- Mobile PCIe (M-PCIe) support: Introduced Option 715 for the U4331A MIPI M-PHY protocol test modules to enable the Mobile PCIe (M-PCIe) decoder. The U4331A already supports the Unipro, UFS, SSIC, and CSI-3 MIPI M-PHY standards.
    - The introduction of the Mobile PCIe protocol decoder includes the following capabilities leveraged from PCIe protocol toolset
        - Performance Statistics
        - Configuration Decode
        - Transaction and Remote Register Access Protocol (RRAP) Decode
    - Additional enhancements to the existing SSIC protocol decoder include
        - Performance Statistics, leveraged from the PCIe toolset.
    - Additional enhancements to the existing CSI-3 protocol decoder include
        - CSI-3 Decompression

Modifications

- Logic and Protocol Analyzer application - General
    - During installation, files are extracted into the Temp directory. If you encounter the following installation error message..."There is not enough space on drive C:\ to extract this package", it means that the Temp directory may have a size limit or that the directory is almost full and files cannot be extracted. The solution to this issue is to clean out the Temp directory (*C:\Users\<user name>\AppData\Local\Temp*) and run the Disk Cleanup tool. Ensure that the "Temporary Files" item is selected for cleanup. (WIT 326481).
    - The Protocol Perform overview pane defect occasionally resulting in perpetual processing has been fixed (WIT 342813)

- An infrequent GUI crash related to tool tip messaging has been fixed (WIT 222432)

- View Scope
  - The DSAX91304A oscilloscope has been added to the list of scopes supported by View Scope (WIT 323454)

- 16850 Series Portable Logic Analyzers
  - An issue where the analyzer would occasionally throw a read memory error has been resolved (WIT 337757).
  - A series of issues running the 16850 Series Logic Analyzer in a repetitive mode (continuous operation) have been resolved
    - Data Indexer issues resulting in time tags 'out of order' (WIT 277196, 206861)
    - Data Indexer fails to complete (WIT 277198)
    - Intermittent application lock up during repetitive operation (WIT 206863)
    - Bucketizer fails to read the last set of memory / memory systems hangs (WIT 277223)

- U4301A PCIe Gen3 8 Gb/s Protocol Analyzer
  - Performance Statistics for flow control has been improved to include header packets.
  - An issue involving the correlation between a U4301A analyzer and a Scope has been rectified. The fix was made available in the 5.80 patch branch version 5.80.1004 and is included in the 6.00 release (WIT 278427).
  - An intermittent issue has been resolved, eliminating the condition where EIOS packets sent before electrical idle were occasionally missing (WIT 180114).
  - Using advanced triggers, a corner-case condition has been resolved where a trigger on a pattern in the down direction was not successful. This and several other downstream bi-directional triggering issues have been resolved. The software has been modified to consistently enable the fixed matchers for the B direction (downstream with interposer in bi-directional mode) (WIT 222918).
  - An infrequent 5.80 application crash involving a version 5.60 ala captured file has been resolved by adding additional code logic. (WIT 326478)

- U4421A MIP D-PHY Protocol Analyzer
  - A popular enhancement request has been implemented for the U4421A software application, making a list of available images in the Image Viewer tab available to the user. The initial enhancement was distributed via 5.80 patch and is now being rolled into the 6.0 release. A 'Save All Images' button has been added to the 'Image View' tab of the Protocol viewer, enabling the image to be saved in BMP format into a user-specified folder in a single click (WIT 319472).
  - CSI-2 compression/decompression has been added per CSI-2 spec version 1.3
  - A U4421A trigger issue has been corrected, involving a situation where a basic trigger could ignore 'payload exclusion'. The code logic now uses the same width pattern matchers on either side of 'And' condition, in both simple and advanced trigger (WIT 241796).
  - An infrequent application crash issue has been resolved, occurring when the 2nd module of a two-module hardware setup was disabled. The fix involved the implementation of a check to verify if previously selected choice pointed to a valid module (WIT 319538).

- U4431A MIPI M-PHY Protocol Analyzer
  - The CSI-3 Protocol mode capability has been enhanced to extract a CSI-3 image when the entire frame is in a single packet. This was accomplished by adding code that uses the image size information from EOP packets as well as image data off-set information (WIT 331352).
  - An intermittent issue experienced by a specific customer involving Hibern8 state raw mode capture has been resolved (WIT 315118).