Keysight U7238C/U7238D MIPI® D-PHYSM Test App

Methods of Implementation



2

Notices

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Manual Part Number U7238-97003

Software Version Version 3.51.0000

Edition

March 2017

Available in electronic format only.

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MIPI® D-PHYSM Test App — At A Glance

The MIPI D-PHY automated test application allows the testing of all MIPI devices with the Keysight 90000, or 9000 Series Infiniium oscilloscope based on the *MIPI Alliance Standard for D-PHY* specification. MIPI stands for Mobile Industry Processor Interface. The MIPI alliance is a collaboration of mobile industry leader with the objective to define and promote open standards for interfaces to mobile application processors.

The MIPI D-PHY Test App:

- · Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Allows you to determine the number of trials for each test, with the new multi trial run capability.
- Provides detailed information of each test that has been run. The result of maximum twenty five worst trials can be displayed at any one time.
- Creates a printable HTML report of the tests that have been run.

Required Equipment and Software

In order to run the MIPI D-PHY automated tests, you need the following equipment and software:

- 90000, or 9000 Series Infiniium oscilloscope. Keysight recommends using 4 GHz and higher bandwidth oscilloscope.
- The minimum version of Infiniium oscilloscope software (see the U7238C/U7238D test application release notes).
- Keysight U7238C/U7238D MIPI D-PHY Test App.
- Differential probe amplifier, with the minimum bandwidth of 5 GHz.
- E2677A differential solder-in probe head, E2675A differential browser probe head, E2678A differential socket probe head and E2669A differential kit which includes E2675A, E2677A and E2678A are recommended.
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Mouse, gty = 1, (provided with the Keysight Infinitum oscilloscope).

The required license is:

• U7238C/U7238D MIPI D-PHY compliance test application (MPI).

In This Book

This manual describes the tests that are performed by the MIPI D-PHY Test App in detail.

- Chapter 1, "Installing the MIPI D-PHY Test App" shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, "Preparing to Take Measurements" shows how to start the MIPI D-PHY Test App and gives a brief overview of how it is used.
- Part A MIPI D-PHY 1.0 contains tests pertaining to MIPI D-PHY 1.0.
- Part B MIPI D-PHY 1.1 contains tests pertaining to MIPI D-PHY 1.1.
- Part C MIPI D-PHY 1.2 contains tests pertaining to MIPI D-PHY 1.2.
- Part I Electrical Characteristics emphasizes on HS Data, HS Clock, LP Data and LP Clock Transmitter tests.
- Part II Global Operation covers Data and Clock Transmitter tests.
- Part III HS Data-Clock Timing covers HS Data-Clock Timing and HS Skew Calibration Burst Tests.
- Part IV Informative Tests covers HS Data Eye Height (Informative) and HS Data Eye Width (Informative) tests.
- Part V Introduction contains calibration and probing information.

See Also

- The MIPI D-PHY Test App's online help, which describes:
 - Starting the MIPI D-PHY test application.
 - · Creating or opening a test project.
 - Setting up MIPI D-PHY test environment.
 - · Selecting tests.
 - Configuring selected tests.
 - Connecting the oscilloscope to the DUT.
 - · Running tests.
 - · Viewing test results.
 - Viewing/printing the HTML test report.
 - Understanding the HTML report.
 - Saving test projects.

Contact Keysight

For more information on MIPI D-PHY Test App or other Keysight Technologies' products, applications and services, please contact your local Keysight office. The complete list is available at:

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Contents

```
In This Book
              Contact Keysight
1 Installing the MIPI D-PHY Test App
              Installing the Software
              Installing the License Key
                                          33
2 Preparing to Take Measurements
              Calibrating the Oscilloscope
              Starting the MIPI D-PHY Test App
                                                 37
                 Online Help Topics
                                    38
              Fixture Options
                                39
                 Manual Load Switching
                                        39
                 Auto Load Switching
   Part A MIPI D-PHY 1.0
```

MIPI D-PHY Test App — At A Glance 3

Part I Electrical Characteristics

3 MIPI D-PHY 1.0 High Speed Data Transmitter (HS Data TX) Electrical Tests

Probing for High Speed Data Transmitter Electrical Tests 46

Test Procedure 47

Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation 49

PASS Condition 49
Test Availability Condition 49
Measurement Algorithm using Test ID 811 50
Test References 50

| Test 1.3.8 HS Data TX V _{CMTX} Mismatch (DV _{CMTX} (1,0)) Method of Implementation 51 |
|---------------------------------------------------------------------------------------------------------------------------------------|
| PASS Condition 51 Test Availability Condition 51 Measurement Algorithm using Test ID 812 51 Test References 52 |
| Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz (DV _{CMTX} (HF)) Method of |
| Implementation 53 PASS Condition 53 Test Availability Condition 54 Measurement Algorithm using Test ID 818 54 Test References 54 |
| Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz (DV _{CMTX} (LF)) Method |
| of Implementation 55 PASS Condition 55 Test Availability Condition 56 Measurement Algorithm using Test ID 819 56 |
| Test References 56 |
| Test 1.3.4 HS Data TX Differential Voltage (V _{OD}) Method of Implementation 57 |
| PASS Condition 57 Test Availability Condition 57 Measurement Algorithm using Test IDs 8131 and 8132 57 Test References 58 |
| Test 1.3.5 HS Data TX Differential Voltage Mismatch (DV _{OD}) Method of |
| Implementation 59 PASS Condition 59 Test Availability Condition 59 Measurement Algorithm using Test ID 8141 60 Test References 60 |
| Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V _{OHHS}) Method of |
| Implementation 61 PASS Condition 61 Test Availability Condition 61 Measurement Algorithm using Test ID 8151 61 Test References 62 |
| Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t _R) Method of Implementation 63 |
| PASS Condition 63 |
| Test Availability Condition 63 Measurement Algorithm using Test ID 8110 63 Test References 63 |

| | Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t _F) Method of Implementation 64 PASS Condition 64 Test Availability Condition 64 Measurement Algorithm using Test ID 8111 64 Test References 64 |
|---|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4 | MIPI D-PHY 1.0 High Speed Clock Transmitter (HS Clock TX) Electrical Tests |
| | Probing for High Speed Clock Transmitter Electrical Tests 66 Test Procedure 66 |
| | Test 1.4.7 HS Clock TX Static Common Mode Voltage (V _{CMTX}) Method of Implementation 68 PASS Condition 68 Test Availability Condition 68 Measurement Algorithm using Test ID 1811 68 Test References 69 |
| | Test 1.4.8 HS Clock TX VCMTX Mismatch (DV _{CMTX} (_{1,0)}) Method of Implementation 70 PASS Condition 70 Test Availability Condition 70 Measurement Algorithm for Test ID 1812 70 |
| | Test References 71 Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz (DV _{CMTX} (HF)) Method of Implementation 72 PASS Condition 72 Test Availability Condition 72 Measurement Algorithm using Test ID 1818 73 Test References 73 |
| | Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz (DV _{CMTX} (LF)) Method of Implementation 74 PASS Condition 74 Test Availability Condition 74 Measurement Algorithm using Test ID 1819 75 Test References 75 |
| | Test 1.4.4 HS Clock TX Differential Voltage (V _{OD}) Method of Implementation 76 PASS Condition 76 Test Availability Condition 76 Measurement Algorithm using Test IDs 18131 and 18132 76 Test References 77 |

| | Test 1.4.5 HS Clock TX Differential Vol tage Mismatch (DV _{OD}) Method of Implementation 78 PASS Condition 78 Test Availability Condition 78 Measurement Algorithm using Test ID 18141 79 Test References 79 |
|---|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | Test 1. 4.6 HS Clock TX Single-Ended Output High Voltage (V _{OHHS}) Method of Implementation 80 PASS Condition 80 Test Availability Condition 80 Measurement Algorithm using Test ID 18151 80 Test References 81 |
| | Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t _R) Method of Implementation 82 PASS Condition 82 Test Availability Condition 82 Measurement Algorithm using Test ID 18110 82 Test References 82 |
| | Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t _F) Method of Implementation 83 PASS Condition 83 Test Availability Condition 83 Measurement Algorithm using Test ID 18111 83 Test References 83 |
| | Test 1.4.17 HS Clock Instantaneous Method of Implementation PASS Condition 84 Test Availability Condition 84 Measurement Algorithm using Test ID 911 84 Measurement Algorithm using Test ID 914 85 Test References 85 |
| 5 | MIPI D-PHY 1.0 Low Power Data Transmitter (LP Data TX) Electrical Tests |
| | Probing for Low Power Transmitter Electrical Tests 88 Test Procedure 88 |
| | Test 1.1.1 LP TX Thevenin Output High Voltage Level (V _{OH}) Method of Implementation 90 |
| | PASS Condition 90 Test Availability Condition 90 Measurement Algorithm using Test ID 821 90 Measurement Algorithm using Test ID 8211 91 Test References 91 |

92

| Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V _{OL}) Method of Implementation PASS Condition 92 Test Availability Condition 92 Measurement Algorithm using Test ID 822 92 Measurement Algorithm using Test ID 8221 93 Test References 93 Test 1.1.3 LP TX 15%-85% Rise Time Level (T _{RLP}) EscapeMode Method of Implementation 94 PASS Condition 94 Test Availability Condition 94 Measurement Algorithm using Test ID 8241 94 Test References 94 |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Test Availability Condition 92 Measurement Algorithm using Test ID 822 92 Measurement Algorithm using Test ID 8221 93 Test References 93 Test 1.1.3 LP TX 15%-85% Rise Time Level (T _{RLP}) EscapeMode Method of Implementation 94 PASS Condition 94 Test Availability Condition 94 Measurement Algorithm using Test ID 8241 94 Test References 94 |
| Measurement Algorithm using Test ID 822 92 Measurement Algorithm using Test ID 8221 93 Test References 93 Test 1.1.3 LP TX 15%-85% Rise Time Level (T _{RLP}) EscapeMode Method of Implementation 94 PASS Condition 94 Test Availability Condition 94 Measurement Algorithm using Test ID 8241 94 Test References 94 |
| Measurement Algorithm using Test ID 8221 93 Test References 93 Test 1.1.3 LP TX 15%-85% Rise Time Level (T _{RLP}) EscapeMode Method of Implementation 94 PASS Condition 94 Test Availability Condition 94 Measurement Algorithm using Test ID 8241 94 Test References 94 |
| Test References 93 Test 1.1.3 LP TX 15%-85% Rise Time Level (T _{RLP}) EscapeMode Method of Implementation 94 PASS Condition 94 Test Availability Condition 94 Measurement Algorithm using Test ID 8241 94 Test References 94 |
| Implementation 94 PASS Condition 94 Test Availability Condition 94 Measurement Algorithm using Test ID 8241 94 Test References 94 |
| PASS Condition 94 Test Availability Condition 94 Measurement Algorithm using Test ID 8241 94 Test References 94 |
| Test Availability Condition 94 Measurement Algorithm using Test ID 8241 94 Test References 94 |
| Measurement Algorithm using Test ID 8241 94 Test References 94 |
| Test References 94 |
| |
| T 144 A D TV 450/ 050/ 5 U T' |
| Test 1.1.4 LP TX 15%-85% Fall Time Level (T _{FLP}) Method of Implementation 95 |
| PASS Condition 95 |
| Test Availability Condition 95 |
| Measurement Algorithm using Test ID 825 95 |
| Measurement Algorithm using Test ID 8251 96 Test References 96 |
| |
| Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock (T _{LP-PULSE-TX}) Method of |
| Implementation 97 |
| PASS Condition 97 |
| Test Availability Condition 97 Measurement Algorithm using Test IDs 827, 8271 and 8272 98 |
| Measurement Algorithm using Test IDs 827, 8271 and 8272 98 Measurement Algorithm using Test IDs 1827, 18271 and 18272 98 |
| Test References 99 |
| Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock (T _{IP-PFR-TX}) Method of |
| Implementation 100 |
| PASS Condition 100 |
| Test Availability Condition 100 |
| Measurement Algorithm using Test ID 828 101 |
| Measurement Algorithm using Test ID 1828 101 |
| Test References 101 |
| Test 1.1.5 LP TX Slew Rate vs. C _{LOAD} Method of Implementation 102 |
| PASS Condition 102 |
| Test Availability Condition 102 Measurement Algorithm using Test IDs 829, 8291 and 8292 102 |

6 MIPI D-PHY 1.0 Low Power Clock Transmitter (LP Clock TX) Electrical Tests Probing for Low Power Transmitter Electrical Tests 106 Test Procedure 106 Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of **Implementation** 108 PASS Condition Test Availability Condition 108 Measurement Algorithm using Test ID 1821 and 28211 108 Measurement Algorithm using Test ID 18211 Test References 109 Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation 110 PASS Condition 110 Test Availability Condition 110 Measurement Algorithm using Test ID 1822 110 Measurement Algorithm using Test ID 18221 111 Measurement Algorithm using Test ID 28221 111 Test References 111 Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation 112 PASS Condition 112 Test Availability Condition 112 Measurement Algorithm using Test ID 18241 112 Measurement Algorithm using Test ID 28241 113 Test References 113 Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation 114 PASS Condition Test Availability Condition 114 Measurement Algorithm using Test ID 1825 114 Measurement Algorithm using Test ID 18251 115 Measurement Algorithm using Test ID 28251 115 Test References 115 Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation 116 PASS Condition 116

Test Availability Condition 116

118

Test References

Measurement Algorithm using Test ID 1829, 18291 and 18292

Measurement Algorithm using Test ID 2829, 28291 and 28292

116

117

Part II Global Operation

7 MIPI D-PHY 1.0 Data Transmitter (Data TX) Global Operation Tests

Probing for Data TX Global Operation Tests 122

Test Procedure 122

Test 1.3.1 HS Entry: Data T_{LPX} Method of Implementation 124

PASS Condition 124

Test Availability Condition 124

Measurement Algorithm using Test ID 511 124

Test References 124

Test 1.3.2 HS Entry: Data TX T_{HS-PRFPARF} Method of Implementation 125

PASS Condition 125

Test Availability Condition 125

Measurement Algorithm using Test ID 557 125

Test References 126

Test 1.3.3 HS Entry: Data TX T_{HS-PREPARE} + T_{HS-ZERO} Method of Implementation 127

PASS Condition 127

Test Availability Condition 127

Measurement Algorithm using Test ID 558 127

Test References 128

Test 1.3.13 HS Exit: Data TX T_{HS-TRAIL} Method of Implementation 129

PASS Condition 129

Test Availability Condition 129

Measurement Algorithm using Test ID 546 129

Test References 130

Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{RFOT}) Method of Implementation 13°

PASS Condition 131

Test Availability Condition 131

Measurement Algorithm using Test ID 549 131

Test References 132

Test 1.3.15 HS Exit: Data TX T_{FOT} Method of Implementation 133

PASS Condition 133

Test Availability Condition 133

Measurement Algorithm using Test ID 547 133

| Measurement Algorithm using Test ID 548 135 Test References 136 |
|---------------------------------------------------------------------------------------------------------------------|
| 8 MIPI D-PHY 1.0 Clock Transmitter (Clock TX) Global Operation Tests |
| Probing for Clock TX Global Operation Tests 138 Test Procedure 139 |
| Test 1.4.1 HS Entry: CLK TX T _{LPX} Method of Implementation 140 |
| PASS Condition 140 Test Availability Condition 140 Measurement Algorithm using Test ID 5510 140 Test References 141 |
| Test 1.4.2 HS Entry: CLK TX T _{CLK-PREPARE} Method of Implementation 142 |
| PASS Condition 142 Test Availability Condition 142 Measurement Algorithm using Test ID 552 142 Test References 143 |
| Test 1.4.3 HS Entry: CLK TX T _{CLK-PREPARE} +T _{CLK-ZERO} Method of Implementation 144 |
| PASS Condition 144 Test Availability Condition 144 Measurement Algorithm using Test ID 554 144 Test References 145 |
| Test 1.5.1 HS Entry: CLK TX T _{CLK-PRE} Method of Implementation 146 |
| PASS Condition 146 Test Availability Condition 146 Measurement Algorithm using Test ID 551 146 Test References 147 |
| Test 1.5.2 HS Exit: CLK TX T _{CLK-POST} Method of Implementation 148 |
| PASS Condition 148 Test Availability Condition 148 Measurement Algorithm using Test ID 555 148 Test References 149 |
| Test 1.4.13 HS Exit: CLK TX T _{CLK-TRAIL} Method of Implementation 150 |
| PASS Condition 150 Test Availability Condition 150 Measurement Algorithm using Test ID 543 150 Test References 151 |
| |

Test 1.3.16 HS Exit: Data TX T_{HS-EXIT} Method of Implementation

PASS Condition 135

Test Availability Condition 135

152

| Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T _{REOT}) Method of Implementation |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PASS Condition 152 Test Availability Condition 152 Measurement Algorithm using Test ID 559 152 Test References 153 |
| Test 1.4.15 HS Exit: CLK TX T _{EOT} Method of Implementation 154 |
| PASS Condition 154 Test Availability Condition 154 Measurement Algorithm using Test ID 544 154 Test References 155 |
| Test 1.4.16 HS Exit: CLK TX T _{HS-EXIT} Method of Implementation 156 |
| PASS Condition 156 Test Availability Condition 156 Measurement Algorithm using Test ID 556 156 Test References 157 |
| Part III HS Data-Clock Timing |
| 9 MIPI D-PHY 1.0 High Speed (HS) Data-Clock Timing Tests |
| Probing for High Speed Data-Clock Timing Tests 162 Test Procedure 163 |
| Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation 164 PASS Condition 164 Test Availability Condition 164 Measurement Algorithm using Test ID 912 164 Test References 164 |
| Test 1.5.4 Data-to-Clock Skew (T _{SKEW(TX)}) Method of Implementation 165 |
| PASS Condition 165 Test Availability Condition 165 Measurement Algorithm using Test ID 913 166 Measurement Algorithm using Test ID 9131 167 Test References 167 |

Part IV Informative Tests

10 MIPI D-PHY 1.0 Informative Tests

HS Data Eye Height (Informative) Method of Implementation 172

PASS Condition 172

Test Availability Condition 172

Measurement Algorithm using Test ID 915 172

Test References 173

HS Data Eye Width (Informative) Method of Implementation 174

PASS Condition 174

Test Availability Condition 174

Measurement Algorithm using Test ID 916 175

Test References 175

Part B MIPI D-PHY 1.1

Part I Electrical Characteristics

11 MIPI D-PHY 1.1 High Speed Data Transmitter (HS Data TX) Electrical Tests

Probing for High Speed Data Transmitter Electrical Tests 182

Test Procedure 183

Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of

Implementation 185

Test References 185

Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($DV_{CMTX}(1.0)$) Method of Implementation 185

Test References 185

Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz (DV_{CMTX}(HF)) Method of

Implementation 185

Test References 185

Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz (DV_{CMTX}(LF)) Method

of Implementation 185

Test References 185

Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation 185

Test References 185

Test 1.3.5 HS Data TX Differential Voltage Mismatch (DV_{OD}) Method of

Implementation 185

| | | TX Single-Ended Output High Vol tage (V _{OHHS}) Method of 185 185 | |
|---------------|-------------------------------------------------------------|--------------------------------------------------------------------------------------------|-----------|
| Т | est 1.3.11 Data La | ne HS-TX 20%-80% Rise Time (t _R) Method of Implementation | 185 |
| | Test References | 185 | |
| T | est 1.3.12 Data La | ne HS-TX 80%-20% Fall Time (t _F) Method of Implementation | 186 |
| | Test References | 186 | |
| 12 MIPI D-PHY | 1.1 High Speed C | Clock Transmitter (HS Clock TX) Electrical Tests | |
| F | | eed Clock Transmitter Electrical Tests 188 188 | |
| | | TX Static Common Mode Vol tage (V _{CMTX}) Method of 190 | |
| Т | est 1.4.8 HS Clock | TX VCMTX Mismatch ($DV_{CMTX}(1,0)$) Method of Implementation | 190 |
| | Test References | 190 | |
| | | ck TX Common-Level Variations Above 450 MHz (DV _{CMTX} (HF)) N 190 190 | lethod of |
| | Test 1.4.9 HS Clock Method of Impleme Test References | TX Common-Level Variations Between 50-450 MHz (DV _{CMTX} (L ntation 190 190 | F)) |
| Т | est 1.4.4 HS Clock | TX Differential Voltage (V _{OD}) Method of Implementation 190 |) |
| | Test References | 190 | |
| | Test 1.4.5 HS Clock mplementation Test References | TX Differential Voltage Mismatch (DV _{OD}) Method of 190 190 | |
| | | k TX Single-Ended Output High Voltage (V_{OHHS}) Method of 190 190 | |
| T | est 1.4.11 Clock La | ane HS-TX 20%-80% Rise Time (t _R) Method of Implementation | 190 |
| | Test References | 190 | |
| Т | est 1.4.12 Clock La | ane HS-TX 80%-20% Fall Time (t _F) Method of Implementation | 191 |
| | Test References | 191 | |
| T | Test 1.4.17 HS Cloc Test References | ck Instantaneous Method of Implementation 191 | |

| Test 1.4.18 Clock Lane HS Clock Del ta UI (UI variation) Method of Implement PASS Condition 192 Test Availability Condition 192 Measurement Algorithm using Test ID 1911 192 Test References 192 | itation 19 | 92 |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----|
| 13 MIPI D-PHY 1.1 Low Power Data Transmitter (LP Data TX) Electrical Tests | | |
| Probing for Low Power Transmitter Electrical Tests 194 Test Procedure 194 | | |
| Test 1.1.1 LP TX Thevenin Output High Vol tage Level (V _{OH}) Method of Implementation 196 PASS Condition 196 Test Availability Condition 196 Measurement Algorithm using Test ID 821 196 Measurement Algorithm using Test ID 8211 197 Test References 197 | | |
| Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V _{OL}) Method of Implem | nentation | 198 |
| PASS Condition 198 Test Availability Condition 198 Measurement Algorithm using Test ID 822 198 Measurement Algorithm using Test ID 8221 199 Test References 199 | | |
| Test 1.1.3 LP TX 15%-85% Rise Time Level (T _{RLP}) EscapeMode Method of | | |
| Implementation 200 PASS Condition 200 Test Availability Condition 200 Measurement Algorithm using Test ID 8241 200 Test References 200 | | |
| Test 1.1.4 LP TX 15%-85% Fall Time Level (T _{FLP}) Method of Implementation | 201 | |
| PASS Condition 201 Test Availability Condition 201 Measurement Algorithm using Test ID 825 201 Measurement Algorithm using Test ID 8251 202 | | |

Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock (T_{LP-PULSE-TX}) Method of Implementation 203

PASS Condition 203

Test Availability Condition 203

Measurement Algorithm using Test IDs 827, 8271 and 8272 204

Measurement Algorithm using Test IDs 1827, 18271 and 18272 204

Test References 205

Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock (T_{LP-PER-TX}) Method of

Implementation 206

PASS Condition 206

Test Availability Condition 206

Measurement Algorithm using Test ID 828 207

Measurement Algorithm using Test ID 1828 207

Test References 207

Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation 208

PASS Condition 208

Test Availability Condition 208

Measurement Algorithm using Test IDs 829, 8291 and 8292 208

Test References 209

14 MIPI D-PHY 1.1 Low Power Clock Transmitter (LP Clock TX) Electrical Tests

Probing for Low Power Transmitter Electrical Tests 212

Test Procedure 212

Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of

Implementation 214

PASS Condition 214

Test Availability Condition 214

Measurement Algorithm using Test ID 1821 and 28211 214

Measurement Algorithm using Test ID 18211 215

Test References 215

Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OI}) Method of Implementation 216

PASS Condition 216

Test Availability Condition 216

Measurement Algorithm using Test ID 1822 216

Measurement Algorithm using Test ID 18221 217

Measurement Algorithm using Test ID 28221 217

| Test 1.2.3 LP TX 15%-85% Rise Time Level (T _{RLP}) Method of Implementation 219 |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PASS Condition 219 Test Availability Condition 219 Measurement Algorithm using Test ID 18241 219 Measurement Algorithm using Test ID 28241 220 Test References 220 |
| Test 1.2.4 LP TX 15%-85% Fall Time Level (T _{FLP}) Method of Implementation 221 |
| PASS Condition 221 Test Availability Condition 221 Measurement Algorithm using Test ID 1825 221 Measurement Algorithm using Test ID 18251 222 Measurement Algorithm using Test ID 28251 222 Test References 223 |
| Test 1.2.5 LP TX Slew Rate vs. C _{LOAD} Method of Implementation 224 |
| PASS Condition 224 Test Availability Condition 224 Measurement Algorithm using Test ID 1829, 18291 and 18292 224 Measurement Algorithm using Test ID 2829, 28291 and 28292 225 Test References 226 |
| Part II Global Operation |
| 15 MIPI D-PHY 1.1 Data Transmitter (Data TX) Global Operation Tests |
| Probing for Data TX Global Operation Tests 230 Test Procedure 230 |
| Test 1.3.1 HS Entry: Data T _{LPX} Method of Implementation 232 Test References 232 |
| Test 1.3.2 HS Entry: Data TX T _{HS-PREPARE} Method of Implementation 232 |
| Test References 232 |
| Test 1.3.3 HS Entry: Data TX T _{HS-PREPARE} + T _{HS-ZERO} Method of Implementation 232 |
| Test References 232 |
| Test 1.3.13 HS Exit: Data TX T _{HS-TRAIL} Method of Implementation 232 |
| Test References 232 |
| Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T _{REOT}) Method of Implementation 23 |
| Test References 232 |
| Test 1.3.15 HS Exit: Data TX T _{EOT} Method of Implementation 232 |
| Test References 232 |

| Test 1.3.16 HS Exit: Data TX T _{HS-EXIT} Method of Implementation 232 | |
|------------------------------------------------------------------------------------------------------------------|-----|
| 16 MIPI D-PHY 1.1 Clock Transmitter (Clock TX) Global Operation Tests | |
| Probing for Clock TX Global Operation Tests 234 Test Procedure 235 | |
| Test 1.4.1 HS Entry: CLK TX T _{LPX} Method of Implementation 236 | |
| Test References 236 | |
| Test 1.4.2 HS Entry: CLK TX T _{CLK-PREPARE} Method of Implementation 236 | |
| Test References 236 | |
| Test 1.4.3 HS Entry: CLK TX T _{CLK-PREPARE} +T _{CLK-ZERO} Method of Implementation 236 | |
| Test References 236 | |
| Test 1.5.1 HS Entry: CLK TX T _{CLK-PRE} Method of Implementation 236 | |
| Test References 236 | |
| Test 1.5.2 HS Exit: CLK TX T _{CLK-POST} Method of Implementation 236 | |
| Test References 236 | |
| Test 1.4.13 HS Exit: CLK TX T _{CLK-TRAIL} Method of Implementation 236 | |
| Test References 236 | |
| , REOF | 236 |
| Test References 236 | |
| Test 1.4.15 HS Exit: CLK TX T _{EOT} Method of Implementation 236 | |
| Test References 236 | |
| Test 1.4.16 HS Exit: CLK TX T _{HS-EXIT} Method of Implementation 237 | |
| Test References 237 | |
| Part III HS Data-Clock Timing | |
| 17 MIPI D-PHY 1.1 High Speed (HS) Data-Clock Timing Tests | |
| Probing for High Speed Data-Clock Timing Tests 242 Test Procedure 243 | |
| Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation 244 Test References 244 | |
| Test 1.5.4 Data-to-Clock Skew (T _{SKEW(TX)}) Method of Implementation 244 | |
| Test References 244 | |

Part IV Informative Tests

18 MIPI D-PHY 1.1 Informative Tests

248

Part C MIPI D-PHY 1.2

Part I Electrical Characteristics

19 MIPI D-PHY 1.2 High Speed Data Transmitter (HS Data TX) Electrical Tests

Probing for High Speed Data Transmitter Electrical Tests 254

Test Procedure 255

Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of

Implementation 257

Test References 257

Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($DV_{CMTX}(1.0)$) Method of Implementation 257

Test References 257

Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz (DV_{CMTX}(HF)) Method of

Implementation 257

Test References 257

Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz (DV_{CMTX}(LF)) Method of Implementation 257

Test References 257

Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation 257

Test References 257

Test 1.3.5 HS Data TX Differential Voltage Mismatch (DV_{OD}) Method of

Implementation 257

Test References 257

Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of

Implementation 257

| | Test 1.3.11 Data Lane HS-TX 20%-80% Rise | Time (t _R) Method of Implementation | 258 |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------|------------------|
| | PASS Condition 258 Test Availability Condition 258 Measurement Algorithm using Test ID 81101 Measurement Algorithm using Test ID 81102 Measurement Algorithm using Test ID 81104 Measurement Algorithm using Test ID 81105 259 Test References 260 | 258 259 259 259 | |
| | Test 1.3.12 Data Lane HS-TX 80%-20% Fall | Time (t _F) Method of Implementation | 261 |
| | PASS Condition 261 Test Availability Condition 261 Measurement Algorithm using Test ID 81111 Measurement Algorithm using Test ID 81112 Measurement Algorithm using Test ID 81114 Measurement Algorithm using Test ID 81115 262 Test References 263 | 261 262 262 262 | |
| 20 MIPI D-I | PHY 1.2 High Speed Clock Transmitter (HS Cl | nck TX) Flectrical Tests | |
| | Probing for High Speed Clock Transmitter El Test Procedure 267 Test 1.4.7 HS Clock TX Static Common Model Implementation 269 Test References 269 | ectrical Tests 267 | |
| | Test 1.4.8 HS Clock TX VCMTX Mismatch (D Test References 269 | V _{CMTX} (_{1,0)}) Method of Implementation | 269 |
| | Test 1.4.10 HS Clock TX Common-Level Vari Implementation 269 Test References 269 | ations Above 450 MHz (DV _{CMTX} (HF)) N | /lethod of |
| | Test 1.4.9 HS Clock TX Common-Level Varia Method of Implementation 269 Test References 269 | tions Between 50-450 MHz (DV _{CMTX} (l | ₋ F)) |
| | Test 1.4.4 HS Clock TX Differential Voltage | (V _{OD}) Method of Implementation 26 | 9 |
| | Test References 269 | | |
| | Test 1.4.5 HS Clock TX Differential Vol tage I Implementation 269 Test References 269 | Mismatch (DV _{OD}) Method of | |

| Test 1. 4.6 HS Clock TX Single-Ended Output High Voltage (V _{OHHS}) Method of Implementation 269 Test References 269 | |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|
| Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t _R) Method of Implementation | n 270 |
| PASS Condition 270 Test Availability Condition 270 Measurement Algorithm using Test ID 181101 270 Measurement Algorithm using Test ID 181102 271 Measurement Algorithm using Test ID 181103 271 Measurement Algorithm using Test ID 181104 272 Measurement Algorithm using Test ID 181105 272 Measurement Algorithm using Test ID 181106 272 Test References 272 | |
| Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t _F) Method of Implementation | 273 |
| PASS Condition 273 Test Availability Condition 273 Measurement Algorithm using Test ID 181111 273 Measurement Algorithm using Test ID 181112 274 Measurement Algorithm using Test ID 181113 274 Measurement Algorithm using Test ID 181114 275 Measurement Algorithm using Test ID 181115 275 Measurement Algorithm using Test ID 181116 275 Test References 275 | |
| Test 1.4.17 HS Clock Instantaneous Method of Implementation 276 Test References 276 | |
| Test 1.4.18 Clock Lane HS Clock Del ta UI (UI variation) Method of Implementation PASS Condition 277 Test Availability Condition 277 Measurement Algorithm using Test ID 1911 277 Test References 277 | n 277 |
| MIPI D-PHY 1.2 Low Power Data Transmitter (LP Data TX) Electrical Tests | |
| Probing for Low Power Transmitter Electrical Tests 280 Test Procedure 280 | |

| Test 1.1.1 LP TX Thevenin Output High Vol tage Level (V _{OH}) Method of Implementation 282 |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PASS Condition 282 Test Availability Condition 282 Measurement Algorithm using Test ID 821 282 Measurement Algorithm using Test ID 8211 283 Test References 283 |
| Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation 284 |
| PASS Condition 284 Test Availability Condition 284 Measurement Algorithm using Test ID 822 284 Measurement Algorithm using Test ID 8221 285 Test References 285 |
| Test 1.1.3 LP TX 15%-85% Rise Time Level (T _{RLP}) EscapeMode Method of |
| Implementation 286 |
| PASS Condition 286 Test Availability Condition 286 Measurement Algorithm using Test ID 8241 286 Test References 286 |
| Test 1.1.4 LP TX 15%-85% Fall Time Level (T _{FLP}) Method of Implementation 287 |
| PASS Condition 287 Test Availability Condition 287 Measurement Algorithm using Test ID 825 287 Measurement Algorithm using Test ID 8251 288 Test References 288 |
| Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock (T _{IP-PULSE-TX}) Method of |
| Implementation 289 |
| PASS Condition 289 Test Availability Condition 289 Measurement Algorithm using Test IDs 827, 8271 and 8272 290 Measurement Algorithm using Test IDs 1827, 18271 and 18272 290 Test References 291 |
| Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock (T _{LP-PER-TX}) Method of |
| Implementation 292 |
| PASS Condition 292 Test Availability Condition 292 Measurement Algorithm using Test ID 828 293 Measurement Algorithm using Test ID 1828 293 |

| Te | PASS Condition 294 Test Availability Condition 294 Measurement Algorithm using Test IDs 829, 8291 and 8292 294 Test References 295 |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22 MIPI D-PHY 1 | .2 Low Power Clock Transmitter (LP Clock TX) Electrical Tests |
| Pro | Debing for Low Power Transmitter Electrical Tests 298 Test Procedure 298 |
| | st 1.2.1 LP TX Thevenin Output High Vol tage Level (V _{OH}) Method of plementation 300 PASS Condition 300 Test Availability Condition 300 Measurement Algorithm using Test ID 1821 and 28211 300 Measurement Algorithm using Test ID 18211 301 Test References 301 |
| Te | st 1.2.2 LP TX Thevenin Output Low Voltage Level (V _{OL}) Method of Implementation 302 |
| | PASS Condition 302 Test Availability Condition 302 Measurement Algorithm using Test ID 1822 302 Measurement Algorithm using Test ID 18221 303 Measurement Algorithm using Test ID 28221 303 Test References 304 |
| Te | st 1.2.3 LP TX 15%-85% Rise Time Level (T _{RLP}) Method of Implementation 305 |
| | PASS Condition 305 Test Availability Condition 305 Measurement Algorithm using Test ID 18241 305 Measurement Algorithm using Test ID 28241 306 Test References 306 |
| Te | st 1.2.4 LP TX 15%-85% Fall Time Level (T _{FLP}) Method of Implementation 307 |
| | PASS Condition 307 Test Availability Condition 307 Measurement Algorithm using Test ID 1825 307 Measurement Algorithm using Test ID 18251 308 Measurement Algorithm using Test ID 28251 308 Test References 309 |

| Test 1.2.5 LP TX Slew Rate vs. C _{LOAD} Method of Implementation 310 | |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| PASS Condition 310 Test Availability Condition 310 Measurement Algorithm using Test ID 1829, 18291 and 18292 310 Measurement Algorithm using Test ID 2829, 28291 and 28292 311 Test References 312 | |
| Part II Global Operation | |
| 23 MIPI D-PHY 1.2 Data Transmitter (Data TX) Global Operation Tests | |
| Probing for Data TX Global Operation Tests 316 Test Procedure 316 | |
| Test 1.3.1 HS Entry: Data T _{LPX} Method of Implementation 318 Test References 318 | |
| Test 1.3.2 HS Entry: Data TX T _{HS-PREPARE} Method of Implementation 318 Test References 318 | |
| Test 1.3.3 HS Entry: Data TX T _{HS-PREPARE} + T _{HS-ZERO} Method of Implementation 318 Test References 318 | |
| Test 1.3.13 HS Exit: Data TX T _{HS-TRAIL} Method of Implementation 318 | |
| Test References 318 | |
| Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T _{REOT}) Method of Implementation 3° | 18 |
| Measurement Algorithm using Test ID 549 318 Test References 318 | |
| Test 1.3.15 HS Exit: Data TX T _{EOT} Method of Implementation 319 | |
| Measurement Algorithm using Test ID 547 319 Test References 319 | |
| Test 1.3.16 HS Exit: Data TX T _{HS-EXIT} Method of Implementation 319 | |
| 24 MIPI D-PHY 1.2 Clock Transmitter (Clock TX) Global Operation Tests | |
| Probing for Clock TX Global Operation Tests 322 Test Procedure 323 | |
| Test 1.4.1 HS Entry: CLK TX T _{LPX} Method of Implementation 324 | |
| Test References 324 | |
| Test 1.4.2 HS Entry: CLK TX T _{CLK-PREPARE} Method of Implementation 324 Test References 324 | |
| | |

| | Test 1.4.3 HS Entry: CLK TX T _{CLK-PREPARE} +T _{CLK-ZERO} Method of Implementation 324 Test References 324 |
|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | Test 1.5.1 HS Entry: CLK TX T _{CLK-PRE} Method of Implementation 324 Test References 324 |
| | Test 1.5.2 HS Exit: CLK TX T _{CLK-POST} Method of Implementation 324 Test References 324 |
| | Test 1.4.13 HS Exit: CLK TX T _{CLK-TRAIL} Method of Implementation 324 Test References 324 |
| | Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T _{REOT}) Method of Implementation 324 Measurement Algorithm using Test ID 559 324 Test References 325 |
| | Test 1.4.15 HS Exit: CLK TX T _{EOT} Method of Implementation 325 |
| | Measurement Algorithm using Test ID 544 325 Test References 325 |
| | Test 1.4.16 HS Exit: CLK TX T _{HS-EXIT} Method of Implementation 325 Test References 325 |
| | Part III HS Data-Clock Timing & HS Skew Calibration Burst |
| 25 | MIPI D-PHY 1.2 High Speed (HS) Data-Clock Timing Tests |
| | Probing for High Speed Data-Clock Timing Tests 330 Test Procedure 331 |
| | Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation 332 Test References 332 |
| | Test 1.5.4 Data-to-Clock Skew (T _{SKEW(TX)}) Method of Implementation 332 Measurement Algorithm using Test ID 913 332 Test References 333 |
| 26 | MIPI D-PHY 1.2 High Speed (HS) Skew Calibration Burst Tests |
| | Probing for High Speed Skew Calibration Burst Tests 336 Test Procedure 337 |

Test 1.5.5 Initial HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation 338

PASS Condition 338

Test Availability Condition 338

Measurement Algorithm using Test ID 917 339

Measurement Algorithm using Test ID 918 339

Test References 339

Test 1.5.6 Periodic HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation 340

PASS Condition 340

Test Availability Condition 340

Measurement Algorithm using Test ID 919 340

Measurement Algorithm using Test ID 920 341

Test References 341

Part IV Informative Tests

27 MIPI D-PHY 1.2 Informative Tests 346

Part V Introduction

28 Calibrating the Infiniium Oscilloscopes and Probes

To Run the Self Calibration 350

Self Calibration 351

Required Equipment for Solder-in and Socketed Probe Head's Calibration 354

Calibration for Solder-in and Socketed Probe Heads 355

Connecting the Probe for Calibration 355

Verifying the Connection 357

Running the Probe Calibration and Deskew 359

Verifying the Probe Calibration 361

Required Equipment for Browser Probe Head Calibration 364

Calibration for Browser Probe Head 365

Connecting the Probe for Calibration 365

29 InfiniiMax Probing

Index

Contents

Keysight U7238C/U7238D MIPI D-PHY Test App Methods of Implementation

1 Installing the MIPI D-PHY Test App

Installing the Software / 32
Installing the License Key / 33

If you purchase the U7238C/U7238D MIPI D-PHY Test App separately, you must also install the software and license key.



1

Installing the Software

- 1 Make sure you have the minimum version of Infiniium oscilloscope software (see the U7238C/U7238D test application release notes) by choosing **Help>About Infiniium...** from the main menu.
- 2 To obtain the MIPI D-PHY Test App, go to Keysight website: http://www.keysight.com/find/scope-apps-sw.
- 3 The link for MIPI D-PHY Test App will appear. Double-click on it and follow the instructions to download and install the application software.

Installing the License Key

- 1 Request a license code from Keysight by following the instructions on the Entitlement Certificate. You will need the oscilloscope's "Option ID Number", which you can find in the Help>About Infiniium... dialog box.
- 2 After you receive your license code from Keysight, choose **Utilities>Install Option License....**
- 3 In the Install Option License dialog, enter your license code and click Install License.
- 4 Click **OK** on the dialog that prompts you to restart the Infiniium oscilloscope application software to complete the license installation.
- 5 Click Close to close the Install Option License dialog.
- 6 Choose File>Exit.
- 7 Restart the Infiniium oscilloscope application software to complete the license installation.

1 Installing the MIPI D-PHY Conformance Test Application

Keysight U7238C/U7238D MIPI D-PHY Test App Methods of Implementation

2 Preparing to Take Measurements

Calibrating the Oscilloscope / 36 Starting the MIPI D-PHY Test App / 37 Fixture Options / 39

Before running the MIPI D-PHY automated tests, calibrate the oscilloscope and probe. After you calibrate the oscilloscope and the probe, start the MIPI D-PHY Test App and perform the test measurements.



Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope and probe, see Chapter 28, "Calibrating the Infiniium Oscilloscopes and Probes".

NOTE

If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, perform an internal calibration again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities>Calibration** menu.

NOTE

If you switch cables between the channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once you perform calibration, label the cables with the channel on which they were calibrated.

Starting the MIPI D-PHY Test App

1 To start the MIPI D-PHY Test App: From the Infiniium oscilloscope's main menu, choose Analyze>Automated Test Apps>U7238C/U7238D MIPI D-PHY Test App.

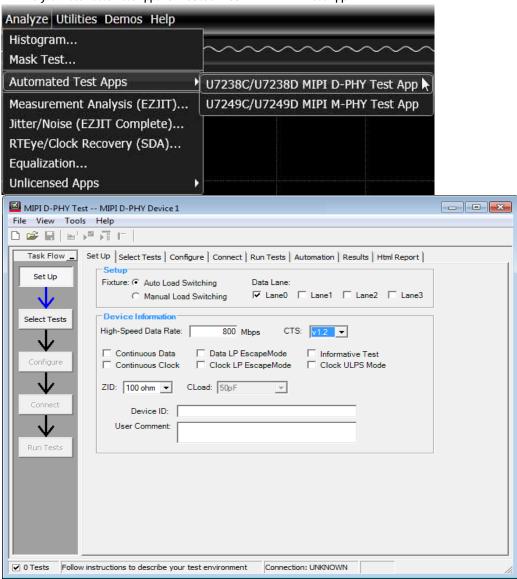


Figure 1 The MIPI D-PHY Test App

NOTE

If U7238C/U7238D MIPI D-PHY Test App does not appear in the **Automated Test Apps** menu, the MIPI D-PHY Test App has not been installed (see Chapter 1, "Installing the MIPI D-PHY Test App").

Figure 1 shows the MIPI D-PHY Test App main window.

The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

| Tab | Description |
|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Set Up | Lets you identify and setup the test environment, including information about the device under test. |
| Select Tests | Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups. |
| Configure | Lets you configure test parameters (like memory depth). This information appears in the HTML report. |
| Connect | Shows you how to connect the oscilloscope to the device under test for the tests to be run. |
| Run Tests | Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing. |
| Results | Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear. |
| HTML Report | Shows a compliance test report that can be printed. |

Online Help Topics

For information on using the MIPI D-PHY Test App, see its online help (which you can access by choosing **Help>Contents...** from the application's main menu).

The MIPI D-PHY Test App's online help describes:

- · Starting the MIPI D-PHY Test App.
 - · To view or minimize the task flow pane.
 - To view or hide the toolbar.
- · Creating or opening a test project.
- Setting up MIPI D-PHY test environment.
- Selecting tests.
- · Configuring selected tests.
- Connecting the oscilloscope to the Device Under Test (DUT).
- · Running tests.
- · Viewing test results.
 - · To show reference images and flash mask hits.
 - · To change margin thresholds.
- · Viewing/printing the HTML test report.
- Understanding the HTML report.
- Saving test projects.

Fixture Options

In some high-speed serial technologies (such as, PCI Express, SATA and so on) that utilize a static, 100-ohm differential reference termination environment, it is typical to use the test equipment input ports as the reference termination load for measurements. However, it is not possible to use the test equipment (in this case, an oscilloscope) as the reference termination because the MIPI D-PHY technology utilizes a dynamic, switchable resistive termination at the receiver (to enable the power-saving feature). This switchable resistive termination, which is a 100-ohm differential reference termination, is enabled during the High-Speed (HS) mode of operation, and disabled (open termination environment) during the Low-Power (LP) mode.

The common approach to perform the MIPI D-PHY test measurements is to utilize some test measurement fixtures that have the capability to handle the required termination load of various forms for the selected tests (High-Speed mode or Low-Power mode tests). In general, there are two types of test fixtures where one type is able to handle the automatic switching of the required termination load and the other type supports only one termination load at a time.

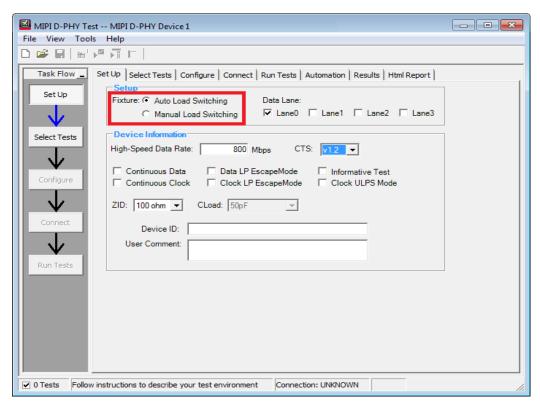


Figure 2 Fixture Options on the MIPI D-PHY Test App

Manual Load Switching

For test fixtures that may handle only static termination environment, either by providing a 100-ohm differential reference termination load or just an open load condition, you must select the **Manual Load Switching** option in the **Fixture** area of the **Set Up** tab of the test compliance application. In such scenarios, when you run tests after selecting some HS mode tests and some LP mode tests under the **Select Tests** tab, the application prompts a connection diagram, which allows you to change the physical set up and use the correct test fixture.

Auto Load Switching

For test fixtures that may handle the dynamic termination load switching criteria, you must select the **Auto Load Switching** option in the **Fixture** area of the **Set Up** tab of the test compliance application. The most common test fixture that you may use is the MIPI D-PHY Reference Termination Board (RTB). You may obtain the MIP D-PHY RTB from the University of New Hampshire InterOperability Lab (UNH-IOL). The UNH-IOL works closely with the MIPI Alliance (standard body for MIPI) and has developed a testing program/fixtures/boards to meet the unique needs of the mobile industry (including the D-PHY RTB). In this scenario, you may use the same test fixture (for example, the RTB) setup to handle the dynamic termination environment required when testing all the HS mode tests.



Figure 3 Sample MIPI D-PHY Reference Termination board (RTB)

| | Part A MIPI D-PHY 1.0 |
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3 MIPI D-PHY 1.0 High Speed Data Transmitter (HS Data TX) Electrical Tests

Probing for High Speed Data Transmitter Electrical Tests / 46

Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation / 49

Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($DV_{CMTX}(1,0)$) Method of Implementation / 51

Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz ($DV_{CMTX}(HF)$) Method of Implementation / 53

Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz (DV $_{\rm CMTX}$ (LF)) Method of Implementation / 55

Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation $\,/\,$ 57

Test 1.3.5 HS Data TX Differential Voltage Mismatch (DV_{OD}) Method of Implementation / 59

Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation / 61

Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation / 63

Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation / 64

This section provides the Methods of Implementation (MOIs) for the High Speed Data Transmitter (HS Data TX) Electrical tests using an Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test App.



3

Probing for High Speed Data Transmitter Electrical Tests

When performing the HS Data TX tests, the MIPI D-PHY Test App may prompt you to make changes to the physical setup. The connections for the HS Data TX tests may look similar to the following diagrams. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

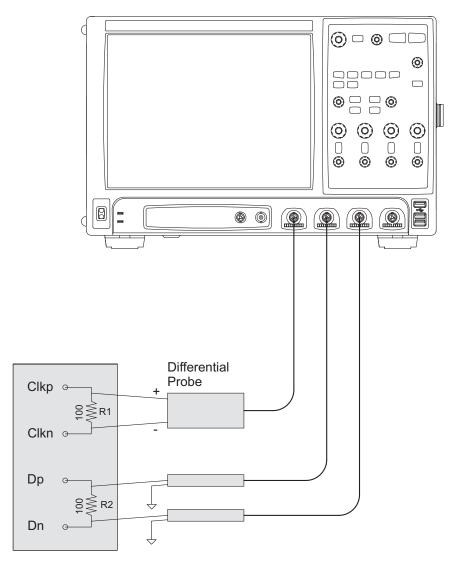


Figure 4 Probing with Three Probes for High Speed Data Transmitter Electrical Tests

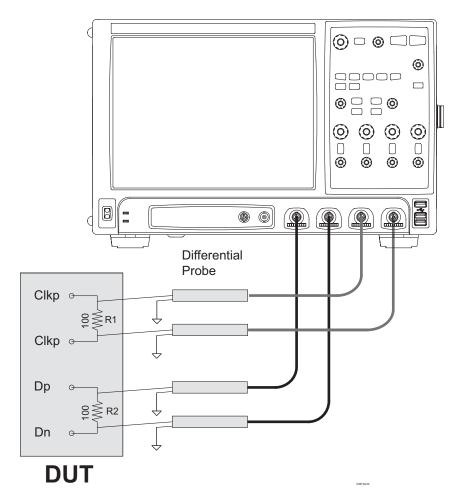


Figure 5 Probing with Four Probes for High Speed Data Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test App. (The channels shown in Figure 4 and Figure 5 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the Set Up tab.
- 3 Enter the High-Speed Data Rate, ZID (termination resistance), CLoad, Device ID and User Comments.
- 4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

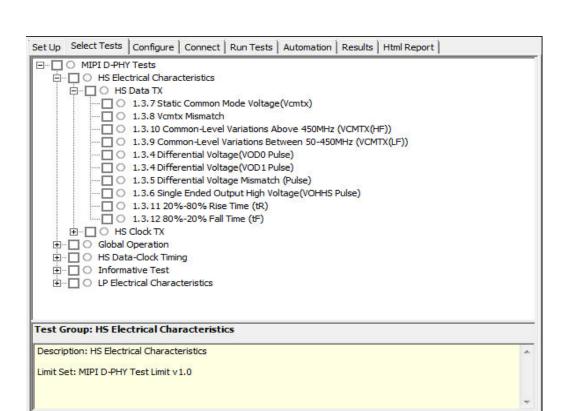


Figure 6 Selecting High Speed Data Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation

The High Speed Data Transmitter Static Common Mode Voltage, V_{CMTX} is defined as the arithmetic mean value of the voltages at the Dp and Dn pins. Because of various types of signal distortion that may occur, it is possible for V_{CMTX} to have different values when a Differential-1 vs. Differential-0 state is driven.

For this test, the values for V_{CMTX} is measured for both the Differential-1 and Differential-0 states and averaged over at least a HS burst.

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

Ideal Single-Ended High Speed Signals

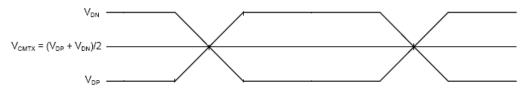


Figure 7 Ideal Single-Ended High Speed Signals

PASS Condition

The measured V_{CMTX} value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 1 Test Availability Condition for Test 1.3.7

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 811 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

3

Measurement Algorithm using Test ID 811

NOTE

Use the Test ID# 811 to remotely access the test.

- 1 Trigger at SoT of HS Data burst (LP11 to LP01).
- 2 For the HS Data, common-mode waveform is required. The waveform can be constructed by using the following equation:

DataCommonMode = $(D_p+D_n)/2$

3 For the HS Clock, differential waveform is required. This can be achieved by directly probing the differential signal or by probing the single-ended clock signal and form a differential signal by using the singled-ended signals with the following equation:

ClockDiff = Clkp - Clkn

- 4 Sample the Common-Mode HS Data waveform by using all the edges of the differential HS Clock as sampler and denote it as V_{CMTX} .
- 5 Separate the V_{CMTX} into 2 arrays; V_{CMTX} for Differential-1 and V_{CMTX} for Differential-0.
- 6 Report the measurement results:
 - Mean V_{CMTX} for Differential-1 and Differential-0
 - V_{CMTX} worst value between Differential-1 and Differential-0
- 7 Compare the measured V_{CMTX} worst value to the compliance test limits.

Test References

See Test 1.3.7 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1,0)}$) Method of Implementation

The common-mode voltage V_{CMTX} is defined as the arithmetic mean value of the voltages at the D_p and D_n pins. Because of various types of signal distortion that occurs, it is possible for V_{CMTX} to have different values when a Differential-1 vs. Differential-0 state is being driven.

For this test, the values for V_{CMTX} are measured for both the Differential-1 and differential-0 states and averaged over at least one HS Data burst. The difference between the V_{CMTX} values for Differential-1 and Differential-0 is computed.

$$V_{\rm CMTX} = \frac{V_{\rm DP} + V_{\rm DN}}{2} \qquad , \qquad \Delta V_{\rm CMTX(1.0)} = \frac{V_{\rm CMTX(1)} - V_{\rm CMTX(0)}}{2} \label{eq:cmtx}$$

Ideal Single-Ended High Speed Signals

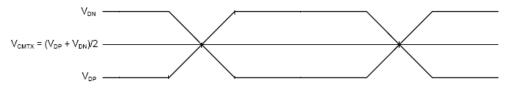


Figure 8 Ideal Single-Ended High Speed Signals

PASS Condition

The measured $\Delta V_{\text{CMTX}(1,0)}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 2 Test Availability Condition for Test 1.3.8

| | Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|---|------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| | Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| _ | 812 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 812

NOTE

Use the Test ID# 812 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - HS TX Static Common Mode Voltage (V_{CMTX}) (Test ID 811)
 - Actual V_{CMTX} for Differential-1 and Differential-0 measurements are performed and test results are stored.
- 2 Compute the V_{CMTX} mismatch using the following calculation:

 V_{CMTX} Mismatch = ([V_{CMTX} for Differential-1] - [V_{CMTX} for Differential-0]) / 2

- 3 MIPI D-PHY 1.0 High Speed Data Transmitter (HS Data TX) Electrical Tests
 - 3 Report the measurement results:
 - + V_{CMTX} for Differential-1 and Differential-0
 - V_{CMTX} mismatch
 - 4 Compare the measured ΔV_{CMTX} mismatch to the compliance test limit.

Test References

See Test 1.3.8 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz ($\Delta V_{CMTX(HF)}$) Method of Implementation

For this $\Delta V_{CMTX(HF)}$ test, the values for V_{CMTX} is obtained by using the following equation:

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

Ideally the common mode voltage should be as per the figure below.

Ideal Single-Ended High Speed Signals V_{DN} $V_{CMTX} = (V_{DP} + V_{DN})/2$

Figure 9 Ideal Single-Ended High Speed Signals

Static ΔV_{CMTX} (SE HS Signals) V_{DN} V_{CMTX} V_{DP} V_{OD(0)}

Possible ΔV_{CMTX} Distortions of the Single-ended HS Signals

Dynamic ∆V_{CMTX} (SE HS Signals)



Figure 10 Possible Distortions of the ΔV_{CMTX} Single-Ended High Speed Signals

The objective of the test is to measure the distortion over the interested frequency band for a HS Data burst.

PASS Condition

The measured $\Delta V_{CMTX(HF)}$ value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 3 Test Availability Condition for Test 1.3.10

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|-------------------|-------------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 818 | Not Applicable | 100 ohm | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 818

NOTE

Use the Test ID# 818 to remotely access the test.

- 1 Trigger at SoT of HS Data burst (LP11 to LP01).
- 2 Find the HS Data bursts.
- 3 For the HS Data, common-mode waveform is required. The waveform can be constructed using the following equation:

DataCommonMode = (Dp+Dn)/2

- 4 A high pass filter with 3dB bandwidth frequency at 450MHz is applied to the common-mode waveform.
- 5 Measure the RMS voltage for the filtered waveform and record as $\Delta V_{CMTX(HF)}$.
- 6 Report the measurement results:
 - ΔV_{CMTX(HF)} value
- 7 Compare the measured $\Delta V_{CMTX(HF)}$ value to the compliance test limit.

Test References

See Test 1.3.10 in CTS v1.0 and Section 8.1.1 Table 17 in the D-PHY Specification v1.0.

Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz ($\Delta V_{CMTX(LF)}$) Method of Implementation

For this $\Delta V_{CMTX(LF)}$ test, the values for V_{CMTX} is obtained by using the following equation:

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

Ideally the common mode voltage should be as per the figure below:

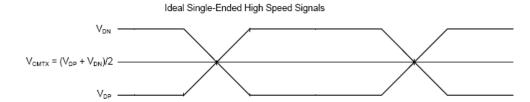


Figure 11 Ideal Single-Ended High Speed Signals

In reality, various type for distortion can happen as shown in figure below:

Static \(\Delta V_{CMTX} \) (SE HS Signals) \(V_{DN} \) \(V_{CMTX} \) \(V_{DP} \) \(V_{OD(0)} \)

Possible ΔV_{CMTX} Distortions of the Single-ended HS Signals

Dynamic ∆V_{CMTX} (SE HS Signals)



Figure 12 Possible Distortions of the ΔV_{CMTX} Single-Ended High Speed Signals

The objective of the test is to measure the distortion over the interested frequency band for a HS data burst.

PASS Condition

The measured $\Delta V_{CMTX(LF)}$ value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 4 Test Availability Condition for Test 1.3.9

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|----------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 819 | Not Applicable | 100 ohm | Not Applicable |

Measurement Algorithm using Test ID 819

NOTE

Use the Test ID# 819 to remotely access the test.

- 1 Trigger at SoT of HS data burst (LP11 to LP01).
- 2 Find the HS data bursts.
- 3 For the HS data, common-mode waveform is required. The waveform can be constructed using the following equation:

DataCommonMode = (Dp+Dn)/2

- 4 A band pass filter with 3dB bandwidth frequency at 50MHz and 450MHz is applied to the common-mode waveform.
- 5 Measure the min and max voltage for the filtered waveform.
- 6 Select the worst absolute value for the min and max voltage and record it as $\Delta V_{CMTX(LF)}$.
- 7 Report the measurement results:
 - ΔV_{CMTX(LF)} value
- 8 Compare the measured $\Delta V_{CMTX(LF)}$ value to the compliance test limit.

Test References

See Test 1.3.9 in CTS v1.0 and Section 8.1.1 Table 17 in the D-PHY Specification v1.0.

Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation

The output differential voltage, V_{OD} is defined as the difference of voltages V_{DP} and V_{DN} at the Dp and Dn pins, respectively.

$$V_{OD} = V_{DP} - V_{DN}$$

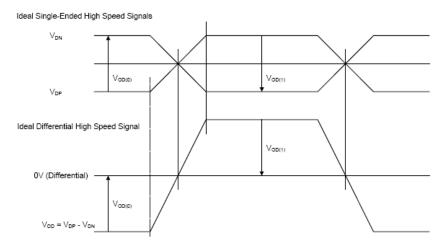


Figure 13 Ideal Single-Ended and Differential High Speed Signals

PASS Condition

The measured V_{OD} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 5 Test Availability Condition for Test 1.3.4

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 8131 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 8132 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test IDs 8131 and 8132

HS Data TX Differential Voltage (V_{OD0} Pulse)

NOTE

Use the Test ID# 8131 to remotely access the test.

3

HS Data TX Differential Voltage (V_{OD1} Pulse)

NOTE

Use the Test ID# 8132 to remotely access the test.

- 1 Trigger at SoT of HS data burst (LP11 to LP01).
- 2 Find the HS data bursts.
- 3 For HS data, differential waveform is required. The waveform can be constructed by using the following equation:

DataDiff = Dp-Dn

4 For the HS Clock, differential waveform is required. The waveform can be constructed by using the following equation:

ClkDiff = Clkp - Clkn

- 5 The acquired waveform is searched for the respective reference data pattern of "011111" for V_{OD1} and "100000" for V_{OD0} test.
- 6 Generates the averaged waveform that consists of all the reference data pattern found.
- The mean value for the histogram window that fall between the centers of the fourth and fifth '1' bits is measured as the mean V_{OD} value using the histogram function.
- 8 Report the measurement results:
 - Mean V_{OD} for Differential-1 or Differential-0
- 9 Compare the mean $V_{\mbox{\scriptsize OD}}$ value to the compliance test limit.

Test References

See Test 1.3.4 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Physical Specification v1.0.

Test 1.3.5 HS Data TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation

The Output Differential Voltage Mismatch, ΔV_{OD} is defined as the difference of the absolute values of the differential output voltage in the Differential-1 state $V_{OD(1)}$ and the differential output voltage in the Differential-0 state $V_{OD(0)}$.

$$\Delta V_{\mathit{OD}} = \left| V_{\mathit{OD}(1)} \right| - \left| V_{\mathit{OD}(0)} \right|$$

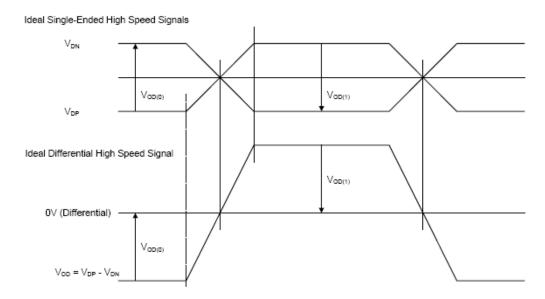


Figure 14 Ideal Single-Ended and Differential High Speed Signals

PASS Condition

The measured ΔV_{OD} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 6 Test Availability Condition for Test 1.3.5

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 8141 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 8141

HS Data TX Differential Voltage Mismatch (Pulse)

NOTE

Use the Test ID# 8141 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - HS Data TX Differential Voltage (V_{OD0} Pulse) (Test ID: 8131)
 - HS Data TX Differential Voltage (V_{OD1} Pulse) (Test ID: 8132)
 - The actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
- 2 Calculate the difference between $V_{\mbox{\scriptsize OD}}$ for Differential-1 and Differential-0.
- 3 Report the measurement results:
 - V_{OD} for Differential-1 and Differential-0
- 4 Compare the measured ΔV_{OD} between Differential-1 and Differential-0 value to the compliance test limit.

Test References

See Test 1.3.5 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation

The output voltages V_{DP} and V_{DN} at the Dp and Dn pins should not exceed the High-Speed output high voltage, V_{OLHS} is the High-Speed output, low voltage on Dp and Dn, and is determined by V_{OD} and V_{CMTX} . The High-Speed V_{OUT} is bounded by the minimum value of V_{OLHS} and the maximum value of V_{OHHS} .

Ideal Single-Ended High Speed Signals V_{DN} $V_{CMTX} = (V_{DP} + V_{DN})/2$ V_{OP} $V_{OD(1)}$

Figure 15 Ideal Single-Ended High Speed Signals

PASS Condition

The measured V_{OHHS} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 7 Test Availability Condition for Test 1.3.6

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|-------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 8151 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | |

Measurement Algorithm using Test ID 8151

HS Data TX Single Ended Output High Voltage (V_{OHHS} Pulse)

NOTE

Use the Test ID# 8151 to remotely access the test.

- 1 Trigger at SoT of HS Data burst (LP11 to LP01).
- 2 Find the HS Data Bursts.
- 3 The acquired single-ended Dp and Dn waveform is searched for the reference data pattern of "011111"
- 4 The averaged waveform that consists of all the reference data patterns found is generated for Dp and Dn.
- The mean value for the histogram window that falls between the centers of the fourth and fifth '1' bits is measured as the mean V_{OHHS} value for each single-ended HS Data signal and denotes each value as V_{OHHS} (Dp) and V_{OHHS} (Dn) using the **Histogram** function.

- 3 MIPI D-PHY 1.0 High Speed Data Transmitter (HS Data TX) Electrical Tests
 - 6 Report the measurement results:
 - V_{OHHS}(Dp)
 - V_{OHHS}(Dn)
 - Worst V_{OHHS} value
 - 7 Compare the worst V_{OHHS} value to the compliance test limits.

Test References

See Test 1.3.5 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation

The rise time, t_R is defined as the transition time between 20% and 80% of the full HS signal swing. The driver must meet the t_R specifications for all the allowable Z_{ID} .

PASS Condition

The measured t_R value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 8 Test Availability Condition for Test 1.3.11

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 8110 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 8110

NOTE

Use the Test ID# 8110 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (Ul_{inst})[Max] (Test ID: 911): UI value measurements for test signal are performed and test results are stored.
 - b HS Data TX Differential Voltage (V_{OD}) (Test ID: 8131, 8132): Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
- 2 Trigger on SoT of HS Data burst (LP11->LP01).
- 3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

DataDiff = Dp-Dn

4 Define the measurement threshold as follows:

Top Level: V_{OD1} (V_{OD} for Differential-1)

Base Level: V_{OD0} (V_{OD} for Differential-0)

- 5 Use a MATLAB script to identify and extract all the "000111" pattern locations found in the differential signal.
- 6 Measure the 20%-80% rise time at all the rising edges of the "000111" pattern that is identified.
- 7 Compare the measured t_R (Mean) value with the maximum and minimum conformance test limits.

Test References

See Test 1.3.11 in CTS v1.0 and Section 9.1.1 Table 17 in the D-PHY Specification v1.0.

3

Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation

The fall time, t_F is defined as the transition time between 80% and 20% of the full HS signal swing. The driver must meet the t_F specifications for all the allowable Z_{ID} .

PASS Condition

The measured t_F value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 9 Test Availability Condition for Test 1.3.12

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 8111 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 8111

NOTE

Use the Test ID# 81111 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (UI_{inst})[Max] (Test ID: 911)
 UI value measurements for test signal are performed and test results are stored.
 - b HS Data TX Differential Voltage (V_{OD}) (Test ID: 8131, 8132)
 Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
- 2 Trigger on SoT of the HS Data burst (LP11->LP01).
- 3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

DataDiff = Dp-Dn

4 Define the measurement threshold as follows:

Top Level: V_{OD1} (V_{OD} for Differential-1)

Base Level: V_{OD0} (V_{OD} for Differential-0)

- 5 Use a MATLAB script to identify and extract all the "111000" pattern locations found in the differential signal.
- 6 Measure the 80%-20% fall time at all the falling edges of the "111000" pattern that is identified.
- 7 Compare the measured value of t_F (Mean) with the maximum and minimum conformance test limits.

Test References

See Test 1.3.12 in CTS v1.0 and Section 9.1.1 Table 17 in the D-PHY Specification v1.0.

Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

4 MIPI D-PHY 1.0 High Speed Clock Transmitter (HS Clock TX) Electrical Tests

Probing for High Speed Clock Transmitter Electrical Tests / 66

Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation / 68 Test 1.4.8 HS Clock TX VCMTX Mismatch ($DV_{CMTX}(1,0)$) Method of Implementation / 70 Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz ($DV_{CMTX}(HF)$) Method of Implementation / 72

Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz ($DV_{CMTX}(LF)$) Method of Implementation / 74

Test 1.4.4 HS Clock TX Differential Voltage (V_{OD}) Method of Implementation / 76

Test 1.4.5 HS Clock TX Differential Voltage Mismatch (DV_{OD}) Method of Implementation / 78

Test 1. 4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation / 80

Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation / 82

Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation / 83

Test 1.4.17 HS Clock Instantaneous Method of Implementation / 84

This section provides the Methods of Implementation (MOIs) for the High Speed Clock Transmitter (HS Clock T_X) Electrical tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.



Probing for High Speed Clock Transmitter Electrical Tests

When performing the HS Clock T_x tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the HS Clock T_X tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

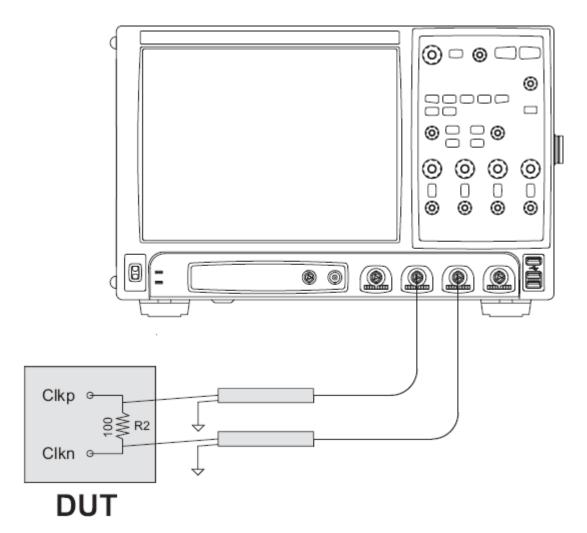


Figure 16 Probing for High Speed Clock Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 16 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.

- 3 Enter the High-Speed Data Rate, ZID (termination resistance), Cload, Device ID and User Comments.
- 4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

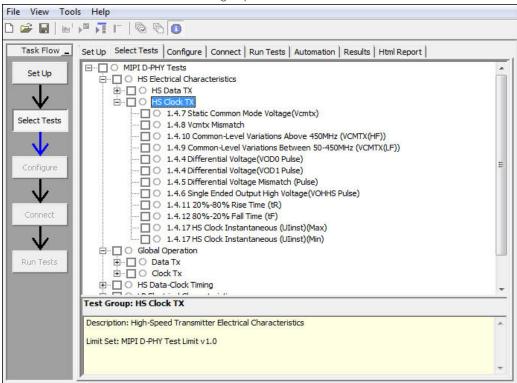


Figure 17 Selecting High Speed Clock Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation

The High Speed Clock Transmitter Common-Mode Voltage, V_{CMTX} is defined as the arithmetic mean value of the voltages at the Clkp and Clkn pins. Because of various types of signal distortion that may occur, it is possible for V_{CMTX} to have different values when a Differential-1 vs. Differential-0 state is driven.

For this test, the values for V_{CMTX} are measured for both the Differential-1 and Differential-0 states and averaged.

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

Ideal Single-Ended High Speed Signals

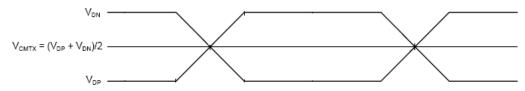


Figure 18 Ideal Single-Ended High Speed Signals

PASS Condition

The measured V_{CMTX} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 10 Test Availability Condition for Test 1.4.7

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 1811 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 1811

NOTE

Use the Test ID# 1811 to remotely access the test.

- 1 Trigger the oscilloscope to acquire Clkp and Clkn.
- 2 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

3 Construct common-mode waveform by using the following equation:

ClkCommonMode = (Clkp+Clkn)/2

Sample the Common-Mode HS Clock waveform by using the center of the differential HS Clock's UI as sampler and denote as $V_{\rm CMTX}$.

- 5 Separate the V_{CMTX} into 2 arrays; V_{CMTX} for Differential-1 and V_{CMTX} for Differential-0.
- 6 Report the measurement results:
 - a Mean V_{CMTX} for Differential-1 and Differential-0
 - $b~~{\rm V_{CMTX}}$ worst value between Differential-1 and Differential-0
- 7 Compare the measured $\ensuremath{V_{CMTX}}$ worst value with the compliance test limits.

Test References

See Test 1.4.7 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.4.8 HS Clock TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1,0)}$) Method of Implementation

The common-mode voltage, V_{CMTX} is defined as the arithmetic mean value of the voltages at the Clkp and Clkn pins. Because of various types of signal distortion that may occur, it is possible for V_{CMTX} to have different values when a Differential-1 vs. Differential-0 state is driven.

For this $\Delta V_{CMTX(1,0)}$ test, the values for V_{CMTX} is measured for both the Differential-1 and Differential-0 states and averaged. The difference between the V_{CMTX} values for Differential-1 and Differential-0 is computed.

$$V_{\rm CMTX} = \frac{V_{\rm DP} + V_{\rm DN}}{2} \quad , \quad \Delta V_{\rm CMTX(1,0)} = \frac{V_{\rm CMTX(1)} - V_{\rm CMTX(0)}}{2} \label{eq:cmtx}$$

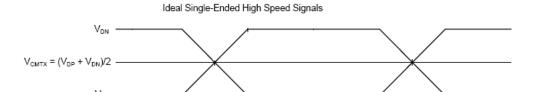


Figure 19 Ideal Single-Ended High Speed Signals

PASS Condition

The measured $\Delta V_{\text{CMTX}(1,0)}$ value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 11 Test Availability Condition for Test 1.4.8

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 1812 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm for Test ID 1812

NOTE

Use the Test ID# 1812 to remotely access the test.

- 1 This test requires the following prerequisite tests.
 - a HS Clock TX Static Common Mode Voltage (V_{CMTX}) (Test ID: 1811)

The actual V_{CMTX} for Differential-1 and Differential-0 measurements are performed and test results are stored.

2 Calculate the $V_{\mbox{\scriptsize CMTX}}$ mismatch using the following equation:

 V_{CMTX} Mismatch = ([V_{CMTX} for Differential-1] - [V_{CMTX} for Differential-0])/2

- 3 Report the measurement results.
 - a V_{CMTX} for Differential-1 and Differential-0
 - b V_{CMTX} Mismatch
- 4 Compare the measured $\Delta V_{\mbox{\scriptsize CMTX}}$ to the compliance test limit.

Test References

See Test 1.4.8 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz ($\Delta V_{CMTX(HF)}$) Method of Implementation

For this $\Delta V_{\text{CMTX}}(\text{HF})$ test, the common mode voltage, V_{CMTX} is obtained by using the following equation:

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

Ideally, the common mode voltage should be as shown in Figure 20. In reality, various types of distortion could take place, as shown in Figure 21.

Ideal Single-Ended High Speed Signals V_{DN} $V_{CMTX} = (V_{DP} + V_{DN})/2$

Figure 20 Ideal Single-Ended High Speed Signals

Possible ΔV_{CMTX} Distortions of the Single-ended HS Signals Static ΔV_{CMTX} (SE HS Signals)

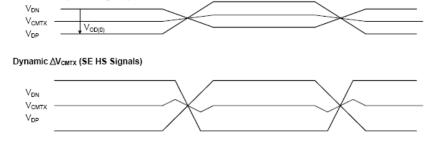


Figure 21 Possible Distortions of the ΔV_{CMTX} Single-Ended High Speed Signals

PASS Condition

The measured $\Delta V_{CMTX(HF)}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 12 Test Availability Condition for Test 1.4.10

| Associated Test ID | High-Speed Data Rate | ZID | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|---------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 1818 | Not Applicable | 100 ohm | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 1818

NOTE

Use the Test ID# 1818 to remotely access the test.

- 1 Trigger the oscilloscope to acquire Clkp and Clkn.
- 2 Construct common-mode waveform using the following equation:

ClkCommonMode = (Clkp+Clkn)/2

- 3 Applies the single pole high pass filter with 3dB bandwidth frequency at 450MHz to the common-mode waveform.
- 4 Measure the RMS voltage for the filtered waveform and record as $\Delta V_{CMTX(HF)}$.
- 5 Report the measurement results:
 - a ΔV_{CMTX(HF)} value
- 6 Compare the measured $\Delta V_{\text{CMTX(HF)}}$ value with the compliance test limit.

Test References

See Test 1.4.10 in CTS v1.0 and Section 8.1.1 Table 17 in the D-PHY Specification v1.0.

Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz ($\Delta V_{CMTX(LF)}$) Method of Implementation

For this $\Delta V_{CMTX(LF)}$ test, the common mode voltage V_{CMTX} is obtained by using the following equation:

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

Ideally, the common mode voltage should be as shown in Figure 22. In reality, various types of distortion could take place, as shown in Figure 23.

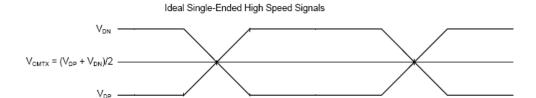


Figure 22 Ideal Single-Ended High Speed Signals

Static ΔV_{CMTX} (SE HS Signals) V_{CMTX} V_{CDP} Dynamic ΔV_{CMTX} (SE HS Signals)

Possible ΔV_{CMTX} Distortions of the Single-ended HS Signals



Figure 23 Possible Distortions of the ΔV_{CMTX} Single-Ended High Speed Signals

PASS Condition

The measured $\Delta V_{CMTX(LF)}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 13 Test Availability Condition for Test 1.4.9

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|----------------|----------------|----------------|----------------|----------------|-------------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 1819 | Not Applicable | 100 ohm | Not Applicable | Not Applicable |

4 MIPI D-PHY 1.0 High Speed Clock Transmitter (HS Clock TX) Electrical Tests

Measurement Algorithm using Test ID 1819

NOTE

Use the Test ID# 1819 to remotely access the test.

- 1 Trigger the oscilloscope to acquire Clkp and Clkn.
- 2 Construct common-mode waveform by using the following equation:

ClkCommonMode = (Clkp + Clkn)/2

- 3 A band pass filter with 3dB bandwidth frequency at 50MHz and 450MHz will be applied to the common-mode waveform.
- 4 Measure the min and max voltage for the filtered waveform.
- 5 Select the worst absolute value for the min and max voltage and record it as $\Delta V_{CMTX(LF)}$.
- 6 Report the measurement results:
 - $a \Delta V_{CMTX(LF)}$ value
- 7 Compare the measured $\Delta V_{CMTX(LF)}$ value with the compliance test limit.

Test References

See Test 1.4.9 in CTS v1.0 and Section 8.1.1 Table 17 in the D-PHY Specification v1.0.

Test 1.4.4 HS Clock TX Differential Voltage (V_{OD}) Method of Implementation

The Output Differential Voltage, V_{OD} is defined as the difference of voltages V_{DP} and V_{DN} at the Dp and Dn pins, respectively.

$$V_{OD} = V_{DP} - V_{DN}$$

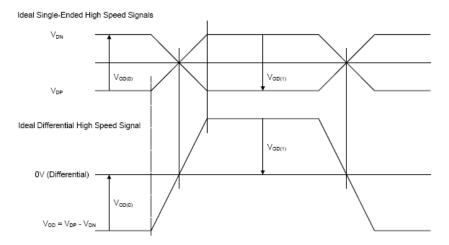


Figure 24 Ideal Single-Ended and Differential High Speed Signals

PASS Condition

The measured V_{OD} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 14 Test Availability Condition for Test 1.4.4

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 18131 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 18132 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test IDs 18131 and 18132

HS Clock TX Differential Voltage (V_{OD0} Pulse)

NOTE

Use the Test ID# 18131 to remotely access the test.

HS Clock TX Differential Voltage (V_{OD1} Pulse)

NOTE

Use the Test ID# 18132 to remotely access the test.

- 1 Trigger the oscilloscope to acquire Clkp and Clkn.
- 2 Construct the differential waveform using the following equation:

ClkDiff = Clkp-Clkn

- 3 Search the acquired waveform for the reference data pattern of "01" for V_{OD1} and "10" for V_{OD0} separately
- 4 Generate the average waveform that consists of the reference data patterns.
- Measure the mean value for the histogram window that falls between the centers of the '1' bits as the Mean V_{OD1} value using the histogram function. For V_{OD0} , set the histogram window to measure the centers of the '0' bits.
- 6 Report the measurement results
 - Mean $V_{\mbox{\scriptsize OD}}$ for Differential-1 and Differential-0
- 7 Compare the mean $V_{\mbox{\scriptsize OD}}$ value to the compliance test limits.

Test References

See Test 1.4.4 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.4.5 HS Clock TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation

The output differential voltage mismatch, ΔV_{OD} is defined as the difference of the absolute values of the differential output voltage in the Differential-1 state $V_{OD(1)}$ and the differential output voltage in the Differential-0 state $V_{OD(0)}$.

$$\Delta V_{\mathit{OD}} = \left| V_{\mathit{OD}(1)} \right| - \left| V_{\mathit{OD}(0)} \right|$$

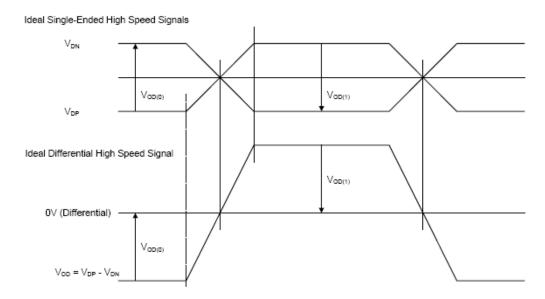


Figure 25 Ideal Single-Ended and Differential High Speed Signals

PASS Condition

The measured ΔV_{OD} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 15 Test Availability Condition for Test 1.4.5

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|-------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 18141 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | |

4 MIPI D-PHY 1.0 High Speed Clock Transmitter (HS Clock TX) Electrical Tests

Measurement Algorithm using Test ID 18141

HS Clock TX Differential Voltage Mismatch (Pulse)

NOTE

Use the Test ID# 18141 to remotely access the test.

- 1 This test requires the following prerequisite tests.
 - a HS Clock TX Differential Voltage (V_{OD0} Pulse) (Test ID: 18131)
 - b HS Clock TX Differential Voltage (V_{OD1} Pulse) (Test ID: 18132)

The actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.

- 2 Calculate the difference between $V_{\mbox{\scriptsize OD}}$ for Differential-1 and Differential-0.
- 3 Report the measurement results.
 - a V_{OD} for Differential-1 and Differential-0
- 4 Compare the measured ΔV_{OD} between Differential-1 and Differential-0 value with the compliance test limit.

Test References

See Test 1.4.5 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1. 4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation

The output voltages V_{DP} and V_{DN} at the Clkp and Clkn pins should not exceed the High-Speed output high voltage, V_{OLHS} is the High-Speed output, low voltage on Clkp and Clkn and is determined by V_{OD} and V_{CMTX} . The High-Speed V_{OUT} is bounded by the minimum value of V_{OLHS} and the maximum value of V_{OHHS} .

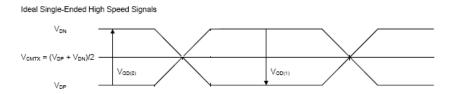


Figure 26 Ideal Single-Ended High Speed Signals

PASS Condition

The measured V_{OHHS} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 16 Test Availability Condition for Test 1.4.6

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 18151 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 18151

HS Clock TX Single Ended Output High Voltage (V_{OHHS} Pulse)

NOTE

Use the Test ID# 18151 to remotely access the test.

- 1 The acquired single-ended Clkp and Clkn waveform is searched for the reference data pattern of "01".
- 2 The averaged waveform that consists of all the reference data patterns found are generated for Clkp and Clkn.
- 3 Measures the mean value for the histogram window that fall between the centers of the '1' bits as the Mean V_{OHHS} value for each single-ended HS Clock signal and denote each value as V_{OHHS} (Clkp) and V_{OHHS} (Clkn), using the **Histogram** function.
- 4 Report the measurement results.
 - V_{OHHS} (Clkp)
 - · V_{OHHS} (Clkn)
 - Worst V_{OHHS} value
- 5 Compare the worst V_{OHHS} value to the compliance test limits.

4 MIPI D-PHY 1.0 High Speed Clock Transmitter (HS Clock TX) Electrical Tests

Test References

See Test 1.4.6 in CTS v1.0 and Section 8.1.1 Table 16 in the D-PHY Specification v1.0.

Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation

The rise time, t_R is defined as the transition time between 20% and 80% of the full HS signal swing. The driver must meet the t_R specifications for all allowable Z_{ID} .

PASS Condition

The measured t_R value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 17 Test Availability Condition for Test 1.4.11

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 18110 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 18110

NOTE

Use the Test ID# 18110 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (Ul_{inst})[Max] (Test ID: 911)
 UI value measurements for test signal are performed and test results are stored.
 - b HS Clock T_X Differential Voltage (V_{OD}) (Test ID: 18131, 18132) Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
- 2 Trigger the oscilloscope to acquire Clkp and Clkn.
- 3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: V_{OD1} (V_{OD} for Differential-1)

Base Level: V_{OD0} (V_{OD} for Differential-0)

- 5 Use a MATLAB script to identify and extract all "01" pattern locations found in the differential signal.
- 6 Measure the 20%-80% rise time at all rising edges of the "01" pattern that is identified.
- 7 Compare the value of the measured t_R (Mean) with the maximum and minimum compliance test limits.

Test References

See Test 1.4.11 in CTS v1.0 and Section 9.1.1 Table 17 in the D-PHY Specification v1.0.

Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation

The fall time, t_F is defined as the transition time between 80% and 20% of the full HS signal swing. The driver must meet the t_F specifications for all allowable Z_{ID} .

PASS Condition

The measured t_F value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 18 Test Availability Condition for Test 1.4.12

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 18111 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 18111

NOTE

Use the Test ID# 18111 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (Ul_{inst})[Max] (Test ID: 911)
 UI value measurements for test signal are performed and test results are stored.
 - b HS Clock T_X Differential Voltage (V_{OD}) (Test ID: 18131, 18132) Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
- 2 Trigger the oscilloscope to acquire Clkp and Clkn.
- 3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: V_{OD1} (V_{OD} for Differential-1)

Base Level: V_{OD0} (V_{OD} for Differential-0)

- 5 Use a MATLAB script to identify and extract all "10" pattern locations found in the differential signal.
- 6 Measure the 80%-20% fall time at all falling edges of the "10" pattern that is identified.
- 7 Compare the value of the measured t_F (Mean) with the maximum and minimum compliance test limits.

Test References

See Test 1.4.12 in CTS v1.0 and Section 9.1.1 Table 17 in the D-PHY Specification v1.0.

Test 1.4.17 HS Clock Instantaneous Method of Implementation

The HS Clock instantaneous test verifies that the HS clock transmitted by clock TX during HS data burst does not exceed the required maximum value.

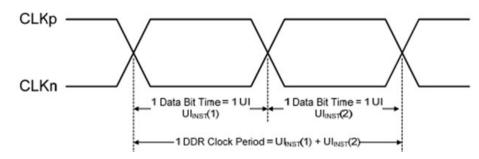


Figure 27 DDR Clock Definition

PASS Condition

The measured instantaneous UI must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 19 Test Availability Condition for Test 1.4.17

| Associated Test ID | High-Speed Data Rate | ZID | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|---------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 911 | Not Applicable | 100 ohm | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 914 | Not Applicable | 100 ohm | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 911

HS Clock Instantaneous (UI_{inst}) [Max]

NOTE

Use the Test ID# 911 to remotely access the test.

- 1 Capture the Clkp and Clkn waveform.
- 2 Construct the differential clock waveform using the following equation:

DiffClock = Clkp-Clkn

- 3 Measure the min, max and average Unit Interval of the differential clock waveform.
- 4 Store the min, max and average Unit Interval values.
- 5 Compare the max Unit Interval to the conformance limit.

4 MIPI D-PHY 1.0 High Speed Clock Transmitter (HS Clock TX) Electrical Tests

Measurement Algorithm using Test ID 914

HS Clock Instantaneous (UI_{inst}) [Min]

NOTE

Use the Test ID# 914 to remotely access the test.

- 1 Capture the Clkp and Clkn waveform.
- 2 Construct the differential clock waveform using the following equation:

DiffClock = Clkp-Clkn

- 3 Measure the min, max and average Unit Interval of the differential clock waveform.
- 4 Store the min, max and average Unit Interval values.
- 5 Compare the min Unit Interval to the conformance limit.

Test References

See Test 1.4.17 in CTS v1.0 and Section 9.1 Table 26 in the D-PHY Specification v1.0.

Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

5 MIPI D-PHY 1.0 Low Power Data Transmitter (LP Data TX) Electrical Tests

Probing for Low Power Transmitter Electrical Tests / 88

Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation / 90

Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{Ol}) Method of Implementation / 92

Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation / 94

Test 1.1.4 LP TX 15%-85% Fall Time Level (T_{FIP}) Method of Implementation / 95

Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock (T_{LP-PULSF-TX}) Method of Implementation / 97

Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock (T_{I P-PFR-TX}) Method of Implementation / 100

Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation / 102

This section provides the Methods of Implementation (MOIs) for the Low Power Data Transmitter (LP Data TX) Electrical tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.



Probing for Low Power Transmitter Electrical Tests

When performing the LP TX tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the LP TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Conformance Test Application for the exact number of probe connections.

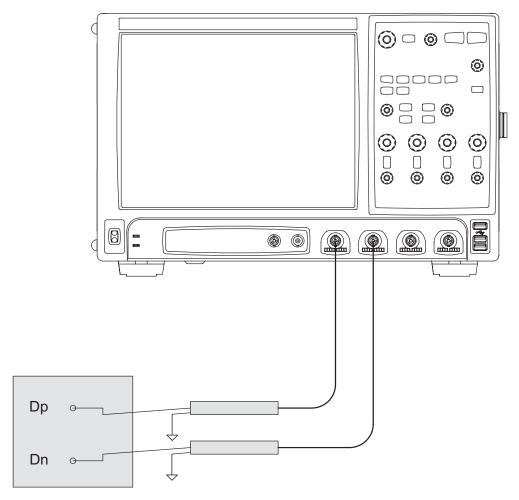


Figure 28 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 28 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, ZID (termination resistance), Cload, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

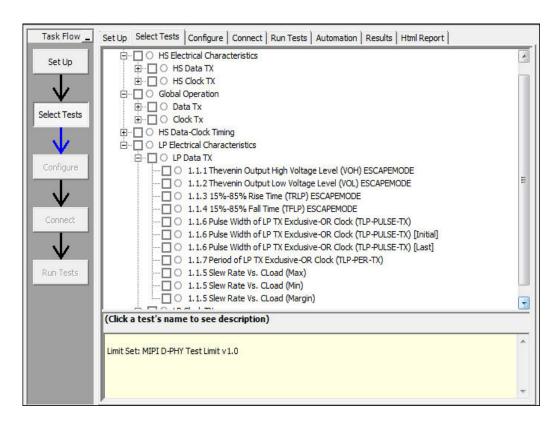


Figure 29 Selecting Low Power Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation

V_{OH} is the Thevenin output high-level voltage in the high-level state, when the pad pin is not loaded.

PASS Condition

The measured V_{OH} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 20 Test Availability Conditions for Test 1.1.1

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 821 | Not Applicable | Disabled | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable |
| 8211 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 821

LP TX Thevenin Output High Voltage Level (V_{OH})



Ensure that **Data LP EscapeMode** is disabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 821 to remotely access the test.

- 1 Trigger the Dp's LP rising edge.
- 2 Position the trigger point at the center of the screen and make sure that the stable Dp LP high level voltage region is visible on the screen.
- 3 Accumulate the data using the persistent display mode.
- 4 Enable the **Histogram** feature and measure the entire display region after the trigger location.
- 5 Take the mode value from the **Histogram** and use this value as V_{OH} for Dp.
- 6 Repeat steps 1 to 6 for Dn.
- 7 Report the measurement results.
 - a V_{OH} value for Dp channel
 - b V_{OH} value for Dn channel
- 8 Compare the measured worst value of V_{OH} with the compliance test limits.

Measurement Algorithm using Test ID 8211

LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8211 to remotely access the test.

- 1 Trigger on LP Data EscapeMode pattern on the data signal. Without the presence of LP Escape mode, the trigger is unable to capture any valid signal for data processing.
- 2 Locate and use the Mark-1 state pattern to determine the end of the EscapeMode sequence.
- 3 Enable the Histogram feature and measure the entire LP Data EscapeMode sequence.
- 4 Take the mode value from the Histogram and use this value as V_{OH} for Dp.
- 5 Repeat steps 1 to 5 for Dn.
- 6 Report the measurement results.
 - a V_{OH} value for Dp channel
 - b V_{OH} value for Dn channel
- 7 Compare the measured worst value of V_{OH} with the conformance test limits.

Test References

See Test 1.1.1 in CTS v1.0 and Section 8.12 Table 18 in the D-PHY Specification v1.0.

Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OI}) Method of Implementation

 V_{OL} is the Thevenin output low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low level state.

PASS Condition

The measured V_{OL} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 21 Test Availability Condition for Test 1.1.2

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 822 | Not Applicable | Disabled | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable |
| 8221 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 822

LP TX Thevenin Output Low Voltage Level (V_{OI})



Ensure that **Data LP EscapeMode** is disabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 822 to remotely access the test.

- 1 This test requires the following prerequisite test(s):
 - a HS Entry: DATA TX T_{HS-PREPARE} (Test ID: 557)
- 2 Trigger the Dp's LP falling edge.
- 3 Position the trigger point at the center of the screen and make sure that the stable Dp LP low level voltage region is visible on the screen.
- 4 Accumulate the data by using the persistent display mode.
- 5 Enable the **Histogram** feature and measure the entire display region after the trigger location.
- 6 Take the mode value from the Histogram and use this value as V_{OL} for Dp.
- 7 Repeat steps 1 to 7 for Dn.
- 8 Report the measurement results:
 - a V_{OI} value for Dp channel
 - b V_{OL} value for Dn channel
- 9 Compare the measured worst value of V_{OL} with the conformance test limits.

Measurement Algorithm using Test ID 8221

LP TX Thevenin Output Low Voltage Level (VOL) ESCAPEMODE

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8221 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
- 2 Trigger on LP Data EscapeMode pattern on the data signal. Without the presence of the LP Escape mode, the trigger is unable to capture any valid signal for data processing.
- 3 Locate and use the Mark -1 state pattern to determine the end of the EscapeMode sequence.
- 4 Enable the **Histogram** feature and measure the entire LP data EscapeMode sequence.
- 5 Take the mode value from the **Histogram** and use this value as V_{OL} for Dp.
- 6 Repeat steps 1 to 6 for Dn.
- 7 Report the measurement results:
 - a V_{OI} value for Dp channel
 - b V_{OL} value for Dn channel
- 8 Compare the measured worst value of $V_{\mbox{\scriptsize OL}}$ with the conformance test limits.

Test References

See Test 1.1.2 in CTS v1.0 and Section 8.1.2 Table 18 in the D-PHY Specification v1.0.

Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation

The T_{RLP} is defined as 15%-85% rise time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD} . The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{RLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 22 Test Availability Condition for Test 1.1.3

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|------------|----------------|------------|----------------|----------------|----------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 8241 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 8241

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8241 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
 - b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221)

 $\ensuremath{V_{OH}}$ and $\ensuremath{V_{OL}}$ values for Low Power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 All the rising edges in the EscapeMode sequence are processed in measuring the corresponding rise time.
- 4 The average 15%-85% rise time for Dp is recorded.
- 5 Repeat the steps for Dn.
- 6 Report the measurement results:
 - a T_{RLP} average value for Dp channel
 - b T_{RLP} average value for Dn channel
- 7 Compare the measured T_{RLP} worst value with the compliance test limit.

Test References

See Test 1.1.3 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.1.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation

The T_{FLP} is defined as 15%-85% fall time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD} . The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{FLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 23 Test Availability Condition for Test 1.1.4

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 825 | Not Applicable | Disabled | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable |
| 8251 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 825

LP TX 15%-85% Fall Time (T_{FLP})



Ensure that **Data LP EscapeMode** is disabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 825 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) (Test ID: 821)
 - b LP TX Thevenin Output Low Voltage Level (V_{OL}) (Test ID: 822)

Measure the V_{OH} and V_{OI} values for the low power signal and test results are stored.

- 2 All falling edges in LP are valid for this measurement.
- 3 Setup the trigger on LP falling edges.
- 4 Depending on the number of observation configuration, the oscilloscope is triggered accordingly.
- 5 The average 15%-85% fall time for Dp is recorded.
- 6 Repeat the same trigger steps for Dn.
- 7 Report the measurement results:
 - a T_{FLP} average value for Dp channel
 - b T_{FLP} average value for Dn channel
- 8 Compare the measured worst value of T_{FLP} with the compliance test limits.

Measurement Algorithm using Test ID 8251

LP TX 15%-85% Fall Time (T_{FLP}) ESCAPEMODE

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8251 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
 - b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221)

Measure the V_{OH} and V_{OI} values for the low power signal and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 All falling edges in the filtered EscapeMode sequence are processed in measuring the corresponding fall time.
- 4 The average 15%-85% fall time for Dp is recorded.
- 5 Repeat steps 1 to 5 for Dn.
- 6 Report the measurement results:
 - a T_{FLP} average value for Dp channel
 - b T_{FLP} average value for Dn channel
- 7 Compare the measured worst value of T_{FLP} with the compliance test limits.

Test References

See Test 1.1.4 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock ($T_{LP-PULSE-TX}$) Method of Implementation

 $T_{LP-PULSE-TX}$ is defined as the pulse width of the DUT Low-Power TX XOR clock. A graphical representation of the XOR operation that creates the LP clock is shown below. The D-PHY Standard actually separates the $T_{LP-PULSE-TX}$ specification into two parts:

- a The first LP XOR clock pulse after a Stop state, or the last LP XOR clock pulse before a Stop state must be wider than 40ns.
- b All other LP XOR clock pulses must be wider than 20ns.

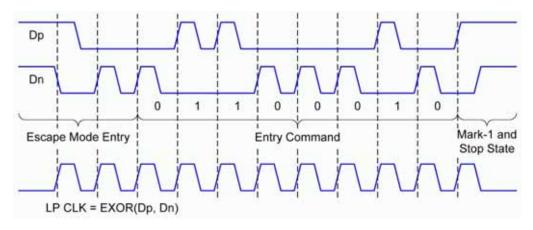


Figure 30 Graphical Representation of the XOR Operation

PASS Condition

The measured $T_{LP-PULSE-TX}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 24 Test Availability Condition for Test 1.1.6

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 827 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 8271 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 8272 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 1827 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 18271 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 18272 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |

Measurement Algorithm using Test IDs 827, 8271 and 8272

LP TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX})

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 827 to remotely access the test.

LP TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX}) [Initial]

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8271 to remotely access the test.

LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$) [Last]

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8272 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - *a* LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211). This is to trigger and capture an EscapeMode sequence data from the test signal.
- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Find all crossing points at the minimum trip level (500mV) and the maximum trip level (930mV) for Dp and Dn individually.
- 4 Find the initial pulse width, last pulse width and minimum width of all the other pulses at the specified minimum trip level and maximum trip level.
- 5 Find the rising-to-rising and falling-to-falling periods of the XOR clock at the mentioned minimum trip level and maximum trip level.
- 6 The worst case value for the pulse width found between the minimum trip level and maximum trip level will be used as the T_{LP-PULSE-TX} value.
- 7 Compare the measured minimum T_{LP-PULSE-TX} value with the compliance test limits.

Measurement Algorithm using Test IDs 1827, 18271 and 18272

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX})

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 1827 to remotely access the test.

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX}) [Initial]

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 18271 to remotely access the test.

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX}) [Last]

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 18272 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211) This is to trigger and capture an EscapeMode sequence data from the test signal.
- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Find all crossing points at the minimum trip level (500mV) and the maximum trip level (930mV) for Clkp and Clkn individually.
- 4 Find the initial pulse width, last pulse width and minimum width of all the other pulses at the specified minimum trip level and maximum trip level.
- Find the rising-to-rising and falling-to-falling periods of the XOR clock at the specified minimum trip level and maximum trip level.
- 6 The worst case value for the pulse width found between the minimum trip level and maximum trip level is used as the $T_{LP-PULSE-TX}$ value.
- 7 Compare the measured minimum T_{I P-PUI SF-TX} value with the compliance test limits.

Test References

See Test 1.1.6 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock (T_{LP-PFR-TX}) Method of Implementation

 $T_{LP\text{-}PER\text{-}TX}$ is defined as the period of the DUT Low-Power TX XOR clock. A graphical representation of the XOR operation that creates the LP clock is shown below. The D-PHY Standard separates the $T_{LP\text{-}PULSE\text{-}TX}$ specification into two parts:

- a The first LP XOR clock pulse after a Stop state, or the last LP XOR clock pulse before a Stop state must be wider than 40ns.
- b All other LP XOR clock pulses must be wider than 20ns.

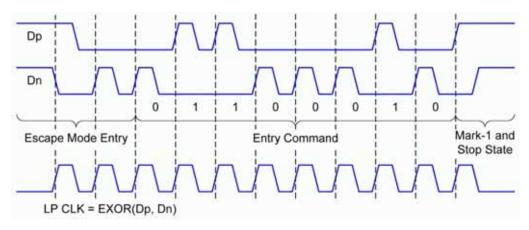


Figure 31 Graphical Representation of the XOR Operation

PASS Condition

The measured $T_{LP-PER-TX}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 25 Test Availability Condition for Test 1.1.7

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 828 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 1828 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |

Measurement Algorithm using Test ID 828

LP TX Period of LP TX Exclusive-OR Clock (T_{LP-PER-TX})

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 828 to remotely access the test.

- 1 This test requires the following prerequisite test(s).
 - a LP TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX}) (Test ID: 827)

The actual measurement algorithm of the $T_{LP-PER-TX}$ is performed in the mentioned prerequisite test

- 2 The minimum value for all the rising-to-rising and falling-to-falling periods of the XOR clock at the minimum trip level (500mV) and the maximum trip level (930mV) is used as the T_{LP-PER-TX} result.
- 3 Compare the measured minimum T_{LP-PER-TX} value to the compliance test limits.

Measurement Algorithm using Test ID 1828

LP Clock TX Period of LP TX Exclusive-OR Clock (T_{LP-PER-TX})

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 1828 to remotely access the test.

- 1 This test requires the following prerequisite test(s).
 - a LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$) (Test ID: 1827) The actual measurement algorithm of the $T_{LP-PER-TX}$ is performed in the mentioned prerequisite test
- 2 The minimum value for all the rising-to-rising and falling-to-falling periods of the XOR clock at the minimum trip level (500mV) and the maximum trip level (930mV) is used as the $T_{LP-PER-TX}$ result.
- 3 Compare the measured minimum T_{IP-PFR-TX} value with the compliance test limits.

Test References

See Test 1.1.7 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation

The slew rate δ V/ δ t_{SR} is the derivative of the LP transmitter output signal voltage over time. The intention of specifying a maximum slew rate value in the specification is to limit EMI (Electro Magnetic Interference).

The specification also states that the Slew Rate must be measured as an average across any 50mV segment of the output signal transition.

PASS Condition

The measured slew rate δ V/ δ t_{SR} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 26 Test Availability Condition for Test 1.1.5

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 829 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 8291 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 8292 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test IDs 829, 8291 and 8292

NOTE

Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test.

- To access the LP TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 829.
- To access the LP TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 8291.
- To access the LP TX Slew Rate Vs. C_{load} (Margin) test remotely, use the Test ID# 8292.
- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
 - b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221)

 $\ensuremath{V_{OH}}$ and $\ensuremath{V_{OL}}$ values for low power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Perform the slew rate measurement on the EscapeMode sequence for both Dp and Dn waveforms individually.

For falling edge,

- a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
- b. Perform the slew rate measurement across the 400mV 930mV region to determine the minimum slew rate result.

For rising edge,

- a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
- b. Perform the slew rate measurement across the 400mV 700mV region to determine the minimum slew rate result.

- c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV 930mV region.
- 4 Calculate the average value from all rising edges' maximum slew rate results. Calculate the average value from all falling edges' maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
- 5 Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
- 6 Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
- 7 The Slew Rate maximum, minimum and margin result values are stored.
- 8 Report the measurement results.
- 9 Compare the measured worst slew rate value with the conformance test limits.

Test References

See Test 1.1.5 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

MIPI D-PHY 1.0 Low Power Data Transmitter (LP Data TX) Electrical Tests

6 MIPI D-PHY 1.0 Low Power Clock Transmitter (LP Clock TX) Electrical Tests

Probing for Low Power Transmitter Electrical Tests / 106 Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation / 108 Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation / 110 Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation / 112 Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation / 114 Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation / 116

This section provides the Methods of Implementation (MOIs) for the Low Power Clock Transmitter (LP Clock TX) Electrical tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test App.



6

Probing for Low Power Transmitter Electrical Tests

When performing the LP TX tests, the MIPI D-PHY Test App will prompt you to make the proper connections. The connections for the LP TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test App for the exact number of probe connections.

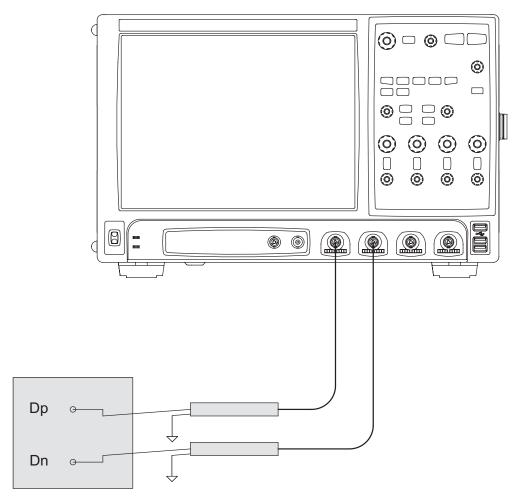


Figure 32 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test App. (The channels shown in Figure 32 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, ZID (termination resistance), Cload, Device ID and User Comments.

File View Tools Help Set Up Select Tests | Configure | Connect | Run Tests | Automation | Results | Html Report | □ □ O HS Electrical Characteristics Set Up ⊕ □ ○ HS Clock TX ☐ ☐ ○ Global Operation ⊕ □ ○ Data Tx Select Tests ⊕ □ ○ Clock Tx ⊞ ☐ ○ HS Data-Clock Timing Ė □ O LP Electrical Characteristics Ė...□ O LP Clock TX □ □ 1.2.1 Thevenin Output High Voltage Level (VOH) ESCAPEMODE ···· □ ○ 1.2.2 Thevenin Output Low Voltage Level (VOL) ESCAPEMODE ···□ ○ 1.2.3 15%-85% Rise Time (TRLP) ESCAPEMODE Connect - 0 1.2.4 15%-85% Fall Time (TFLP) ESCAPEMODE ○ 1.1.6 Pulse Width of LP TX Exclusive-OR Clock (TLP-PULSE-TX) 1.1.6 Pulse Width of LP TX Exclusive-OR Clock (TLP-PULSE-TX) [Initial] ... □ ○ 1.1.6 Pulse Width of LP TX Exclusive-OR Clock (TLP-PULSE-TX) [Last] □ ○ 1.1.7 Period of LP TX Exclusive-OR Clock (TLP-PER-TX) ... □ ○ 1.2.5 Slew Rate Vs. CLoad (Max) ... □ ○ 1.2.5 Slew Rate Vs. CLoad (Min) - 1.2.5 Slew Rate Vs. CLoad (Margin) Test Group: LP Clock TX

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

Figure 33 Selecting Low Power Transmitter Electrical Tests

Limit Set: MIPI D-PHY Test Limit v 1.0

Description: Low-Power Transmitter Electrical Characteristics

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

6

Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation

V_{OH} is the Thevenin output high-level voltage in the high-level state, when the pad pin is not loaded.

PASS Condition

The measured V_{OH} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 27 Test Availability Condition for Test 1.2.1

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 1821 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Disabled | Not Applicable |
| 18211 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 28211 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Enabled | Not Applicable |

Measurement Algorithm using Test ID 1821 and 28211

LP Clock TX Thevenin Output High Voltage Level (VOH)



Ensure that the Clock LP EscapeMode and Clock ULPS Mode are disabled on the Device Information section of the Set Up tab of the MIPI D-PHY Test application. Use the Test ID# 1821 to remotely access the test.

ULPS Clock TX Thevenin Output High Voltage Level (VOH) ULPSMODE



Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28211 to remotely access the test.

- 1 Trigger the Clkp's LP rising edge.
- 2 Position the trigger point at the center of the screen and make sure that the stable Clkp LP high level voltage region is visible on the screen.
- 3 Accumulate the data by using the persistent display mode.
- 4 Enable the **Histogram** feature and measure the entire display region after the trigger location.
- 5 Take the mode value from the Histogram and use this value as V_{OH} for Clkp.
- 6 Repeat steps 1 to 6 for Clkn.
- 7 Report the measurement results.
 - a V_{OH} value for Clkp channel
 - b V_{OH} value for Clkn channel
- 8 Compare the measured worst value of V_{OH} with the compliance test limits.

Measurement Algorithm using Test ID 18211

LP Clock TX Thevenin Output High Voltage Level (VOH) ESCAPEMODE

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18211 to remotely access the test.

- 1 Trigger on an EscapeMode pattern on the data signal. Without the presence of the LP Escape mode, the trigger is unable to capture any valid signal for data processing.
- 2 Locate and use the Mark-1 state pattern to determine the end of the EscapeMode sequence.
- 3 Enable the **Histogram** feature and measure the entire LP EscapeMode sequence.
- 4 Take the mode value from the **Histogram** and use this value as V_{OH} for Clkp.
- 5 Repeat steps 1 to 4 for Clkn.
- 6 Report the measurement results.
 - a V_{OH} value for Clkp channel
 - b V_{OH} value for Clkn channel
- 7 Compare the measured worst value of V_{OH} with the compliance test limits.

Test References

See Test 1.2.1 in CTS v1.0 and Section 8.1.2 Table 18 in the D-PHY Specification v1.0.

6

Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OI}) Method of Implementation

 V_{OL} is the Thevenin output low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low level state.

PASS Condition

The measured V_{OL} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 28 Test Availability Condition for Test 1.2.2

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 1822 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Disabled | Not Applicable |
| 18221 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 28221 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Enabled | Not Applicable |

Measurement Algorithm using Test ID 1822

LP Clock TX Thevenin Output Low Voltage Level (V_{OL})



Ensure that the Clock LP EscapeMode and Clock ULPS Mode are disabled on the Device Information section of the Set Up tab of the MIPI D-PHY Test application. Use the Test ID# 1822 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Entry: CLK TX T_{CLK-PREPARE} (Test ID: 552)
- 2 Trigger the Clkp's LP falling edge.
- 3 Position the trigger point at the center of the screen and make sure that the stable Clkp LP low level voltage region is visible on the screen.
- 4 Accumulate the data by using the persistent display mode.
- 5 Enable the **Histogram** feature and measure the entire display region after the trigger location.
- 6 Take the mode value from the **Histogram** and use this value as V_{OL} for Clkp.
- 7 Repeat steps 1 to 7 for Clkn.
- 8 Report the measurement results:
 - a V_{OL} value for Clkp channel
 - b V_{OI} value for Clkn channel
- 9 Compare the measured worst value of V_{OL} with the compliance test limits.

Measurement Algorithm using Test ID 18221

LP Clock TX Thevenin Output Low Voltage Level (VOL) ESCAPEMODE

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18221 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
- 2 Trigger on an EscapeMode pattern on the data signal. Without the presence of LP Escape mode, the trigger is unable to capture any valid signal for data processing.
- 3 Locate and use the Mark -1 state pattern to determine the end of the EscapeMode sequence.
- 4 Enable the **Histogram** feature and measure the entire LP EscapeMode sequence.
- 5 Take the mode value from the **Histogram** and use this value as V_{OL} for Clkp.
- 6 Repeat steps 1 to 6 for Clkn.
- 7 Report the measurement results:
 - a V_{OI} value for Clkp channel
 - b V_{OL} value for Clkn channel
- 8 Compare the measured worst value of V_{OL} with the compliance test limits.

Measurement Algorithm using Test ID 28221

ULPS Clock TX Thevenin Output Low Voltage Level (VOL) ULPSMODE

NOTE

Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28221 to remotely access the test.

- 1 This test requires the following prerequisite test(s):
 - a ULPS Clock TX Thevenin Output High Voltage Level (VOH) ULPSMODE (Test ID: 28211)
- 2 Trigger the Clkp's LP falling edge.
- 3 Position the trigger point at the center of the screen and make sure that the stable Clkp LP low level voltage region is visible on the screen.
- 4 Accumulate the data by using the persistent display mode.
- 5 Enable the **Histogram** feature and measure the entire display region after the trigger location.
- 6 Take the mode value from the Histogram and use this value as V_{OI} for Clkp.
- 7 Repeat steps 1 to 7 for Clkn.
- 8 Report the measurement results:
 - a V_{OI} value for Clkp channel
 - b V_{OI} value for Clkn channel
- 9 Compare the measured worst value of V_{OI} with the conformance test limits.

Test References

See Test 1.2.2 in CTS v1.0 and Section 8.1.2 Table 18 in the D-PHY Specification v1.0.

Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation

The T_{RLP} is defined as 15%-85% rise time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD} . The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{RLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 29 Test Availability Condition for Test 1.2.3

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 18241 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 28241 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Enabled | Not Applicable |

Measurement Algorithm using Test ID 18241

LP Clock TX 15%-85% Rise Time (T_{RLP}) ESCAPEMODE



Select Clock LP Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18241 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
 - b LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 18221)

 $\ensuremath{V_{OH}}$ and $\ensuremath{V_{OL}}$ values for Low Power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Perform rise time measurement on the EscapeMode sequence for both Clkp and Clkn waveforms individually.
- 4 The max, mean and min result values are stored.
- 5 Report the measurement results:
 - a T_{RLP} average value for Clkp channel
 - b T_{RLP} average value for Clkn channel
- 6 Compare the measured T_{RLP} worst value derived from the T_{RLP} average value for Clkp and Clkn to the compliance test limit.

Measurement Algorithm using Test ID 28241

ULPS Clock TX 15%-85% Rise Time (TRLP) ULPSMODE

NOTE

Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28241 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
 - b ULPS Clock TX Thevenin Output Low Voltage Level (V_{OI}) ULPSMODE (Test ID: 28221)

 $\rm V_{OH}$ and $\rm V_{OL}$ values for Low Power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Perform rise time measurement on the EscapeMode sequence for both Clkp and Clkn waveforms individually.
- 4 The max, mean and min result values are stored.
- 5 Report the measurement results:
 - a T_{RLP} average value for Clkp channel
 - b T_{RLP} average value for Clkn channel
- 6 Compare the measured T_{RLP} worst value derived from the T_{RLP} average value for Clkp and Clkn to the compliance test limit.

Test References

See Test 1.2.3 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation

The T_{FLP} is defined as 15%-85% fall time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD} . The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{FLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 30 Test Availability Condition for Test 1.2.4

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 1825 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Disabled | Not Applicable |
| 18251 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 28251 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Enabled | Not Applicable |

Measurement Algorithm using Test ID 1825

LP Clock TX 15%-85% Fall Time (T_{FLP})



Ensure that the Clock LP EscapeMode and Clock ULPS Mode are disabled on the Device Information section of the Set Up tab of the MIPI D-PHY Test application. Use the Test ID# 1825 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) (Test ID: 1821)
 - b LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) (Test ID: 1822)

 $\rm V_{OH}$ and $\rm V_{OL}$ values for Low Power signal measurements are performed and test results are stored.

- 2 Trigger is setup to trigger on LP falling edges.
- 3 The oscilloscope is triggered to capture the falling edges to be processed based on the "LP Observations" configuration in the **Configure** tab.
- 4 The average 15%-85% fall time for Clkp is recorded.
- 5 Repeat the same trigger steps for Clkn.
- 6 Report the measurement results:
 - a T_{FLP} average value for Clkp channel
 - b T_{FLP} average value for Clkn channel
- 7 Compare the measured worst value of T_{FLP} with the compliance test limits.

Measurement Algorithm using Test ID 18251

LP Clock TX 15%-85% Fall Time (T_{FLP}) ESCAPEMODE

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18251 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (VOH) ESCAPEMODE (Test ID: 18211)
 - b LP Clock TX Thevenin Output Low Voltage Level (VOI) ESCAPEMODE (Test ID: 18221)

 $\ensuremath{\text{V}_{\text{OH}}}$ and $\ensuremath{\text{V}_{\text{OL}}}$ values for low power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Perform fall time measurement on the EscapeMode sequence for both Clkp and Clkn waveforms individually.
- 4 The maximum, mean and minimum result values are stored.
- 5 Report the measurement results:
 - a T_{FLP} average value for Clkp channel
 - b T_{FLP} average value for Clkn channel
- 6 Compare the measured worst value of T_{FLP} derived from the average value of T_{FLP} for Clkp and Clkn to the compliance test limits.

Measurement Algorithm using Test ID 28251

ULPS Clock TX 15%-85% Fall Time (T_{FLP}) ULPSMODE

NOTE

Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28251 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
 - b ULPS Clock TX Thevenin Output Low Voltage Level (V_{OL}) ULPSMODE (Test ID: 28221)

 $\ensuremath{V_{OH}}$ and $\ensuremath{V_{OL}}$ values for low power signal measurements are performed and test results are stored.

- 2 Trigger is setup to trigger on LP falling edges.
- 3 The oscilloscope is triggered to capture the falling edges to be processed based on the "LP Observations" configuration in the Configure tab.
- 4 The average 15%-85% fall time for Clkp is recorded.
- 5 Repeat the same trigger steps for Clkn.
- 6 Report the measurement results:
 - a T_{FLP} average value for Clkp channel
 - b T_{FLP} average value for Clkn channel
- 7 Compare the measured worst value of T_{FLP} to the compliance test limits.

Test References

| 6 | MIPI D-PHY 1 | 1.0 Low Power | Clock | Transmitter | (LP | Clock 7 | ΓX) Electrical | Tests |
|---|--------------|---------------|-------|-------------|-----|---------|----------------|-------|
| | | | | | | | | |

See Test 1.2.4 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation

The slew rate δ V/ δ t_{SR} is the derivative of the LP transmitter output signal voltage over time. The intention of specifying a maximum slew rate value in the specification is to limit EMI (Electro Magnetic Interference).

The specification also states that the Slew Rate must be measured as an average across any 50mV segment of the output signal transition.

PASS Condition

The measured slew rate δ V/ δ t_{SR} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 31 Test Availability Condition for Test 1.2.5

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 1829 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 18291 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 18292 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 2829 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled | Not Applicable |
| 28291 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled | Not Applicable |
| 28292 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled | Not Applicable |

Measurement Algorithm using Test ID 1829, 18291 and 18292

LP Clock TX Slew Rate Vs. C_{Load} (Max) /

LP Clock TX Slew Rate Vs. C_{Load} (Min) /

LP Clock TX Slew Rate Vs. C_{Load} (Margin)

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test.

- To access the LP Clk TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 1829.
- To access the LP CIk TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 18291.
- To access the LP Clk TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 18292.
- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
 - b LP Clock TX Thevenin Output Low Voltage Level (VOL) ESCAPEMODE (Test ID: 18221)

 V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Perform the slew rate measurement on the EscapeMode sequence for both Clkp and Clkn waveforms individually.

For falling edge,

- a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
- b. Perform the slew rate measurement across the 400mV 930mV region to determine the minimum slew rate result.

For rising edge,

- a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
- b. Perform the slew rate measurement across the 400mV 700mV region to determine the minimum slew rate result.
- c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV 930mV region.
- 4 Calculate the average value from all rising edges' maximum slew rate results. Calculate the average value from all falling edges' maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
- 5 Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
- 6 Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
- 7 The Slew Rate maximum, minimum and margin result values are stored.
- 8 Report the measurement results.
- 9 Compare the measured worst slew rate value for Clkp and Clkn to the compliance test limits.

ULPS Clock TX Slew Rate Vs. C_{I pad} (Max) ULPSMODE/

ULPS Clock TX Slew Rate Vs. C_{Load} (Min) ULPSMODE/

ULPS Clock TX Slew Rate Vs. C_{I oad} (Margin) ULPSMODE

Measurement Algorithm using Test ID 2829, 28291 and 28292

NOTE

Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test.

- To access the ULPS Clk TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 2829.
- To access the ULPS Clk TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 28291.
- To access the ULPS CIk TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 28292.
- 1 This test requires the following prerequisite tests:
 - a ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
 - b ULPS Clock TX Thevenin Output Low Voltage Level (V_{OL}) ULPSMODE (Test ID: 28221)

 $\ensuremath{V_{OH}}$ and $\ensuremath{V_{OL}}$ values for low power signal measurements are performed and test results are stored.

- 2 The oscilloscope is triggered to capture rising and falling edges to be processed based on the "Number of ULPS Slew Edge" configuration in the **Configure** tab.
- 3 Perform the slew rate measurement on the mentioned triggered data for both Clkp and Clkn waveforms individually.

For falling edge,

- a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
- b. Perform the slew rate measurement across the 400mV 930mV region to determine the minimum slew rate result.

For rising edge,

- a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
- b. Perform the slew rate measurement across the 400mV 700mV region to determine the minimum slew rate result.
- c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV 930mV region.
- 4 Calculate the average value from all rising edges' maximum slew rate results. Calculate the average value from all falling edges' maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
- 5 Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
- 6 Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
- 7 The Slew Rate maximum, minimum and margin result values are stored.
- 8 Report the measurement results.
- 9 Compare the measured worst slew rate value for Clkp and Clkn to the compliance test limits.

Test References

See Test 1.2.5 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

MIPI D-PHY 1.0 Low Power Clock Transmitter (LP Clock TX) Electrical Tests

| Part II Global Operation |
|-----------------------------|
| |



Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

7 MIPI D-PHY 1.0 Data Transmitter (Data TX) Global Operation Tests

Probing for Data TX Global Operation Tests / 122

Test 1.3.1 HS Entry: Data T_{I PX} Method of Implementation / 124

Test 1.3.2 HS Entry: Data TX $T_{HS-PREPARE}$ Method of Implementation $\,/\,$ 125

Test 1.3.3 HS Entry: Data TX $T_{HS-PREPARE} + T_{HS-ZERO}$ Method of Implementation / 127

Test 1.3.13 HS Exit: Data TX $T_{HS-TRAII}$ Method of Implementation / 129

Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation / 131

Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation / 133 Test 1.3.16 HS Exit: Data TX $T_{HS-EXIT}$ Method of Implementation / 135

This section provides the Methods of Implementation (MOIs) for the Data Transmitter (Data TX) Global Operation tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.



Probing for Data TX Global Operation Tests

When performing the Data TX tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the Data TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Conformance Test Application for the exact number of probe connections.

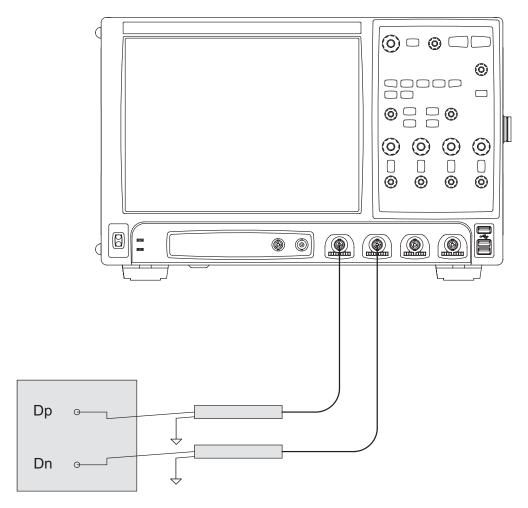


Figure 34 Probing for Data TX Global Operation Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 34 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, ZID (termination resistance), CLoad, Device ID and User Comments.

Task Flow _ Set Up Select Tests | Configure | Connect | Run Tests | Automation | Results | Html Report | □ □ O MIPI D-PHY Tests Set Up ☐ ☐ ○ HS Electrical Characteristics HS Data TX ⊕ □ ○ HS Clock TX ☐ Global Operation Select Tests □ O Data Tx □ ○ 1.3.1 HS Entry: DATA TLPX □ ○ 1.3.2 HS Entry: DATA TX THS-PREPARE ... □ ○ 1.3.3 HS Entry: DATA TX THS-PREPARE+THS-ZERO Configure --- O 1.3.13 HS Exit: DATA TX THS-TRAIL --- 1.3.14 HS Exit: DATA TX TREOT -- O 1.3.15 HS Exit: DATA TX TEOT 1.3.16 HS Exit: DATA TX THS-EXIT Connect ⊕ □ ○ Clock Tx □ □ ○ Informative Test --- □ ○ HS Data Eye Height (Informative) Run Tests ☐ ○ HS Data Eye Width (Informative) □ □ O LP Electrical Characteristics ⊞ □ ○ LP Data TX ⊞ □ O LP Clock TX Test Group: Data Tx Description: Data Transmission Timing Characteristics Limit Set: MIPI D-PHY Test Limit v1.0

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

Figure 35 Selecting Data TX Global Operation Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.3.1 HS Entry: Data T_{LPX} Method of Implementation

This test verifies that the last LP-01's duration prior to HS Data burst is within the specification.

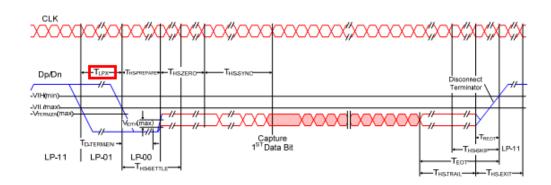


Figure 36 High-Speed Data Transmission in Bursts

PASS Condition

The T_{LPX} must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 32 Test Availability Condition for Test 1.3.1

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|------------|-------------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 511 | Not Applicable | 100 ohm | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 511

NOTE

Use the Test ID# 511 to remotely access the test.

- 1 Trigger on the Dp's falling edge in LP-01 at the SoT.
- 2 Denote the time when the Dp falling edge first crosses V_{II} (max), as T1.
- 3 Denote the time when the first Dn falling edge after T1 crosses VIL(max), as T2.
- 4 Calculate T_{LPX} by using the following equation:

$$T_{IPX} = T2-T1$$

- Report the T_{LPX} measurement.
- 6 Compare the T_{LPX} to the conformance test limit.

Test References

See Test 1.3.1 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.3.2 HS Entry: Data TX T_{HS-PRFPARF} Method of Implementation

This test verifies that the last LP-00's duration prior to HS Data burst is within the specification.

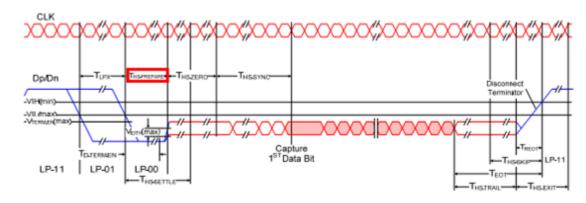


Figure 37 High-Speed Data Transmission in Bursts

PASS Condition

The T_{HS-PREPARE} must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 33 Test Availability Condition for Test 1.3.2

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 557 | Not Applicable | 100 ohm | Disabled | Not Applicable |

Measurement Algorithm using Test ID 557

NOTE

Use the Test ID# 557 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - HS Clock Instantaneous: UI_{inst} [Max] (Test ID: 911)
 - The minimum, maximum and average Unit Interval of the differential clock waveform is measured and test results are stored.
- 2 Trigger on the Dp's falling edge in LP-01 at the SoT.
- 3 Denote the time when the first Dn falling edge after LP-01 crosses V_{II} (max), as T2.
- 4 Construct the differential waveform of Dp and Dn by using the following formula:

DataDiff = Dp-Dn

5 Find and denote the first falling edge of the differential waveform that crosses - V_{IDTH}(max) as T3. T3 must be greater than T2. 6 Calculate T_{HS-PREPARE} by using the following equation:

$$T_{HS-PREPARE} = T3-T2$$

- 7 Report the T_{HS-PREPARE}.measured.
- 8 Compare the $T_{\mbox{\scriptsize HS-PREPARE}}$ value with the conformance test limit.

Test References

See Test 1.3.2 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.3.3 HS Entry: Data TX T_{HS-PREPARE} + T_{HS-ZERO} Method of Implementation

This test verifies that the duration in time HS TX driving the line in HS0 prior to HS Sync sequence is within the specification. HS Sync-Sequence: 0001110101.

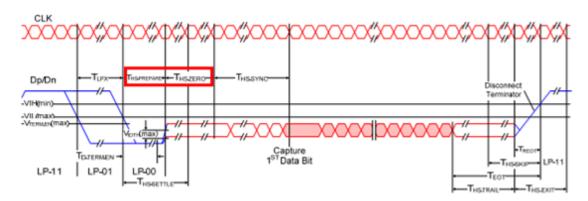


Figure 38 High-Speed Data Transmission in Bursts

PASS Condition

The average $T_{\text{HS-PREPARE}} + T_{\text{HS-ZERO}}$ must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 34 Test Availability Condition for Test 1.3.3

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|------------|-------------------|----------------|----------------|-------------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 558 | Not Applicable | 100 ohm | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 558

NOTE

Use the Test ID# 558 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous: UI_{inst} [Max] (Test ID: 911)

The minimum, maximum and average Unit Interval of the differential clock waveform is measured and test results are stored.

- 2 Trigger on Dp's falling edge in LP-01 at the SoT.
- 3 Denote the time when the first Dn falling edge after Dp falling crosses VIL(max), as T2.
- 4 Construct the differential waveform of Dp and Dn by using the following formula:

DataDiff = Dp-Dn

- 5 Find and denote the first rising edge of the differential waveform that crosses -V_{IDTH}(max) as T4. where, T4 is where the bit pattern "000" occurs in HS Sync sequence ends.
- 6~ Find and denote the next rising edge that crosses $\rm V_{\rm IDTH}(max)$ after T4 as T5.
 - where, T5 is where the bit pattern "111" occurs in HS Sync sequence ends.
- 7 The bit pattern "000" of HS Sync sequence should be the same length in time as the bit pattern "111", thus the time duration for the bit pattern "000" should be T5 T4.
- 8 Calculate T_{HS-PREPARE} + T_{HS-ZERO} by using the following equation:

$$T_{HS-PREPARE} + T_{HS-ZERO} = T4-(T5-T4)-T2$$

- 9 Report the measured T_{HS-PREPARE} + T_{HS-ZERO}.
- 10 Compare the average T_{HS-PREPARE} + T_{HS-ZERO} with the conformance test limit.

Test References

See Test 1.3.3 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.3.13 HS Exit: Data TX T_{HS-TRAIL} Method of Implementation

This test verifies that the duration in time of HS TX driving the line in inverted final differential state following the last payload data bit of a HS Data burst is equal or greater than the minimum required value.

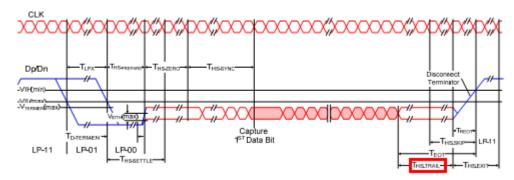


Figure 39 High-Speed Data Transmission in Bursts

PASS Condition

The average T_{HS-TRAIL} must be equal or greater than the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 35 Test Availability Condition for Test 1.3.13

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 546 | Not Applicable | 100 ohm | Disabled | Not Applicable |

Measurement Algorithm using Test ID 546

NOTE

Use the Test ID# 546 to remotely access the test.

- 1 Trigger on Dp's falling edge in LP-01 at the SoT.
- 2 Go to EoT of the same burst.
- 3 Find the time where the last payload data bit's differential edge crosses +/-V_{IDTH}(max), denoted as T6.
- 4 Find the time when the last TX differential edge crosses +/-V_{IDTH}(max), and denote it as T7. Note that T7 must be greater than T6.
- 5 Use the following calculation:

$$T_{HS-TRAII} = T7-T6$$

- 6 Report the measured T_{HS-TRAIL}.
- 7 Compare the measured T_{HS-TRAIL} with the conformance test limits.

Test References

See Test 1.3.13 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

7

Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation

The rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.

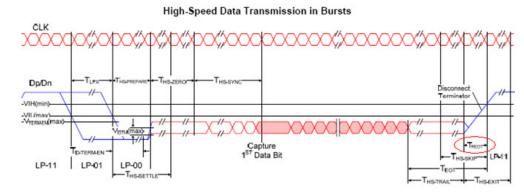


Figure 40 High-Speed Data Transmission in Bursts

PASS Condition

The measured T_{REOT} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 36 Test Availability Condition for Test 1.3.14

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 549 | Not Applicable | 100 ohm | Disabled | Not Applicable |

Measurement Algorithm using Test ID 549

NOTE

Use the Test ID# 549 to remotely access the test.

- 1 Trigger on Dp's falling edge in LP-01 at the SoT.
- 2 Go to EoT.
- 3 Find the time where the last data TX differential edge crosses +/-V_{IDTH}(max), denoted as T1.
- Find the time where Dp rising edge crosses V_{IH}(min)(880mV), and denote it as T2. Note that T2 must be greater than T1.
- 5 Use the following calculation:

$$T_{RFOT} = T2-T1$$

- 6 Report the measured T_{RFOT}.
- 7 Compare the measured T_{REOT} with the conformance test limits.

Test References

See Test 1.3.14 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.3.15 HS Exit: Data TX T_{FOT} Method of Implementation

This test verifies that the combined duration of the $T_{HS-TRAIL}$ and T_{REOT} intervals of the DUT Data TX is less than the maximum required value.

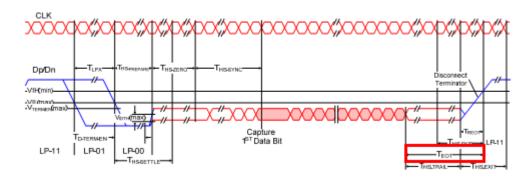


Figure 41 High-Speed Data Transmission in Bursts

PASS Condition

The average T_{EOT} value must be equal or less than the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 37 Test Availability Condition for Test 1.3.15

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|------------|-------------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 547 | Not Applicable | 100 ohm | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 547

NOTE

Use the Test ID# 547 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - HS Clock Instantaneous: Ul_{inst} [Max] (Test ID: 911)
 - The minimum, maximum and average Unit Interval of the differential clock waveform is measured and test results are stored.
- 2 Trigger on Dp's falling edge in LP-01 at the SoT.
- 3 Go to EoT.
- 4 Find the time when the last data differential edge crosses +/-V_{IDTH}(max), and denote it as T6.
- 5 Find the time where Dp rising edge crosses VIH(min)(880mV), and denote it as T8. Note that T8 must greater than T6.
- 6 Use the following calculation:

$$T_{EOT} = T8-T6$$

- 7 Report the measured T_{EOT} .
- 8 Compare the measured $T_{\mbox{EOT}}$ with the conformance test limits.

Test References

See Test 1.3.15 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

7

Test 1.3.16 HS Exit: Data TX T_{HS-EXIT} Method of Implementation

This test verifies that the Data TX remains in LP-11 state after exiting HS mode is greater than the minimum required value.

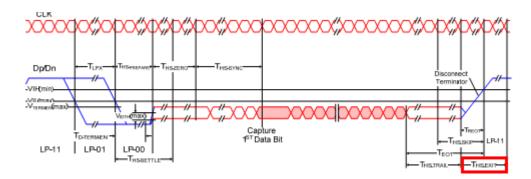


Figure 42 High-Speed Data Transmission in Bursts

PASS Condition

The average T_{HS-EXIT} value must be equal or greater than the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 38 Test Availability Condition for Test 1.3.16

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 548 | Not Applicable | 100 ohm | Disabled | Not Applicable |

Measurement Algorithm using Test ID 548

NOTE

Use the Test ID# 548 to remotely access the test.

- 1 Trigger on the Dp's falling edge in LP-01 at the SoT.
- 2 Go to EoT of the same burst.
- 3 Find the time when the last Data TX differential edge crosses +/-V_{IDTH}(max), and denote it as T7.
- Find the time after T7 when Dp falling edge starts to cross VIL(min), and denote it as T9.
- 5 Use the following calculation:

$$T_{HS-FXIT} = T9-T7$$

- 6 Report the measured $T_{HS-EXIT}$.
- 7 Compare the measured $T_{\mbox{\scriptsize HS-EXIT}}$ with the conformance test limits.

Test References

See Test 1.3.16 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

MIPI D-PHY 1.0 Data Transmitter (Data TX) Global Operation Tests

Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

8 MIPI D-PHY 1.0 Clock Transmitter (Clock TX) Global Operation Tests

Probing for Clock TX Global Operation Tests / 138

Test 1.4.1 HS Entry: CLK TX T_{I PX} Method of Implementation / 140

Test 1.4.2 HS Entry: CLK TX T_{CLK-PREPARE} Method of Implementation / 142

Test 1.4.3 HS Entry: CLK TX $T_{CLK-PREPARE} + T_{CLK-ZERO}$ Method of Implementation / 144

Test 1.5.1 HS Entry: CLK TX $T_{CLK-PRF}$ Method of Implementation / 146

Test 1.5.2 HS Exit: CLK TX $T_{CLK-POST}$ Method of Implementation / 148

Test 1.4.13 HS Exit: CLK TX $T_{CLK-TRAIL}$ Method of Implementation / 150

Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{RFOT}) Method of Implementation / 152

Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation / 154 Test 1.4.16 HS Exit: CLK TX $T_{HS-EXIT}$ Method of Implementation / 156

This section provides the Methods of Implementation (MOIs) for the Clock Transmitter (Clock TX) Global Operation tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.



Probing for Clock TX Global Operation Tests

When performing the Clock TX tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the Clock TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Conformance Test Application for the exact number of probe connections.

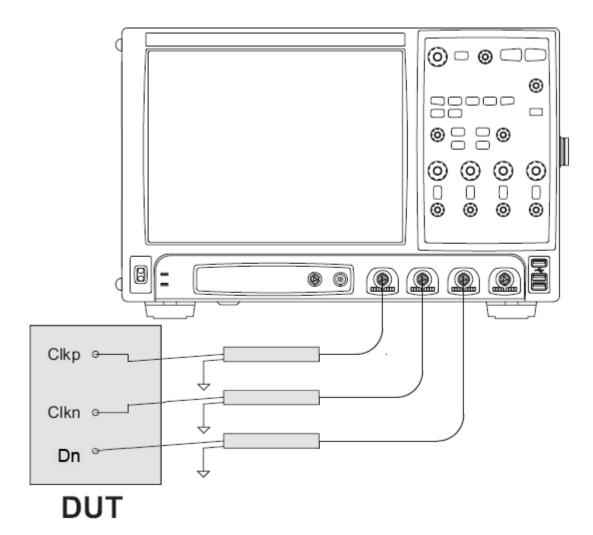


Figure 43 Probing for Clock TX Global Operation Tests

You can identify the channels used for each signal in the Configuration tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 43 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, ZID (termination resistance), Cload, Device ID and User Comments.
- 4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

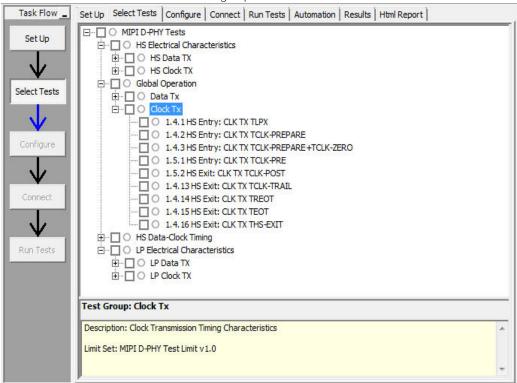


Figure 44 Selecting Clock TX Global Operation Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.1 HS Entry: CLK TX T_{I PX} Method of Implementation

This test verifies that the duration in time for the Clock TX to remain in LP-01 (Stop) state before entering the HS mode is greater than the minimum required value.

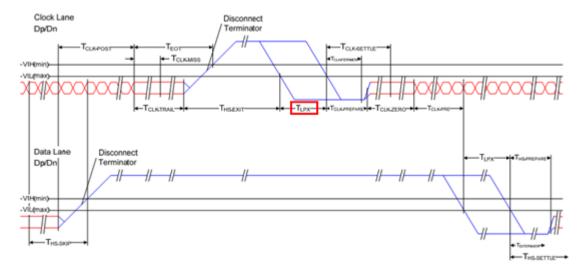


Figure 45 Switching the Clock Lane between Clock Transmission and Low-Power Mode

PASS Condition

The T_{LPX} must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 39 Test Availability Condition for Test 1.4.1

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|-------------------|------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 5510 | Not Applicable | 100 ohm | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 5510

NOTE

Use the Test ID# 5510 to remotely access the test.

- 1 Trigger on the Clkn's falling edge after LP-01.
- 2 Find the time of Clkp falling edge before the trigger position that crosses V_{IL}(max) and denote it as T1.
- 3 Find the time of Clkn falling edge after the T1 that crosses V_{II} (max) and denote it as T2
- 4 Construct T_{LPX} using the following equation:

$$T_{LPX} = T2-T1$$

- $\label{eq:thmoson} 5 \quad \text{Report the T_{LPX} measurement.}$
- 6 Compare the measured T_{LPX} to the conformance limit.

Test References

See Test 1.4.1 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.4.2 HS Entry: CLK TX T_{CLK-PREPARE} Method of Implementation

This test verifies that the duration in time for the Clock TX to remain in LP-00 state before entering HS mode is within the required value.

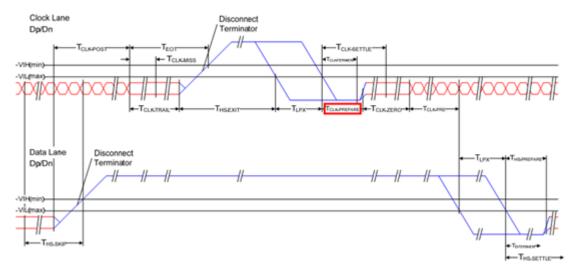


Figure 46 Switching the Clock Lane between Clock Transmission and Low-Power Mode

PASS Condition

The $T_{\text{CLK-PREPARE}}$ shall be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 40 Test Availability Condition for Test 1.4.2

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|----------------|------------|----------------|----------------|-------------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 552 | Not Applicable | 100 ohm | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 552

NOTE

Use the Test ID# 552 to remotely access the test.

- 1 Trigger on the Clkn falling edge after LP-01.
- 2 Find the time of Clkp falling edge before the trigger position that crosses V_{IL}(max). Mark the time as T1.
- 3 Find the time of Clkn falling edge after the T1 that crosses V_{II} (max) and denote it as T2.
- 4 Construct the differential clock waveform using the following equation:

DiffClock = Clkp-Clkn

- 5 Find the time when DiffClock's falling edges first crosses -V_{IDTH}(MAX) after T2, and denote it as T3
- 6 Calculate T_{CLK-PREPARE} using the following equation:

$$T_{CLK-PREPARE} = T3-T2$$

- 7 Report the T_{CLK-PREPARE}.measurement.
- 8 Compare $T_{\text{CLK-PREPARE}}$ with the conformance test limit.

Test References

See Test 1.4.2 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.4.3 HS Entry: CLK TX T_{CLK-PREPARE+}T_{CLK-ZERO} Method of Implementation

This test verifies that the duration in time for Clock TX to remain in LP-00 and HS0 state before starting clock transmission is greater than the minimum required value.

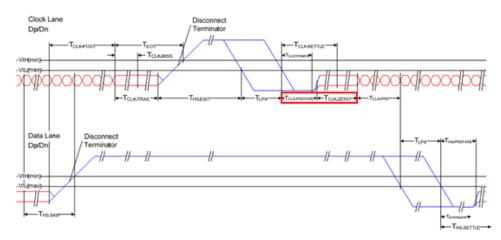


Figure 47 Switching the Clock Lane between Clock Transmission and Low Power Mode

PASS Condition

The T_{CLK-PREPARE}+T_{CLK-ZERO} must be within the conformance limit as specified in the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 41 Test Availability Condition for Test 1.4.3

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|-------------------|------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 554 | Not Applicable | 100 ohm | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 554

NOTE

Use the Test ID# 554 to remotely access the test.

- 1 Trigger on the Clkn falling edge after LP-01.
- 2 Find the time of Clkp falling edge before the trigger position that crosses V_{IL} (max) and denote it as T1.
- 3 Find the time of Clkn falling edge after the T1 that crosses V_{IL} (max) and denote it as T2.
- 4 Construct the differential clock waveform by using the following equation:

DiffClock = Clkp-Clkn

5 Find the time when the DiffClock's falling edges first crosses -V_{IDTH}(max) after T2 and denote it as T3.

- 6 Find the time when the DiffClock's rising edges first crosses -V_{IDTH}(max) after T3 and denote it as T4
- 7 Calculate $T_{CLK-PREPARE} + T_{CLK-ZERO}$ by using the following equation:

$$T_{CLK-PREPARE} + T_{CLK-ZERO} = T4-T2$$

- 8 Report the T_{CLK-PREPARE}.+T_{CLK-ZERO} measurement.
- 9 Compare the $T_{CLK\text{-PREPARE}} + T_{CLK\text{-ZERO}}$ value with the conformance test limit.

Test References

See Test 1.4.3 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.5.1 HS Entry: CLK TX T_{CLK-PRF} Method of Implementation

This test verifies that the duration in time for the Clock TX start to transmit clock until the Data TX is switch from LP11 (Stop) to LP01 state. The duration has to be greater than the required minimum value.

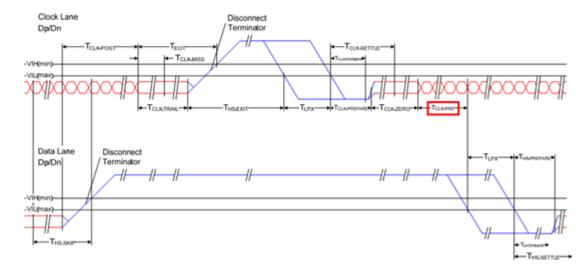


Figure 48 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

PASS Condition

The $T_{CLK-PRE}$ value must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 42 Test Availability Condition for Test 1.5.1

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|----------------|------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 551 | Not Applicable | 100 ohm | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 551

NOTE

Use the Test ID# 551 to remotely access the test.

- 1 This test requires the following prerequisite test:
 - a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)
 - Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.
- 2 Trigger on the Clkn's falling edge after LP-01.

3 Construct the differential clock waveform using the following equation:

- 4 Find the time when the DiffClock's rising edge first crosses -V_{IDTH}(max) after LP-00. Denote the time as T1.
- 5 Find the time when the Dp's LP falling edge from the same burst crosses V_{IL} (max). Mark the first edges found next to T1 as T2.
- 6 Calculate T_{CLK-PRE} using the following equation:

$$T_{CLK-PRE} = T2-T1$$

- 7 Report the T_{CLK-PRE} measurement.
- 8 Compare the $T_{\text{CLK-PRE}}$ value with the conformance test limit.

Test References

See Test 1.5.1 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.5.2 HS Exit: CLK TX T_{CLK-POST} Method of Implementation

This test verifies that the DUT Clock Lane HS transmitter continues to transmit clock signaling for the minimum required duration after the last Data Lane switches to LP mode.

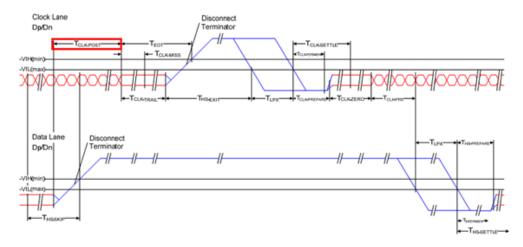


Figure 49 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

PASS Condition

The average T_{CLK-POST} must be equal or greater than the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 43 Test Availability Condition for Test 1.5.2

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|----------------|------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 555 | Not Applicable | 100 ohm | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 555

NOTE

Use the Test ID# 555 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.

- 2 Trigger on the Clkn's falling edge after LP-01.
- 3 Back trace to the previous EoT.

4 Construct the differential clock waveform using the following equation:

- 5 Find the time when the DiffClock crosses +/-V_{IDTH}(max) after last payload clock bit. Denote this time as T2.
- 6 Find the time when the last DiffData differential edge crosses +/-V_{IDTH}(max). Denote the time as T1. Note that T2 must be greater than T1.
- 7 Calculate T_{CLK-POST} using the following equation:

$$T_{CLK-POST} = T2-T1$$

- 8 Report the $T_{CLK-POST}$ measured.
- 9 Compare the $T_{\text{CLK-POST}}$ value with the conformance test limit.

Test References

See Test 1.5.2 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.4.13 HS Exit: CLK TX T_{CLK-TRAII} Method of Implementation

This test verifies that the duration for Clock TX to drive the final HS-0 differential state following the last payload clock bit is equal or greater than the minimum required value.

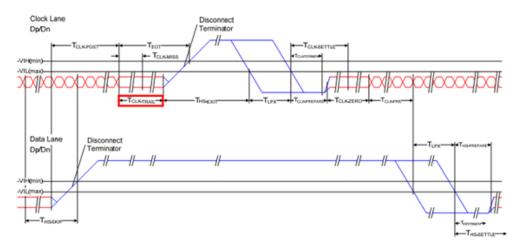


Figure 50 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

PASS Condition

The average $T_{CLK-TRAIL}$ must be equal or greater than the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 44 Test Availability Condition for Test 1.4.13

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|----------------|------------|----------------|----------------|-------------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 543 | Not Applicable | 100 ohm | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 543

NOTE

Use the Test ID# 543 to remotely access the test.

- 1 Trigger on the Clkn's falling edge after LP-01.
- 2 Back trace to the previous EoT.
- 3 Construct the differential clock waveform by using the following equation:

DiffClock = Clkp-Clkn

4 Find the time when the DiffClock crosses +/-V_{IDTH}(max) after last payload clock bit and denote it as T1.

- 5 Find the time when the DiffClock crosses +/-V_{IDTH}(max) before switching to LP and denote the time as T2. Note that T2 must be greater than T1.
- 6 Calculate $T_{\text{CLK-TRAIL}}$ by using the following equation:

$$T_{CLK-TRAIL} = T2-T1$$

- 7 Report the T_{CLK-TRAIL} measured.
- 8 Compare the $T_{\mbox{CLK-TRAIL}}$ value with the conformance test limit.

Test References

See Test 1.4.13 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation

This rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.

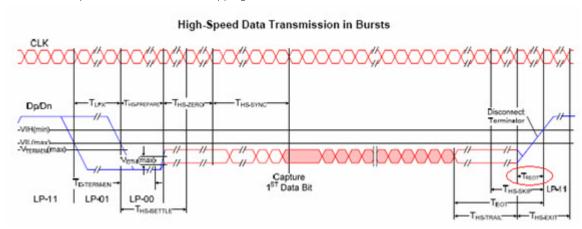


Figure 51 High Speed Data Transmission in Bursts

PASS Condition

The measured T_{EOT} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 45 Test Availability Condition for Test 1.4.14

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|----------------|------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 559 | Not Applicable | 100 ohm | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 559

NOTE

Use the Test ID# 559 to remotely access the test.

- 1 Trigger on the Clkn's falling edge in LP-01 at the SoT.
- 2 Go to EoT.
- 3 Find the time where last Clock TX differential edge crosses +/-VIDTH(max), marked as T1.
- Find the time where Clkp rising edge crosses VIH(min)(880mV), marked as T2. Note that T2 must be greater than T1.
- 5 Use the equation:

 $T_{REOT} = T2-T1$

6 Report the measured T_{REOT}.

7 Compare the measured T_{REOT} value to the compliance test limits.

Test References

See Test 1.4.14 in CTS v1.0 and Section 8.1.2 Table 19 in the D-PHY Specification v1.0.

Test 1.4.15 HS Exit: CLK TX T_{FOT} Method of Implementation

This test verifies the time from start of $T_{\text{CLK-TRAIL}}$ period to start of LP-11 state is within the conformance limit.

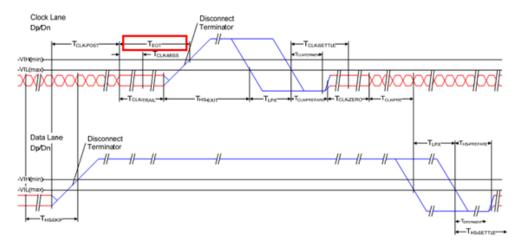


Figure 52 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

PASS Condition

The average T_{EOT} value must be equal or less than the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 46 Test Availability Condition for Test 1.4.15

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|-------------------|------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 544 | Not Applicable | 100 ohm | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 544

NOTE

Use the Test ID# 544 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.

- 2 Trigger on the Clkn's falling edge after LP-01.
- 3 Back trace to the previous EoT.
- 4 Construct the differential clock waveform by using the following equation:

DiffClock = Clkp-Clkn

- 5 Find the time when the DiffClock crosses $+/-V_{IDTH}$ (max) after last payload clock bit. Denote the time as T1.
- 6 Find the time when the Clkp TX rising edge crosses V_{IH} (min)(880mV). Denote the time as T2. Note that T2 must be greater than T1.
- 7 Calculate T_{EOT} using the following equation:

$$T_{EOT} = T2-T1$$

- 8 Report the T_{EOT} measurement.
- 9 Compare the measured $\rm T_{\rm EOT}$ value with the conformance test limit.

Test References

See Test 1.4.15 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

Test 1.4.16 HS Exit: CLK TX T_{HS-FXIT} Method of Implementation

This test verifies that the duration in time for the Clock TX to remain in LP-11 (Stop) state after exiting the HS mode is greater than the minimum required value.



Figure 53 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

PASS Condition

The average $T_{THS-EXIT}$ must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 47 Test Availability Condition for Test 1.4.16

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|----------------|------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 556 | Not Applicable | 100 ohm | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 556

NOTE

Use the Test ID# 556 to remotely access the test.

- 1 Trigger on the Clkn's falling edge after LP-01.
- 2 Find and mark the time when the Clkp's falling edge before the trigger position that crosses $V_{IL}(max)$ and denote it as T1.
- 3 Construct the differential clock waveform by using the following equation:

DiffClock = Clkp-Clkn

4 Find the time when the DiffClock last crosses +V_{IDTH}(max) or -V_{IDTH}(max) before T1, mark it as T0.

5 Calculate T_{HS-EXIT} by using the following equation:

$$T_{HS-EXIT} = T1-T0$$

- $\label{eq:continuous} 6 \quad \text{Report the $T_{HS\text{-}EXIT}$ measurement.}$
- 7 Compare the measured $T_{\mbox{\scriptsize HS-EXIT}}$ to conformance limit.

Test References

See Test 1.4.16 in CTS v1.0 and Section 5.9 Table 14 in the D-PHY Specification v1.0.

MIPI D-PHY 1.0 Clock Transmitter (Clock TX) Global Operation Tests

| | | | | | | | | | | | | | | | | | Part III HS Data-Clock Timing |
|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------|
| | | | | | | | | | | | | | | | | | |



Keysight U7238C/U7238D MIPI D-PHY Test App Methods of Implementation

9 MIPI D-PHY 1.0 High Speed (HS) Data-Clock Timing Tests

Probing for High Speed Data-Clock Timing Tests $\,/\,$ 162 Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation $\,/\,$ 164 Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation $\,/\,$ 165

This section provides the Methods of Implementation (MOIs) for the High Speed (HS) Data-Clock Timing tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test App.



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Probing for High Speed Data-Clock Timing Tests

When performing the HS Data-Clock Timing tests, the MIPI D-PHY Test App will prompt you to make the proper connections. The connections for the HS Data-Clock Timing tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

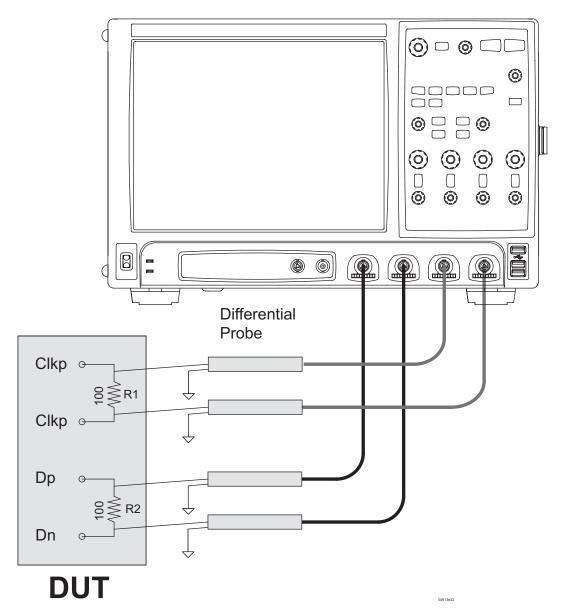


Figure 54 Probing for HS Data-Clock Timing Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test App. (The channels shown in Figure 54 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, ZID (Termination Resistance), CLoad, Device ID and User Comments.
- 4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

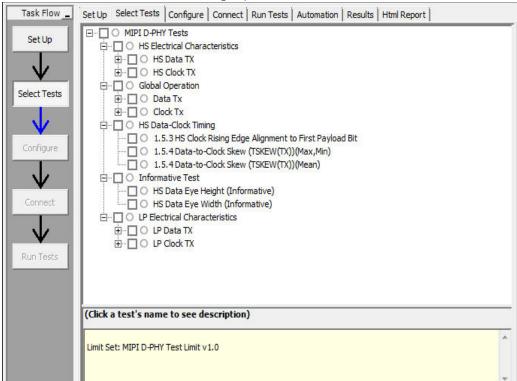


Figure 55 Selecting HS Data-Clock Timing Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation

This test verifies that the first payload bit of the HS transmission burst aligns with differential HS clock's rising edge.

PASS Condition

A DiffClock rising edge must be found during the bit period of the first payload bit for the test to be considered as pass.

Test Availability Condition

Table 48 Test Availability Condition for Test 1.5.3

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-------------------|---------|------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 912 | Not Applicable | 100 ohm | Disabled | Not Applicable |

Measurement Algorithm using Test ID 912

NOTE

Use the Test ID# 912 to remotely access the test.

- 1 Trigger on Dn falling edge after LP-01.
- 2 Find the first payload bit which is the first bit that comes after HS sync sequence.
- 3 Construct the differential clock waveform by using the following equation:

DiffClock = Clkp-Clkn

- 4 Verify if there is a DiffClock rising edge found during the bit period of the first payload bit.
- 5 Report "Pass" as the final test result if there is a DiffClock rising edge found during the bit period of the first payload bit.
- 6 Report "Fail" as the final test result if no DiffClock rising edge is found during the bit period of the first payload bit.

Test References

See Test 1.5.3 in CTS v1.0 and Section 9.2 in the D-PHY Specification v1.0.

Test 1.5.4 Data-to-Clock Skew (T_{SKEW(TX)}) Method of Implementation

This test verifies that the Data to Clock Skew, measured at the transmitter is within the required specification. Based on the specifications, the mentioned T_{Skew} parameter is defined as the allowed deviation of the data launch time to the ideal 1/2UI displaced quadrature clock edge.

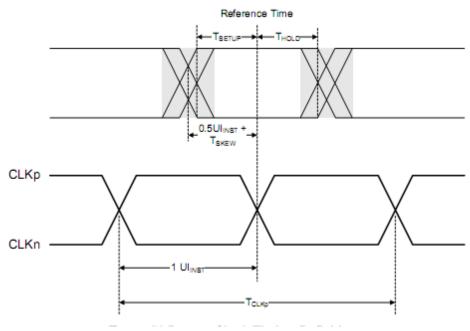


Figure 56 Data to Clock Timing Definitions

PASS Condition

The $T_{SKEW(TX)}$ in UI must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 49 Test Availability Condition for Test 1.5.4

| Associated Test ID | High-Speed Data Rate | ZID | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|---------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 913 | Not Applicable | 100 ohm | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 9131 | Not Applicable | 100 ohm | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 913

NOTE

Use the Test ID# 913 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.

- 2 Dp, Dn, Clkp and Clkn waveforms are captured.
- 3 Construct the differential clock waveform using the following equation:

4 Construct the differential data waveform by using the following equation:

- 5 Using the DiffClock's rising and falling edges, fold the DiffData to form a data eye.
- 6 Use the **Histogram** feature to find out the furthest edges on the left of the DiffData left crossing and use it to calculate the T_{Skew} (max).
- 7 Use the Histogram feature to find out the nearest edges on the left of the DiffData left crossing and use it to calculate the T_{Skew} (min).
- 8 Use the **Histogram** feature to find out the mean of the DiffData left crossing and use it to calculate the T_{Skew} (mean).
- 9 Calculate T_{Skew} values (max/min) in units of seconds and in units of UI using the following equation:

$$T_{Skew(TX)}$$
 (in seconds) = (T_{Skew} - T_{Center}) - MeanSkewRef
$$T_{Skew(TX)}$$
 (in UI) = T_{Skew} /MeanUI

NOTE

MeanSkewRef = [0.5 * MeanUI obtained from the prerequisite test]

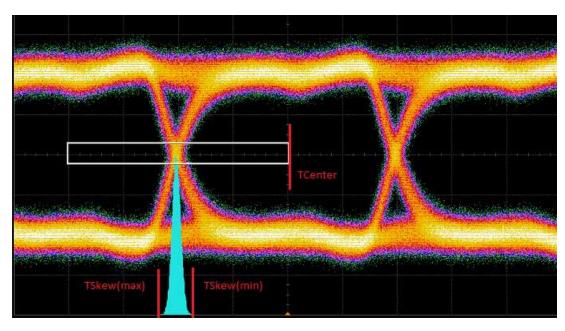


Figure 57 Data Eye

10 Calculate T_{Skew} (mean) in units of UI using the following equation:

$$T_{Skew(TX)}$$
 (in UI) = T_{Skew} /MeanUI

- 11 The T_{Skew} (worst) is determined based on the T_{Skew} (max) and T_{Skew} (min) values with reference to the compliance test limit
- 12 Compare the $T_{\mbox{Skew}}$ (worst) value with the conformance test limits.

Measurement Algorithm using Test ID 9131



Use the Test ID# 9131 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a Data-to-Clock Skew $[T_{Skew(TX)}]$ (Max, Min) (Test ID: 913) Measure the value of T_{Skew} (mean) and the test results are stored.
- 2 Use the value of T_{Skew} (mean) measured in the prerequisite test as the final test result and compare the value to the conformance test limits.

Test References

See Test 1.5.4 in CTS v1.0 and Section 9.2.1 Table 27 in the D-PHY Specification v1.0..

9 MIPI D-PHY 1.0 High Speed (HS) Data-Clock Timing Tests

| | Part IV Informative Tests |
|--|---------------------------|
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| | |



Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

10 MIPI D-PHY 1.0 Informative Tests

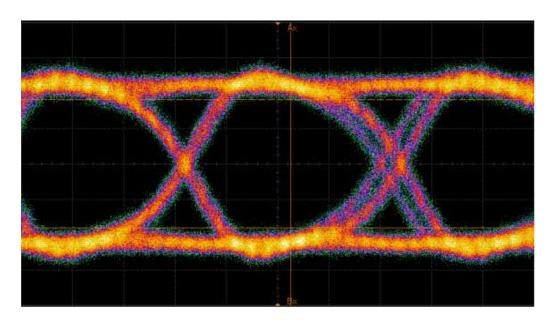
HS Data Eye Height (Informative) Method of Implementation / 172 HS Data Eye Width (Informative) Method of Implementation / 174

This section provides the Methods of Implementation (MOIs) for the informative tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application. These tests are meant to provide additional test information on the DUT. The MIPI DPHY CTS specification do not explicitly specify these tests.



HS Data Eye Height (Informative) Method of Implementation

This test measures the eye height parameter of the test data signal by generating an Eye diagram based on the data and clock signal.



PASS Condition

The measured eye height must be within the limit as set by the user under the Configure tab of the application.

Test Availability Condition

Table 50 Test Availability Condition for HS Data Eye Height

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|-------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 915 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled |

Measurement Algorithm using Test ID 915

NOTE

Select Informative Test on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 915 to remotely access the test.

- 1 Dp, Dn, Clkp and Clkn waveforms are captured.
- 2 Construct the differential clock waveform using the following equation:

DiffClock = Clkp-Clkn

3 Construct the differential data waveform using the following equation:

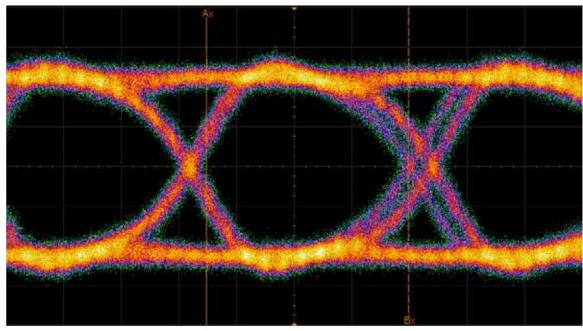
- 4 Using DiffClock's rising and falling edges, fold the DiffData to form a data eye.
- 5 By utilizing histogram, the Eye Height and Eye Width parameters are measured.
 - a The Eye Height measurement is made at 50% location of the eye diagram.
 - b The Eye Width measurement is made at the OV threshold level.
- 6 Report the measured Eye Height and Eye Width.
- 7 Compare measured Eye Height to the test limit. The test limit for this test is configurable under the **Configure** Tab of the application.

Test References

HS Data Eye Height Test is considered as Informative test.

HS Data Eye Width (Informative) Method of Implementation

This test measures the eye width parameter of the test data signal by generating an eye diagram based on the data and clock signal.



PASS Condition

The measured eye width must be within the limit as set by the user under the **Configure** tab of the application.

Test Availability Condition

Table 51 Test Availability Condition for HS Data Eye Width

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|-------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 916 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled |

Measurement Algorithm using Test ID 916



Select Informative Test on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 916 to remotely access the test.

- 1 This test requires the following pre-requisite test(s).
 - a HS Data Eye Height (Informative) (Test ID: 915)
 - : Using DiffClock's rising and falling edges, fold the DiffData to form a data eye.
 - : By utilizing histogram, the Eye Height and Eye Width parameters are measured.
 - : The Eye Height measurement is made at 50% location of the eye diagram.
 - : The Eye Width measurement is made at the 0V threshold level.
- 2 Report the measured Eye Height and Eye Width.
- 3 Compare measured Eye Width to the test limit. The test limit for this test is configurable under the **Configure** Tab of the application.

Test References

HS Data Eye Width Test is considered as Informative test.

| | | | | | | | | | | | | | | | Part B MIPI D-PHY 1.1 |
|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------|
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11 MIPI D-PHY 1.1 High Speed Data Transmitter (HS Data TX) Electrical Tests

Probing for High Speed Data Transmitter Electrical Tests / 182

Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation / 185

Test 1.3.8 HS Data TX V_{CMTX} Mismatch (DV_{CMTX}(1,0)) Method of Implementation / 185

Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz ($DV_{CMTX}(HF)$) Method of Implementation / 185

Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz (DV $_{\rm CMTX}$ (LF)) Method of Implementation / 185

Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation $\,/\,$ 185

Test 1.3.5 HS Data TX Differential Voltage Mismatch (DV $_{
m OD}$) Method of Implementation $\,/\,$ 185

Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation / 185

Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation / 185

Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation / 186

This section provides the Methods of Implementation (MOIs) for the High Speed Data Transmitter (HS Data TX) Electrical tests using an Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test App.

MIPI D-PHY 1.1 HS Data TX tests are the same as MIPI D-PHY 1.0 HS Data TX tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 High Speed Data Transmitter (HS Data TX) Electrical Tests"

The current chapter lists the references from the MIPI D-PHY 1.1 CTS.



Probing for High Speed Data Transmitter Electrical Tests

When performing the HS Data TX tests, the MIPI D-PHY Test App may prompt you to make changes to the physical setup. The connections for the HS Data TX tests may look similar to the following diagrams. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

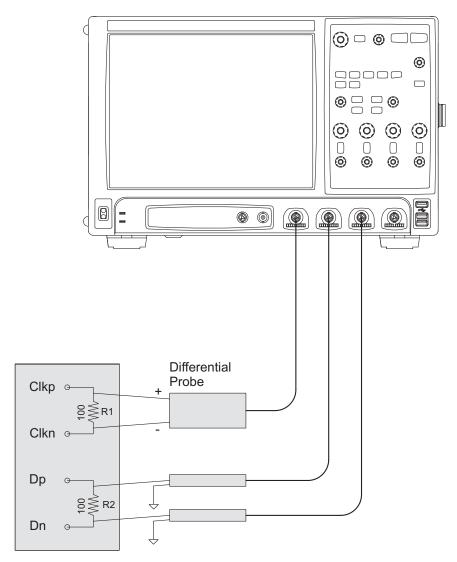


Figure 58 Probing with Three Probes for High Speed Data Transmitter Electrical Tests

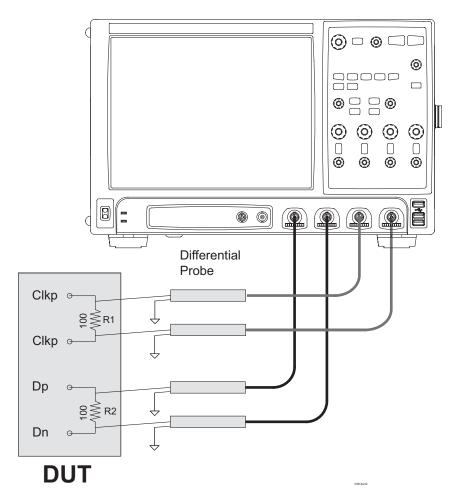


Figure 59 Probing with Four Probes for High Speed Data Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test App. (The channels shown in Figure 58 and Figure 59 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, ZID (termination resistance), Device ID and User Comments.
- 4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

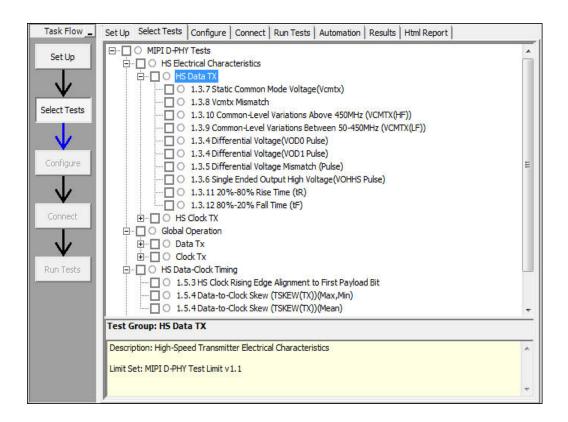


Figure 60 Selecting High Speed Data Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation

Test References

See Test 1.3.7 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1.0)}$) Method of Implementation

Test References

See Test 1.3.8 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz ($\Delta V_{CMTX(HF)}$) Method of Implementation

Test References

See Test 1.3.10 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz ($\Delta V_{CMTX(LF)}$) Method of Implementation

Test References

See Test 1.3.9 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation

Test References

See Test 1.3.4 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.3.5 HS Data TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation

Test References

See Test 1.3.5 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation

Test References

See Test 1.3.6 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation

Test References

See Test 1.3.11 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation

Test References

See Test 1.3.12 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

12 MIPI D-PHY 1.1 High Speed Clock Transmitter (HS Clock TX) Electrical Tests

Probing for High Speed Clock Transmitter Electrical Tests / 188

Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation / 190

Test 1.4.8 HS Clock TX VCMTX Mismatch (DV_{CMTX}(1,0)) Method of Implementation / 190

Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz ($DV_{CMTX}(HF)$) Method of Implementation / 190

Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz (DV $_{\rm CMTX}$ (LF)) Method of Implementation / 190

Test 1.4.4 HS Clock TX Differential Voltage (V_{OD}) Method of Implementation / 190

Test 1.4.5 HS Clock TX Differential Voltage Mismatch (DV_{OD}) Method of Implementation / 190

Test 1. 4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation / 190

Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation / 190

Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation / 191

Test 1.4.17 HS Clock Instantaneous Method of Implementation / 191

Test 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Method of Implementation / 192

This section provides the Methods of Implementation (MOIs) for the High Speed Clock Transmitter (HS Clock T_X) Electrical tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.

MIPI D-PHY 1.1 HS Clock TX tests are the same as MIPI D-PHY 1.0 HS Clock TX tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. There is, however, an additional test that is supported by MIPI D-PHY 1.1 and not by MIPI D-PHY 1.0. The current chapter describes this test and lists the references from the MIPI D-PHY 1.1 CTS.

"Test 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Method of Implementation"

For details of MIPI D-PHY 1.0 tests, refer to "MIPI D-PHY 1.0 High Speed Clock Transmitter (HS Clock TX) Electrical Tests"



Probing for High Speed Clock Transmitter Electrical Tests

When performing the HS Clock T_x tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the HS Clock T_X tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

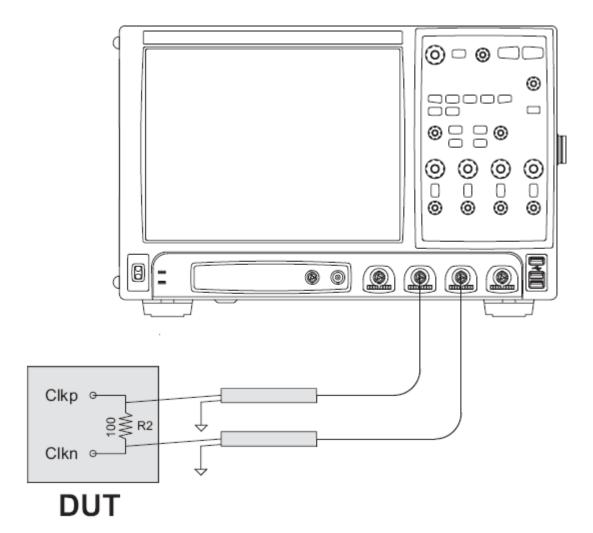


Figure 61 Probing for High Speed Clock Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 61 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, ZID (termination resistance), Device ID and User Comments.

Task Flow _ Set Up Select Tests | Configure | Connect | Run Tests | Automation | Results | Html Report □ □ O MIPI D-PHY Tests Set Up □ □ ○ HS Electrical Characteristics ⊕ □ ○ HS Data TX ⊟ O HS Clock TX --- ☐ ○ 1.4.7 Static Common Mode Voltage(Vcmtx) Select Tests ... □ ○ 1.4.8 Vcmtx Mismatch □ ○ 1.4.10 Common-Level Variations Above 450MHz (VCMTX(HF)) □ ○ 1.4.9 Common-Level Variations Between 50-450MHz (VCMTX(LF)) 1.4.4 Differential Voltage (VOD0 Pulse) Configure □ ○ 1.4.4 Differential Voltage(VOD1 Pulse) □ □ 1.4.5 Differential Voltage Mismatch (Pulse) □ 1.4.6 Single Ended Output High Voltage(VOHHS Pulse) □ ○ 1.4.11 20%-80% Rise Time (tR) Connect - □ ○ 1.4.12 80%-20% Fall Time (tF) - □ ○ 1.4.17 HS Clock Instantaneous (UIinst)(Max) -- □ ○ 1.4.17 HS Clock Instantaneous (UIinst)(Min) · □ ○ 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Run Tests ☐ Global Operation ⊕ □ ○ Clock Tx □ □ O HS Data-Clock Timing Test Group: HS Clock TX Description: High-Speed Transmitter Electrical Characteristics Limit Set: MIPI D-PHY Test Limit v1.1

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

Figure 62 Selecting High Speed Clock Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation

Test References

See Test 1.4.7 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.4.8 HS Clock TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1.0)}$) Method of Implementation

Test References

See Test 1.4.8 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz ($\Delta V_{\text{CMTX(HF)}}$) Method of Implementation

Test References

See Test 1.4.10 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz ($\Delta V_{CMTX(LF)}$) Method of Implementation

Test References

See Test 1.4.9 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Test 1.4.4 HS Clock TX Differential Voltage (V_{OD}) Method of Implementation

Test References

See Test 1.4.4 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.4.5 HS Clock TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation

Test References

See Test 1.4.5 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1. 4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation

Test References

See Test 1.4.6 in CTS v1.1 and Section 9.1.1 Table 16 in the D-PHY Specification v1.1.

Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation

Test References

See Test 1.4.11 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation

Test References

See Test 1.4.12 in CTS v1.1 and Section 9.1.1 Table 17 in the D-PHY Specification v1.1.

Test 1.4.17 HS Clock Instantaneous Method of Implementation

Test References

See Test 1.4.17 in CTS v1.1 and Section 10.1 Table 26 in the D-PHY Specification v1.1.

Test 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Method of Implementation

Clock Lane HS Clock Delta UI (UI variation) verifies that the frequency stability of the DUT HS Clock during a signal burst is within the conformance limits.

PASS Condition

The measured UI variation must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 52 Test Availability Condition for Test 1.4.18

| Associated | High-Speed | ZID | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|----------------|---------|----------------|----------------|----------------|----------------|-------------------|----------------|
| Test ID | Data Rate | | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 1911 | Not Applicable | 100 ohm | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 1911

NOTE

Use the Test ID# 1911 to remotely access the test.

- 1 This test requires the following prerequisite test(s).
 - a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

The minimum, maximum and average Unit Interval of the differential clock waveform is measured and stored.

2 Calculate the UI_Variant_min and UI_Variant_max according to the following equation:

UI_Variant_min = ((Ulinst_min - Uiinst_mean) / Ulinst_mean) * 100%

UI_Variant_max = ((Ulinst_max - Uiinst_mean) / Ulinst_mean) * 100%

- 3 Determine the UI_variant_worst based on the UI_Variant_min and UI_Variant_max calculated above.
- 4 Compare the worst measured value of UI_variant_worst with the conformance limit.

Test References

See Test 1.4.18 in CTS v1.1 and Section 10.1 Table 26 in the D-PHY Specification v1.1.

Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

13 MIPI D-PHY 1.1 Low Power Data Transmitter (LP Data TX) Electrical Tests

Probing for Low Power Transmitter Electrical Tests / 194

Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation / 196

Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation / 198

Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation / 200

Test 1.1.4 LP TX 15%-85% Fall Time Level ($T_{\rm FLP}$) Method of Implementation / 201

Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock (T_{LP-PULSE-TX}) Method of Implementation / 203

Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock (T_{I P-PFR-TX}) Method of Implementation / 206

Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation / 208

This section provides the Methods of Implementation (MOIs) for the Low Power Data Transmitter (LP Data TX) Electrical tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.



Probing for Low Power Transmitter Electrical Tests

When performing the LP TX tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the LP TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Conformance Test Application for the exact number of probe connections.

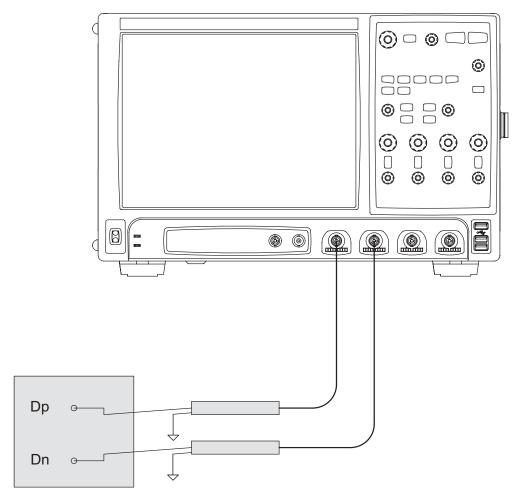


Figure 63 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 63 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, ZID (termination resistance) Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

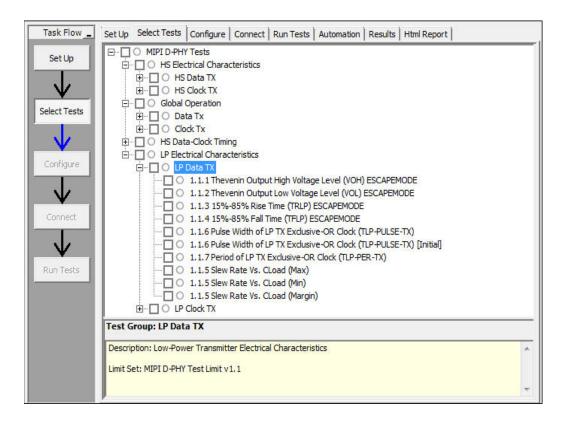


Figure 64 Selecting Low Power Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation

V_{OH} is the Thevenin output high-level voltage in the high-level state, when the pad pin is not loaded.

PASS Condition

The measured V_{OH} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 53 Test Availability Conditions for Test 1.1.1

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 821 | Not Applicable | Disabled | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable |
| 8211 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 821

LP TX Thevenin Output High Voltage Level (V_{OH})



Ensure that **Data LP EscapeMode** is disabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 821 to remotely access the test.

- 1 Trigger the Dp's LP rising edge.
- 2 Position the trigger point at the center of the screen and make sure that the stable Dp LP high level voltage region is visible on the screen.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
- 4 Accumulate the data using the persistent display mode.
- 5 Enable the **Histogram** feature and measure the entire display region after the trigger location.
- 6 Take the mode value from the Histogram and use this value as V_{OH} for Dp.
- 7 Repeat steps 1 to 6 for Dn.
- 8 Report the measurement results.
 - a V_{OH} value for Dp channel
 - b V_{OH} value for Dn channel
- 9 Compare the measured worst value of V_{OH} with the compliance test limits.

Measurement Algorithm using Test ID 8211

LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8211 to remotely access the test.

- 1 Trigger on LP Data EscapeMode pattern on the data signal. Without the presence of LP Escape mode, the trigger is unable to capture any valid signal for data processing.
- 2 Locate and use the Mark-1 state pattern to determine the end of the EscapeMode sequence.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired EscapeMode sequence waveform data.
- 4 Enable the **Histogram** feature and measure the entire LP Data EscapeMode sequence.
- 5 Take the mode value from the **Histogram** and use this value as V_{OH} for Dp.
- 6 Repeat steps 1 to 5 for Dn.
- 7 Report the measurement results.
 - a V_{OH} value for Dp channel
 - b V_{OH} value for Dn channel
- 8 Compare the measured worst value of V_{OH} with the conformance test limits.

Test References

See Test 1.1.1 in CTS v1.1 and Section 9.1.2 Table 18 in the D-PHY Specification v1.1.

Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OI}) Method of Implementation

 V_{OL} is the Thevenin output low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low level state.

PASS Condition

The measured V_{OL} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 54 Test Availability Condition for Test 1.1.2

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 822 | Not Applicable | Disabled | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable |
| 8221 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 822

LP TX Thevenin Output Low Voltage Level (V_{OL})



Ensure that **Data LP EscapeMode** is disabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 822 to remotely access the test.

- 1 This test requires the following prerequisite test(s):
 - a HS Entry: DATA TX T_{HS-PREPARE} (Test ID: 557)
- 2 Trigger the Dp's LP falling edge.
- 3 Position the trigger point at the center of the screen and make sure that the stable Dp LP low level voltage region is visible on the screen.
- 4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
- 5 Accumulate the data by using the persistent display mode.
- 6 Enable the **Histogram** feature and measure the entire display region after the trigger location.
- 7 Take the mode value from the Histogram and use this value as V_{OL} for Dp.
- 8 Repeat steps 1 to 7 for Dn.
- 9 Report the measurement results:
 - a V_{OI} value for Dp channel
 - b V_{OL} value for Dn channel
- 10 Compare the measured worst value of V_{OL} with the conformance test limits.

Measurement Algorithm using Test ID 8221

LP TX Thevenin Output Low Voltage Level (VOL) ESCAPEMODE

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8221 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
- 2 Trigger on LP Data EscapeMode pattern on the data signal. Without the presence of the LP Escape mode, the trigger is unable to capture any valid signal for data processing.
- 3 Locate and use the Mark -1 state pattern to determine the end of the EscapeMode sequence.
- 4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired EscapeMode sequence waveform data.
- 5 Enable the **Histogram** feature and measure the entire LP data EscapeMode sequence.
- 6 Take the mode value from the ${\bf Histogram}$ and use this value as ${\bf V}_{\rm OL}$ for Dp.
- 7 Repeat steps 1 to 6 for Dn.
- 8 Report the measurement results:
 - a V_{OI} value for Dp channel
 - b V_{OL} value for Dn channel
- 9 Compare the measured worst value of V_{OL} with the conformance test limits.

Test References

See Test 1.1.2 in CTS v1.1 and Section 9.1.2 Table 18 in the D-PHY Specification v1.1.

Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation

The T_{RLP} is defined as 15%-85% rise time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD} . The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{RLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 55 Test Availability Condition for Test 1.1.3

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|------------|----------------|------------|----------------|----------------|----------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 8241 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 8241

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8241 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
 - b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221)

 $\rm V_{OH}$ and $\rm V_{OL}$ values for Low Power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 A 400 MHz, 4th-order Butterworth low pass test filter is applied to the mentioned EscapeMode sequence data prior to performing the actual rise time measurement.
- 4 All the rising edges in the filtered EscapeMode sequence are processed in measuring the corresponding rise time.
- 5 The average 15%-85% rise time for Dp is recorded.
- 6 Repeat the steps for Dn.
- 7 Report the measurement results:
 - a T_{RLP} average value for Dp channel
 - b T_{RLP} average value for Dn channel
- 8 Compare the measured T_{RLP} worst value with the compliance test limit.

Test References

See Test 1.1.3 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.1.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation

The T_{FLP} is defined as 15%-85% fall time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD} . The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{FLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 56 Test Availability Condition for Test 1.1.4

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 825 | Not Applicable | Disabled | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable |
| 8251 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 825

LP TX 15%-85% Fall Time (T_{FLP})



Ensure that **Data LP EscapeMode** is disabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 825 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) (Test ID: 821)
 - b LP TX Thevenin Output Low Voltage Level (V_{OL}) (Test ID: 822)

Measure the V_{OH} and V_{OI} values for the low power signal and test results are stored.

- 2 All falling edges in LP are valid for this measurement.
- 3 Setup the trigger on LP falling edges.
- 4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
- 5 Depending on the number of observation configuration, the oscilloscope is triggered accordingly.
- 6 The average 15%-85% fall time for Dp is recorded.
- 7 Repeat the same trigger steps for Dn.
- 8 Report the measurement results:
 - a T_{FLP} average value for Dp channel
 - b T_{FLP} average value for Dn channel
- 9 Compare the measured worst value of T_{FLP} with the compliance test limits.

Measurement Algorithm using Test ID 8251

LP TX 15%-85% Fall Time (T_{FLP}) ESCAPEMODE

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8251 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
 - b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221) Measure the V_{OH} and V_{OI} values for the low power signal and test results are stored.
- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to measuring the actual fall time.
- 4 All falling edges in the filtered EscapeMode sequence are processed in measuring the corresponding fall time.
- 5 The average 15%-85% fall time for Dp is recorded.
- 6 Repeat steps 1 to 5 for Dn.
- 7 Report the measurement results:
 - a T_{FLP} average value for Dp channel
 - b T_{FLP} average value for Dn channel
- 8 Compare the measured worst value of T_{FLP} with the compliance test limits.

Test References

See Test 1.1.4 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock ($T_{LP-PULSE-TX}$) Method of Implementation

 $T_{LP-PULSE-TX}$ is defined as the pulse width of the DUT Low-Power TX XOR clock. A graphical representation of the XOR operation that creates the LP clock is shown below. The D-PHY Standard actually separates the $T_{LP-PULSE-TX}$ specification into two parts:

- a The first LP XOR clock pulse after a Stop state, or the last LP XOR clock pulse before a Stop state must be wider than 40ns.
- b All other LP XOR clock pulses must be wider than 20ns.

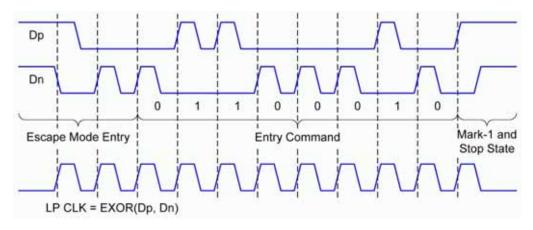


Figure 65 Graphical Representation of the XOR Operation

PASS Condition

The measured $T_{LP-PULSE-TX}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 57 Test Availability Condition for Test 1.1.6

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 827 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 8271 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 8272 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Enabled |
| 1827 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 18271 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 18272 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Enabled |

Measurement Algorithm using Test IDs 827, 8271 and 8272

LP TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX})

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 827 to remotely access the test.

LP TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX}) [Initial]

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8271 to remotely access the test.

LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$) [Last]

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8272 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211). This is to trigger and capture an EscapeMode sequence data from the test signal.
- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data.
- 4 Find all crossing points at the minimum trip level (500mV) and the maximum trip level (930mV) for Dp and Dn individually.
- 5 Find the initial pulse width, last pulse width and minimum width of all the other pulses at the specified minimum trip level and maximum trip level.
- 6 Find the rising-to-rising and falling-to-falling periods of the XOR clock at the mentioned minimum trip level and maximum trip level.
- 7 The worst case value for the pulse width found between the minimum trip level and maximum trip level will be used as the T_{LP-PULSE-TX} value.
- 8 Compare the measured minimum T_{LP-PULSE-TX} value with the compliance test limits.

Measurement Algorithm using Test IDs 1827, 18271 and 18272

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX})

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 1827 to remotely access the test.

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX}) [Initial]

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 18271 to remotely access the test.

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX}) [Last]

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 18272 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211) This is to trigger and capture an EscapeMode sequence data from the test signal.
- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data.
- 4 Find all crossing points at the minimum trip level (500mV) and the maximum trip level (930mV) for Clkp and Clkn individually.
- 5 Find the initial pulse width, last pulse width and minimum width of all the other pulses at the specified minimum trip level and maximum trip level.
- 6 Find the rising-to-rising and falling-to-falling periods of the XOR clock at the specified minimum trip level and maximum trip level.
- 7 The worst case value for the pulse width found between the minimum trip level and maximum trip level is used as the T_{LP-PULSE-TX} value.
- 8 Compare the measured minimum $T_{LP-PULSE-TX}$ value with the compliance test limits.

Test References

See Test 1.1.6 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock (T_{LP-PFR-TX}) Method of Implementation

 $T_{LP\text{-}PER\text{-}TX}$ is defined as the period of the DUT Low-Power TX XOR clock. A graphical representation of the XOR operation that creates the LP clock is shown below. The D-PHY Standard separates the $T_{LP\text{-}PULSE\text{-}TX}$ specification into two parts:

- a The first LP XOR clock pulse after a Stop state, or the last LP XOR clock pulse before a Stop state must be wider than 40ns.
- b All other LP XOR clock pulses must be wider than 20ns.

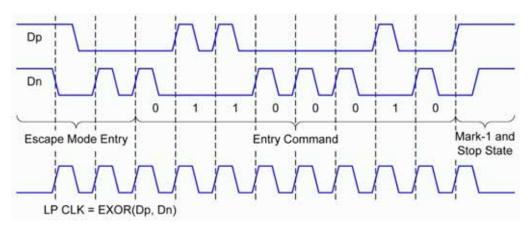


Figure 66 Graphical Representation of the XOR Operation

PASS Condition

The measured $T_{LP-PER-TX}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 58 Test Availability Condition for Test 1.1.7

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 828 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 1828 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |

Measurement Algorithm using Test ID 828

LP TX Period of LP TX Exclusive-OR Clock (T_{LP-PER-TX})

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 828 to remotely access the test.

- 1 This test requires the following prerequisite test(s).
 - a LP TX Pulse Width of LP TX Exclusive-OR Clock (T_{I P-PUI SF-TX}) (Test ID: 827)

The actual measurement algorithm of the $T_{LP-PER-TX}$ is performed in the mentioned prerequisite test.

- 2 The minimum value for all the rising-to-rising and falling-to-falling periods of the XOR clock at the minimum trip level (500mV) and the maximum trip level (930mV) is used as the T_{LP-PER-TX} result.
- 3 Compare the measured minimum T_{LP-PER-TX} value to the compliance test limits.

Measurement Algorithm using Test ID 1828

LP Clock TX Period of LP TX Exclusive-OR Clock (T_{LP-PER-TX})

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 1828 to remotely access the test.

- 1 This test requires the following prerequisite test(s).
 - a LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$) (Test ID: 1827) The actual measurement algorithm of the $T_{LP-PER-TX}$ is performed in the mentioned prerequisite test
- 2 The minimum value for all the rising-to-rising and falling-to-falling periods of the XOR clock at the minimum trip level (500mV) and the maximum trip level (930mV) is used as the $T_{LP-PER-TX}$ result.
- 3 Compare the measured minimum T_{IP-PFR-TX} value with the compliance test limits.

Test References

See Test 1.1.7 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation

The slew rate δ V/ δ t_{SR} is the derivative of the LP transmitter output signal voltage over time. The intention of specifying a maximum slew rate value in the specification is to limit EMI (Electro Magnetic Interference).

The specification also states that the Slew Rate must be measured as an average across any 50mV segment of the output signal transition.

PASS Condition

The measured slew rate δ V/ δ t_{SR} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 59 Test Availability Condition for Test 1.1.5

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 829 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 8291 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 8292 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test IDs 829, 8291 and 8292

NOTE

Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test.

- To access the LP TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 829.
- To access the LP TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 8291.
- To access the LP TX Slew Rate Vs. C_{load} (Margin) test remotely, use the Test ID# 8292.
- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
 - b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221)

 $\ensuremath{V_{OH}}$ and $\ensuremath{V_{OL}}$ values for low power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual slew rate measurement.
- 4 Perform the slew rate measurement on the filtered EscapeMode sequence for both Dp and Dn waveforms individually.

For falling edge,

- a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
- b. Perform the slew rate measurement across the 400mV 930mV region to determine the minimum slew rate result.

For rising edge,

a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.

- b. Perform the slew rate measurement across the 400mV 700mV region to determine the minimum slew rate result.
- c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV 930mV region.
- 5 Calculate the average value from all rising edges' maximum slew rate results. Calculate the average value from all falling edges' maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
- 6 Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
- 7 Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
- 8 The Slew Rate maximum, minimum and margin result values are stored.
- 9 Report the measurement results.
- 10 Compare the measured worst slew rate value with the conformance test limits.

Test References

See Test 1.1.5 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Keysight U7238C/U7238D MIPI D-PHY Test App Methods of Implementation

14 MIPI D-PHY 1.1 Low Power Clock Transmitter (LP Clock TX) Electrical Tests

Probing for Low Power Transmitter Electrical Tests / 212

Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation / 214

Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OI}) Method of Implementation / 216

Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation / 219

Test 1.2.4 LP TX 15%-85% Fall Time Level ($T_{\rm FLP}$) Method of Implementation / 221

Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation / 224

This section provides the Methods of Implementation (MOIs) for the Low Power Clock Transmitter (LP Clock TX) Electrical tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test App.



Probing for Low Power Transmitter Electrical Tests

When performing the LP TX tests, the MIPI D-PHY Test App will prompt you to make the proper connections. The connections for the LP TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test App for the exact number of probe connections.

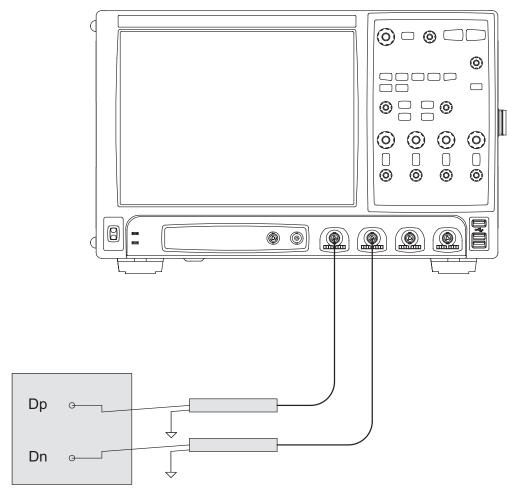


Figure 67 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test App. (The channels shown in Figure 67 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, ZID (termination resistance), Device ID and User Comments.

Task Flow _ Set Up Select Tests | Configure | Connect | Run Tests | Automation | Results | Html Report | □ □ O MIPI D-PHY Tests Set Up □ □ O HS Electrical Characteristics ⊕ □ ○ HS Data TX Global Operation Select Tests ⊕ □ ○ Data Tx ⊞ □ ○ Clock Tx HS Data-Clock Timing □ □ O LP Electrical Characteristics Configure ⊞ □ ○ LP Data TX □ O LP Clock T. □ ○ 1.2.1 Thevenin Output High Voltage Level (VOH) ESCAPEMODE □ 1.2.2 Thevenin Output Low Voltage Level (VOL) ESCAPEMODE 1.2.3 15%-85% Rise Time (TRLP) ESCAPEMODE □ ○ 1.2.4 15%-85% Fall Time (TFLP) ESCAPEMODE □ □ 1.1.6 Pulse Width of LP TX Exclusive-OR Clock (TLP-PULSE-TX) □ □ 1.1.6 Pulse Width of LP TX Exclusive-OR Clock (TLP-PULSE-TX) [Initial] 1.1.7 Period of LP TX Exclusive-OR Clock (TLP-PER-TX) Run Tests □ ○ 1.2.5 Slew Rate Vs. CLoad (Max) 1.2.5 Slew Rate Vs. CLoad (Min) □ ○ 1.2.5 Slew Rate Vs. CLoad (Margin) Test Group: LP Clock TX Description: Low-Power Transmitter Electrical Characteristics Limit Set: MIPI D-PHY Test Limit v 1.1

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

Figure 68 Selecting Low Power Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation

V_{OH} is the Thevenin output high-level voltage in the high-level state, when the pad pin is not loaded.

PASS Condition

The measured V_{OH} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 60 Test Availability Condition for Test 1.2.1

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 1821 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Disabled | Not Applicable |
| 18211 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 28211 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Enabled | Not Applicable |

Measurement Algorithm using Test ID 1821 and 28211

LP Clock TX Thevenin Output High Voltage Level (VOH)

NOTE

Ensure that the Clock LP EscapeMode and Clock ULPS Mode are disabled on the Device Information section of the Set Up tab of the MIPI D-PHY Test application. Use the Test ID# 1821 to remotely access the test.

ULPS Clock TX Thevenin Output High Voltage Level (VOH) ULPSMODE



Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28211 to remotely access the test.

- 1 Trigger the Clkp's LP rising edge.
- 2 Position the trigger point at the center of the screen and make sure that the stable Clkp LP high level voltage region is visible on the screen.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
- 4 Accumulate the data by using the persistent display mode.
- 5 Enable the Histogram feature and measure the entire display region after the trigger location.
- 6 Take the mode value from the ${f Histogram}$ and use this value as ${f V}_{OH}$ for Clkp.
- 7 Repeat steps 1 to 6 for Clkn.
- 8 Report the measurement results.
 - a V_{OH} value for Clkp channel
 - b V_{OH} value for Clkn channel
- 9 Compare the measured worst value of V_{OH} with the compliance test limits.

Measurement Algorithm using Test ID 18211

LP Clock TX Thevenin Output High Voltage Level (VOH) ESCAPEMODE

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18211 to remotely access the test.

- 1 Trigger on an EscapeMode pattern on the data signal. Without the presence of the LP Escape mode, the trigger is unable to capture any valid signal for data processing.
- 2 Locate and use the Mark-1 state pattern to determine the end of the EscapeMode sequence.
- 3 Apply a 400 MHz, 4th order Butterworth low pass test filter to the specified EscapeMode sequence data.
- 4 Enable the **Histogram** feature and measure the entire LP EscapeMode sequence.
- 5 Take the mode value from the ${f Histogram}$ and use this value as ${f V}_{OH}$ for Clkp.
- 6 Repeat steps 1 to 4 for Clkn.
- 7 Report the measurement results.
 - a V_{OH} value for Clkp channel
 - b V_{OH} value for Clkn channel
- 8 Compare the measured worst value of V_{OH} with the compliance test limits.

Test References

See Test 1.2.1 in CTS v1.1 and Section 9.1.2 Table 18 in the D-PHY Specification v1.1.

Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OI}) Method of Implementation

 V_{OL} is the Thevenin output low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low level state.

PASS Condition

The measured V_{OL} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 61 Test Availability Condition for Test 1.2.2

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 1822 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Disabled | Not Applicable |
| 18221 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 28221 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Enabled | Not Applicable |

Measurement Algorithm using Test ID 1822

LP Clock TX Thevenin Output Low Voltage Level (V_{OL})



Ensure that the Clock LP EscapeMode and Clock ULPS Mode are disabled on the Device Information section of the Set Up tab of the MIPI D-PHY Test application. Use the Test ID# 1822 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Entry: CLK TX T_{CLK-PREPARE} (Test ID: 552)
- 2 Trigger the Clkp's LP falling edge.
- 3 Position the trigger point at the center of the screen and make sure that the stable Clkp LP low level voltage region is visible on the screen.
- 4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
- 5 Accumulate the data by using the persistent display mode.
- 6 Enable the **Histogram** feature and measure the entire display region after the trigger location.
- 7 Take the mode value from the **Histogram** and use this value as V_{OL} for Clkp.
- 8 Repeat steps 1 to 7 for Clkn.
- 9 Report the measurement results:
 - a V_{OI} value for Clkp channel
 - b V_{OI} value for Clkn channel
- 10 Compare the measured worst value of V_{OL} with the compliance test limits.

Measurement Algorithm using Test ID 18221

LP Clock TX Thevenin Output Low Voltage Level (VOL) ESCAPEMODE

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18221 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
- 2 Trigger on an EscapeMode pattern on the data signal. Without the presence of LP Escape mode, the trigger is unable to capture any valid signal for data processing.
- 3 Locate and use the Mark -1 state pattern to determine the end of the EscapeMode sequence.
- 4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data.
- 5 Enable the **Histogram** feature and measure the entire LP EscapeMode sequence.
- 6 Take the mode value from the **Histogram** and use this value as V_{OL} for Clkp.
- 7 Repeat steps 1 to 6 for Clkn.
- 8 Report the measurement results:
 - a V_{OI} value for Clkp channel
 - b V_{OL} value for Clkn channel
- 9 Compare the measured worst value of V_{OL} with the compliance test limits.

Measurement Algorithm using Test ID 28221

ULPS Clock TX Thevenin Output Low Voltage Level (V_{OL}) ULPSMODE



Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28221 to remotely access the test.

- 1 This test requires the following prerequisite test(s):
 - a ULPS Clock TX Thevenin Output High Voltage Level (VOH) ULPSMODE (Test ID: 28211)
- 2 Trigger the Clkp's LP falling edge.
- 3 Position the trigger point at the center of the screen and make sure that the stable Clkp LP low level voltage region is visible on the screen.
- 4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
- 5 Accumulate the data by using the persistent display mode.
- 6 Enable the **Histogram** feature and measure the entire display region after the trigger location.
- 7 Take the mode value from the ${\bf Histogram}$ and use this value as ${\bf V}_{\rm OL}$ for Clkp.
- 8 Repeat steps 1 to 7 for Clkn.
- 9 Report the measurement results:
 - a V_{OI} value for Clkp channel
 - b V_{OI} value for Clkn channel
- 10 Compare the measured worst value of V_{OL} with the conformance test limits.

Test References

See Test 1.2.2 in CTS v1.1 and Section 9.1.2 Table 18 in the D-PHY Specification v1.1.

Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation

The T_{RLP} is defined as 15%-85% rise time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD} . The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{RLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 62 Test Availability Condition for Test 1.2.3

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 18241 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 28241 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Enabled | Not Applicable |

Measurement Algorithm using Test ID 18241

LP Clock TX 15%-85% Rise Time (T_{RLP}) ESCAPEMODE



Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18241 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
 - b LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 18221)

 $V_{\mbox{\scriptsize OH}}$ and $V_{\mbox{\scriptsize OL}}$ values for Low Power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual rise time measurement.
- 4 Perform rise time measurement on the filtered EscapeMode sequence for both Clkp and Clkn waveforms individually.
- 5 The max, mean and min result values are stored.
- 6 Report the measurement results:
 - a T_{RLP} average value for Clkp channel
 - b T_{RIP} average value for Clkn channel
- 7 Compare the measured T_{RLP} worst value derived from the T_{RLP} average value for Clkp and Clkn to the compliance test limit.

Measurement Algorithm using Test ID 28241

ULPS Clock TX 15%-85% Rise Time (TRLP) ULPSMODE

NOTE

Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28241 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
 - b ULPS Clock TX Thevenin Output Low Voltage Level (V_{OI}) ULPSMODE (Test ID: 28221)

 ${
m V}_{
m OH}$ and ${
m V}_{
m OL}$ values for Low Power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual rise time measurement.
- 4 Perform rise time measurement on the filtered EscapeMode sequence for both Clkp and Clkn waveforms individually.
- 5 The max, mean and min result values are stored.
- 6 Report the measurement results:
 - a T_{RLP} average value for Clkp channel
 - b T_{RLP} average value for Clkn channel
- 7 Compare the measured T_{RLP} worst value derived from the T_{RLP} average value for Clkp and Clkn to the compliance test limit.

Test References

See Test 1.2.3 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation

The T_{FLP} is defined as 15%-85% fall time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD} . The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{FLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 63 Test Availability Condition for Test 1.2.4

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 1825 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Disabled | Not Applicable |
| 18251 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 28251 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Enabled | Not Applicable |

Measurement Algorithm using Test ID 1825

LP Clock TX 15%-85% Fall Time (T_{FLP})



Ensure that the Clock LP EscapeMode and Clock ULPS Mode are disabled on the Device Information section of the Set Up tab of the MIPI D-PHY Test application. Use the Test ID# 1825 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) (Test ID: 1821)
 - b LP Clock TX Thevenin Output Low Voltage Level (VOL) (Test ID: 1822)

 $\rm V_{OH}$ and $\rm V_{OL}$ values for Low Power signal measurements are performed and test results are stored.

- 2 Trigger is setup to trigger on LP falling edges.
- 3 The oscilloscope is triggered to capture the falling edges to be processed based on the "LP Observations" configuration in the **Configure** tab.
- 4 Apply a 400 MHz, 4th-order Butterworth low pass test filter to the specified triggered data prior to performing the actual fall time measurement.
- 5 The average 15%-85% fall time for Clkp is recorded.
- 6 Repeat the same trigger steps for Clkn.
- 7 Report the measurement results:
 - a T_{FLP} average value for Clkp channel
 - b T_{FLP} average value for Clkn channel
- 8 Compare the measured worst value of T_{FLP} with the compliance test limits.

Measurement Algorithm using Test ID 18251

LP Clock TX 15%-85% Fall Time (T_{FLP}) ESCAPEMODE

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18251 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
 - b LP Clock TX Thevenin Output Low Voltage Level (VOL) ESCAPEMODE (Test ID: 18221)

 V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual fall time measurement.
- 4 Perform fall time measurement on the filtered EscapeMode sequence for both Clkp and Clkn waveforms individually.
- 5 The maximum, mean and minimum result values are stored.
- 6 Report the measurement results:
 - a T_{FLP} average value for Clkp channel
 - b T_{FLP} average value for Clkn channel
- 7 Compare the measured worst value of T_{FLP} derived from the average value of T_{FLP} for Clkp and Clkn to the compliance test limits.

Measurement Algorithm using Test ID 28251

ULPS Clock TX 15%-85% Fall Time (T_{FLP}) ULPSMODE



Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28251 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
 - b ULPS Clock TX Thevenin Output Low Voltage Level (V_{OI}) ULPSMODE (Test ID: 28221)

 $\ensuremath{V_{OH}}$ and $\ensuremath{V_{OL}}$ values for low power signal measurements are performed and test results are stored.

- 2 Trigger is setup to trigger on LP falling edges.
- 3 The oscilloscope is triggered to capture the falling edges to be processed based on the "LP Observations" configuration in the **Configure** tab.
- 4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned trigger data prior to measuring the actual fall time.
- 5 The average 15%-85% fall time for Clkp is recorded.
- 6 Repeat the same trigger steps for Clkn.

- 7 Report the measurement results:
 - a T_{FLP} average value for Clkp channel
 - b T_{FLP} average value for Clkn channel
- 8 Compare the measured worst value of $T_{\mbox{\scriptsize FLP}}$ to the compliance test limits.

Test References

See Test 1.2.4 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation

The slew rate δ V/ δ t_{SR} is the derivative of the LP transmitter output signal voltage over time. The intention of specifying a maximum slew rate value in the specification is to limit EMI (Electro Magnetic Interference).

The specification also states that the Slew Rate must be measured as an average across any 50mV segment of the output signal transition.

PASS Condition

The measured slew rate δ V/ δ t_{SR} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 64 Test Availability Condition for Test 1.2.5

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 1829 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 18291 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 18292 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 2829 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled | Not Applicable |
| 28291 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled | Not Applicable |
| 28292 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled | Not Applicable |

Measurement Algorithm using Test ID 1829, 18291 and 18292

LP Clock TX Slew Rate Vs. C_{Load} (Max) /

LP Clock TX Slew Rate Vs. C_{Load} (Min) /

LP Clock TX Slew Rate Vs. C_{Load} (Margin)

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test.

- To access the LP Clk TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 1829.
- To access the LP CIk TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 18291.
- To access the LP Clk TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 18292.
- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (VOH) ESCAPEMODE (Test ID: 18211)
 - b LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 18221)

- $\rm V_{OH}$ and $\rm V_{OL}$ values for low power signal measurements are performed and test results are stored
- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual slew rate measurement.
- 4 Perform the slew rate measurement on the filtered EscapeMode sequence for both Clkp and Clkn waveforms individually.

For falling edge,

- a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result
- b. Perform the slew rate measurement across the 400mV 930mV region to determine the minimum slew rate result.

For rising edge,

- a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
- b. Perform the slew rate measurement across the 400mV 700mV region to determine the minimum slew rate result.
- c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700 mV 930 mV region.
- 5 Calculate the average value from all rising edges' maximum slew rate results. Calculate the average value from all falling edges' maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
- 6 Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
- 7 Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
- 8 The Slew Rate maximum, minimum and margin result values are stored.
- 9 Report the measurement results.
- 10 Compare the measured worst slew rate value for Clkp and Clkn to the compliance test limits.

ULPS Clock TX Slew Rate Vs. C_{Load} (Max) ULPSMODE/

ULPS Clock TX Slew Rate Vs. C_{I.oad} (Min) ULPSMODE/

ULPS Clock TX Slew Rate Vs. C_{Load} (Margin) ULPSMODE

Measurement Algorithm using Test ID 2829, 28291 and 28292

NOTE

Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test.

- To access the ULPS Clk TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 2829.
- To access the ULPS CIk TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 28291.
- To access the ULPS CIk TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 28292.
- 1 This test requires the following prerequisite tests:
 - a ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
 - b ULPS Clock TX Thevenin Output Low Voltage Level (V_{OL}) ULPSMODE (Test ID: 28221)

- $\ensuremath{V_{OH}}$ and $\ensuremath{V_{OL}}$ values for low power signal measurements are performed and test results are stored.
- 2 The oscilloscope is triggered to capture rising and falling edges to be processed based on the "Number of ULPS Slew Edge" configuration in the **Configure** tab.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired waveform data prior to performing the actual slew rate measurement.
- 4 Perform the slew rate measurement on the mentioned triggered data for both Clkp and Clkn waveforms individually.

For falling edge,

- a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
- b. Perform the slew rate measurement across the 400mV 930mV region to determine the minimum slew rate result.

For rising edge,

- a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
- b. Perform the slew rate measurement across the 400mV 700mV region to determine the minimum slew rate result.
- c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV 930mV region.
- 5 Calculate the average value from all rising edges' maximum slew rate results. Calculate the average value from all falling edges' maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
- 6 Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
- 7 Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
- 8 The Slew Rate maximum, minimum and margin result values are stored.
- 9 Report the measurement results.
- 10 Compare the measured worst slew rate value for Clkp and Clkn to the compliance test limits.

Test References

See Test 1.2.5 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

| Part II Global Operation |
|-----------------------------|
| |



Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

15 MIPI D-PHY 1.1 Data Transmitter (Data TX) Global Operation Tests

Probing for Data TX Global Operation Tests / 230

Test 1.3.1 HS Entry: Data T_{I PX} Method of Implementation / 232

Test 1.3.2 HS Entry: Data TX $T_{HS-PREPARE}$ Method of Implementation / 232

Test 1.3.3 HS Entry: Data TX $T_{HS-PREPARE} + T_{HS-ZERO}$ Method of Implementation / 232

Test 1.3.13 HS Exit: Data TX $T_{HS-TRAIL}$ Method of Implementation / 232

Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{RFOT}) Method of Implementation / 232

Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation / 232 Test 1.3.16 HS Exit: Data TX $T_{HS-EXIT}$ Method of Implementation / 232

This section provides the Methods of Implementation (MOIs) for the Data Transmitter (Data TX) Global Operation tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.

MIPI D-PHY 1.1 Data TX Global Operation tests are the same as MIPI D-PHY 1.0 Data TX Global Operation tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 Data Transmitter (Data TX) Global Operation Tests"

The current chapter lists the references from the MIPI D-PHY 1.1 CTS.



Probing for Data TX Global Operation Tests

When performing the Data TX tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the Data TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Conformance Test Application for the exact number of probe connections.

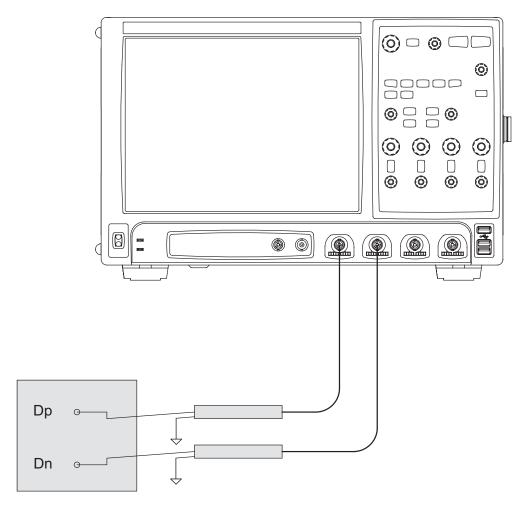


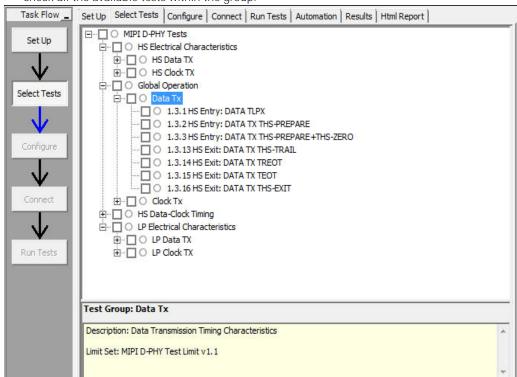
Figure 69 Probing for Data TX Global Operation Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 69 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, ZID (termination resistance) Device ID and User Comments.



4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

Figure 70 Selecting Data TX Global Operation Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.3.1 HS Entry: Data T_{I PX} Method of Implementation

Test References

See Test 1.3.1 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.3.2 HS Entry: Data TX T_{HS-PREPARE} Method of Implementation

Test References

See Test 1.3.2 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.3.3 HS Entry: Data TX T_{HS-PREPARE} + T_{HS-ZERO} Method of Implementation

Test References

See Test 1.3.3 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.3.13 HS Exit: Data TX T_{HS-TRAIL} Method of Implementation

Test References

See Test 1.3.13 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation

Test References

See Test 1.3.14 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.3.15 HS Exit: Data TX T_{FOT} Method of Implementation

Test References

See Test 1.3.15 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.3.16 HS Exit: Data TX T_{HS-EXIT} Method of Implementation

Test References

See Test 1.3.16 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

16 MIPI D-PHY 1.1 Clock Transmitter (Clock TX) Global Operation Tests

Probing for Clock TX Global Operation Tests / 234

Test 1.4.1 HS Entry: CLK TX T_{I PX} Method of Implementation / 236

Test 1.4.2 HS Entry: CLK TX $T_{CLK-PREPARE}$ Method of Implementation / 236

Test 1.4.3 HS Entry: CLK TX $T_{CLK-PREPARE} + T_{CLK-ZERO}$ Method of Implementation / 236

Test 1.5.1 HS Entry: CLK TX $T_{CLK-PRF}$ Method of Implementation / 236

Test 1.5.2 HS Exit: CLK TX $T_{CLK-POST}$ Method of Implementation / 236

Test 1.4.13 HS Exit: CLK TX $T_{CLK-TRAIL}$ Method of Implementation / 236

Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{RFOT}) Method of Implementation / 236

Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation / 236 Test 1.4.16 HS Exit: CLK TX $T_{HS-EXIT}$ Method of Implementation / 237

This section provides the Methods of Implementation (MOIs) for the Clock Transmitter (Clock TX) Global Operation tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.

MIPI D-PHY 1.1 Clock TX Global Operation tests are the same as MIPI D-PHY 1.0 Clock TX Global Operation tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 Clock Transmitter (Clock TX) Global Operation Tests"

The current chapter lists the references from the MIPI D-PHY 1.1 CTS.



Probing for Clock TX Global Operation Tests

When performing the Clock TX tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the Clock TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Conformance Test Application for the exact number of probe connections.

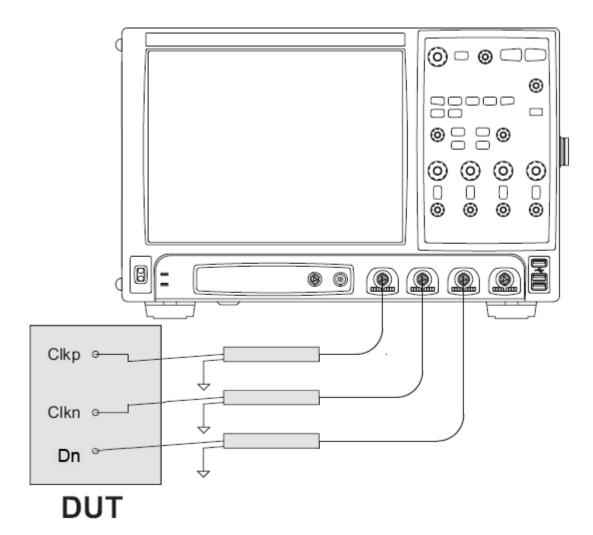


Figure 71 Probing for Clock TX Global Operation Tests

You can identify the channels used for each signal in the Configuration tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 71 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, ZID (termination resistance), Device ID and User Comments.
- 4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

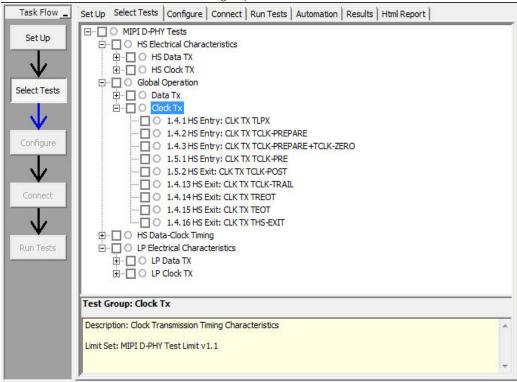


Figure 72 Selecting Clock TX Global Operation Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.1 HS Entry: CLK TX T_{I PX} Method of Implementation

Test References

See Test 1.4.1 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.4.2 HS Entry: CLK TX T_{CLK-PREPARE} Method of Implementation

Test References

See Test 1.4.2 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.4.3 HS Entry: CLK TX T_{CLK-PREPARE}+T_{CLK-ZERO} Method of Implementation

Test References

See Test 1.4.3 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.5.1 HS Entry: CLK TX T_{CLK-PRF} Method of Implementation

Test References

See Test 1.5.1 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.5.2 HS Exit: CLK TX T_{CLK-POST} Method of Implementation

Test References

See Test 1.5.2 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.4.13 HS Exit: CLK TX T_{CLK-TRAIL} Method of Implementation

Test References

See Test 1.4.13 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation

Test References

See Test 1.4.14 in CTS v1.1 and Section 9.1.2 Table 19 in the D-PHY Specification v1.1.

Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation

Test References

See Test 1.4.15 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

Test 1.4.16 HS Exit: CLK TX $T_{\mbox{HS-EXIT}}$ Method of Implementation

Test References

See Test 1.4.16 in CTS v1.1 and Section 6.9 Table 14 in the D-PHY Specification v1.1.

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Keysight U7238C/U7238D MIPI D-PHY Test App Methods of Implementation

17 MIPI D-PHY 1.1 High Speed (HS) Data-Clock Timing Tests

Probing for High Speed Data-Clock Timing Tests / 242
Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation / 244
Test 1.5.4 Data-to-Clock Skew (T_{SKEW(TX)}) Method of Implementation / 244

This section provides the Methods of Implementation (MOIs) for the High Speed (HS) Data-Clock Timing tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test App.

MIPI D-PHY 1.1 High Speed (HS) Data-Clock Timing tests are the same as MIPI D-PHY 1.0 High Speed (HS) Data-Clock Timing tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 High Speed (HS) Data-Clock Timing Tests"

The current chapter lists the references from the MIPI D-PHY 1.1 CTS.



Probing for High Speed Data-Clock Timing Tests

When performing the HS Data-Clock Timing tests, the MIPI D-PHY Test App will prompt you to make the proper connections. The connections for the HS Data-Clock Timing tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

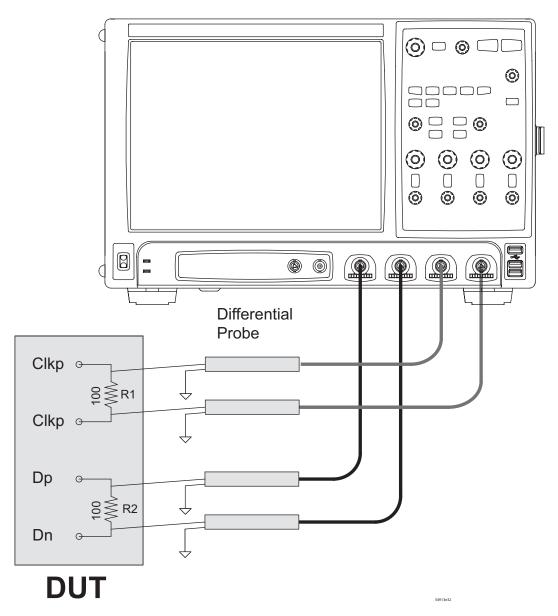


Figure 73 Probing for HS Data-Clock Timing Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test App. (The channels shown in Figure 73 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, ZID (termination resistance), Device ID and User Comments.
- 4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

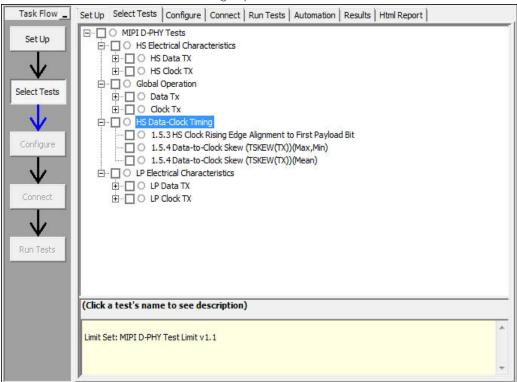


Figure 74 Selecting HS Data-Clock Timing Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation

Test References

See Test 1.5.3 in CTS v1.1 and Section 10.2 in the D-PHY Specification v1.1.

Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation

Test References

See Test 1.5.4 in CTS v1.1 and Section 10.2.1 Table 27 in the D-PHY Specification v1.1..

| | | Part IV Informative Tests |
|--|--|---------------------------|
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Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

18 MIPI D-PHY 1.1 Informative Tests

MIPI D-PHY 1.1 Informative tests are the same as MIPI D-PHY 1.0 Informative tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 Informative Tests"



| | | | | | | | | | | | | | | | | Part C MIPI D-PHY 1.2 |
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19 MIPI D-PHY 1.2 High Speed Data Transmitter (HS Data TX) Electrical Tests

Probing for High Speed Data Transmitter Electrical Tests / 254

Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation / 257

Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($DV_{CMTX}(1.0)$) Method of Implementation / 257

Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz ($DV_{CMTX}(HF)$) Method of Implementation / 257

Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz (DV $_{\rm CMTX}$ (LF)) Method of Implementation / 257

Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation / 257

Test 1.3.5 HS Data TX Differential Voltage Mismatch (DV_{OD}) Method of Implementation / 257

Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation / 257

Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation / 258

Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation / 261

This section provides the Methods of Implementation (MOIs) for the High Speed Data Transmitter (HS Data TX) Electrical tests using an Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test App.

MIPI D-PHY 1.2 HS Data TX tests are similar to the MIPI D-PHY 1.0 HS Data TX tests. Hence, most of the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 High Speed Data Transmitter (HS Data TX) Electrical Tests"

The current chapter lists the references from the MIPI D-PHY 1.2 CTS and describes the difference in the Method of Implementation from the corresponding MIPI D-PHY 1.0 test for the following tests:

"Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation"

"Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation"



Probing for High Speed Data Transmitter Electrical Tests

When performing the HS Data TX tests, the MIPI D-PHY Test App may prompt you to make changes to the physical setup. The connections for the HS Data TX tests may look similar to the following diagrams. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

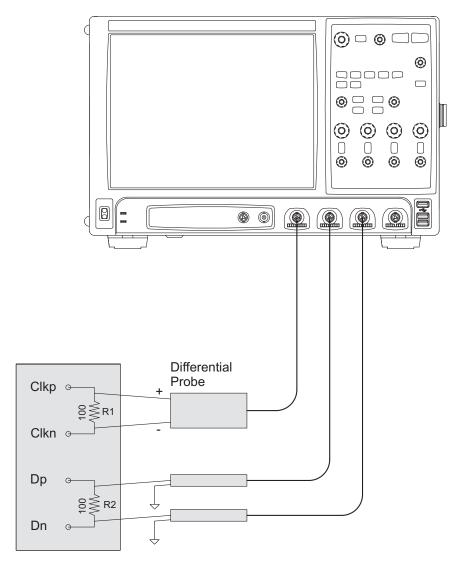


Figure 75 Probing with Three Probes for High Speed Data Transmitter Electrical Tests

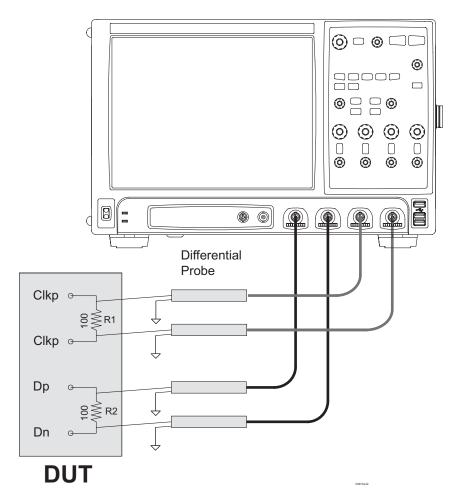


Figure 76 Probing with Four Probes for High Speed Data Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test App. (The channels shown in Figure 75 and Figure 76 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, Device ID and User Comments.
- 4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

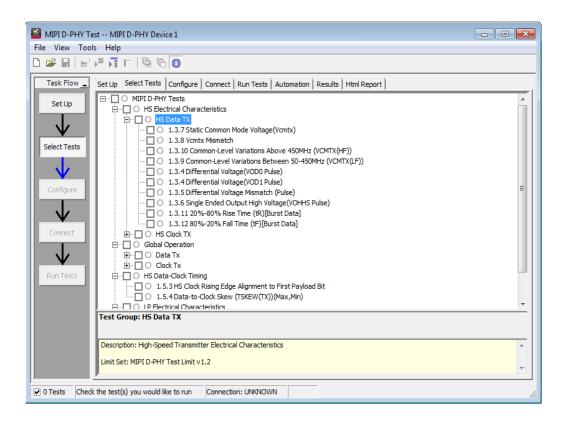


Figure 77 Selecting High Speed Data Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.3.7 HS Data TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation

Test References

See Test 1.3.7 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.8 HS Data TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1.0)}$) Method of Implementation

Test References

See Test 1.3.8 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.10 HS Data TX Common Level Variations Above 450 MHz ($\Delta V_{CMTX(HF)}$) Method of Implementation

Test References

See Test 1.3.10 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.9 HS Data TX Common Level Variations Between 50-450 MHz ($\Delta V_{CMTX(LF)}$) Method of Implementation

Test References

See Test 1.3.9 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.4 HS Data TX Differential Voltage (V_{OD}) Method of Implementation

Test References

See Test 1.3.4 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.5 HS Data TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation

Test References

See Test 1.3.5 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.6 HS Data TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation

Test References

See Test 1.3.6 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation

The rise time, t_R is defined as the transition time between 20% and 80% of the full HS signal swing. The driver must meet the t_R specifications for all the allowable Z_{ID} .

PASS Condition

The measured t_R value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 65 Test Availability Condition for Test 1.3.11

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 81101 | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 81102 | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 81104 | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled |
| 81105 | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled |

Measurement Algorithm using Test ID 81101

NOTE

Use the Test ID# 81101 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Entry: Data TX T_{HS-PREPARE} + T_{HS-ZERO} (Test ID: 558 for Test ID: 81101)

Actual value for V_{HS 7FRO} is measured and test results are stored.

- 2 Trigger on SoT of HS Data burst (LP11->LP01).
- 3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

DataDiff = Dp-Dn

4 Define the measurement threshold as follows:

Top Level: Inverse of V_{HS ZERO}

Base Level: V_{HS_ZERO}

- 5 Use a MATLAB script to identify and extract all the "000111" pattern locations found in the differential signal.
- 6 Measure the 20%-80% rise time at all the rising edges of the "000111" pattern that is identified.
- 7 Compare the measured t_R (Mean) value with the maximum conformance test limit.

Measurement Algorithm using Test ID 81102

NOTE

Use the Test ID# 81102 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (Ul_{inst})[Max] (Test ID: 911)
 UI value measurements for test signal are performed and test results are stored.
 - b HS Data TX Differential Voltage (V_{OD}) (Test ID: 8131, 8132) Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
- 2 Trigger on SoT of HS Continuous Data.
- 3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

DataDiff = Dp-Dn

4 Define the measurement threshold as follows:

Top Level: V_{OD1} (V_{OD} for Differential-1)

Base Level: V_{OD0} (V_{OD} for Differential-0)

- 5 Use a MATLAB script to identify and extract all the "000111" pattern locations found in the differential signal.
- 6 Measure the 20%-80% rise time at all the rising edges of the "000111" pattern that is identified.
- 7 Compare the measured t_R (Mean) value with the maximum conformance test limit.

Measurement Algorithm using Test ID 81104

NOTE

Use the Test ID# 81104 to remotely access the test.

This test is an informative test.

- 1 This test requires the following prerequisite test:
 - Data Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 81101)
 Rise time measurements are performed and t_R (Mean) test result is stored.
- 2 Compare the measured t_R (Mean) value with the minimum conformance test limits.

Measurement Algorithm using Test ID 81105

NOTE

Use the Test ID# 81105 to remotely access the test.

This test is an informative test.

- 1 This test requires the following prerequisite test:
 - a Data Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 81102) Rise time measurements are performed and t_R (Mean) test result is stored.
- 2 Compare the measured t_R (Mean) value with the minimum conformance test limits.

Test References

See Test 1.3.11 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation

The fall time, t_F is defined as the transition time between 80% and 20% of the full HS signal swing. The driver must meet the t_F specifications for all the allowable Z_{ID} .

PASS Condition

The measured t_F value for the test signal must be within the conformance limit as specified in the CTS section mentioned under Test References section.

Test Availability Condition

Table 66 Test Availability Condition for Test 1.3.12

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 81111 | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 81112 | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 81114 | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled |
| 81115 | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled |

Measurement Algorithm using Test ID 81111

NOTE

Use the Test ID# 81111 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Entry: Data TX T_{HS-PREPARE} + T_{HS-ZERO} (Test ID: 558 for Test ID: 81111)

Actual value for V_{HS 7FRO} is measured and test results are stored.

- 2 Trigger on SoT of the HS Data burst (LP11->LP01).
- 3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

DataDiff = Dp-Dn

4 Define the measurement threshold as follows:

Top Level: Inverse of V_{HS ZERO}

Base Level: V_{HS_ZERO}

- 5 Use a MATLAB script to identify and extract all the "111000" pattern locations found in the differential signal.
- 6 Measure the 80%-20% fall time at all the falling edges of the "111000" pattern that is identified.
- 7 Compare the measured value of t_E (Mean) with the maximum conformance test limit.

Measurement Algorithm using Test ID 81112

NOTE

Use the Test ID# 81112 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (Ul_{inst})[Max] (Test ID: 911)
 UI value measurements for test signal are performed and test results are stored.
 - b HS Data TX Differential Voltage (V_{OD}) (Test ID: 8131, 8132) Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
- 2 Trigger on SoT of HS Continuous Data.
- 3 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform using the following equation:

Data_{Diff} = Dp-Dn

4 Define the measurement threshold as follows:

Top Level: V_{OD1} (V_{OD} for Differential-1)

Base Level: V_{OD0} (V_{OD} for Differential-0)

- 5 Use a MATLAB script to identify and extract all the "111000" pattern locations found in the differential signal.
- 6 Measure the 80%-20% fall time at all the falling edges of the "111000" pattern that is identified.
- 7 Compare the measured t_F (Mean) value with the maximum conformance test limit.

Measurement Algorithm using Test ID 81114

NOTE

Use the Test ID# 81114 to remotely access the test.

This test is an informative test.

- 1 This test requires the following prerequisite test:
 - a Data Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 81111) Fall time measurements are performed and t_F (Mean) test result is stored.
- 2 Compare the measured t_F (Mean) value with the minimum conformance test limits.

Measurement Algorithm using Test ID 81115

NOTE

Use the Test ID# 81115 to remotely access the test.

This test is an informative test.

- 1 This test requires the following prerequisite test:
 - a Data Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 81112) Fall time measurements are performed and t_F (Mean) test result is stored.
- 2 Compare the measured t_F (Mean) value with the minimum conformance test limits.

Test References

See Test 1.3.12 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

20 MIPI D-PHY 1.2 High Speed Clock Transmitter (HS Clock TX) Electrical Tests

Probing for High Speed Clock Transmitter Electrical Tests / 267

Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation / 269

Test 1.4.8 HS Clock TX VCMTX Mismatch (DV_{CMTX}(1,0)) Method of Implementation / 269

Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz ($DV_{CMTX}(HF)$) Method of Implementation / 269

Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz ($DV_{CMTX}(LF)$) Method of Implementation / 269

Test 1.4.4 HS Clock TX Differential Voltage (V_{OD}) Method of Implementation / 269

Test 1.4.5 HS Clock TX Differential Voltage Mismatch (DV_{OD}) Method of Implementation / 269

Test 1. 4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation / 269

Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation / 270

Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation / 273

Test 1.4.17 HS Clock Instantaneous Method of Implementation / 276

Test 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Method of Implementation / 277

This section provides the Methods of Implementation (MOIs) for the High Speed Clock Transmitter (HS Clock T_X) Electrical tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.

MIPI D-PHY 1.2 HS Clock TX tests are similar to the MIPI D-PHY 1.0 HS Clock TX tests. Hence, they share the same Method of Implementation (MOI) as many of the corresponding MIPI D-PHY 1.0 tests. There is, however, an additional test that is supported by MIPI D-PHY 1.2 and not by MIPI D-PHY 1.0. Also, two tests have different methods of implementation from the corresponding MIPI D-PHY 1.0 tests. The current chapter describes these tests and lists the references from the MIPI D-PHY 1.2 CTS.

"Test 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Method of Implementation" (Not in MIPI D-PHY 1.0)
"Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation" (Different from MIPI D-PHY 1.0)

"Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation" (Different from MIPI D-PHY 1.0)



For details of MIPI D-PHY 1.0 tests, refer to "MIPI D-PHY 1.0 High Speed Clock Transmitter (HS Clock TX) Electrical Tests"

Probing for High Speed Clock Transmitter Electrical Tests

When performing the HS Clock T_x tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the HS Clock T_X tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

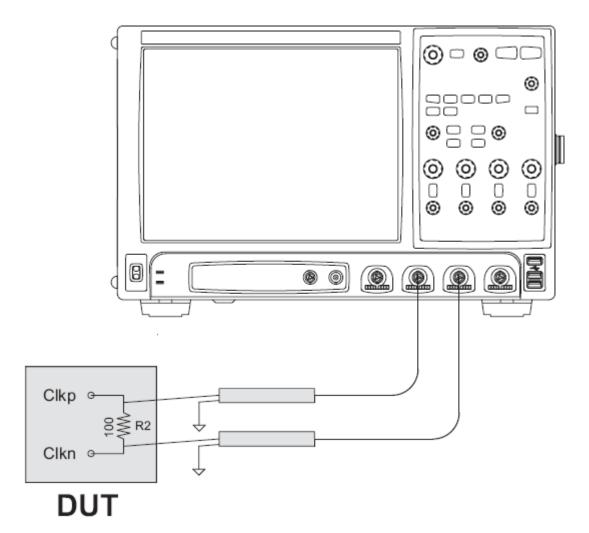


Figure 78 Probing for High Speed Clock Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 78 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

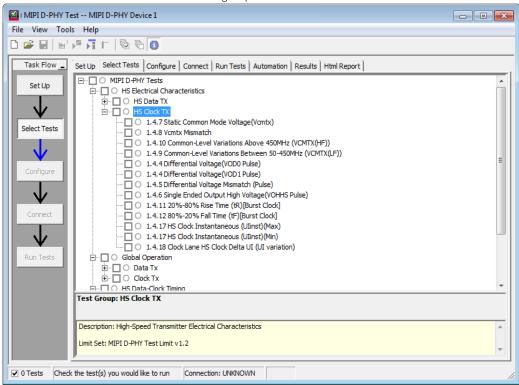


Figure 79 Selecting High Speed Clock Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.7 HS Clock TX Static Common Mode Voltage (V_{CMTX}) Method of Implementation

Test References

See Test 1.4.7 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.8 HS Clock TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1.0)}$) Method of Implementation

Test References

See Test 1.4.8 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.10 HS Clock TX Common-Level Variations Above 450 MHz ($\Delta V_{CMTX(HF)}$) Method of Implementation

Test References

See Test 1.4.10 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.9 HS Clock TX Common-Level Variations Between 50-450 MHz ($\Delta V_{CMTX(LF)}$) Method of Implementation

Test References

See Test 1.4.9 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.4 HS Clock TX Differential Voltage (V_{OD}) Method of Implementation

Test References

See Test 1.4.4 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.5 HS Clock TX Differential Voltage Mismatch (ΔV_{OD}) Method of Implementation

Test References

See Test 1.4.5 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1. 4.6 HS Clock TX Single-Ended Output High Voltage (V_{OHHS}) Method of Implementation

Test References

See Test 1.4.6 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R) Method of Implementation

The rise time, t_R is defined as the transition time between 20% and 80% of the full HS signal swing. The driver must meet the t_R specifications for all allowable Z_{ID} .

PASS Condition

The measured t_R value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 67 Test Availability Condition for Test 1.4.11

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------------------------------------------|-------------------------------------------------------|-----------------------|------------------------|--------------------|---------------------|
| 181101 | Not Applicable | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 181102 | Not Applicable | Disabled | Dependency on Continuous Data option setting | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 181103 | Not Applicable | Dependency on Continuous Clock option setting | Enabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 181104 | Not Applicable | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Enabled |
| 181105 | Not Applicable | Disabled | Dependency on Continuous Data option setting | Not Applicable | Not Applicable | Not Applicable | Enabled |
| 181106 | Not Applicable | Dependency on Continuous Clock option setting | Enabled | Not Applicable | Not Applicable | Not Applicable | Enabled |

Measurement Algorithm using Test ID 181101

NOTE

Use the Test ID# 181101 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (Ulinst) [Max] (Test ID: 911)

Measure the UI value for the test signal and test results are stored.

b HS Entry: CLK TX T_{CLK-PREPARE} + T_{CLK-ZERO} (Test ID: 554)

Measure the actual value of $V_{HS\ ZERO}$ and the test results are stored.

- 2 Trigger the oscilloscope to acquire Clkp and Clkn.
- 3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: Inverse of V_{HS_ZERO}

Base Level: V_{HS_ZERO}

- 5 Use a MATLAB script to identify and extract all "01" pattern locations found in the differential signal.
- 6 Measure the 20%-80% rise time at all rising edges of the "01" pattern that is identified.
- 7 Compare the value of the measured t_R (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181102

NOTE

Use the Test ID# 181102 to remotely access the test.

- 1 This test requires the following prerequisite test:
 - a Data Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 81101) Measure the actual value of $V_{HS\ ZERO}$ and the test results are stored.
- 2 Trigger the oscilloscope to acquire Clkp and Clkn.
- 3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: Inverse of V_{HS ZERO}

Base Level: V_{HS ZERO}

- 5 Use a MATLAB script to identify and extract all "01" pattern locations found in the differential signal.
- 6 Measure the 20%-80% rise time at all rising edges of the "01" pattern that is identified.
- 7 Compare the value of the measured t_R (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181103

NOTE

Use the Test ID# 181103 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (Ul_{inst})[Max] (Test ID: 911)
 UI value measurements for test signal are performed and test results are stored.
 - b HS Clock T_X Differential Voltage (V_{OD}) (Test ID: 18131, 18132)
 Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
- 2 Trigger the oscilloscope to acquire Clkp and Clkn.
- 3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: V_{OD1} (V_{OD} for Differential-1)

Base Level: V_{OD0} (V_{OD} for Differential-0)

- 5 Use a MATLAB script to identify and extract all "01" pattern locations found in the differential signal.
- 6 Measure the 20%-80% rise time at all rising edges of the "01" pattern that is identified.
- 7 Compare the value of the measured t_R (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181104

NOTE

Use the Test ID# 181104 to remotely access the test.

This test is an informative test.

- 1 This test requires the following prerequisite test:
 - a Clock Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 181101) Rise time measurements are performed and t_R (Mean) test result is stored.
- 2 Compare the value of the measured t_R (Mean) with the minimum compliance test limits.

Measurement Algorithm using Test ID 181105

NOTE

Use the Test ID# 181105 to remotely access the test.

This test is an informative test.

- 1 This test requires the following prerequisite test:
 - a Clock Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 181102) Rise time measurements are performed and t_R (Mean) test result is stored.
- 2 Compare the value of the measured t_R (Mean) with the minimum compliance test limits.

Measurement Algorithm using Test ID 181106

NOTE

Use the Test ID# 181106 to remotely access the test.

This test is an informative test.

- 1 This test requires the following prerequisite test:
 - a Clock Lane HS-TX 20%-80% Rise Time (t_R) (Test ID: 181103) Rise time measurements are performed and t_R (Mean) test result is stored.
- 2 Compare the value of the measured t_R (Mean) with the minimum compliance test limits.

Test References

See Test 1.4.11 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F) Method of Implementation

The fall time, t_F is defined as the transition time between 80% and 20% of the full HS signal swing. The driver must meet the t_F specifications for all allowable Z_{ID} .

PASS Condition

The measured t_F value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 68 Test Availability Condition for Test 1.4.12

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------------------------------------------|-------------------------------------------------------|-----------------------|------------------------|--------------------|---------------------|
| 181111 | Not Applicable | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 181112 | Not Applicable | Disabled | Dependency on Continuous Data option setting | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 181113 | Not Applicable | Dependency on Continuous Clock option setting | Enabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 181114 | Not Applicable | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable | Enabled |
| 181115 | Not Applicable | Disabled | Dependency on Continuous Data option setting | Not Applicable | Not Applicable | Not Applicable | Enabled |
| 181116 | Not Applicable | Dependency on Continuous Clock option setting | Enabled | Not Applicable | Not Applicable | Not Applicable | Enabled |

Measurement Algorithm using Test ID 181111

NOTE

Use the Test ID# 181111 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.

b HS Entry: CLK TX T_{CLK-PREPARE} + T_{CLK-ZERO} (Test ID: 554)

Measure the actual value of $V_{\mbox{\scriptsize HS}}$ ZERO and the test results are stored.

- 2 Trigger the oscilloscope to acquire Clkp and Clkn.
- 3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: Inverse of V_{HS_ZERO}

Base Level: V_{HS ZERO}

- 5 Use a MATLAB script to identify and extract all "10" pattern locations found in the differential signal.
- 6 Measure the 80%-20% fall time at all falling edges of the "10" pattern that is identified.
- 7 Compare the value of the measured t_F (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181112

NOTE

Use the Test ID# 181112 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a Data Lane HS-TX 80%-20% Fall Time ($t_{\rm F}$) (Test ID: 81111) Measure the actual value of $V_{\rm HS}$ $_{\rm TFRO}$ and the test results are stored.
- 2 Trigger the oscilloscope to acquire Clkp and Clkn.
- 3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: Inverse of V_{HS ZERO}

Base Level: V_{HS_ZERO}

- 5 Use a MATLAB script to identify and extract all "10" pattern locations found in the differential signal.
- 6 Measure the 80%-20% fall time at all falling edges of the "10" pattern that is identified.
- 7 Compare the value of the measured t_F (Mean) with the maximum compliance test limit.

Measurement Algorithm using Test ID 181113

NOTE

Use the Test ID# 181113 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (Ul_{inst})[Max] (Test ID: 911)
 UI value measurements for test signal are performed and test results are stored.
 - b HS Clock T_X Differential Voltage (V_{OD}) (Test ID: 18131, 18132) Actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
- 2 Trigger the oscilloscope to acquire Clkp and Clkn.
- 3 Construct differential waveform by using the following equation:

ClkDiff = Clkp-Clkn

4 Define the measurement threshold as:

Top Level: V_{OD1} (V_{OD} for Differential-1)

Base Level: V_{OD0} (V_{OD} for Differential-0)

- 5 Use a MATLAB script to identify and extract all "10" pattern locations found in the differential signal.
- 6 Measure the 80%-20% fall time at all falling edges of the "10" pattern that is identified.
- 7 Compare the value of the measured t_F (Mean) with the maximum compliance test limits.

Measurement Algorithm using Test ID 181114

NOTE

Use the Test ID# 181114 to remotely access the test.

This test is an informative test.

- 1 This test requires the following prerequisite test:
 - a Clock Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 181111) Fall time measurements are performed and t_F (Mean) test result is stored.
- 2 Compare the value of the measured t_E (Mean) with the minimum compliance test limits.

Measurement Algorithm using Test ID 181115

NOTE

Use the Test ID# 181115 to remotely access the test.

This test is an informative test.

- 1 This test requires the following prerequisite test:
 - a Clock Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 181112) Fall time measurements are performed and t_F (Mean) test result is stored.
- 2 Compare the value of the measured t_F (Mean) with the minimum compliance test limits.

Measurement Algorithm using Test ID 181116

NOTE

Use the Test ID# 181116 to remotely access the test.

This test is an informative test.

- 1 This test requires the following prerequisite test:
 - a Clock Lane HS-TX 80%-20% Fall Time (t_F) (Test ID: 181113) Fall time measurements are performed and t_F (Mean) test result is stored.
- 2 Compare the value of the measured t_F (Mean) with the minimum compliance test limits.

Test References

See Test 1.4.12 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.17 HS Clock Instantaneous Method of Implementation

Test References

See Test 1.4.17 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Method of Implementation

Clock Lane HS Clock Delta UI (UI variation) verifies that the frequency stability of the DUT HS Clock during a signal burst is within the conformance limits.

PASS Condition

The measured UI variation must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 69 Test Availability Condition for Test 1.4.18

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 1911 | <=1.5Gbps | Not Applicable |

Measurement Algorithm using Test ID 1911

NOTE

Use the Test ID# 1911 to remotely access the test.

- 1 This test requires the following prerequisite test(s).
 - a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)

The minimum, maximum and average Unit Interval of the differential clock waveform is measured and stored.

2 Calculate the UI_Variant_min and UI_Variant_max according to the following equation:

UI_Variant_min = ((Ulinst_min - Uiinst_mean) / Ulinst_mean) * 100%

UI_Variant_max = ((Ulinst_max - Uiinst_mean) / Ulinst_mean) * 100%

- 3 Determine the UI_variant_worst based on the UI_Variant_min and UI_Variant_max calculated above.
- 4 Compare the worst measured value of UI_variant_worst with the conformance limit.

Test References

See Test 1.4.18 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

21 MIPI D-PHY 1.2 Low Power Data Transmitter (LP Data TX) Electrical Tests

Probing for Low Power Transmitter Electrical Tests / 280

Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation / 282

Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation / 284

Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation / 286

Test 1.1.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation / 287

Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock (T_{LP-PULSE-TX}) Method of Implementation / 289

Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock (T_{LP-PFR-TX}) Method of Implementation / 292

Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation / 294

This section provides the Methods of Implementation (MOIs) for the Low Power Data Transmitter (LP Data TX) Electrical tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.



Probing for Low Power Transmitter Electrical Tests

When performing the LP TX tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the LP TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Conformance Test Application for the exact number of probe connections.

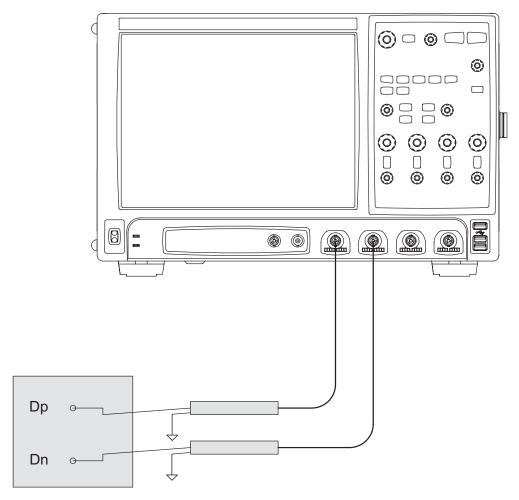


Figure 80 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 80 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

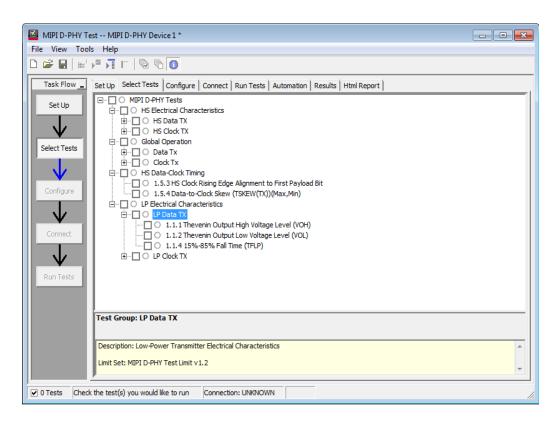


Figure 81 Selecting Low Power Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.1.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation

V_{OH} is the Thevenin output high-level voltage in the high-level state, when the pad pin is not loaded.

PASS Condition

The measured V_{OH} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 70 Test Availability Conditions for Test 1.1.1

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 821 | Not Applicable | Disabled | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable |
| 8211 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 821

LP TX Thevenin Output High Voltage Level (V_{OH})



Ensure that **Data LP EscapeMode** is disabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 821 to remotely access the test.

- 1 Trigger the Dp's LP rising edge.
- 2 Position the trigger point at the center of the screen and make sure that the stable Dp LP high level voltage region is visible on the screen.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
- 4 Accumulate the data using the persistent display mode.
- 5 Enable the **Histogram** feature and measure the entire display region after the trigger location.
- 6 Take the mode value from the Histogram and use this value as V_{OH} for Dp.
- 7 Repeat steps 1 to 6 for Dn.
- 8 Report the measurement results.
 - a V_{OH} value for Dp channel
 - b V_{OH} value for Dn channel
- 9 Compare the measured worst value of V_{OH} with the compliance test limits.

LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8211 to remotely access the test.

- 1 Trigger on LP Data EscapeMode pattern on the data signal. Without the presence of LP Escape mode, the trigger is unable to capture any valid signal for data processing.
- 2 Locate and use the Mark-1 state pattern to determine the end of the EscapeMode sequence.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired EscapeMode sequence waveform data.
- 4 Enable the **Histogram** feature and measure the entire LP Data EscapeMode sequence.
- 5 Take the mode value from the **Histogram** and use this value as V_{OH} for Dp.
- 6 Repeat steps 1 to 5 for Dn.
- 7 Report the measurement results.
 - a V_{OH} value for Dp channel
 - b V_{OH} value for Dn channel
- 8 Compare the measured worst value of V_{OH} with the conformance test limits.

Test References

See Test 1.1.1 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.1.2 LP TX Thevenin Output Low Voltage Level (V_{OI}) Method of Implementation

 V_{OL} is the Thevenin output low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low level state.

PASS Condition

The measured V_{OL} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 71 Test Availability Condition for Test 1.1.2

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 822 | Not Applicable | Disabled | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable |
| 8221 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 822

LP TX Thevenin Output Low Voltage Level (V_{OL})



Ensure that **Data LP EscapeMode** is disabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 822 to remotely access the test.

- 1 This test requires the following prerequisite test(s):
 - a HS Entry: DATA TX T_{HS-PREPARE} (Test ID: 557)
- 2 Trigger the Dp's LP falling edge.
- 3 Position the trigger point at the center of the screen and make sure that the stable Dp LP low level voltage region is visible on the screen.
- 4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
- 5 Accumulate the data by using the persistent display mode.
- 6 Enable the **Histogram** feature and measure the entire display region after the trigger location.
- 7 Take the mode value from the Histogram and use this value as V_{OL} for Dp.
- 8 Repeat steps 1 to 7 for Dn.
- 9 Report the measurement results:
 - a VOI value for Dp channel
 - b V_{OL} value for Dn channel
- 10 Compare the measured worst value of V_{OL} with the conformance test limits.

LP TX Thevenin Output Low Voltage Level (VOL) ESCAPEMODE

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8221 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
- 2 Trigger on LP Data EscapeMode pattern on the data signal. Without the presence of the LP Escape mode, the trigger is unable to capture any valid signal for data processing.
- 3 Locate and use the Mark -1 state pattern to determine the end of the EscapeMode sequence.
- 4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired EscapeMode sequence waveform data.
- 5 Enable the **Histogram** feature and measure the entire LP data EscapeMode sequence.
- 6 Take the mode value from the Histogram and use this value as V_{OL} for Dp.
- 7 Repeat steps 1 to 6 for Dn.
- 8 Report the measurement results:
 - a V_{OI} value for Dp channel
 - b V_{OL} value for Dn channel
- 9 Compare the measured worst value of V_{OL} with the conformance test limits.

Test References

See Test 1.1.2 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.1.3 LP TX 15%-85% Rise Time Level (T_{RLP}) EscapeMode Method of Implementation

The T_{RLP} is defined as 15%-85% rise time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD} . The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{RLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 72 Test Availability Condition for Test 1.1.3

| Associated | High-Speed Data | Continuous | Continuous | Data LP | Clock LP | Clock ULPS | Informative |
|------------|-----------------|------------|----------------|------------|----------------|----------------|----------------|
| Test ID | Rate | Data | Clock | EscapeMode | EscapeMode | Mode | Test |
| 8241 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 8241

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8241 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
 - b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221)

 $\rm V_{OH}$ and $\rm V_{OL}$ values for Low Power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 A 400 MHz, 4th-order Butterworth low pass test filter is applied to the mentioned EscapeMode sequence data prior to performing the actual rise time measurement.
- 4 All the rising edges in the filtered EscapeMode sequence are processed in measuring the corresponding rise time.
- 5 The average 15%-85% rise time for Dp is recorded.
- 6 Repeat the steps for Dn.
- 7 Report the measurement results:
 - a T_{RIP} average value for Dp channel
 - b T_{RLP} average value for Dn channel
- 8 Compare the measured T_{RLP} worst value with the compliance test limit.

Test References

See Test 1.1.3 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.1.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation

The T_{FLP} is defined as 15%-85% fall time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD} . The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{FLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 73 Test Availability Condition for Test 1.1.4

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 825 | Not Applicable | Disabled | Not Applicable | Disabled | Not Applicable | Not Applicable | Not Applicable |
| 8251 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 825

LP TX 15%-85% Fall Time (T_{FLP})



Ensure that **Data LP EscapeMode** is disabled on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY test application. Use the Test ID# 825 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) (Test ID: 821)
 - b LP TX Thevenin Output Low Voltage Level (V_{OI}) (Test ID: 822)

Measure the V_{OH} and V_{OI} values for the low power signal and test results are stored.

- 2 All falling edges in LP are valid for this measurement.
- 3 Setup the trigger on LP falling edges.
- 4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
- 5 Depending on the number of observation configuration, the oscilloscope is triggered accordingly.
- 6 The average 15%-85% fall time for Dp is recorded.
- 7 Repeat the same trigger steps for Dn.
- 8 Report the measurement results:
 - a T_{FLP} average value for Dp channel
 - b T_{FLP} average value for Dn channel
- 9 Compare the measured worst value of T_{FLP} with the compliance test limits.

LP TX 15%-85% Fall Time (T_{FLP}) ESCAPEMODE

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8251 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
 - b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221) Measure the V_{OH} and V_{OI} values for the low power signal and test results are stored.
- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to measuring the actual fall time.
- 4 All falling edges in the filtered EscapeMode sequence are processed in measuring the corresponding fall time.
- 5 The average 15%-85% fall time for Dp is recorded.
- 6 Repeat steps 1 to 5 for Dn.
- 7 Report the measurement results:
 - a T_{FLP} average value for Dp channel
 - b T_{FLP} average value for Dn channel
- 8 Compare the measured worst value of T_{FLP} with the compliance test limits.

Test References

See Test 1.1.4 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.1.6 LP TX Pulse Width of LP TX Exclusive-Or Clock ($T_{LP-PULSE-TX}$) Method of Implementation

 $T_{LP-PULSE-TX}$ is defined as the pulse width of the DUT Low-Power TX XOR clock. A graphical representation of the XOR operation that creates the LP clock is shown below. The D-PHY Standard actually separates the $T_{LP-PULSE-TX}$ specification into two parts:

- a The first LP XOR clock pulse after a Stop state, or the last LP XOR clock pulse before a Stop state must be wider than 40ns.
- b All other LP XOR clock pulses must be wider than 20ns.

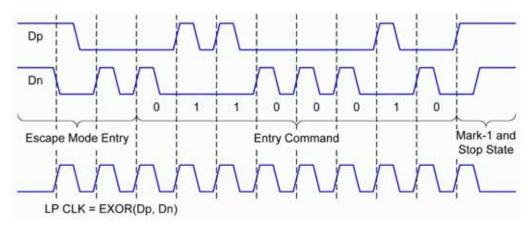


Figure 82 Graphical Representation of the XOR Operation

PASS Condition

The measured $T_{LP-PULSE-TX}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 74 Test Availability Condition for Test 1.1.6

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 827 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 8271 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 8272 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Enabled |
| 1827 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 18271 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 18272 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Enabled |

Measurement Algorithm using Test IDs 827, 8271 and 8272

LP TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX})

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 827 to remotely access the test.

LP TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX}) [Initial]

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8271 to remotely access the test.

LP TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$) [Last]

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 8272 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - *a* LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211). This is to trigger and capture an EscapeMode sequence data from the test signal.
- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data.
- 4 Find all crossing points at the minimum trip level (500mV) and the maximum trip level (930mV for data rates that are less than or equal to 1.5 Gbps or 790mV for data rates greater than 1.5 Gbps) for Dp and Dn individually.
- 5 Find the initial pulse width, last pulse width and minimum width of all the other pulses at the specified minimum trip level and maximum trip level.
- 6 Find the rising-to-rising and falling-to-falling periods of the XOR clock at the mentioned minimum trip level and maximum trip level.
- 7 The worst case value for the pulse width found between the minimum trip level and maximum trip level will be used as the T_{I P-PULSE-TX} value.
- 8 Compare the measured minimum $T_{LP-PULSE-TX}$ value with the compliance test limits.

Measurement Algorithm using Test IDs 1827, 18271 and 18272

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$)

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 1827 to remotely access the test.

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX}) [Initial]

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 18271 to remotely access the test.

LP Clock TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX}) [Last]

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 18272 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - *a* LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211) This is to trigger and capture an EscapeMode sequence data from the test signal.
- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data.
- 4 Find all crossing points at the minimum trip level (500mV) and the maximum trip level (930mV for data rates that are less than or equal to 1.5 Gbps or 790mV for data rates greater than 1.5 Gbps) for Clkp and Clkn individually.
- 5 Find the initial pulse width, last pulse width and minimum width of all the other pulses at the specified minimum trip level and maximum trip level.
- 6 Find the rising-to-rising and falling-to-falling periods of the XOR clock at the specified minimum trip level and maximum trip level.
- 7 The worst case value for the pulse width found between the minimum trip level and maximum trip level is used as the $T_{LP-PULSE-TX}$ value.
- 8 Compare the measured minimum T_{LP-PULSF-TX} value with the compliance test limits.

Test References

See Test 1.1.6 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.1.7 LP TX Period of LP TX Exclusive-OR Clock (T_{LP-PFR-TX}) Method of Implementation

 $T_{LP\text{-}PER\text{-}TX}$ is defined as the period of the DUT Low-Power TX XOR clock. A graphical representation of the XOR operation that creates the LP clock is shown below. The D-PHY Standard separates the $T_{LP\text{-}PULSE\text{-}TX}$ specification into two parts:

- a The first LP XOR clock pulse after a Stop state, or the last LP XOR clock pulse before a Stop state must be wider than 40ns.
- b All other LP XOR clock pulses must be wider than 20ns.

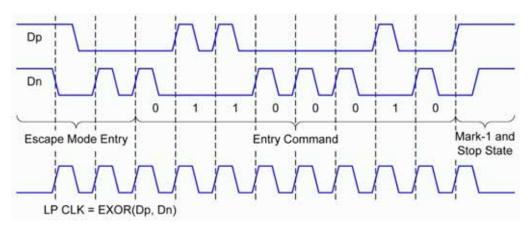


Figure 83 Graphical Representation of the XOR Operation

PASS Condition

The measured $T_{LP-PER-TX}$ value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 75 Test Availability Condition for Test 1.1.7

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 828 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 1828 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |

LP TX Period of LP TX Exclusive-OR Clock (T_{LP-PER-TX})

NOTE

Select Data LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 828 to remotely access the test.

- 1 This test requires the following prerequisite test(s).
 - a LP TX Pulse Width of LP TX Exclusive-OR Clock (T_{LP-PULSE-TX}) (Test ID: 827)
 - The actual measurement algorithm of the $T_{LP-PER-TX}$ is performed in the mentioned prerequisite test
- 2 The minimum value for all the rising-to-rising and falling-to-falling periods of the XOR clock at the minimum trip level (500mV) and the maximum trip level (930mV for data rates that are less than or equal to 1.5 Gbps or 790mV for data rates greater than 1.5 Gbps) is used as the $T_{I,P-PFR-TX}$ result.
- 3 Compare the measured minimum T_{LP-PFR-TX} value to the compliance test limits.

Measurement Algorithm using Test ID 1828

LP Clock TX Period of LP TX Exclusive-OR Clock (T_{LP-PER-TX})

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY test application to enable this test. Use the Test ID# 1828 to remotely access the test.

- 1 This test requires the following prerequisite test(s).
 - a LP Clock TX Pulse Width of LP TX Exclusive-OR Clock ($T_{LP-PULSE-TX}$) (Test ID: 1827) The actual measurement algorithm of the $T_{LP-PER-TX}$ is performed in the mentioned prerequisite test.
- The minimum value for all the rising-to-rising and falling-to-falling periods of the XOR clock at the minimum trip level (500mV) and the maximum trip level (930mV for data rates that are less than or equal to 1.5 Gbps or 790mV for data rates greater than 1.5 Gbps) is used as the T_{LP-PER-TX} result.
- 3 Compare the measured minimum T_{IP-PFR-TX} value with the compliance test limits.

Test References

See Test 1.1.7 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.1.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation

The slew rate δ V/ δ t_{SR} is the derivative of the LP transmitter output signal voltage over time. The intention of specifying a maximum slew rate value in the specification is to limit EMI (Electro Magnetic Interference).

The specification also states that the Slew Rate must be measured as an average across any 50mV segment of the output signal transition.

PASS Condition

The measured slew rate δ V/ δ t_{SR} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 76 Test Availability Condition for Test 1.1.5

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 829 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 8291 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |
| 8292 | Not Applicable | Disabled | Not Applicable | Enabled | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test IDs 829, 8291 and 8292

NOTE

Select **Data LP EscapeMode** on the **Device Information** section of the **Set Up** tab of the MIPI D-PHY Test application to enable this test.

- To access the LP TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 829.
- To access the LP TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 8291.
- To access the LP TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 8292.
- 1 This test requires the following prerequisite tests:
 - a LP TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 8211)
 - b LP TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 8221)

 $\mbox{V}_{\mbox{OH}}$ and $\mbox{V}_{\mbox{OL}}$ values for low power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual slew rate measurement.
- 4 Perform the slew rate measurement on the filtered EscapeMode sequence for both Dp and Dn waveforms individually.

For falling edge,

- a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result
- b. Perform the slew rate measurement across the 400mV 930mV region for data rate <= 1.5 Gbps OR 400mV 790mV region for data rate > 1.5 Gbps to determine the minimum slew rate result.

For rising edge,

a. Perform the slew rate measurement across entire signal edge to determine the maximum slew

rate result.

- b. Perform the slew rate measurement across the 400mV 700mV region for data rate <= 1.5 Gbps OR 400mV 550mV region for data rate > 1.5 Gbps to determine the minimum slew rate result
- c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV 930mV region for data rate <= 1.5 Gbps OR 550mV 790mV region for data rate > 1.5 Gbps.
- 5 Calculate the average value from all rising edges' maximum slew rate results. Calculate the average value from all falling edges' maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
- 6 Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
- 7 Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
- 8 The Slew Rate maximum, minimum and margin result values are stored.
- 9 Report the measurement results.
- 10 Compare the measured slew rate results with the conformance test limits.

Test References

See Test 1.1.5 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

21 MIPI D-PHY 1.2 Low Power Data Transmitter (LP Data TX) Electrical Tests

22 MIPI D-PHY 1.2 Low Power Clock Transmitter (LP Clock TX) Electrical Tests

Probing for Low Power Transmitter Electrical Tests / 298

Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation / 300

Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation / 302

Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation $\,/\,$ 305

Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation / 307

Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation / 310

This section provides the Methods of Implementation (MOIs) for the Low Power Clock Transmitter (LP Clock TX) Electrical tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test App.



Probing for Low Power Transmitter Electrical Tests

When performing the LP TX tests, the MIPI D-PHY Test App will prompt you to make the proper connections. The connections for the LP TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test App for the exact number of probe connections.

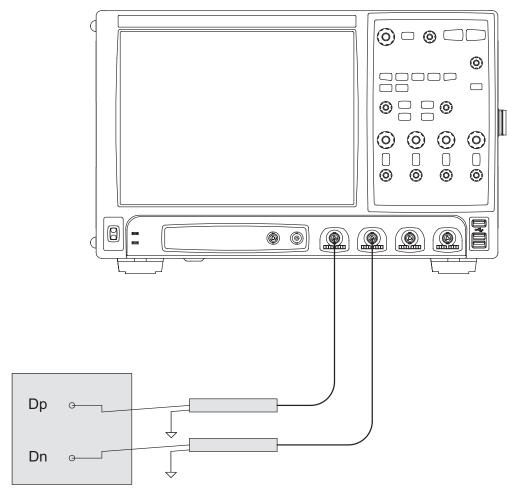


Figure 84 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test App. (The channels shown in Figure 84 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

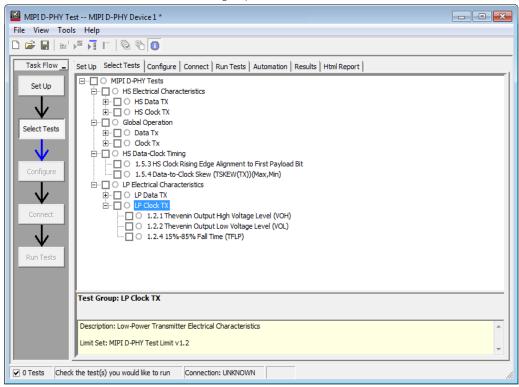


Figure 85 Selecting Low Power Transmitter Electrical Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.2.1 LP TX Thevenin Output High Voltage Level (V_{OH}) Method of Implementation

V_{OH} is the Thevenin output high-level voltage in the high-level state, when the pad pin is not loaded.

PASS Condition

The measured V_{OH} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 77 Test Availability Condition for Test 1.2.1

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 1821 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Disabled | Not Applicable |
| 18211 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 28211 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Enabled | Not Applicable |

Measurement Algorithm using Test ID 1821 and 28211

LP Clock TX Thevenin Output High Voltage Level (VOH)

NOTE

Ensure that the Clock LP EscapeMode and Clock ULPS Mode are disabled on the Device Information section of the Set Up tab of the MIPI D-PHY Test application. Use the Test ID# 1821 to remotely access the test.

ULPS Clock TX Thevenin Output High Voltage Level (VOH) ULPSMODE



Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28211 to remotely access the test.

- 1 Trigger the Clkp's LP rising edge.
- 2 Position the trigger point at the center of the screen and make sure that the stable Clkp LP high level voltage region is visible on the screen.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
- 4 Accumulate the data by using the persistent display mode.
- 5 Enable the Histogram feature and measure the entire display region after the trigger location.
- 6 Take the mode value from the **Histogram** and use this value as V_{OH} for Clkp.
- 7 Repeat steps 1 to 6 for Clkn.
- 8 Report the measurement results.
 - a V_{OH} value for Clkp channel
 - b V_{OH} value for Clkn channel
- 9 Compare the measured worst value of V_{OH} with the compliance test limits.

LP Clock TX Thevenin Output High Voltage Level (VOH) ESCAPEMODE

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18211 to remotely access the test.

- 1 Trigger on an EscapeMode pattern on the data signal. Without the presence of the LP Escape mode, the trigger is unable to capture any valid signal for data processing.
- 2 Locate and use the Mark-1 state pattern to determine the end of the EscapeMode sequence.
- 3 Apply a 400 MHz, 4th-order Butterworth low pass test filter to the specified EscapeMode sequence data.
- 4 Enable the **Histogram** feature and measure the entire LP EscapeMode sequence.
- 5 Take the mode value from the **Histogram** and use this value as V_{OH} for Clkp.
- 6 Repeat steps 1 to 4 for Clkn.
- 7 Report the measurement results.
 - a V_{OH} value for Clkp channel
 - b V_{OH} value for Clkn channel
- 8 Compare the measured worst value of V_{OH} with the compliance test limits.

Test References

See Test 1.2.1 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.2.2 LP TX Thevenin Output Low Voltage Level (V_{OL}) Method of Implementation

 V_{OL} is the Thevenin output low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low level state.

PASS Condition

The measured V_{OL} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the Test References section.

Test Availability Condition

Table 78 Test Availability Condition for Test 1.2.2

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 1822 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Disabled | Not Applicable |
| 18221 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 28221 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Enabled | Not Applicable |

Measurement Algorithm using Test ID 1822

LP Clock TX Thevenin Output Low Voltage Level (V_{OL})



Ensure that the Clock LP EscapeMode and Clock ULPS Mode are disabled on the Device Information section of the Set Up tab of the MIPI D-PHY Test application. Use the Test ID# 1822 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Entry: CLK TX T_{CLK-PREPARE} (Test ID: 552)
- 2 Trigger the Clkp's LP falling edge.
- Position the trigger point at the center of the screen and make sure that the stable Clkp LP low level voltage region is visible on the screen.
- 4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
- 5 Accumulate the data by using the persistent display mode.
- 6 Enable the **Histogram** feature and measure the entire display region after the trigger location.
- 7 Take the mode value from the Histogram and use this value as V_{OI} for CIkp.
- 8 Repeat steps 1 to 7 for Clkn.
- 9 Report the measurement results:
 - a V_{OI} value for Clkp channel
 - b V_{OI} value for Clkn channel
- 10 Compare the measured worst value of V_{OL} with the compliance test limits.

LP Clock TX Thevenin Output Low Voltage Level (VOL) ESCAPEMODE

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18221 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
- 2 Trigger on an EscapeMode pattern on the data signal. Without the presence of LP Escape mode, the trigger is unable to capture any valid signal for data processing.
- 3 Locate and use the Mark -1 state pattern to determine the end of the EscapeMode sequence.
- 4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data.
- 5 Enable the **Histogram** feature and measure the entire LP EscapeMode sequence.
- 6 Take the mode value from the **Histogram** and use this value as V_{OL} for Clkp.
- 7 Repeat steps 1 to 6 for Clkn.
- 8 Report the measurement results:
 - a V_{OI} value for Clkp channel
 - b V_{OL} value for Clkn channel
- 9 Compare the measured worst value of V_{OL} with the compliance test limits.

Measurement Algorithm using Test ID 28221

ULPS Clock TX Thevenin Output Low Voltage Level (V_{OL}) ULPSMODE



Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28221 to remotely access the test.

- 1 This test requires the following prerequisite test(s):
 - a ULPS Clock TX Thevenin Output High Voltage Level (VOH) ULPSMODE (Test ID: 28211)
- 2 Trigger the Clkp's LP falling edge.
- 3 Position the trigger point at the center of the screen and make sure that the stable Clkp LP low level voltage region is visible on the screen.
- 4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired test waveform data.
- 5 Accumulate the data by using the persistent display mode.
- 6 Enable the **Histogram** feature and measure the entire display region after the trigger location.
- 7 Take the mode value from the **Histogram** and use this value as V_{OL} for Clkp.
- 8 Repeat steps 1 to 7 for Clkn.
- 9 Report the measurement results:
 - a V_{OI} value for Clkp channel
 - b V_{OI} value for Clkn channel
- 10 Compare the measured worst value of V_{OL} with the conformance test limits.

Test References

See Test 1.2.2 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.2.3 LP TX 15%-85% Rise Time Level (T_{RLP}) Method of Implementation

The T_{RLP} is defined as 15%-85% rise time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD} . The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{RLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 79 Test Availability Condition for Test 1.2.3

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 18241 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 28241 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Enabled | Not Applicable |

Measurement Algorithm using Test ID 18241

LP Clock TX 15%-85% Rise Time (T_{RLP}) ESCAPEMODE



Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18241 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
 - b LP Clock TX Thevenin Output Low Voltage Level (V_{OL}) ESCAPEMODE (Test ID: 18221)

 $V_{\mbox{\scriptsize OH}}$ and $V_{\mbox{\scriptsize OL}}$ values for Low Power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual rise time measurement.
- 4 Perform rise time measurement on the filtered EscapeMode sequence for both Clkp and Clkn waveforms individually.
- 5 The max, mean and min result values are stored.
- 6 Report the measurement results:
 - a T_{RLP} average value for Clkp channel
 - b T_{RIP} average value for Clkn channel
- 7 Compare the measured T_{RLP} worst value derived from the T_{RLP} average value for Clkp and Clkn to the compliance test limit.

ULPS Clock TX 15%-85% Rise Time (TRLP) ULPSMODE

NOTE

Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28241 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
 - b ULPS Clock TX Thevenin Output Low Voltage Level (V_{OI}) ULPSMODE (Test ID: 28221)

 $\rm V_{OH}$ and $\rm V_{OL}$ values for Low Power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual rise time measurement.
- 4 Perform rise time measurement on the filtered EscapeMode sequence for both Clkp and Clkn waveforms individually.
- 5 The max, mean and min result values are stored.
- 6 Report the measurement results:
 - a T_{RIP} average value for Clkp channel
 - b T_{RLP} average value for Clkn channel
- 7 Compare the measured T_{RLP} worst value derived from the T_{RLP} average value for Clkp and Clkn to the compliance test limit.

Test References

See Test 1.2.3 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.2.4 LP TX 15%-85% Fall Time Level (T_{FLP}) Method of Implementation

The T_{FLP} is defined as 15%-85% fall time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD} . The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

PASS Condition

The measured T_{FLP} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 80 Test Availability Condition for Test 1.2.4

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 1825 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Disabled | Not Applicable |
| 18251 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 28251 | Not Applicable | Not Applicable | Disabled | Not Applicable | Disabled | Enabled | Not Applicable |

Measurement Algorithm using Test ID 1825

LP Clock TX 15%-85% Fall Time (T_{FLP})



Ensure that the Clock LP EscapeMode and Clock ULPS Mode are disabled on the Device Information section of the Set Up tab of the MIPI D-PHY Test application. Use the Test ID# 1825 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) (Test ID: 1821)
 - b LP Clock TX Thevenin Output Low Voltage Level (VOL) (Test ID: 1822)

 $\rm V_{OH}$ and $\rm V_{OL}$ values for Low Power signal measurements are performed and test results are stored.

- 2 Trigger is setup to trigger on LP falling edges.
- 3 The oscilloscope is triggered to capture the falling edges to be processed based on the "LP Observations" configuration in the **Configure** tab.
- 4 The average 15%-85% fall time for Clkp is recorded.
- 5 Repeat the same trigger steps for Clkn.
- 6 Report the measurement results:
 - a T_{FLP} average value for Clkp channel
 - b T_{FLP} average value for Clkn channel
- 7 Compare the measured worst value of T_{FLP} with the compliance test limits.

LP Clock TX 15%-85% Fall Time (T_{FLP}) ESCAPEMODE

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 18251 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (V_{OH}) ESCAPEMODE (Test ID: 18211)
 - b LP Clock TX Thevenin Output Low Voltage Level (VOL) ESCAPEMODE (Test ID: 18221)

 V_{OH} and V_{OL} values for low power signal measurements are performed and test results are stored.

- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual fall time measurement.
- 4 Perform fall time measurement on the filtered EscapeMode sequence for both Clkp and Clkn waveforms individually.
- 5 The maximum, mean and minimum result values are stored.
- 6 Report the measurement results:
 - a T_{FLP} average value for Clkp channel
 - b T_{FLP} average value for Clkn channel
- 7 Compare the measured worst value of T_{FLP} derived from the average value of T_{FLP} for Clkp and Clkn to the compliance test limits.

Measurement Algorithm using Test ID 28251

ULPS Clock TX 15%-85% Fall Time (T_{FLP}) ULPSMODE



Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test. Use the Test ID# 28251 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
 - b ULPS Clock TX Thevenin Output Low Voltage Level (V_{OI}) ULPSMODE (Test ID: 28221)

 $\ensuremath{V_{OH}}$ and $\ensuremath{V_{OL}}$ values for low power signal measurements are performed and test results are stored.

- 2 Trigger is setup to trigger on LP falling edges.
- 3 The oscilloscope is triggered to capture the falling edges to be processed based on the "LP Observations" configuration in the **Configure** tab.
- 4 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned trigger data prior to measuring the actual fall time.
- 5 The average 15%-85% fall time for Clkp is recorded.
- 6 Repeat the same trigger steps for Clkn.

- 7 Report the measurement results:
 - a T_{FLP} average value for Clkp channel
 - b T_{FLP} average value for Clkn channel
- 8 Compare the measured worst value of $T_{\mbox{\scriptsize FLP}}$ to the compliance test limits.

Test References

See Test 1.2.4 in D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.2.5 LP TX Slew Rate vs. C_{LOAD} Method of Implementation

The slew rate δ V/ δ t_{SR} is the derivative of the LP transmitter output signal voltage over time. The intention of specifying a maximum slew rate value in the specification is to limit EMI (Electro Magnetic Interference).

The specification also states that the Slew Rate must be measured as an average across any 50mV segment of the output signal transition.

PASS Condition

The measured slew rate δ V/ δ t_{SR} value for the test signal must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 81 Test Availability Condition for Test 1.2.5

| Associated Test ID | High-Speed Data Rate | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 1829 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 18291 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 18292 | Not Applicable | Not Applicable | Disabled | Not Applicable | Enabled | Disabled | Not Applicable |
| 2829 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled | Not Applicable |
| 28291 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled | Not Applicable |
| 28292 | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Enabled | Not Applicable |

Measurement Algorithm using Test ID 1829, 18291 and 18292

LP Clock TX Slew Rate Vs. C_{Load} (Max) /

LP Clock TX Slew Rate Vs. C_{Load} (Min) /

LP Clock TX Slew Rate Vs. C_{Load} (Margin)

NOTE

Select Clock LP EscapeMode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test.

- To access the LP Clk TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 1829.
- To access the LP CIk TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 18291.
- To access the LP Clk TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 18292.
- 1 This test requires the following prerequisite tests:
 - a LP Clock TX Thevenin Output High Voltage Level (VOH) ESCAPEMODE (Test ID: 18211)
 - b LP Clock TX Thevenin Output Low Voltage Level (VOL) ESCAPEMODE (Test ID: 18221)

- $\rm V_{OH}$ and $\rm V_{OL}$ values for low power signal measurements are performed and test results are stored.
- 2 The entire captured LP EscapeMode sequence done in the prerequisite test is used.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the mentioned EscapeMode sequence data prior to performing the actual slew rate measurement.
- 4 Perform the slew rate measurement on the filtered EscapeMode sequence for both Clkp and Clkn waveforms individually.

For falling edge,

- a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
- b. Perform the slew rate measurement across the 400mV 930mV region for data rate <= 1.5 Gbps or 400mV 790mV region for data rate > 1.5 Gbps to determine the minimum slew rate result.

For rising edge,

- a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
- b. Perform the slew rate measurement across the 400mV 700mV region for data rate <= 1.5 Gbps or 400mV-550mV region for data rate > 1.5 Gbps to determine the minimum slew rate result
- c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV 930mV region for data rate <= 1.5 Gbps or 550mV 790mV region for data rate > 1.5 Gbps.
- 5 Calculate the average value from all rising edges' maximum slew rate results. Calculate the average value from all falling edges' maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
- 6 Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
- 7 Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
- 8 The Slew Rate maximum, minimum and margin result values are stored.
- 9 Report the measurement results.
- 10 Compare the measured worst slew rate value for Clkp and Clkn to the compliance test limits.

ULPS Clock TX Slew Rate Vs. C_{I oad} (Max) ULPSMODE/

ULPS Clock TX Slew Rate Vs. C_{Load} (Min) ULPSMODE/

ULPS Clock TX Slew Rate Vs. C_{Load} (Margin) ULPSMODE

Measurement Algorithm using Test ID 2829, 28291 and 28292

NOTE

Select Clock ULPS Mode on the Device Information section of the Set Up tab of the MIPI D-PHY Test application to enable this test.

- To access the ULPS Clk TX Slew Rate Vs. C_{Load} (Max) test remotely, use the Test ID# 2829.
- To access the ULPS Clk TX Slew Rate Vs. C_{Load} (Min) test remotely, use the Test ID# 28291.
- To access the ULPS CIk TX Slew Rate Vs. C_{Load} (Margin) test remotely, use the Test ID# 28292.
- 1 This test requires the following prerequisite tests:
 - a ULPS Clock TX Thevenin Output High Voltage Level (V_{OH}) ULPSMODE (Test ID: 28211)
 - b ULPS Clock TX Thevenin Output Low Voltage Level (V_{OI}) ULPSMODE (Test ID: 28221)
 - $\ensuremath{V_{OH}}$ and $\ensuremath{V_{OL}}$ values for low power signal measurements are performed and test results are stored.
- 2 The oscilloscope is triggered to capture rising and falling edges to be processed based on the "Number of ULPS Slew Edge" configuration in the **Configure** tab.
- 3 Apply a 4th-order Butterworth low pass test filter with a cut-off frequency of 400 MHz to the acquired waveform data prior to performing the actual slew rate measurement.
- 4 Perform the slew rate measurement on the mentioned triggered data for both Clkp and Clkn waveforms individually.
 - For falling edge,
 - a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
 - b. Perform the slew rate measurement across the 400mV 930mV region for data rate <= 1.5 Gbps or 400mV 790mV region for data rate > 1.5 Gbps to determine the minimum slew rate result.
 - For rising edge,
 - a. Perform the slew rate measurement across entire signal edge to determine the maximum slew rate result.
 - b. Perform the slew rate measurement across the 400mV 700mV region for data rate <= 1.5 Gbps or 400mV-550mV region for data rate > 1.5 Gbps to determine the minimum slew rate result.
 - c. Measure the minimum margin between the measured slew rate curve and the minimum slew rate limit line across the 700mV 930mV region for data rate <= 1.5 Gbps or 550mV 790mV region for data rate > 1.5 Gbps.
- 5 Calculate the average value from all rising edges' maximum slew rate results. Calculate the average value from all falling edges' maximum slew rate results. Find the maximum values of these results and use it as Slew Rate max result.
- 6 Calculate the average value from all rising edges' minimum slew rate results. Calculate the average value from all falling edges' minimum slew rate results. Find the minimum values of these results and use it as Slew Rate min result.
- 7 Calculate the average value from all rising edges' slew rate margin results. Find the worst case values of these results and use it as Slew Rate margin result.
- 8 The Slew Rate maximum, minimum and margin result values are stored.
- 9 Report the measurement results.
- 10 Compare the measured worst slew rate value for Clkp and Clkn to the compliance test limits.

Test References

See Test 1.2.5 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

| Part II Global Operation |
|-----------------------------|
| |



Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

23 MIPI D-PHY 1.2 Data Transmitter (Data TX) Global Operation Tests

Probing for Data TX Global Operation Tests / 316

Test 1.3.1 HS Entry: Data T_{I PX} Method of Implementation / 318

Test 1.3.2 HS Entry: Data TX $T_{HS-PREPARE}$ Method of Implementation / 318

Test 1.3.3 HS Entry: Data TX $T_{HS-PREPARE} + T_{HS-ZERO}$ Method of Implementation / 318

Test 1.3.13 HS Exit: Data TX $T_{HS-TRAIL}$ Method of Implementation / 318

Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation / 318

Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation / 319 Test 1.3.16 HS Exit: Data TX $T_{HS-EXIT}$ Method of Implementation / 319

This section provides the Methods of Implementation (MOIs) for the Data Transmitter (Data TX) Global Operation tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.

MIPI D-PHY 1.2 Data TX Global Operation tests are similar to the MIPI D-PHY 1.0 Data TX Global Operation tests. Hence, most of the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 Data Transmitter (Data TX) Global Operation Tests"

The current chapter lists the references from the MIPI D-PHY 1.2 CTS and describes the difference in the Method of Implementation from the corresponding MIPI D-PHY 1.0 test for the following test:

"Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{RFOT}) Method of Implementation"

"Test 1.3.15 HS Exit: Data TX T_{EOT} Method of Implementation"



Probing for Data TX Global Operation Tests

When performing the Data TX tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the Data TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Conformance Test Application for the exact number of probe connections.

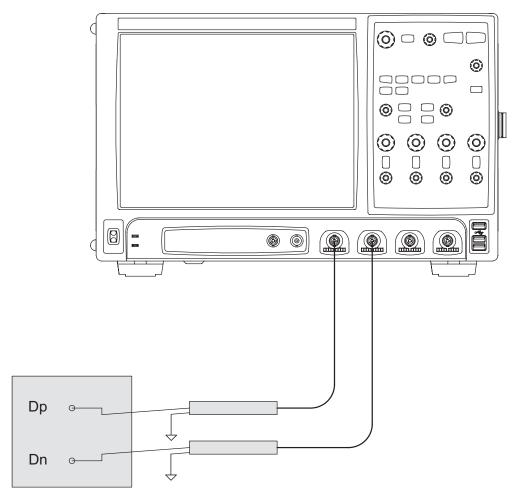


Figure 86 Probing for Data TX Global Operation Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 86 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

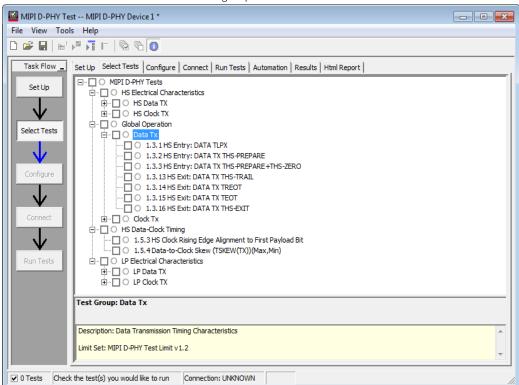


Figure 87 Selecting Data TX Global Operation Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.3.1 HS Entry: Data T_{LPX} Method of Implementation

Test References

See Test 1.3.1 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.2 HS Entry: Data TX T_{HS-PRFPARF} Method of Implementation

Test References

See Test 1.3.2 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.3 HS Entry: Data TX T_{HS-PREPARE} + T_{HS-ZERO} Method of Implementation

Test References

See Test 1.3.3 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.13 HS Exit: Data TX T_{HS-TRAIL} Method of Implementation

Test References

See Test 1.3.13 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.14 LP TX 30%-85% Post -EoT Rise Time (T_{REOT}) Method of Implementation

This test is similar to the corresponding MIPI D-PHY 1.0 test. This section describes only the changes from the MIPI D-PHY 1.0 test. For details of the corresponding MIPI D-PHY 1.0 test, refer to "MIPI D-PHY 1.0 Data Transmitter (Data TX) Global Operation Tests".

Measurement Algorithm using Test ID 549

NOTE

Use the Test ID# 549 to remotely access the test.

- 1 Trigger on Dp's falling edge in LP-01 at the SoT.
- 2 Go to EoT.
- 3 Find the time where the last data TX differential edge crosses +/-V_{IDTH}(max), denoted as T1.
- 4 Find the time where Dp rising edge crosses V_{IH} (min) (880mV for data rate <= 1.5 Gbps OR 740mV for data rate > 1.5 Gbps), and denote it as T2. Note that T2 must be greater than T1.
- 5 Use the following calculation:

$$T_{REOT} = T2-T1$$

- 6 Report the measured T_{RFOT}.
- 7 Compare the measured T_{RFOT} with the conformance test limits.

Test References

See Test 1.3.14 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.15 HS Exit: Data TX T_{FOT} Method of Implementation

Measurement Algorithm using Test ID 547

NOTE

Use the Test ID# 547 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - HS Clock Instantaneous: $\mathrm{UI}_{\mathrm{inst}}$ [Max] (Test ID: 911)
 - The minimum, maximum and average Unit Interval of the differential clock waveform is measured and test results are stored.
- 2 Trigger on Dp's falling edge in LP-01 at the SoT.
- 3 Go to EoT.
- 4 Find the time when the last data differential edge crosses +/-V_{IDTH}(max), and denote it as T6.
- 5 Find the time where Dp rising edge crosses VIH(min)(880mV for data rate <= 1.5 Gbps OR 740mV for data rate > 1.5 Gbps), and denote it as T8. Note that T8 must greater than T6.
- 6 Use the following calculation:

$$T_{FOT} = T8-T6$$

- 7 Report the measured T_{EOT}.
- 8 Compare the measured T_{FOT} with the conformance test limits.

Test References

See Test 1.3.15 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.3.16 HS Exit: Data TX T_{HS-EXIT} Method of Implementation

Test References

See Test 1.3.16 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

24 MIPI D-PHY 1.2 Clock Transmitter (Clock TX) Global Operation Tests

Probing for Clock TX Global Operation Tests / 322

Test 1.4.1 HS Entry: CLK TX T_{I PX} Method of Implementation / 324

Test 1.4.2 HS Entry: CLK TX T_{CLK-PREPARE} Method of Implementation / 324

Test 1.4.3 HS Entry: CLK TX $T_{CLK-PREPARE} + T_{CLK-ZERO}$ Method of Implementation / 324

Test 1.5.1 HS Entry: CLK TX $T_{CLK-PRE}$ Method of Implementation / 324

Test 1.5.2 HS Exit: CLK TX $T_{CLK-POST}$ Method of Implementation $\,/\,$ 324

Test 1.4.13 HS Exit: CLK TX $T_{CLK-TRAIL}$ Method of Implementation / 324

Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{RFOT}) Method of Implementation / 324

Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation / 325 Test 1.4.16 HS Exit: CLK TX $T_{HS-EXIT}$ Method of Implementation / 325

This section provides the Methods of Implementation (MOIs) for the Clock Transmitter (Clock TX) Global Operation tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.

MIPI D-PHY 1.2 Clock TX Global Operation tests are similar to the MIPI D-PHY 1.0 Clock TX Global Operation tests. Hence, most of the tests share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 Clock Transmitter (Clock TX) Global Operation Tests"

The current chapter lists the references from the MIPI D-PHY 1.2 CTS and describes the difference in the Method of Implementation from the corresponding MIPI D-PHY 1.0 test for the following test:

"Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{RFOT}) Method of Implementation"

"Test 1.4.15 HS Exit: CLK TX T_{EOT} Method of Implementation"



Probing for Clock TX Global Operation Tests

When performing the Clock TX tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the Clock TX tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Conformance Test Application for the exact number of probe connections.

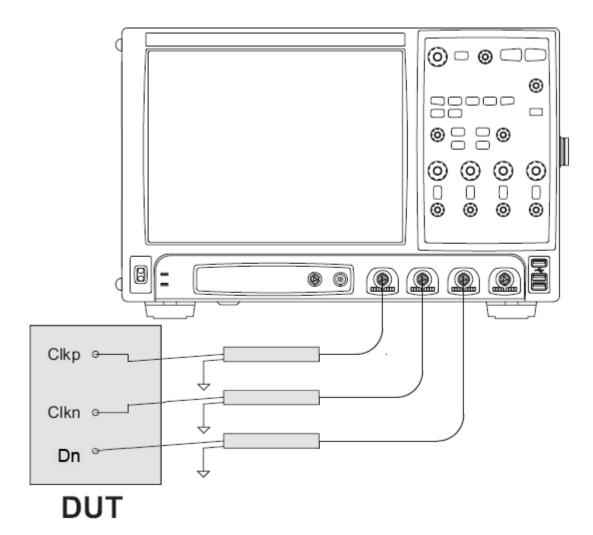


Figure 88 Probing for Clock TX Global Operation Tests

You can identify the channels used for each signal in the Configuration tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 88 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, Device ID and User Comments.
- 4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

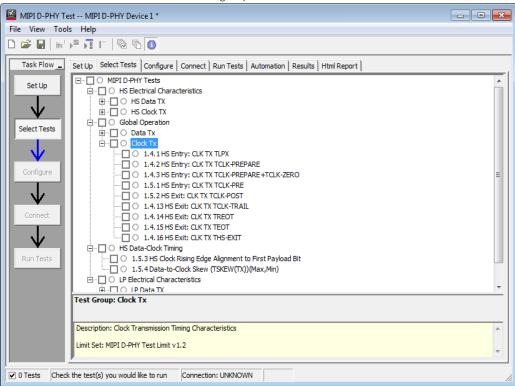


Figure 89 Selecting Clock TX Global Operation Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.4.1 HS Entry: CLK TX T_{I PX} Method of Implementation

Test References

See Test 1.4.1 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.2 HS Entry: CLK TX T_{CLK-PRFPARF} Method of Implementation

Test References

See Test 1.4.2 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.3 HS Entry: CLK TX T_{CLK-PREPARE}+T_{CLK-ZERO} Method of Implementation

Test References

See Test 1.4.3 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.5.1 HS Entry: CLK TX T_{CLK-PRF} Method of Implementation

Test References

See Test 1.5.1 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.5.2 HS Exit: CLK TX T_{CLK-POST} Method of Implementation

Test References

See Test 1.5.2 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.13 HS Exit: CLK TX T_{CLK-TRAIL} Method of Implementation

Test References

See Test 1.4.13 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.14 LP TX 30%-85% Post-EoT Rise Time (T_{REOT}) Method of Implementation

This test is similar to the corresponding MIPI D-PHY 1.0 test. This section describes only the changes from the MIPI D-PHY 1.0 test. For details of the corresponding MIPI D-PHY 1.0 test, refer to "MIPI D-PHY 1.0 Clock Transmitter (Clock TX) Global Operation Tests".

Measurement Algorithm using Test ID 559

NOTE

Use the Test ID# 559 to remotely access the test.

- 1 Trigger on the Clkn's falling edge in LP-01 at the SoT.
- 2 Go to EoT.

- 3 Find the time where last Clock TX differential edge crosses +/-VIDTH(max), marked as T1.
- 4 Find the time where Clkp rising edge crosses VIH(min) (880mV for data rate <= 1.5 Gbps or 740mV for data rate > 1.5 Gbps), marked as T2. Note that T2 must be greater than T1.
- 5 Use the equation:

$$T_{RFOT} = T2-T1$$

- 6 Report the measured T_{REOT}.
- 7 Compare the measured T_{REOT}value to the compliance test limits.

Test References

See Test 1.4.14 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.15 HS Exit: CLK TX T_{FOT} Method of Implementation

Measurement Algorithm using Test ID 544

NOTE

Use the Test ID# 544 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (UI_{inst}) [Max] (Test ID: 911)
 Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.
- 2 Trigger on the Clkn's falling edge after LP-01.
- 3 Back trace to the previous EoT.
- 4 Construct the differential clock waveform by using the following equation:

- 5 Find the time when the DiffClock crosses +/-V_{IDTH}(max) after last payload clock bit. Denote the time as T1.
- 6 Find the time when the Clkp TX rising edge crosses V_{IH} (min)(880mV for data rate <= 1.5 Gbps OR 740mV for data rate > 1.5 Gbps). Denote the time as T2. Note that T2 must be greater than T1.
- 7 Calculate T_{EOT} using the following equation:

$$T_{FOT} = T2-T1$$

- 8 Report the T_{EOT} measurement.
- 9 Compare the measured T_{FOT} value with the conformance test limit.

Test References

See Test 1.4.15 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.4.16 HS Exit: CLK TX T_{HS-EXIT} Method of Implementation

Test References

See Test 1.4.16 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

MIPI D-PHY 1.2 Clock Transmitter (Clock TX) Global Operation Tests

| | | | | | | | | | | | | | | | | Part III HS Data-Clock Timing & HS Skew |
|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------------------------|
| | | | | | | | | | | | | | | | | |



Keysight U7238C/U7238D MIPI D-PHY Test App Methods of Implementation

25 MIPI D-PHY 1.2 High Speed (HS) Data-Clock Timing Tests

Probing for High Speed Data-Clock Timing Tests / 330 Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation / 332 Test 1.5.4 Data-to-Clock Skew ($T_{SKEW(TX)}$) Method of Implementation / 332

This section provides the Methods of Implementation (MOIs) for the High Speed (HS) Data-Clock Timing tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test App.



Probing for High Speed Data-Clock Timing Tests

When performing the HS Data-Clock Timing tests, the MIPI D-PHY Test App will prompt you to make the proper connections. The connections for the HS Data-Clock Timing tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

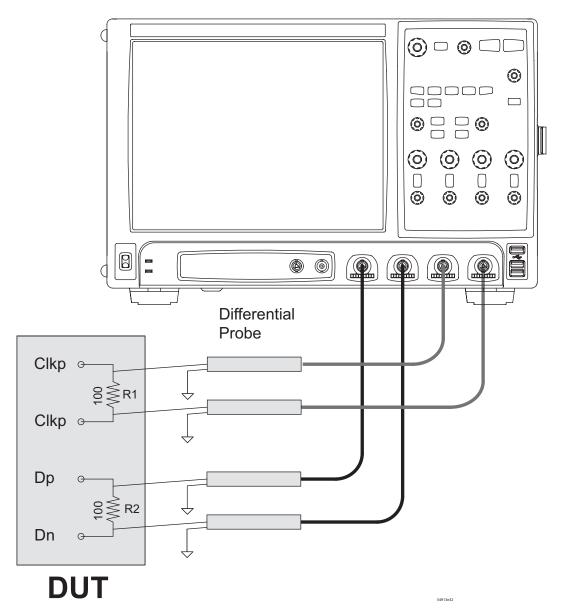


Figure 90 Probing for HS Data-Clock Timing Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test App. (The channels shown in Figure 90 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, Device ID and User Comments.
- 4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

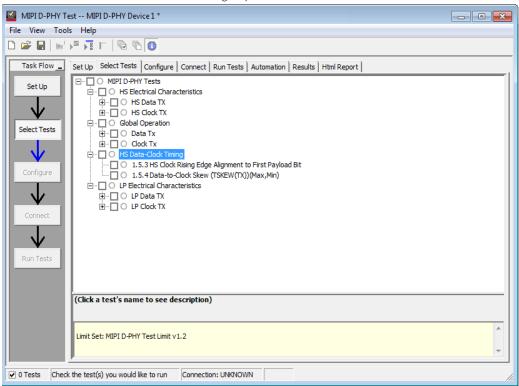


Figure 91 Selecting HS Data-Clock Timing Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Method of Implementation

This test has the same method of implementation as the corresponding MIPI D-PHY 1.0 test. For details, refer to "MIPI D-PHY 1.0 High Speed (HS) Data-Clock Timing Tests".

Test References

See Test 1.5.3 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.5.4 Data-to-Clock Skew (T_{SKEW(TX)}) Method of Implementation

This test is similar to the corresponding MIPI D-PHY 1.0 test. This section describes only the changes from the MIPI D-PHY 1.0 test. For details of the corresponding MIPI D-PHY 1.0 test, refer to "MIPI D-PHY 1.0 High Speed (HS) Data-Clock Timing Tests".

Measurement Algorithm using Test ID 913

NOTE

Use the Test ID# 913 to remotely access the test.

- 1 This test requires the following prerequisite tests:
 - a HS Clock Instantaneous (Ul_{inst}) [Max] (Test ID: 911)

Measure the minimum, maximum and average values of the Unit Interval for the differential clock waveform and the test results are stored.

- 2 Dp, Dn, Clkp and Clkn waveforms are captured.
- 3 Construct the differential clock waveform using the following equation:

4 Construct the differential data waveform by using the following equation:

- 5 Using the DiffClock's rising and falling edges, fold the DiffData to form a data eye.
- 6 Use the Histogram feature to find out the furthest edges on the left of the DiffData left crossing and use it to calculate the T_{Skew} (max).
- 7 Use the Histogram feature to find out the nearest edges on the left of the DiffData left crossing and use it to calculate the T_{Skew} (min).
- 8 Use the **Histogram** feature to find out the mean of the DiffData left crossing and use it to calculate the T_{Skew} (mean).
- 9 Calculate T_{Skew} values (max/min) in units of seconds and in units of UI using the following equation:

$$T_{Skew(TX)}$$
 (in seconds) = (T_{Skew} - T_{Center}) - MeanSkewRef
$$T_{Skew(TX)}$$
 (in UI) = T_{Skew} /MeanUI

NOTE

For HS rates <= 1.5 Gbps, the MeanSkewRef is calculated as: MeanSkewRef = [0.5 * MeanUI obtained from the prerequisite test] For HS rates > 1.5 Gbps, the MeanSkewRef is calculated as: MeanSkewRef = $[Measured T_{Skew} (mean) - T_{Center}]$

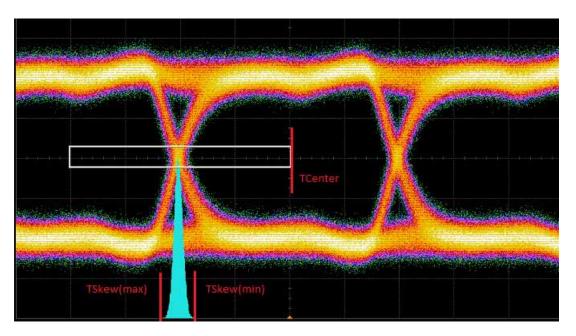


Figure 92 Data Eye

10 Calculate T_{Skew} (mean) in units of UI using the following equation:

$$T_{Skew(TX)}$$
 (in UI) = T_{Skew} /MeanUI

- 11 The T_{Skew} (worst) is determined based on the T_{Skew} (max) and T_{Skew} (min) values with reference to the compliance test limit
- 12 Compare the T_{Skew} (worst) value with the conformance test limits.

Test References

See Test 1.5.4 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Keysight U7238C/U7238D MIPI D-PHY Test App Methods of Implementation

26 MIPI D-PHY 1.2 High Speed (HS) Skew Calibration Burst Tests

Probing for High Speed Skew Calibration Burst Tests / 336
Test 1.5.5 Initial HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation / 239

Test 1.5.6 Periodic HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation / 340

This section provides the Methods of Implementation (MOIs) for the High Speed (HS) Skew Calibration Burst tests using a Keysight 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Test App.



Probing for High Speed Skew Calibration Burst Tests

When performing the HS Skew Calibration Burst tests, the MIPI D-PHY Test App will prompt you to make the proper connections. The connections for the HS Skew Calibration Burst tests may look similar to the following diagram. Refer to the **Connect** tab in MIPI D-PHY Test app for the exact number of probe connections.

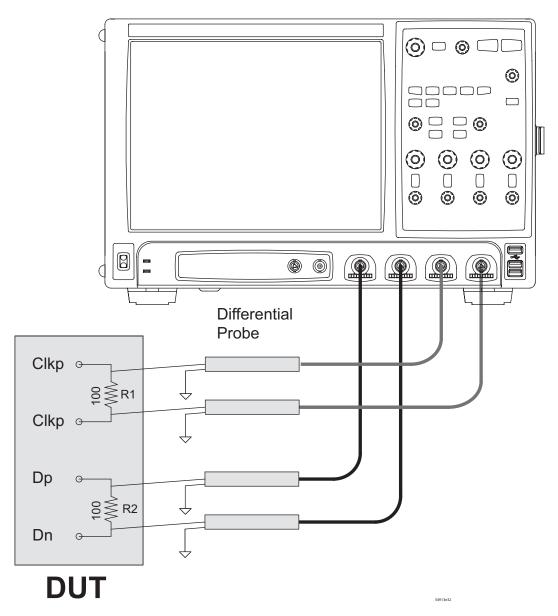


Figure 93 Probing for HS Skew Calibration Burst Tests

You can identify the channels used for each signal in the **Configure** tab of the MIPI D-PHY Test App. (The channels shown in Figure 93 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 29, "InfiniiMax Probing".

Test Procedure

- 1 Start the automated test application as described in "Starting the MIPI D-PHY Test App".
- 2 In the MIPI D-PHY Test app, click the **Set Up** tab.
- 3 Enter the High-Speed Data Rate, Device ID and User Comments.
- 4 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

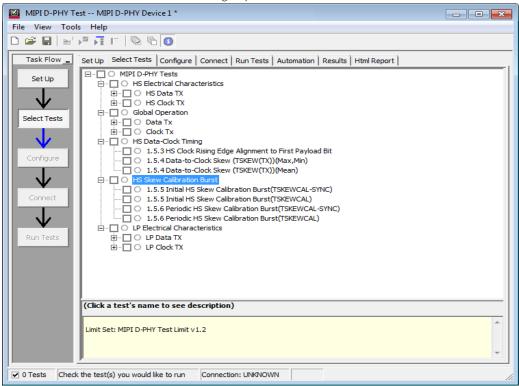


Figure 94 Selecting HS Skew Calibration Burst Tests

5 Follow the MIPI D-PHY Test app's task flow to set up the configuration options, run the tests and view the tests results.

Test 1.5.5 Initial HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation

This test verifies that TSKEWCAL-SYNC and TSKEWCAL are within the specification. $\label{eq:total_symmetry}$

6

High-Speed Skew Calibration

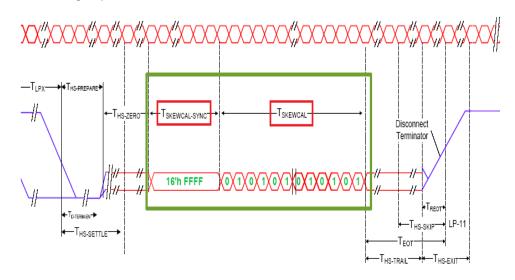


Figure 95 Normal Mode versus Skew Calibration

PASS Condition

The TSKEWCAL-SYNC and TSKEWCAL values must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 82 Test Availability Condition for Test 1.5.5

| Associated Test ID | High-Speed Data Rate | ZID | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|---------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 917 | >1.5 Gbps | 100 ohm | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 918 | > 1.5 Gbps | 100 ohm | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 917

NOTE

Use the Test ID# 917 to remotely access the test.

- 1 Trigger on Dp's falling edge in LP-01 on Initial HS Skew calibration burst.
- 2 Construct the differential waveform of Dp and Dn by using the following equation:

Data_{Diff} = Dp - Dn

- 3 Measure the average Unit Interval value of the differential data waveform.
- 4 Find the first rising edge of the differential waveform that crosses 0V after the LP-00 state. Mark the time as T_1 .
- 5 Find and mark the next falling edge that crosses OV. Mark the time as T₂.
- 6 Calculate TSKEWCAL-SYNC using the following equation:

 $TSKEWCAL-SYNC = T_2-T_1$

- 7 From the T_2 position, find the final edge position where the bit pattern "01010101..." ends. Mark the position as T_3 .
- 8 Calculate TSKEWCAL using the following equation:

 $TSKEWCAL = T_3 - T_2$

9 Report the measurement result:

TSKEWCAL-SYNC

10 Compare the TSKEWCAL-SYNC value with the compliance test limits.

Measurement Algorithm using Test ID 918

NOTE

Use the Test ID# 918 to remotely access the test.

- 1 This test requires the following prerequisite test:
 - a Initial HS Skew Calibration Burst (TSKEWCAL-SYNC) (Test ID: 917) Actual TSKEWCAL value is measured and test result is stored.
- 2 Report the measurement result:

TSKEWCAL

3 Compare the TSKEWCAL value with the compliance test limit.

Test References

See Test 1.5.5 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

Test 1.5.6 Periodic HS Skew Calibration Burst (TSKEWCAL-SYNC, TSKEWCAL) Method of Implementation

This test verifies that TSKEWCAL-SYNC and TSKEWCAL are within the specification.

PASS Condition

The TSKEWCAL-SYNC and TSKEWCAL values must be within the conformance limit as specified in the CTS specification mentioned under the References section.

Test Availability Condition

Table 83 Test Availability Condition for Test 1.5.6

| Associated Test ID | High-Speed Data Rate | ZID | Continuous Data | Continuous Clock | Data LP EscapeMode | Clock LP EscapeMode | Clock ULPS Mode | Informative Test |
|-----------------------|-------------------------|---------|--------------------|---------------------|-----------------------|------------------------|--------------------|---------------------|
| 919 | > 1.5 Gbps | 100 ohm | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |
| 920 | > 1.5 Gbps | 100 ohm | Disabled | Not Applicable | Not Applicable | Not Applicable | Not Applicable | Not Applicable |

Measurement Algorithm using Test ID 919

NOTE

Use the Test ID# 919 to remotely access the test.

- 1 Trigger on Dp's falling edge in LP-01 on Periodic HS Skew calibration burst.
- 2 Construct the differential waveform of Dp and Dn by using the following equation:

$$Data_{Diff} = Dp - Dn$$

- 3 Measure the average Unit Interval value of the differential data waveform.
- 4 Find the first rising edge of the differential waveform that crosses 0V after the LP-00 state. Mark the time as T_1 .
- 5 Find and mark the next falling edge that crosses OV. Mark the time as T₂.
- 6 Calculate TSKEWCAL-SYNC using the following equation:

$$TSKEWCAL-SYNC = T_2-T_1$$

- 7 From the T_2 position, find the final edge position where the bit pattern "01010101..." ends. Mark the position as T_3 .
- 8 Calculate TSKEWCAL using the following equation:

$$TSKEWCAL = T_3 - T_2$$

9 Report the measurement result:

TSKEWCAL-SYNC

10 Compare the TSKEWCAL-SYNC value with the compliance test limits.

Measurement Algorithm using Test ID 920

NOTE

Use the Test ID# 920 to remotely access the test.

- 1 This test requires the following prerequisite test:
 - *a* Periodic HS Skew Calibration Burst (TSKEWCAL-SYNC) (Test ID: 919) Actual TSKEWCAL value is measured and test result is stored.
- 2 Report the measurement result:

TSKEWCAL

3 Compare the TSKEWCAL value with the compliance test limit.

Test References

See Test 1.5.6 in the D-PHY Physical Layer Conformance Test Suite v1.2r09 (29Sep2014).

26 MIPI D-PHY 1.2 High Speed (HS) Skew Calibration Burst Tests

| | | Part IV Informative Tests |
|--|--|---------------------------|
| | | |
| | | |



Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

27 MIPI D-PHY 1.2 Informative Tests

MIPI D-PHY 1.2 Informative tests are the same as MIPI D-PHY 1.0 Informative tests. Hence, they share the same Method of Implementation (MOI) as the corresponding MIPI D-PHY 1.0 tests. For details, refer to "MIPI D-PHY 1.0 Informative Tests"



| | Part V Introduction |
|--|------------------------|
| | |



Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

28 Calibrating the Infiniium Oscilloscopes and Probes

To Run the Self Calibration / 350
Self Calibration / 351
Required Equipment for Solder-in and Socketed Probe Heads Calibration / 354
Calibration for Solder-in and Socketed Probe Heads / 355
Verifying the Probe Calibration / 361
Required Equipment for Browser Probe Head Calibration / 364
Calibration for Browser Probe Head / 365

This section describes the Keysight Infiniium oscilloscopes calibration procedures.



To Run the Self Calibration

NOTE

Let the Oscilloscope Warm Up Before Adjusting. Warm up the oscilloscope for 30 minutes before starting calibration procedure. Failure to allow warm up may result in inaccurate calibration.

The self calibration uses signals generated in the oscilloscope to calibrate channel sensitivity, offsets, and trigger parameters. You should run the self calibration

- · yearly, or according to your periodic needs,
- · when you replace the acquisition assembly or acquisition hybrids,
- · when you replace the hard drive or any other assembly,
- when the oscilloscope's operating temperature (after the 30 minute warm-up period) is more than ±5 °C different from that of the last calibration.

To calibrate the 90000 Series Infiniium oscilloscope in preparation for running the MIPI D-PHY automated tests, you need the following equipment:

Table 84 Equipment Required

| Equipment | Critical Specifications | Keysight Part Number |
|-------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|-------------------------------------|
| Adapters (2 supplied with oscilloscope except for the DS090254A) | 3.5 mm (f) to precision BNC No substitute | Keysight 54855-67604 |
| Cable Assembly | 50 Ù characteristic impedance BNC (m) connectors ~ 36 inches (91 cm) to 48 inches (122 cm) long | Keysight 8120-1840 |
| Cable Assembly (supplied with oscilloscope except for the DSO90254A which can use a good quality BNC cable) | No substitute | Keysight 54855-61620 |
| 10 MHz Signal Source (required for time scale calibration) | Frequency accuracy better than 0.4 ppm | Keysight 53131A with Opt. 010 |

Self Calibration

NOTE

Calibration time: It will take approximately 1 hour to run the self calibration on the oscilloscope, including the time required to change cables from channel to channel.

- 1 Let the Oscilloscope warm up before running the Self Calibration.
 The self calibration should only be done after the oscilloscope has run for 30 minutes at ambient temperature with the cover installed. Calibration of an oscilloscope that has not warmed up may result in an inaccurate calibration.
- 2 Pull down the **Utilities** menu and select **Calibration**.

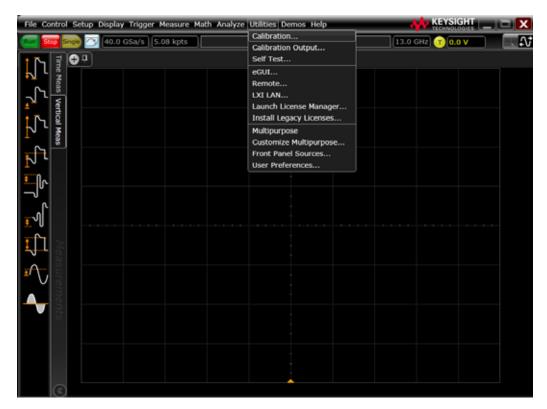


Figure 96 Utilities menu on the Oscilloscope

3 Click the check box to clear the Cal Memory Protect condition.
You cannot run self calibration if the **Cal Memory Protect** option is checked. See Figure 97.

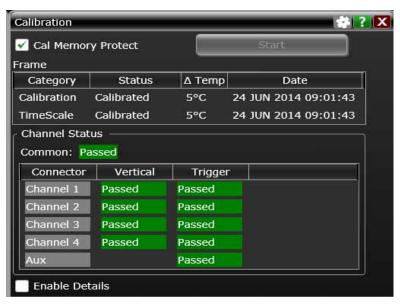


Figure 97 Oscilloscope Calibration Window

- 4 Click **Start**, then follow the instructions on the screen.
 The routine will ask you to do the following things in sequence:
 - a Decide if you want to perform the Time Scale Calibration. Your choices are:

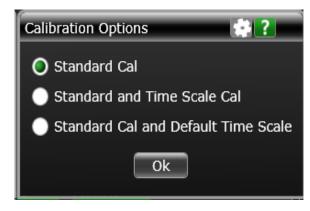


Figure 98 Calibration Options pop-up for Time Scale Calibration

- Standard Cal Time scale calibration will not be performed. Time scale calibration factors from
 the previous time scale calibration will be used and the 10 MHz reference signal will not be
 required. The remaining calibration procedure will continue.
- Standard and Time Scale Cal Performs the time scale calibration. This option requires you to
 connect a 10 MHz reference signal to channel 1 that meets the following specifications. Failure
 to use a reference signal that meets this specification will result in an inaccurate calibration.

Frequency: 10 MHz ±0.4 ppm = 10 MHz ±4 Hz Amplitude: 0.2 Vpeak-to-peak to 5.0 Vpeak-to-peak

Wave shape: Sine or Square

- Standard Cal and Default Time Scale Factory time scale calibration factors will be used. The
 10 MHz reference signal will not be required. The remaining calibration procedure will
 continue.
- b Disconnect everything from all inputs and Aux Out.
- c Connect the calibration cable from Aux Out to channel 1.
- You must use the 54855-61620 cable assembly with two 54855-67604 adapters for all
 oscilloscopes except for the DSO90254A which can use a good quality BNC cable. Failure to
 use the appropriate calibration cable will result in an inaccurate calibration.
- d Connect the calibration cable from Aux Out to each of the channel inputs as requested.
- e Connect the 50 Û BNC cable from the Aux Out to the Aux Trig on the front panel of the oscilloscope.
- f A Passed/Failed indication is displayed for each calibration section. If any section fails, check the calibration cables and run the oscilloscope Self Test in the **Utilities** menu.
- g Once the calibration procedure is completed, click **Close**.

Required Equipment for Solder-in and Socketed Probe Heads Calibration

NOTE

Each probe is calibrated with the oscilloscope channel to which it is connected. Do not switch probes between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the probes be labeled with the channel on which they were calibrated.

Before performing MIPI D-PHY tests you should calibrate the probes. Calibration of the solder-in probe heads consist of a vertical calibration and a skew calibration. The vertical calibration should be performed before the skew calibration. Both calibrations should be performed for best probe measurement performance.

The calibration procedure requires the following parts.

- · BNC (male) to SMA (male) adaptor
- Deskew fixture
- 50 Ω SMA terminator

Calibration for Solder-in and Socketed Probe Heads

NOTE

Before calibrating the probe, verify that the Infiniium oscilloscope has been calibrated recently and that the calibration temperature is within ± 5 °C. If this is not the case, calibrate the oscilloscope before calibrating the probe. This information is found in the Infiniium Calibration dialog box.

Connecting the Probe for Calibration

For the following procedure, refer to Figure 99 below.

- 1 Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.
- 2 Connect the 50 Ω SMA terminator to the connector farthest from yellow pincher.
- 3 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.
- 4 Connect the probe to an oscilloscope channel.
- 5 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.
- 6 Push down the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.
- 7 Release the yellow pincher.



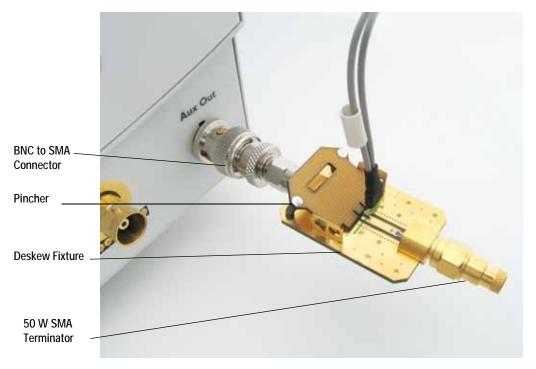


Figure 99 Solder-in Probe Head Calibration Connection Example

Verifying the Connection

- 1 On the Infiniium oscilloscope, press the autoscale button on the front panel.
- 2 Set the volts per division to 100 mV/div.
- 3 Set the horizontal scale to 1.00 ns/div.
- 4 Set the horizontal position to approximately 3ns. You should see a waveform similar to that in Figure 100 below.

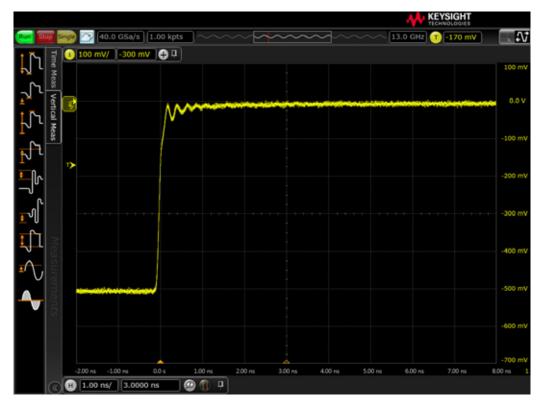


Figure 100 Example of a Good Connection Waveform

If you see a waveform similar to that of Figure 101 below, then you have a bad connection and should check all of your probe connections.



Figure 101 Example of a Bad Connection Waveform

Running the Probe Calibration and Deskew

1 On the Infiniium oscilloscope in the **Setup** menu, select the channel connected to the probe, as shown in Figure 102.

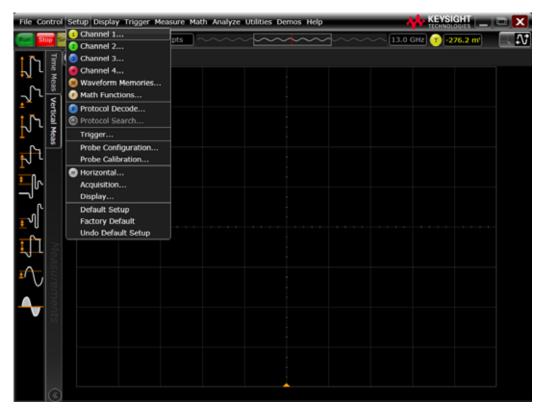


Figure 102 Channel Setup Window.

2 In the **Channel** dialog box, select the **Probe...** button, as shown in Figure 103.



Figure 103 Channel Dialog Box

3 In the Probe Calibration dialog box, select the Calibrated Atten (3.4:1) radio button.



Figure 104 Probe Calibration setup window

- 4 Click the **Start Atten/Offset Cal...** button and follow the on-screen instructions for the vertical calibration procedure.
- 5 Once the vertical calibration has successfully completed, select the **Calibrated Skew...** button.
- 6 Select the **Start Skew Cal...** button and follow the on-screen instructions for the skew calibration. At the end of each calibration, the oscilloscope prompts you if the calibration was or was not successful.

Verifying the Probe Calibration

If you have successfully calibrated the probe, it is not necessary to perform this verification. However, if you want to verify that the probe was properly calibrated, the following procedure will help you verify the calibration.

The calibration procedure requires the following parts:

- · BNC (male) to SMA (male) adaptor
- · SMA (male) to BNC (female) adaptor
- BNC (male) to BNC (male) 12 inch cable such as the Keysight 8120-1838
- Keysight 54855-61620 calibration cable (Infiniium oscilloscopes with bandwidths of 6 GHz and greater only)
- Keysight 54855-67604 precision 3.5 mm adaptors (Infiniium oscilloscopes with bandwidths of 6 GHz and greater only)
- · Deskew fixture

To verify the calibration, follow the procedure below. (Refer to Figure 105)

- 1 Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.
- 2 Connect the SMA (male) to BNC (female) to the connector farthest from the yellow pincher.
- 3 Connect the BNC (male) to BNC (male) cable to the BNC connector on the deskew fixture to one of the unused oscilloscope channels. For infinitum oscilloscopes with bandwidths of 6 GHz and greater, use the 54855-61620 calibration cable and the two 54855-64604 precision 3.5 mm adaptors.
- 4 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.
- 5 Connect the probe to an oscilloscope channel.
- 6 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.
- Push down on the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.
- 8 Release the yellow pincher.
- 9 On the oscilloscope, press the autoscale button on the front panel.
- 10 Select **Setup** menu and choose the channel connected to the BNC cable from the pull-down menu.
- 11 Select the Probe... button.
- 12 Select the Calibrated Skew radio button.
- 13 Once the skew calibration is completed, close all dialog boxes.

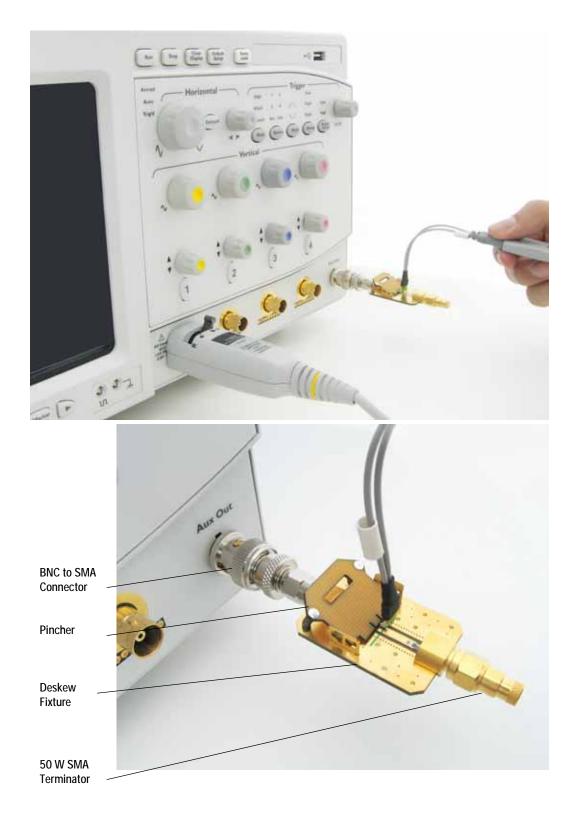


Figure 105 Probe Calibration Verification Connection Example

- 14 Select the **Start Skew Cal...** button and follow the on-screen instructions.
- 15 Set the vertical scale for the displayed channels to 100mV/div.
- 16 Set the horizontal range to 1.00ns/div.
- 17 Set the horizontal position to approximately 3ns.
- 18 Change the vertical position knobs of both channels until the waveforms overlap each other.
- 19 Select the **Setup** menu and choose **Acquisition**... from the pull-down menu.
- 20 In the **Acquisition Setup** dialog box enable averaging. When you close the dialog box, you should see waveforms similar to that in Figure 106.



Figure 106 Calibration Probe Waveform Example

Required Equipment for Browser Probe Head Calibration

NOTE

Before calibrating the probe, verify that the Infiniium oscilloscope has been calibrated recently and that the calibration temperature is within ± 5 °C. If this is not the case, calibrate the oscilloscope before calibrating the probe. This information is found in Infiniium Calibration dialog box.

Calibration of the hand-held browser probe heads consists of a vertical calibration and a skew calibration. The vertical calibration should be performed before the skew calibration. Both calibrations should be performed for the best probe measurement performance.

The calibration procedure requires the following parts.

- · BNC (male) to SMA (male) adaptor
- Deskew fixture
- 50 Ω SMA terminator

Calibration for Browser Probe Head

Connecting the Probe for Calibration

For the following procedure, refer to Figure 107 below.

- 1 Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.
- 2 Connect the 50 Ω SMA terminator to the connector farthest from the yellow pincher.
- 3 Connect the BNC side of the deskew fixture to the Aux Out of the Infiniium oscilloscope.
- 4 Connect the probe to an oscilloscope channel.
- 5 Place the positive resistor tip of the browser on the center conductor of the deskew fixture between the green line and front end of the yellow pincher. The negative resistor tip or ground pin of the browser must be on either of the two outer conductors (ground) of the deskew fixture.
- 6 On the Infiniium oscilloscope in the **Setup** menu, select the channel connected to the probe.
- 7 In the **Channel Setup** dialog box, select the **Probe...** button.
- 8 In the Probe Calibration dialog box, select the Calibrated Atten (3.4:1) radio button.
- 9 Select the **Start Atten/Offset Cal...** button and follow the on-screen instructions for the vertical calibration procedure.
- 10 Once the vertical calibration has successfully completed, select the **Calibrated Skew...** button.
- 11 Select the Start Skew Cal... button and follow the on-screen instructions for the skew calibration.





Figure 107 Browser Probe Head Calibration Connection Example

Keysight U7238C/U7238D MIPI D-PHY Conformance Test Application

Methods of Implementation

29 InfiniiMax Probing



Figure 108 1168A and 1169A InfiniiMax Probe Amplifier

Differential probe amplifier, with minimum bandwidth of 5 GHz is required. Keysight recommends 1132A, 1134A, 1168A and 1169A probe amplifiers.

Table 85 Recommended InfiniiMax I and InfiniiMax II Series Probe Amplifiers

| Model | Band wid th | Description |
|-------|-------------|-------------------------------|
| 1132A | 5 GHz | InfiniiMax I probe amplifier |
| 1134A | 7 GHz | InfiniiMax I probe amplifier |
| 1168A | 10 GHz | InfiniiMax II probe amplifier |
| 1169A | 12 GHz | InfiniiMax II probe amplifier |

Keysight also recommends E2677A differential solder-in probe head, E2675A differential browser probe head, E2678A differential socket probe head and E2669A differential kit which includes E2675A, E2677A and E2678A.





Figure 109 E2677A Differential Solder-in Probe Head

Table 86 Probe Head Characteristics (with 11684A and 1169A probe amplifiers with limitations)

| Probe Head | Model Number | Differential Measurement (BW, input C, input R) | Single-Ended Measurement (BW, input C, input R) |
|----------------------------------------------------------------------------|---------------------------------------------|----------------------------------------------------|----------------------------------------------------|
| Differential solder-in (Higher loading, high frequency response variation) | E2677A | 12 GHz, 0.27 pF, 50 kOhm | 12 GHz, 0.44 pF, 25 kOhm |
| Differential socket (Higher loading) | E2678A | 12 GHz, 0.34 pF, 50 kOhm | 7 GHz, 0.56 pF, 25 kOhm |
| Differential browser - wide span | E2675A | 6 GHz, 0.32 pF, 50 kOhm | 6 GHz, 0.57 pF, 25 kOhm |
| Differential kit | E2669A (includes E2675A, E2677A and E2678A) | | |

Index

| Numerics | HS Clock TX Common-Level Variations Above 450 MHz, 72, 190, 269 | Probing for High Speed Data Transmitter Electrical Tests, 46, |
|---------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|----------------------------------------------------------------------|
| 15%-85% Fall Time Level (TFLP), 95, 201, 287 | HS Clock TX Common-Level Variations Between 50-450 MHz, 74, 190, 269 | 182, 254 Probing for High Speed Data-Clock |
| 15%-85% Rise Time Level (TRLP), 94, 200, 286 | HS Clock TX Differential Voltage, 76, 190, 269 | Timing Tests, 162, 242, 330, 336 Probing for Low Power Transmitter |
| С | HS Clock TX Differential Voltage Mismatch, 78, 190, 269 HS Clock TX Single-Ended Output | Electrical Tests, 88, 106, 194, 212, 280, 298 |
| calibrating the oscilloscope, 349 CLK TX TCLK-POST, 148, 236, 324 | High Voltage, 80, 190, 269 HS Clock TX Static Common Mode | R |
| CLK TX TCLK-PRE, 146, 236, 324 CLK TX TCLK-PREPARE, 142, 236, 324 | Voltage, 68, 190, 269 HS Clock TX VCMTX Mismatch, 70, 190, 269 | RAM reliability test software, 3 report, 38 |
| CLK TX TCLK-PREPARE+TCLK-ZERO, 144, 236, 324 | HS Data Eye Height (Informative) Test, 172, 248, 346 | required equipment and software, 3 results, 38 run tests, 38 |
| CLK TX TCLK-TRAIL, 150, 236, 324 CLK TX TLPX, 140, 236, 324 | HS Data Eye Width (Informative) Test, 174 | |
| Clock Lane HS Clock Delta UI (UI variation), 192, 277 | HS Data TX 20%-80% Rise Time, 63, 185, 258 | S calcut touts 20 |
| Common Level Variations Above 450 MHz, 53, 185, 257 | HTML report, 38 | select tests, 38 start the MIPI D-PHY Conformance |
| Common Level Variations Between 50-450 MHz, 55, 185, 257 | 1 | Test Application, 37 |
| configure, 38 connect, 38 | in this book, 4 | T |
| | K | Thevenin Output High Voltage Level, 90, 108, 196, 214, 282, 300 |
| Data TX TEOT, 133, 232, 319 | keyboard, 3 | Thevenin Output Low Voltage Level, 92, 110, 198, 216, 284, 302 |
| Data TX THS-EXIT, 135, 232, 319 Data TX THS-PREPARE, 125, 232, 318 | L | TLPX, 124, 232, 318 TREOT, 152, 236, 324 |
| Data TX THS-PREPARE + THS-ZERO, 127, 232, 318 | license key, installing, 33 | TSKEW(TX), 165, 244, 332 TX Exclusive-Or Clock |
| Data TX THS-TRAIL, 129, 232, 318 differential browser, 3, 367 | LP TX 15%-85% Rise Time Level (TRLP), 112, 219, 305 | (TLP-PULSE-TX), 97, 203, 289 TX Period of LP TX Exclusive-OR Clock |
| differential blowser, 3, 367 differential socket, 3, 367 | LP TX Slew Rate vs. CLOAD, 116, 224, 310 | (TLP-PER-TX), 100, 206, 292 TX Slew Rate vs. CLOAD, 102, 208, 294 |
| differential solder-in probe head, 3, | M | V |
| | mouse, 3 | VCMTX, 49, 68, 185, 190, 257, 269 |
| First Dayland Dit 164 244 222 | Р | VCMTX Mismatch Test, 51, 185, 257 VOD, 57, 185, 257 |
| First Payload Bit, 164, 244, 332 | Probing for Clock TX Global Operation | VOHHS, 61, 185, 257 |
| Н | Tests, 138, 234, 322 | |
| HS Clock Instantaneous, 84, 191, 276 HS Clock TX 20%-80% Fall Time | Probing for Data TX Global Operation Tests, 122, 230, 316 Probing for High Speed Clock | |
| (tF), 83, 191, 273 HS Clock TX 20%-80% Rise Time (tR), 82, 190, 270 | Transmitter Electrical Tests, 66, 188, 267 | |
| | | |

Index