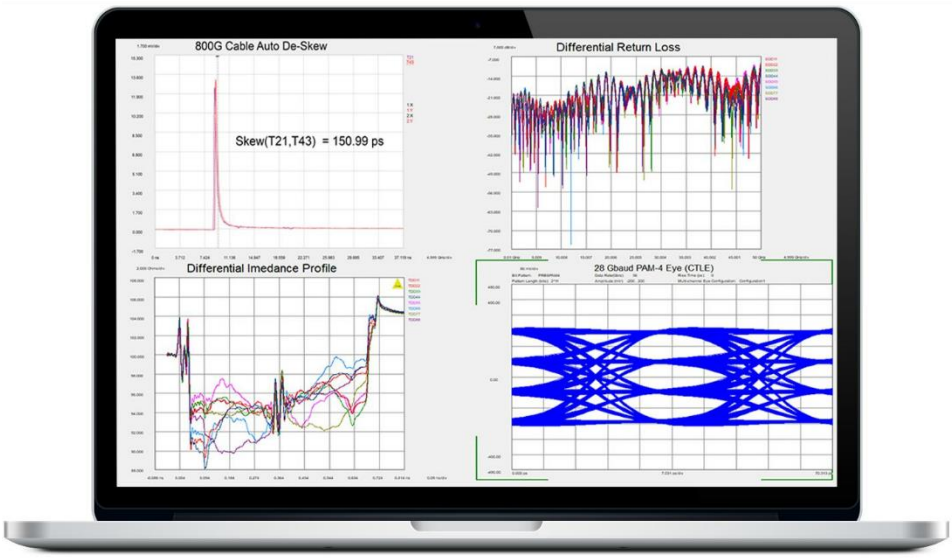
Physical Layer Test System (PLTS) 2025

Include data collection & analysis software for frequency and time domain data with optional instrument control

Introduction

The Physical Layer Test System (PLTS) is the industry standard for signal integrity measurements and data post-processing tools for high-speed interconnects such as cables, backplanes, PCBs, and connectors. Many signal integrity laboratories around the world have benefited from the power of PLTS in the R&D prototype test phase and high-volume manufacturing phases. Today's 1.6 Tbps internet infrastructure demands multiport channel analysis to mitigate crosstalk issues that can cause bit errors. The new PLTS 2025 has now migrated to a powerful 64-bit application that enables deeper memory for large data files and achieves 16- or 32-port S-parameter measurements.



KEYSIGHT

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Why is physical layer testing required?

The next generation computer and communication systems now being developed will handle data rates of multiple gigabits/second. Many systems will incorporate processors and SERDES chip sets that exceed Gigahertz clock frequencies. New and troubling input/output issues are emerging as switches, routers, server blades, and storage area networking equipment moving toward 800 Gbps data rates. Digital design engineers choosing chip-to-chip, chip-to-module and backplane technologies for these systems are finding signal integrity challenges that have not been encountered before.

Traditional parallel bus topologies have run out of bandwidth. As parallel busses become wider, the complexity and cost to route on PC boards increase dramatically. The growing skew between data and clock lines has become increasingly difficult to resolve within parallel busses. The solution is fast serial channels. The newer serial bus structure has quickly replaced the parallel bus structure for high-speed digital systems. Engineers have been turning to a multitude of gigabit serial interconnect protocols with embedded clocking to achieve the goal of simple routing and more bandwidth per channel. However, these serial differential interconnects bring their own set of problems.

In order to maintain the same total bandwidth as the older parallel bus, the new serial bus needs to increase its data rate. As the data rate increases through serial interconnects, the rise time of the data transition from a zero-logic level to a one logic level becomes shorter. This shorter rise time creates larger reflections at impedance discontinuities and degrade the eye diagram at the end of the channel. As a result, physical layer components such as printed circuit board traces, connectors, cables, and IC packages can no longer be ignored. In fact, in many cases, the silicon is so fast that the physical layer device has become the bottleneck.

In order to maintain signal integrity throughout the complete channel, engineers are moving away from single- ended circuits and now use differential circuits. The differential circuit provides good Common Mode Rejection Ratio (CMRR) and helps shield adjacent PCB traces from crosstalk. Properly designed differential transmission lines will minimize the undesirable effect of mode conversion and enhance the maximum data rate throughput possible. Unfortunately, differential signaling technology is not always an intuitive science.

Differential transmission lines coupled with the microwave effects of high-speed data have created the need for new design and validation tools for the digital design engineer. Understanding the fundamental properties of signal propagation through measurement and post measurement analysis is mandatory for today's leading- edge telecommunication and computer systems. The traditional Time Domain Reflectometer (TDR) is still a very useful tool, but many times the Vector Network Analyzer (VNA) is needed for the complete characterization of physical layer components. There is a strong need for a test and measurement system that will allow simple characterization of complex microwave behavior seen in high-speed digital interconnects. In fact, many digital standards groups have now recognized the importance of specifying frequency domain physical layer measurements as a compliance requirement.

Many high-speed protocols have adopted the SDD21 parameter (input differential insertion loss) as a required measurement to ensure channel compliance (Figure 3). This parameter is an indication of the frequency response that the differential signal sees as it propagates through the highspeed serial channel. An example of a proposed SDD21 compliance mask is shown in Figure 1 for the Channel Electrical Interface (CEI) working group for the Optical Internetworking Forum (OIF).

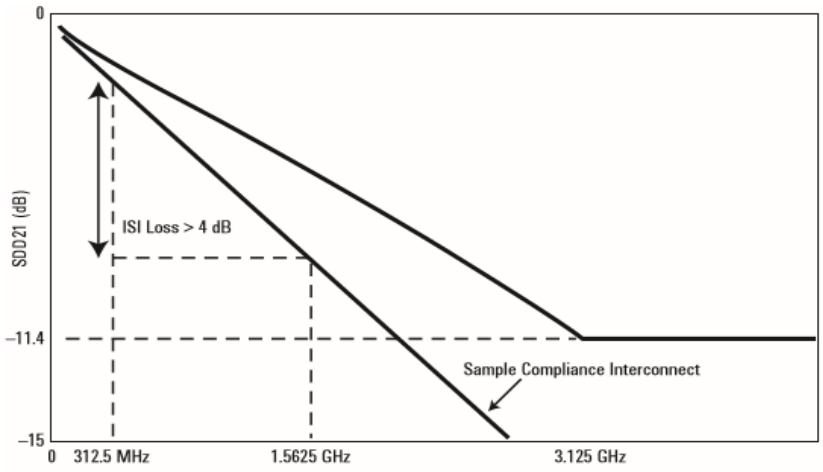


Figure 2. Many digital standards are now using frequency domain measurements for compliance testing, such as this input differential insertion loss (SDD21) mask

A single test system can provide the total view

As the combination of both time-domain and frequency domain analysis becomes more important, the need for multiple test systems becomes difficult to manage. A single test system that can fully characterize differential high-speed digital devices, while leaving domain and format of the analysis up to the designer, is a very powerful tool. Keysight's Physical Layer Test System (PLTS) is designed specifically for this purpose.

PLTS has been designed specifically for signal integrity analysis. PLTS software guides the user through hardware setup and calibration and controls the data acquisition. It automatically applies patented transformation algorithms to present the data in both frequency and time domains, in both forward and reverse transmission and reflection terms, and in all possible modes of operation (single ended, differential, and mode-conversion).

A powerful virtual bit pattern generator feature allows a user-defined binary sequence to be applied to the measured data to convolve eye pattern diagrams. Next, highly accurate RLCG models can be extracted and used to enhance the accuracy of your models and simulations. While PLTS is predominantly an R&D tool, a SCPI interface with a rich set of commands enables remote and manufacturing applications. Also, manufacturing applications benefit from the custom characterization report inside PLTS that allows users to document all multi-domain data required automatically.

PLTS provides design confidence through complete characterization

Physical-layer structures have increasingly become the bottleneck in high-speed digital system performance. At low data rates, these interconnects are electrically short. The driver and receiver are typically the biggest contributors to signal integrity. But as clock speeds, bus speeds, and link speeds all push past the gigabit-per-second mark, physical layer characterization becomes more critical. These interconnects become microwave transmission lines and need to be characterized carefully to avoid internet infrastructure failure.

Another challenge for today's digital designers is the trend to differential topologies. Fully understanding device performance requires analysis in all possible modes of operation.

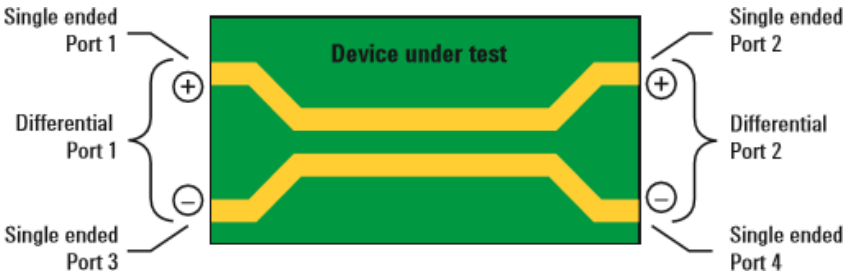


Figure 3. A differential structure operates in many modes. Single-ended analysis can reveal sources of asymmetry on this differential transmission line.

Time-domain analysis is typically used for characterization of these physical-layer structures, but often, the designer concentrates only on the intended modes of operation. For a complete time-domain view, step and impulse responses in reflection and transmission (TDR and TDT) must be seen. The analysis must include the unintended modes of operation as well.

Frequency-domain analysis, again in all possible modes of operation, is also necessary for fully characterizing these physical-layer structures. The s-parameter model describes the analog behavior exhibited by these digital structures. This behavior includes reflections from discontinuities, frequency dependent losses, crosstalk, and EMI performance.

For translating device performance into standards compliance, eye diagrams add an important statistical analysis. And for leveraging this complete characterization into improved simulations, measurement-based s-parameter or RLCG model extraction completes the picture.

Table 1. Complete characterization includes forward and reverse transmission and reflection, in all possible modes of operation, in both frequency and time domains

	Time Doman		Frequency Domain	
Mode	TDR	TDT	Reflection	Transmission
Differential	TDD11 TDD22	TDD21 TDD12	SDD11 SDD22	SDD21 SDD12
Diff-to-comm	TCD11 TCD22	TCD21 TCD22	SCD11 SCD22	SCD21 SCD12
Comm to diff	TDC11 TDC22	TDC21 TDC12	SDC11 SDC22	SDC21 SDC12
Common	TCC11 TCC22	TCC21 TCC12	SCC11 SCC22	SCC21 SCC12
Single-ended	T11 T22 T33 T44	T21 T31 T41 T12 T32 T42 T13 T23 T43 T14 T24 T34	S11 S22 S33 S44	S21 S31 S41 S12 S32 S42 S13 S23 S43 S14 S24 S34

1. An RLCG equivalent circuit model, also known as Telegrapher's Parameters, describes the electrical behavior of a passive transmission line. The model is a distributed network consisting of series resistance and inductance (R and L) and parallel capacitance and conductance (C and G).

PLTS enables mode-conversion analysis for early insight into EMI problems

The benefits of differential signaling include lower voltage swings, immunity from power supply noise, a reduced dependency on RF ground, and improved EMI performance (reduced generation and susceptibility). The extent to which a device can take advantage of these benefits is directly related to device symmetry.

Symmetric devices only respond to, and only generate differential signals. These ideal devices do not respond to or generate common-mode signals, and they reject radiated external signals (i.e., power supply noise, harmonics of digital clocks or data, and EMI from other RF circuitry).

Asymmetric devices, however, do not exhibit these benefits. When stimulated differentially, an asymmetric device will produce a common-mode response in addition to the intended differential response, and cause EMI radiation. Conversely, with a common-mode stimulus, an asymmetric device will produce an unintended differential response. This mode conversion is a source of EMI susceptibility.

Mode-conversion analysis is an important tool for understanding and improving device symmetry and provides the designer with early insight to identify and resolve EMI problems at the design stage (Figure 5).

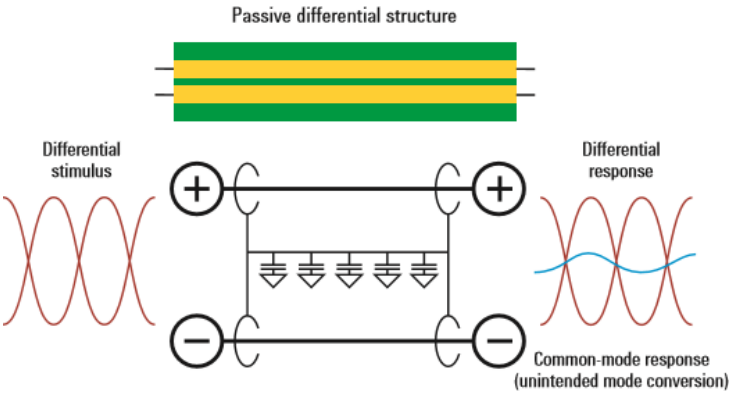


Figure 4. The new enhanced mode conversion algorithm greatly improves differential response.

> “PLTS 2025 is used in many high-speed digital applications worldwide including 800G Ethernet, Fibre Channel, Automotive Ethernet, USB Type-C, PCIe, DDR, HDMI, SATA, Thunderbolt, and many more.”

Mode conversion

A practical application of how mode conversion helps identify problems in physical layer devices is shown in Figure 5. This shows a XAUI backplane with two daughter cards that typically transmit data at

3.125 Gbps. The design objective for this high-speed differential channel is to minimize the crosstalk between adjacent differential PCB traces throughout the length of the channel. The channel consists of the linear passive combination of the backplane and two daughter cards. Any mode conversion from differential mode to common mode will generate EMI and create crosstalk that will be incident upon other channels and will degrade performance. However, locating the exact structure within the channel that creates the most mode conversion is not simple.

Looking at figure 5, the differential to common mode conversion time domain reflection parameter (TCD11) is time aligned with the differential impedance profile of the channel (TDD11) below it. A marker is placed on the largest magnitude peak of TCD11. This is where the physical structure within the channel is creating the most mode conversion and thus the source of the most crosstalk. We can align the TDD11 to the TCD11 in time and therefore co-locate the problematic structure on TDD11. To relate this structure to the channel, we use the differential impedance profile as a reference. From previous analysis, we know that the two capacitive discontinuities on TDD11 are the daughter card via field and motherboard via field, respectively. Since the marker falls upon the second discontinuity on TDD11, it is deduced that the motherboard via field is the biggest culprit to causing crosstalk in adjacent channels.

This shows how identifying the mode conversion in a channel can be intuitive with proper analysis.

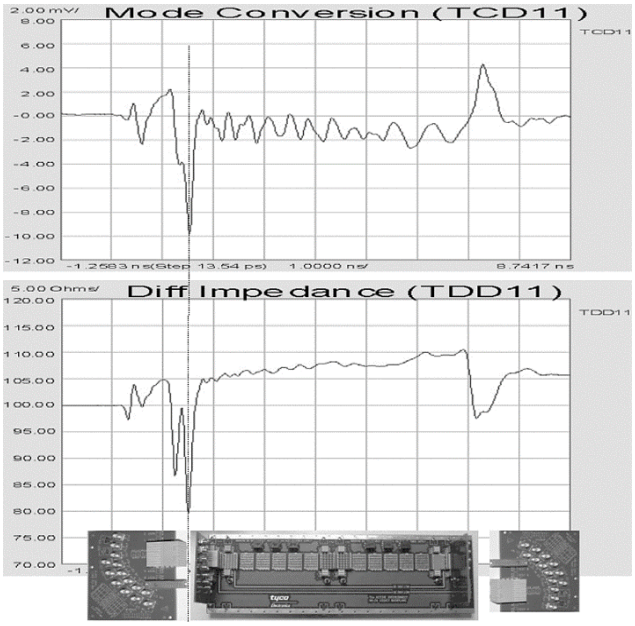


Figure 5. By aligning the impedance profile with the mode conversion profile, PLTS allows the pinpointing of crosstalk-generating structures within physical layer devices.

Remove unwanted effects from the measurement

Error correction

Over the years, many different approaches have been developed for removing the effects of the test fixture from the measurement (shown in Figure 7). The level of difficulty for each error correction technique is linearly related to the accuracy of each method. Time domain gating is perhaps the simplest and most straightforward method, but it is also the least accurate. Likewise, de-embedding is the most complicated method, but it is the most accurate. It is important to have a test system that will allow flexibility of choosing the method of error correction desired for each application

Error correction techniques fall into two fundamental categories: direct measurement (pre-measurement processing) and de-embedding (post-measurement processing). Direct measurement requires specialized calibration standards that are connected to the end of a coaxial test cable and measured.

The accuracy of the device measurement relies on the quality of these physical standards. De-embedding uses a model of the test fixture and mathematically removes the fixture characteristics from the overall measurement. This fixture de-embedding procedure can produce very accurate results.

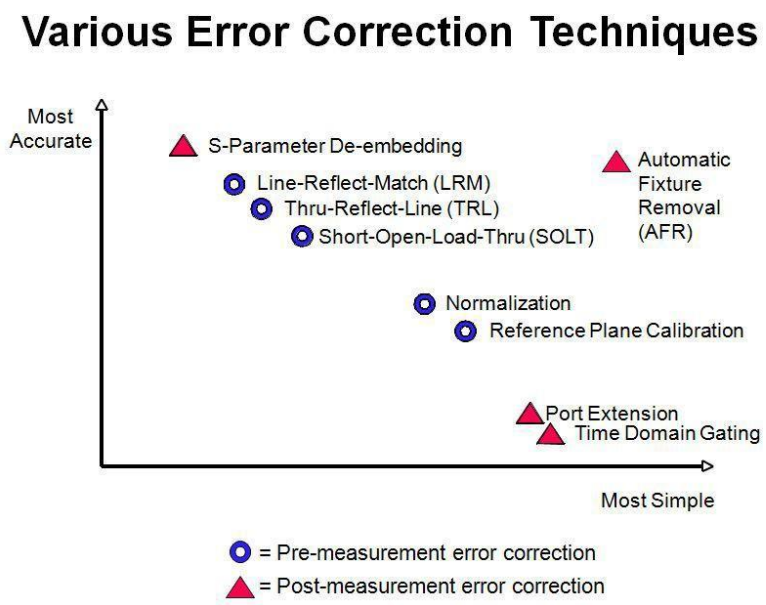


Figure 6. PLTS has advanced error correction techniques to allow flexibility for many applications

Port Extension (also known as Phase Rotation) mathematically extends the calibration reference plane to the DUT.

This technique is easy to use but assumes the fixture – the unwanted structure – looks like a perfect transmission line: a flat magnitude response, a linear phase response, and constant impedance. If the fixture is very well designed, this technique can provide good results.

Because gating essentially considers the magnitude of the unwanted discontinuity, and Port Extensions consider phase (electrical length), using the two tools together may provide optimum results.

Time-domain gating (Figure 7) is like port extension, in that it is also very easy and fast. The user simply defines two points in time or distance, and the software mathematically replaces the actual measured data in that section with data representing an "ideal" transmission line. The return loss is then recalculated to show the effects of the change in the frequency domain.

One practical application of time-domain gating is as a confidence check before replacing a suspect connector.

Figure 7 illustrates how this technique might be used.

De-embedding (Figure 8) uses an accurate linear model of the fixture, or measured s-parameter data of the fixture. This fixture data can then be removed mathematically from the DUT measurement data in post-processing.

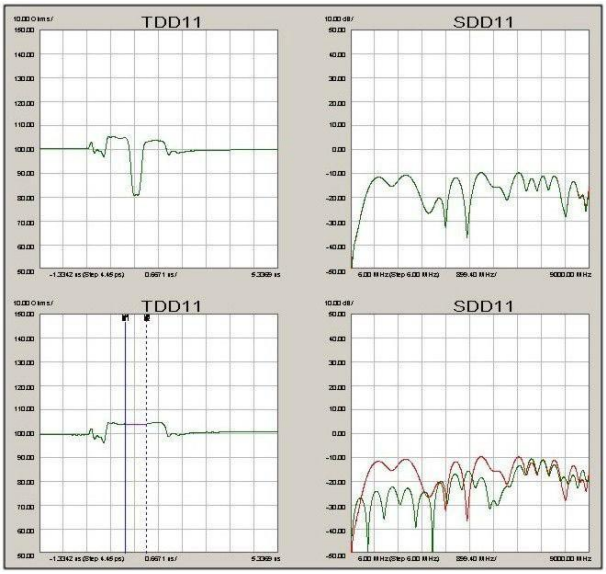


Figure 7. In this rather extreme example of time-domain gating, the top plots show the measured differential step impedance and return loss. The lower left plot shows a gate added to remove the large discontinuity in the center of the trace. On the lower right, the measured and the recalculated return losses are displayed. In this case, the gate improved the return loss by more than 10 dB within the frequency band of interest.

Calibration at the DUT reference plane has the advantage that the precise characteristics of the fixture do not need to be known beforehand, as they are measured and corrected for during the calibration process.

An example of this technique is microprobing using a calibration substrate, where the calibration reference plane is established at the probe tips, rather than at the end of the coaxial test cables.

Advanced calibration techniques (TRL/LRM) –originally developed for wafer probing applications – provide additional options.

PLTS Key Features

Automatic Fixture Removal (AFR)

As shown in figure below, Automatic Fixture Removal is the most accurate method of de-embedding a test fixture with the most ease-of-use. Keysight invented this technology years ago and continues to improve the AFR algorithm to enhance accuracy. The latest version of AFR inside accounts for such subtle effects as mode conversion within a poorly designed test fixture. For additional details in this innovative de-embedding method, please refer to our Technical Document entitled, “The ABC’s of AFR” found in the PLTS Technical Library here: www.keysight.com/find/plts.

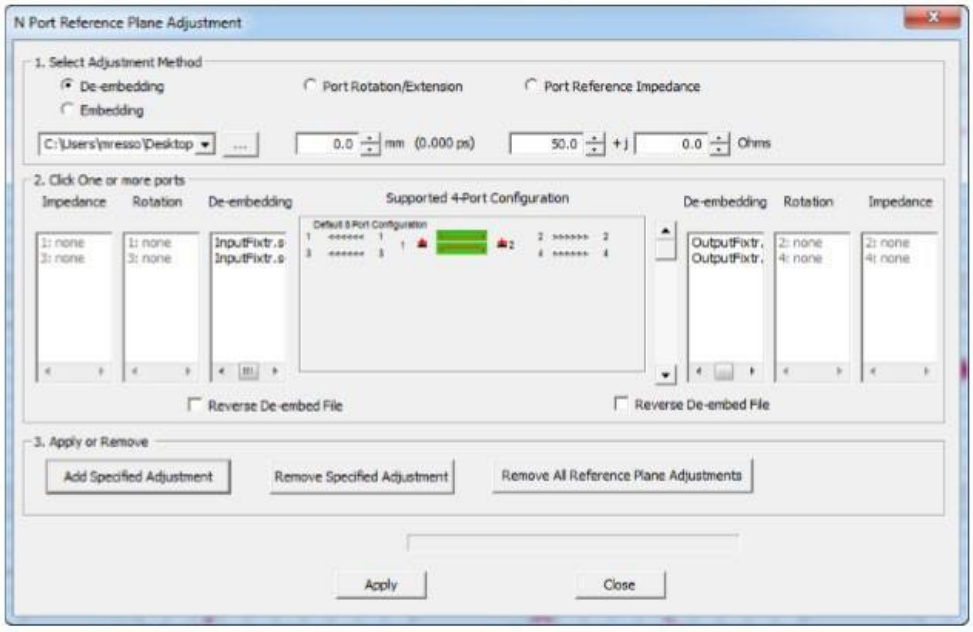


Figure 8. The effects of test fixtures can be removed from the device in post-processing through de-embedding.

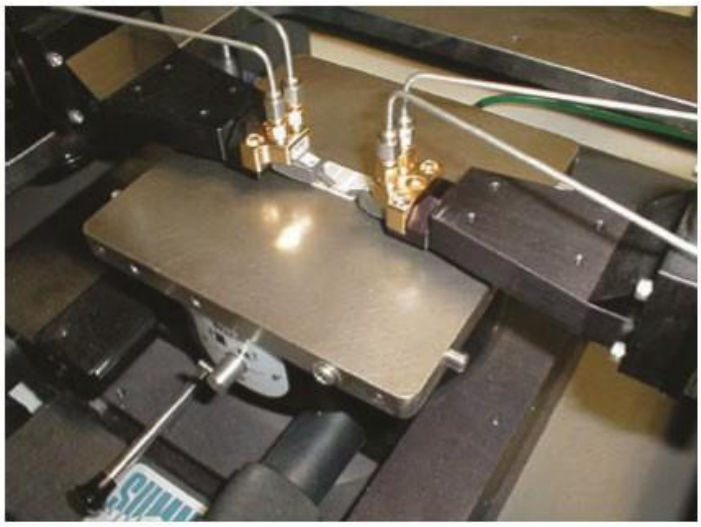


Figure 9. A microprobing application, where the calibration is performed using an impedance standard substrate, establishes the calibration reference plane at the probe tips.

PLTS support for microprobing applications

Keysight works closely with leading microprobe and probe station suppliers to provide the best complete system solutions possible.

One of the most significant measurement challenges is connectivity. Test equipment provides a controlled coaxial environment, but what if the DUT – the backplane, the interface connector, the IC package – is non-coaxial?

Test fixtures can provide the required connectivity, but at a cost. The quality of the test fixture – its connectors, impedance discontinuities, parasitics, and dielectric losses – all contribute to less than ideal performance of the fixture. Subsequently, the accuracy of the device measurement is degraded.

Several techniques are available to remove these fixture effects (see Remove Unwanted Effects from the Measurement on page 6), but the accuracy of these techniques is greatly impacted by the quality of the fixture itself, or the availability of an accurate s- parameter model of the fixture (used for de- embedding). Microprobing can offer the user the ability to forego the test fixture and launch the stimulus directly at the device input. The response can be measured directly at the device output. Additionally, when calibration substrates are available, calibration can be performed directly at the probe tips. This achieves co-location of the calibration reference plane with the device measurement reference plane.

PLTS has the flexibility to accommodate many microprobe configurations. By adding the calibration substrate coefficients as a calibration kit, the process becomes as straightforward as a coaxial calibration.

Figure 10. Cascade Microtech's Summit probe station

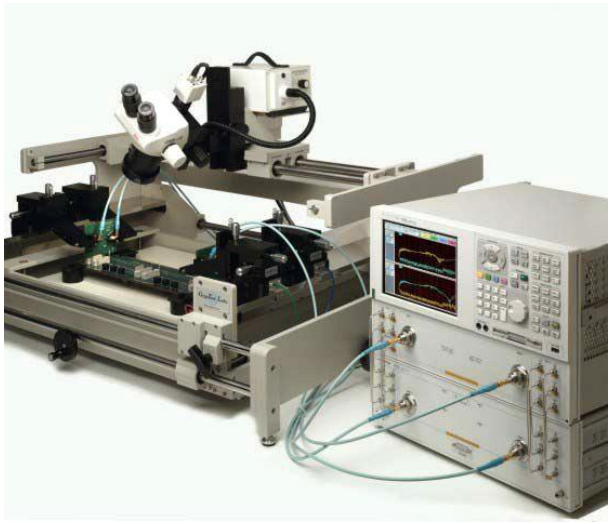


Figure 11. GigaTest lab's GT-4060 probe station

PLTS simplifies the measurement process

Device characterization with PLTS software is straight-forward. The user interface has been designed to make setup, calibration, and measurement intuitive and error-free. A wizard guides the user through all the required steps. The last prompt is to connect the device under-test and initiate the measurement. Setup and calibration differ slightly between TDR-based and VNA based systems. However, in both cases the PLTS software provides an intuitive wizard to assist in the step-by- step process.

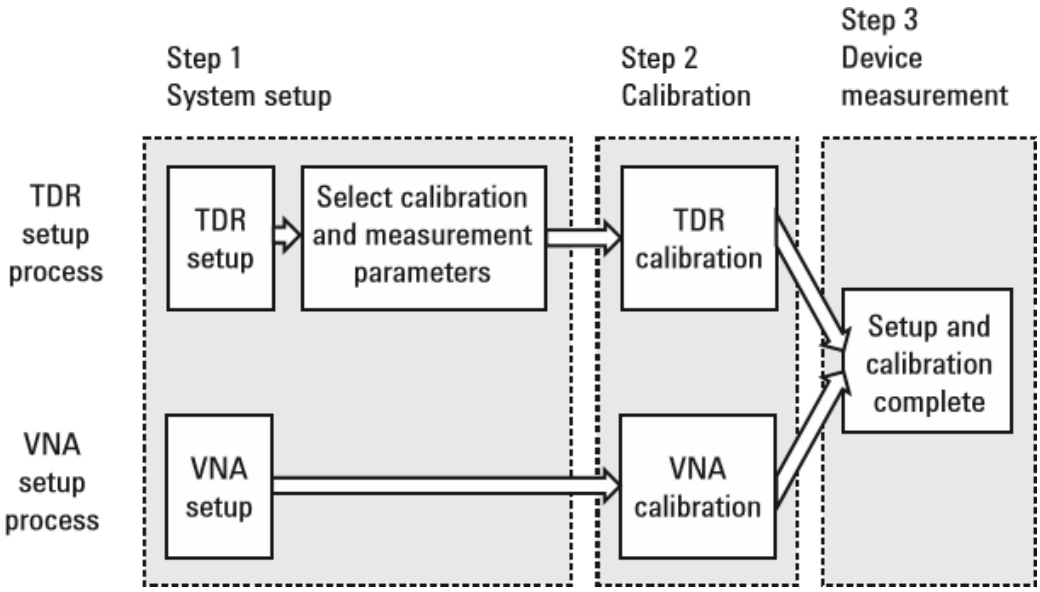


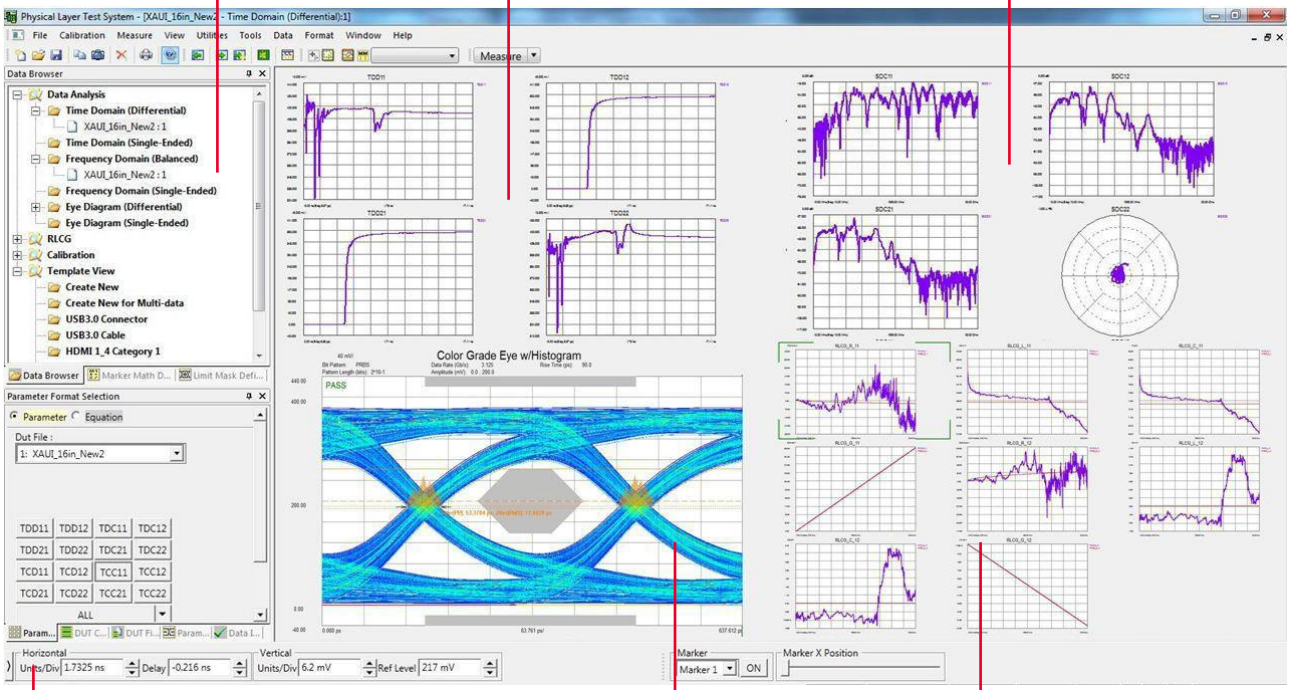
Figure 12. PLTS has a three-step system set up to make measurements intuitive and error-free

Data analysis with N-port PLTS

File and view management with the data browser

Time domain analysis:
• 2 n^2 parameters
• 7 formats
• time or distance

Frequency domain analysis:
• 2 n^2 parameters
• 8 formats



Format, scaling, and marker control with easy access toolbars

Plot and trace management with context-sensitive parameter buttons

Eye diagram analysis:
• 2 n^2 parameters
• 8 formats

RLCG model extraction:
• 2 n^2 parameters

Data analysis

All supported analysis types and formats are available immediately after the measurement is completed, and at any time thereafter. PLTS flexibility allows the user to begin where they are most familiar.

Time-domain analysis

The mixed-mode time domain is a common starting point. Initially, sixteen parameters are displayed in thumbnail view as shown below. These thumbnails represent four modes of device operation: differential, common-mode, and the two mode-conversion types (common-mode stimulus with differential response and differential stimulus with common-mode response). A double mouse click on any of these thumbnails will expand the selected parameter to full screen for closer analysis.

Not shown here are the additional sixteen single- ended time-domain parameters.

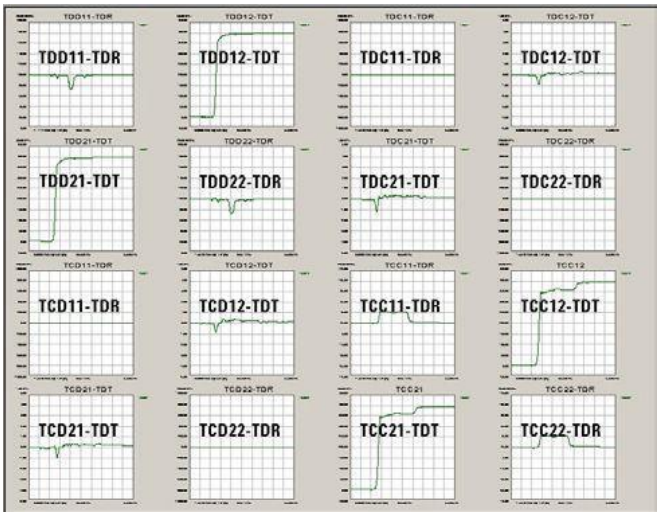


Figure 13. The mixed-mode time-domain matrix

Frequency-domain analysis

The mixed-mode frequency domain is another common starting point. Initially, sixteen parameters are displayed in thumbnail view as shown below. These thumbnails represent four modes of device operation: differential, common- mode, and the two mode-conversion types (common- mode stimulus with differential response and differential stimulus with common-mode response). A double mouse-click on any of these thumbnails will expand the selected parameter to full screen for close analysis.

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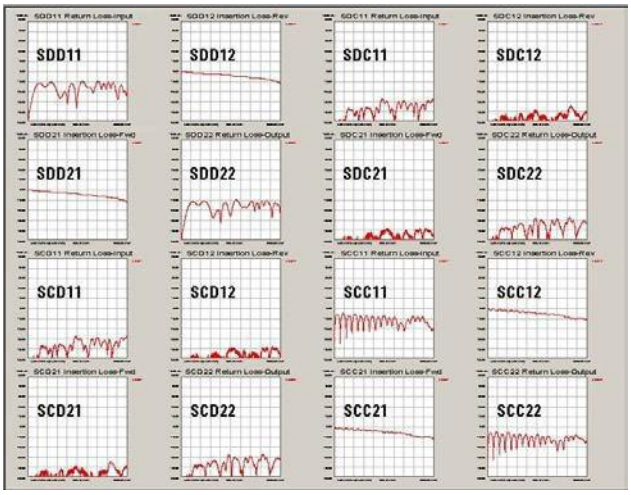


Figure 14. The mixed-mode frequency-domain matrix.

Measurement-based Eye Diagram Analysis

Using the built-in digital pattern generator, the user can define virtual bit pattern (as wide as 2^32-1 bits). PLTS then convolves the selected bit pattern with the device impulse response to create an extremely accurate measurement-based eye pattern diagram.

This eliminates the need for a hardware pulse/pattern generator, and its flexibility allows for a great deal of "What if…" analysis.

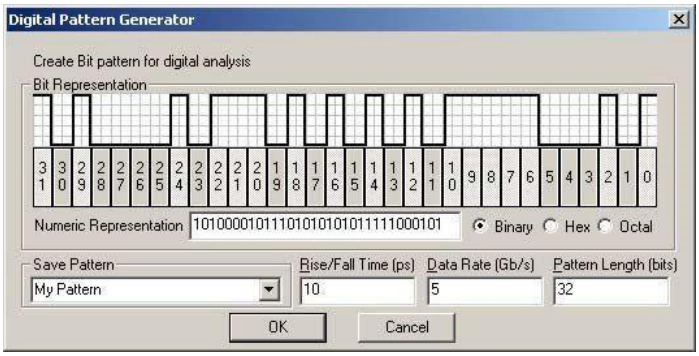


Figure 15. The digital pattern generator.

After the eye pattern is generated, marker functions can be used to make typical measurements like jitter, eye opening, rise and fall times, and more.

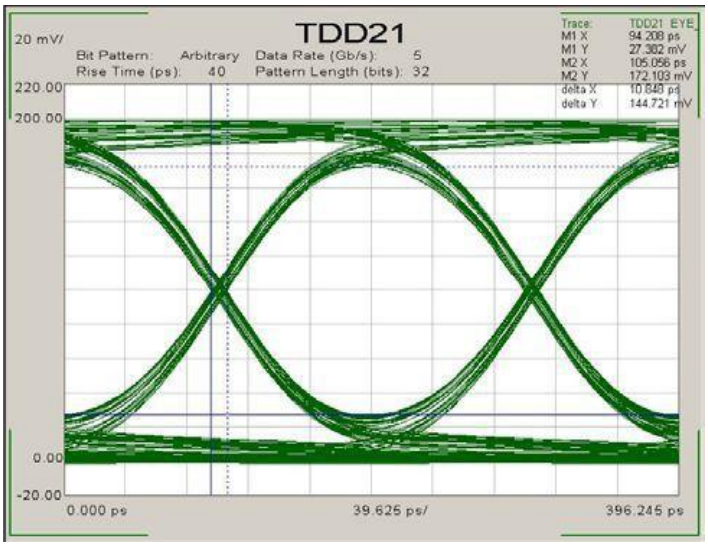


Figure 16. Eye pattern diagram.

Multi-channel simulation

The standard PLTS eye diagram is using an ideal data source (no jitter, no noise) to simulate the overlapped waveform data of the NRZ (non-return-zero) signals as well as PAM4 signals transmitted through the measured backplane channel. To add advanced eye diagram capabilities, PLTS has a powerful feature to modify the Tx (transmitter) and Rx (receiver), and to add Xtalk (crosstalk) and inject jitter effects to simulate real-world applications. This multi-channel simulation can quickly and efficiently simulate the following conditions:

- Specify bit pattern settings for data sources (either Tx or Xtalk) – Inject jitter to the data sources, the jitter includes RJ (random jitter), PJ (periodic jitter) and ISI (inter-symbol interference or so-called Dirac jitter)
- Add source noise by specifying SNR (signal-to-noise ratio per symbol).
- Add source equalization (the same meaning with pre-emphasis/de-emphasis).
- Add Rx multiple equalization types of CTLE, FFE, and DFE (automatically or specify the taps manually).
- Add Xtalk effects from sources on other ports.
- Import IBIS-AMI models for TX and RX for advanced channel analysis

PLTS uses MATLAB to add jitter, noise, Tx and Rx equalization in this fashion: PLTS invokes a MATLAB dynamic link library in the background for doing the multi-channel eye simulation. For this feature, only the MATLAB Compiler Runtime (MCR) needs to be installed, and that has been included in PLTS install package.

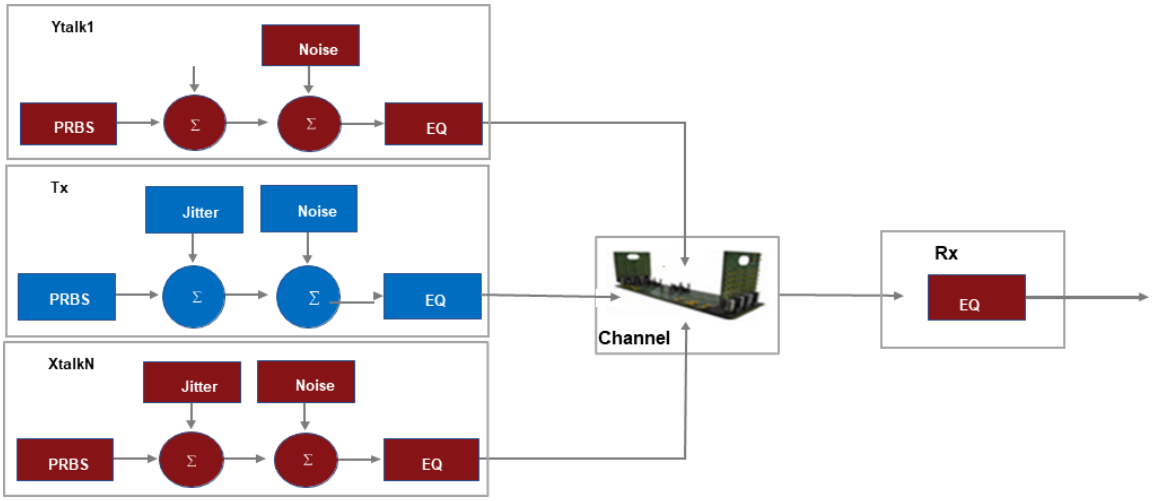


Figure 17. Multi-Channel Simulation is a fast and simple simulation engine specifically designed for high-speed digital interconnect channels. It allows quick results with a minimal learning curve yet provides powerful capabilities with full transmitter and receiver customization. Even IBIS-AMI models of transmitters and receivers are utilized for application specific chipset analysis.

Detailed functionalities

Open or import a data set ([DEMO] E8364B 12-port 10 MHz-20 GHz. dut for example) and view the data in frequency domain single-ended analysis mode, then go to the eye diagram view (either differential or single-ended). Now the menu of <Tools>-><Multi-channel Eye Diagram> is enabled.

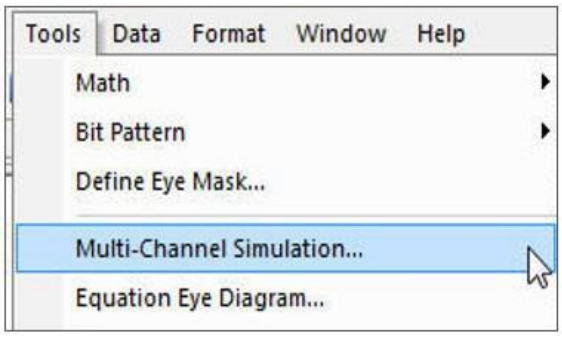


Figure 18. To activate Multi-Channel Simulation mode, select it from the Tools Menu.

Click on the menu and the window below pops up:

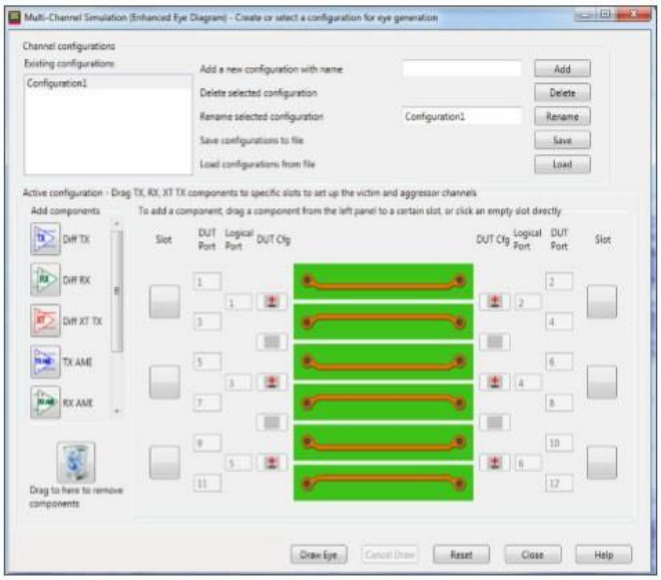


Figure 19. Main dialog box for Multi-Channel Simulation mode.

Multi-channel eye diagram configuration: including the DUT configuration and the channel setup. The channel setup includes the information on which ports the Tx, Rx and Xtalks are added and the detailed settings of the Tx, Rx and Xtalks.

The multi-channel eye diagram configuration is dependent on a specific DUT configuration, if you select another data set with a different DUT configuration, this window will automatically update the multi-channel eye diagram configurations that match the current DUT configuration in the list. This also means you can use one configuration to simulate the eye diagrams of many data sets with the same DUT configuration.

From the Buttons you can Add, Delete, Rename, Save, Load configurations.

Channel setup

The simulation channels can be set up by dragging Tx, Rx and Xtalk components to specific slots. To start the simulation, there must be one Tx, one Rx, 0~N Xtalks. In the configuration below, a transmission channel of SDD43 and two Xtalk channels of SDD41 and SDD45 were set up.

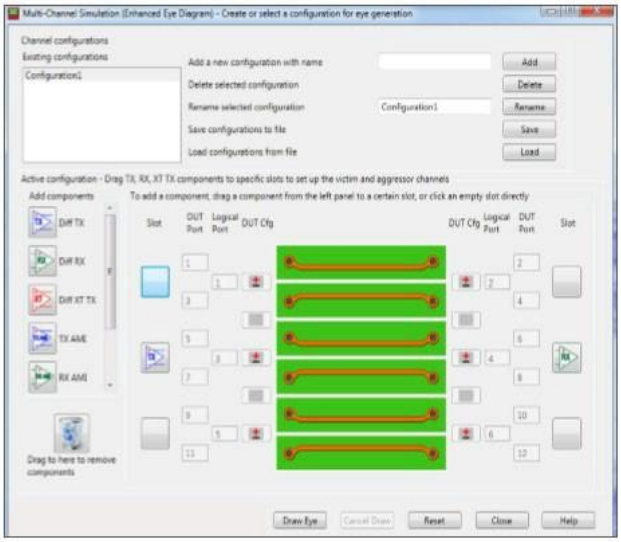
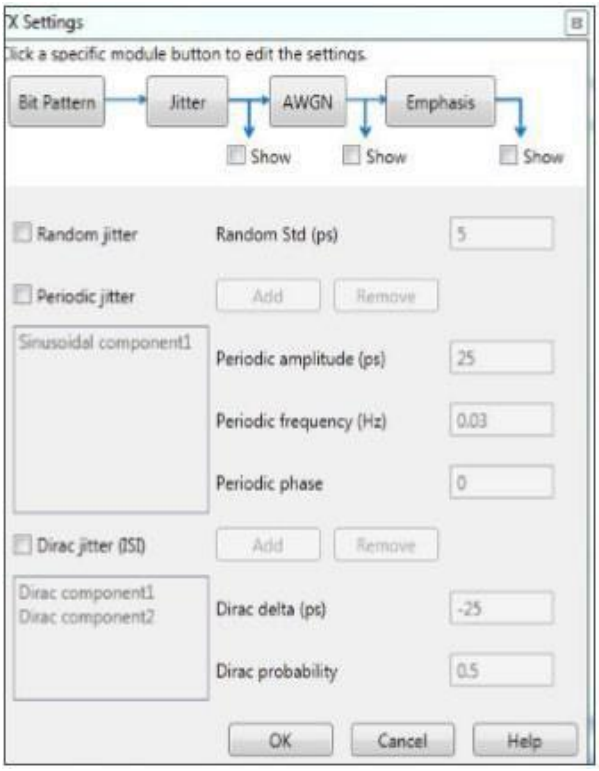


Figure 20. Near-end and far-end crosstalk simulation is simple and fast.

1.2 Tx Settings

Click on the added Tx module (blue button) or right-click on it and select “Edit”, one can change the Tx settings.



1. Ports - specify which port this module is added on. If you change the port number, the module will be moved to the new port specified.
2. Pattern - bit pattern settings.
3. Jitter - timing jitter is defined as the deviation of a signal’s timing clock from the ideal clock. Timing jitter can be divided into two main subcategories: deterministic and random jitter.
4. Equalization - in serial data transmission, pre-emphasis/ de-emphasis is often used to compensate for losses over the channel which is larger at higher frequencies. The high frequency content is emphasized compared to the low frequency content which is de- emphasized. This is a form of transmitter equalization.

Figure 21. Transmitter and Receiver settings can be edited for pre-emphasis, jitter injection, noise injection, and multitude of equalization types.

RLCG model extraction

RLCG (resistance, inductance, capacitance, and conductance) models describe the electrical behavior of passive transmission lines in an equivalent circuit model.

From the measured S-parameters of a device, PLTS calculates the R, L, C, G, complex propagation constant, and complex characteristic impedance.

This provides a highly accurate, measurement-based coupled transmission line model for export into modeling and simulation software such as Keysight ADS, Synopsis HSPICE, and others.

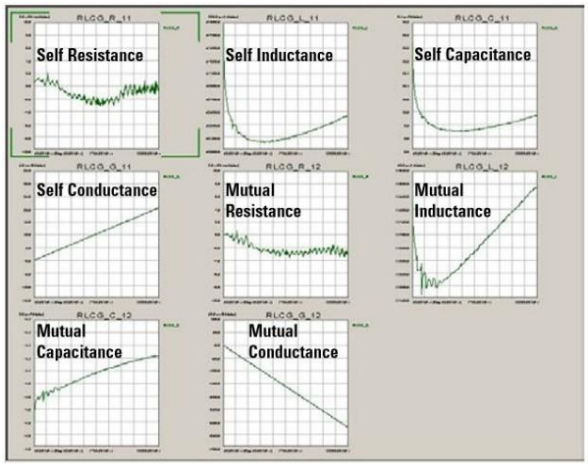


Figure 22. RLCG model extraction (W-Element shown).

Channel Operating Margin (COM)

As emerging standards become more complex for signal integrity engineers, the tools they use in the SI laboratory must become equally sophisticated. Such revolutionary test and measurement capabilities are now inside the PLTS platform with the additional of Channel Operating Margin (COM). Simply put, the COM MATLAB-based subroutine is automatically run in the background of PLTS based on a standardized configuration spreadsheet defined by the IEEE standards. This enables the design engineer to make component trade-offs inside a given channel design to optimize interoperability. The COM tool in PLTS takes a half-day testing procedure and turns it into a 10-15 minute measurement driven automatically with a graphical user interface. An example of the COM output from PLTS is shown below.

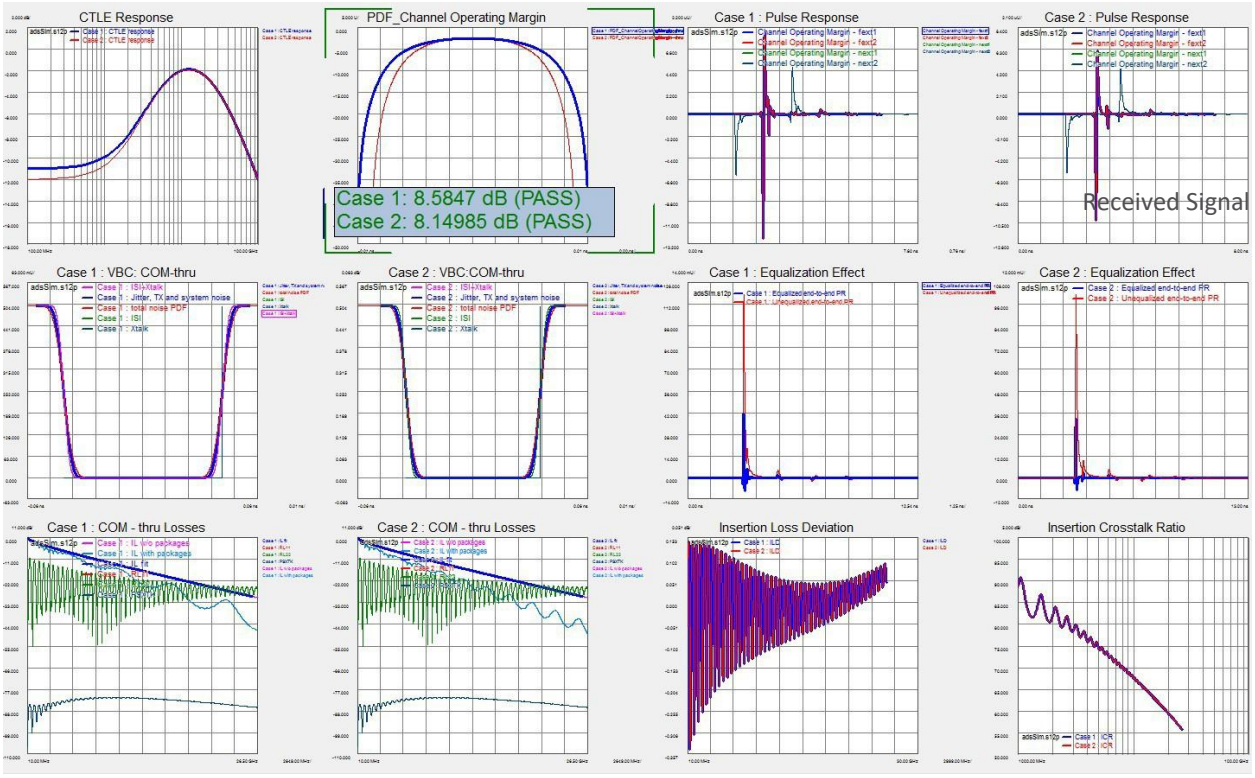
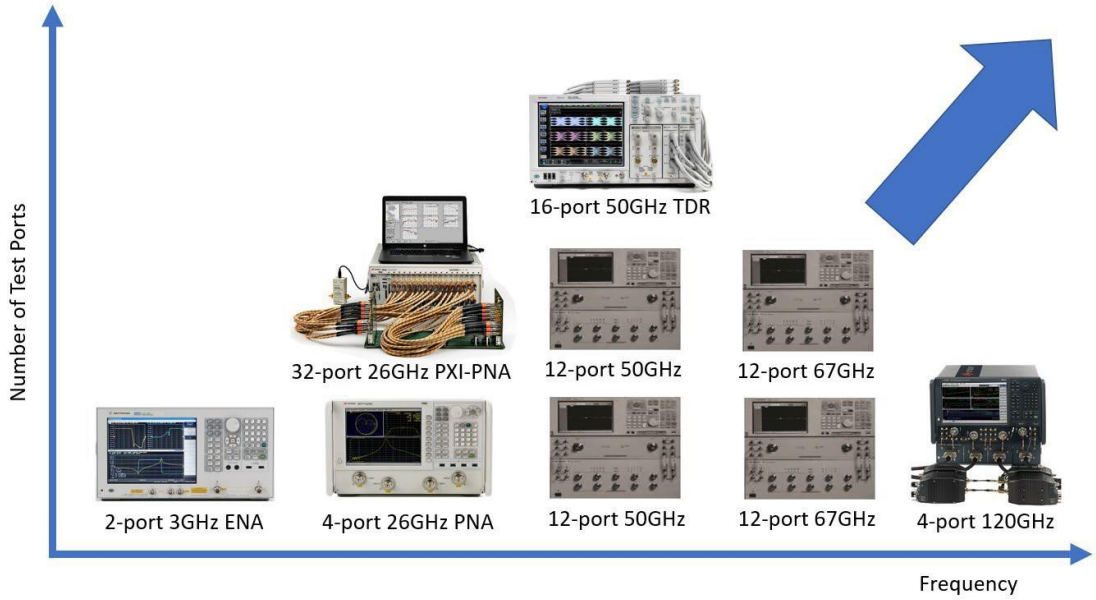


Figure 23. Channel Operating Margin (COM) testing inside PLTS platform enables design engineer to make interoperability trade-off studies to maximize performance/cost ratio in high-speed digital channels.

PLTS Signal Integrity Solutions Portfolio



For all hardware configurations see PNA Family Microwave Network Analyzers Configuration Guide, part number 5992-1465EN.

PLTS Ordering Guide

PLTS system requirements

To ensure that PLTS operates effectively, your PC should have the following minimum requirements:

	Measurement mode ONLY	Off-Line analysis mode
	In the lab, controlling test equipment and making quick analysis of the results	In your office, performing "What if …." Analysis characterization, cross-domain analysis, filtering, waveform math, and eye diagram simulation.
CPU	1.5 GHz Quad-core	1.5 GHz Quad-core
	4 GB	4+ GB
Main memory (RAM)		
Virtual memory – As a general rule, virtual memory should be 1.5 to 2 times the size of main memory	6 GB+	6 GB+
GPIB interface With PLTS 4.2 PLTS can connect to a PNA over LAN	Keysight 82357A USB/GPIB Interface for Windows or supported GPIB card (any National Instruments or Keysight 82340/41 or 82350 GPIB Card)	No GPIB connection is required to use PLTS off-line. Saved (stored) measurement files can be recalled at any time for analysis
Operating systems	Windows 11 64 bit or Windows 10 64 bit	Windows 11 64 bit or Windows 10 64 bit
Screen resolution	1280 x 1024 or greater required	1280 x 1024 or greater required
Display colors	High color (16 Bit) or greater	High color (16 Bit) or greater

VNA support[2]

The following Keysight vector network analyzers are supported by PLTS 2025 Firmware selection may depend on CPU and model number: (http://na.support.keysight.com/pna/cputype.html)

- All PNA (N522xA/B) series
- All PNA-X (N524xA/B) series
- All PNA-L (N523xA/B) series
- All PNA mm-Wave (N5290/91A)
- E5080A/B series
- E5081A series
- E5061B OPT. xL5 (Power Integrity)
- M937xA PXI-VNA
- M980xA PXI-VNA
- M983xA PXI-VNA
- P50xxA/B series USB-VNA
- P937xA/B series USB-VNA
- P938xB series USB-VNA

For the most up-to-date recommended firmware, please go to the Keysight PNA Firmware Support website at http://na.support.keysight.com/pna/firmware/firmware.htm.

E5071C-PLTS compatibility guide

The E5071C VNA is partially supported by PLTS 2025 software. The E5071C can be controlled, calibrated and measured remotely from PLTS software running on an external laptop. All the standard post-processing capability is available such as multi-domain analysis. However, there are some limitations. See list below.

1. PLTS 2025 does not support E5071C measurement collection through Option 5 (advanced calibration with Automatic Fixture Removal). However, AFR can be accomplished with the E5071C if the user imports the S-parameter data in manually. This support strategy is similar to the 86100 DCA's limitations with PLTS.
2. The E5071C does not support N-port calibration through PLTS software.
3. PLTS requires that the ENA have firmware A.08.00 or higher

PLTS Legacy software license migration reference matrix

Legacy	Description	New
N1930B-1xx	PLTS Base Analysis	N19301B
N1930B-3xx	PLTS Measurement and Calibration	N19303B
N1930B-5xx	PLTS Advanced Calibration	N19305B
N1930B-6xx	PAM-4 Analysis	N19306B
N1930B-7xx	PLTS N-Port Measurement and Analysis	N19307B

1. Previous "Transportable" license was USB dongle based. In the new structure it is a USB portable license
2. There are now subscription licenses, and the duration is available from 12 to 60 months.
3. Subscription licenses are also available for Network, USB, and the new Transportable license types.

Important notes regarding PLTS software configuration

1. If PLTS Studio is used (PLTS N19301B this will allow data analysis of files up to and including 4 ports (*s4p Touchstone files). However, if data is to be analyzed from files containing more than 4 ports (for example, 12-port data from a *s12p Touchstone file), the appropriate PLTS multiport option must be purchased (PLTS N19307B)
2. The VNA firmware options 550 or 551 must be ordered in conjunction with PLTS to work properly as a calibration and measurement system. Option 550 is for applications of 4 ports or less, while option 551 is for applications greater than 4 ports.
3. PLTS N19301B is required for N19303B, N19305B, N19306B, N19307B, or N19308B.
4. PLTS has an annual support called Keysight Care Software Support Subscription. Each new PLTS license must be accompanied by a support subscription (12, 24 or 36 months). Before the original support subscription expires, a new support subscription must be purchased. Depending how long the product is off support, there is a penalty to re-add support.
5. PLTS N19303B is required for instrument control portions of N19305B. As noted in 3 above, PLTS N19301B is required for either N19303B, N19305B, N19306B, N19307B, or N19308B.
6. PNA firmware is updated frequently and the newer PNA firmware version has backward compatibility and works well with the latest PLTS software.

Keysight software Licensing options provide flexibility and support

Projects ramp up and down, teams grow and shrink, and projects move location. In such a dynamic environment, you need flexible licensing options that allow you to balance your project's requirements. Whether your software will be a staple for years to come or you have a short-term need for a leading-edge measurement application, Keysight's licensing puts you in charge.

Choose your term. Choose your type. Keep control of your budget.

- Select a node-locked, transportable, USB portable or floating license type, depending on how much flexibility you need.
- Select a subscription or perpetual license term, depending on how long you need to use the software.
- Each license is sold with a KeysightCare software support subscription which provides technical support with ensured response time, proactive software updates, enhancements and fixes.

Choose a license term and type that best suits your requirements from the table below.

Table 1. License Terms

License Term	Options
Perpetual	Licenses can be used indefinitely.
Subscription	Licenses can be used through the term of the subscription. Available between 3 and 36 months or with user-selected start and end dates.

Table 2. License Type

License Type	Descriptions
Node locked	License can be used on one specified instrument/computer.
Transportable	License can be used on one instrument/computer at a time but may be transferred to another using Keysight Software Manager (internet connection required).
USB Portable	License can be used on one instrument/computer at a time but can be transferred to another using a certified USB dongle (available for additional purchase, Keysight part number E8900-D10).
Floating	Networked instruments/computers can access a license from a server one at a time. Multiple licenses may be purchased for concurrent usage. Three types of floating license are available: **Single Site:** 1-mile radius from the server; **Single Region[1]:** Americas; Europe; Asia; **Worldwide** (export restriction identified in End User License Agreement (EULA))

1. Americas (North, Central, and South America, Canada); Europe (European Continent, Middle Eastern Europe, Africa, India); Asia (North and South Asia, Pacific Countries, China, Taiwan, Japan)

KeysightCare software support subscription provides peace of mind amid evolving technologies.

- Ensure your software is always current with the latest enhancements and measurement standards.
- Gain additional insight into your measurement problems with live access to our team of technical experts.
- Stay on schedule with fast turnaround times and priority escalations when you need support.

Table 3. KeysightCare software support subscription

Subscription	Description
KeysightCare Software Support	Perpetual licenses are sold with a software support subscription between 12 to 60 months or with user-selected start and end dates.
	Software subscription licenses include software support through the term of the license.

Ordering Information

- Step 1. Choose your software product.
- Step 2. Choose your license term: perpetual or subscription.
- Step 3. Choose your license type: node-locked, transportable, USB portable, or floating.
- Step 4. Depending on the license term, choose your support subscription duration.

Product	License Type	Perpetual License & Support Subscription			Subscription
N1930yB[1]	Node-locked (fixed)	**SW1000-LIC-0x** License Type available as an attribute	+	**SW1000-SUP-0x** Durations available from 12 to 60 months	**SW1000-SUB-0x** License Type & Durations available from 3 to 36 months
	Transportable				
	USB Portable[2]				
	Floating (single site)				
	Floating (single region)				
	Floating (worldwide)				

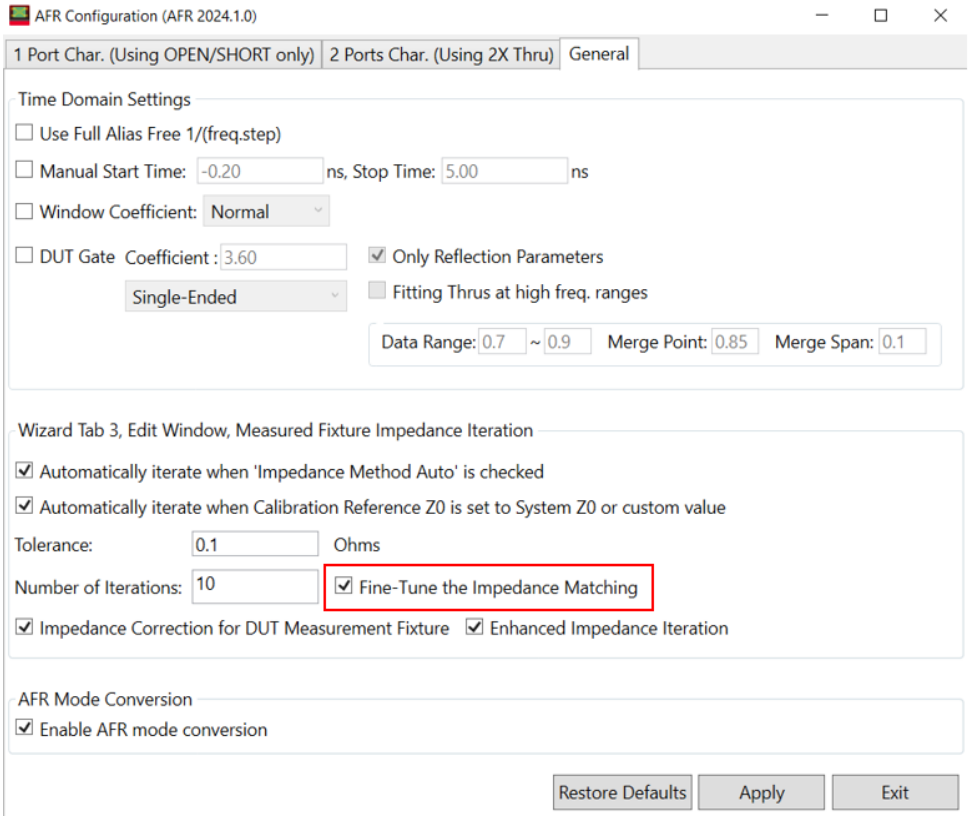
1. y:1,3,5,6,7 or 8
2. USB portable license requires a certified USB dongle (available for additional purchase, Keysight part number E8900-D10)

What's New with PLTS 2025?

Automatic Fixture Removal (AFR) enhanced algorithm for ultimate de-embedding accuracy

Fine-tune the impedance matching between fixture output and DUT input

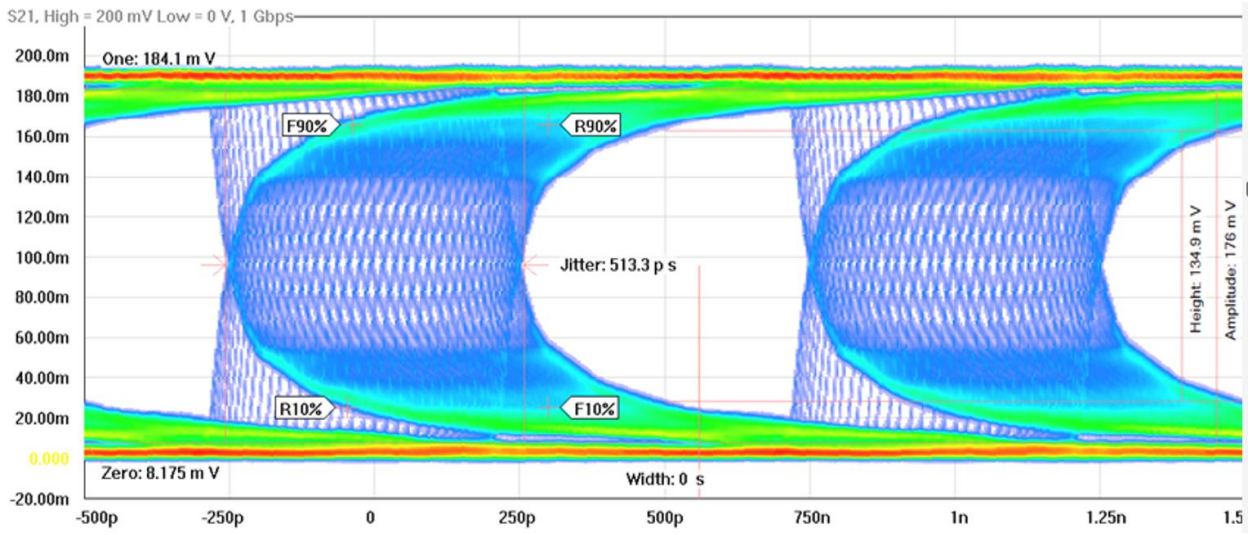
When extracting the fixture model in advanced de-embedding tools such as PLTS, it is critical to consider the mismatch between the fixture and the DUT. If this impedance mismatch is too great, then the induced reflections from this non-ideal interface will distort the results of the de-embedded channel. In order to avoid this costly mistake, the new PLTS 2025 AFR algorithm has been improved to ensure that the extracted fixture model is impedance matched precisely to the DUT input impedance automatically. This extra step of refining the fixture model will enhance accuracy, precision and high frequency analysis. In the spirit of the traditional PLTS intuitive graphical user interface, this can be accomplished with simply checking the box noted below. Search PLTS 2025 Help topic for details.



Choose StatEye virtual PRBS pattern for faster eye diagram generation of long patterns

Statistical eye virtual PRBS generator saves design time

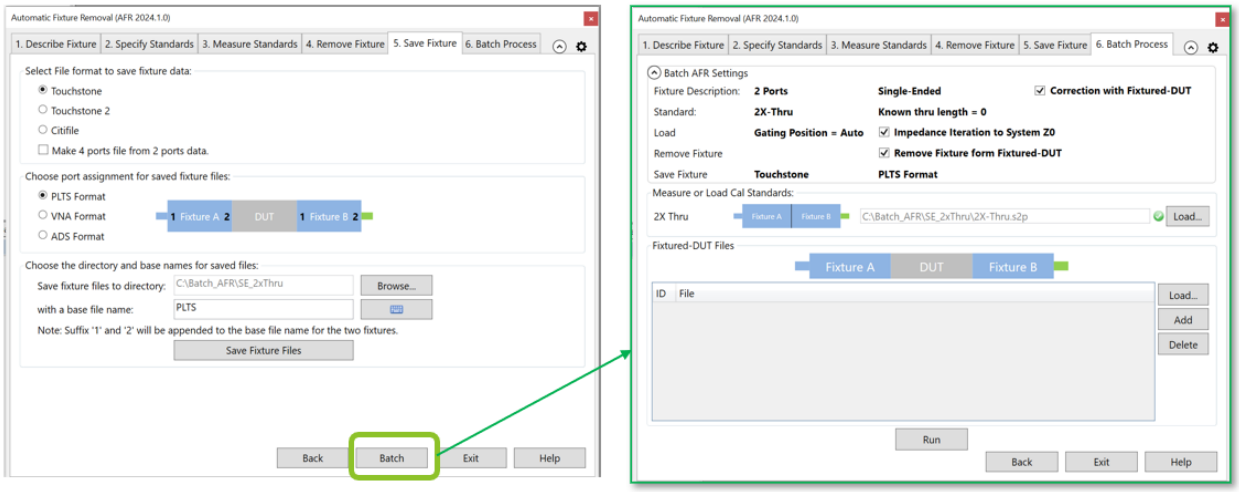
When creating eye diagrams from s-parameters, well executed algorithms can extract device impulse response and then convolve with a PRBS virtual pattern generator for precise synthesized eye diagrams. However, when some standards testing procedures require long bit patterns this eye generation can literally take hours to complete. Using the new StatEye capability in PLTS, we can turn hours into seconds, thus shortening the typical design cycle time for interconnect.



Batch Mode Automatic Fixture Removal (AFR)

Now de-embed multiple channels with one fixture model

High-speed digital design challenges often require de-embedding test fixtures in order to achieve “channel-only” performance characterization. If the same fixture has been used for multiple channel measurements, then precious analysis time can be saved with the new Batch Mode AFR in PLTS 2025. A simple graphical user interface will reduce design cycle time by a factor of 5 quite easily when using this new batch methodology as shown below.



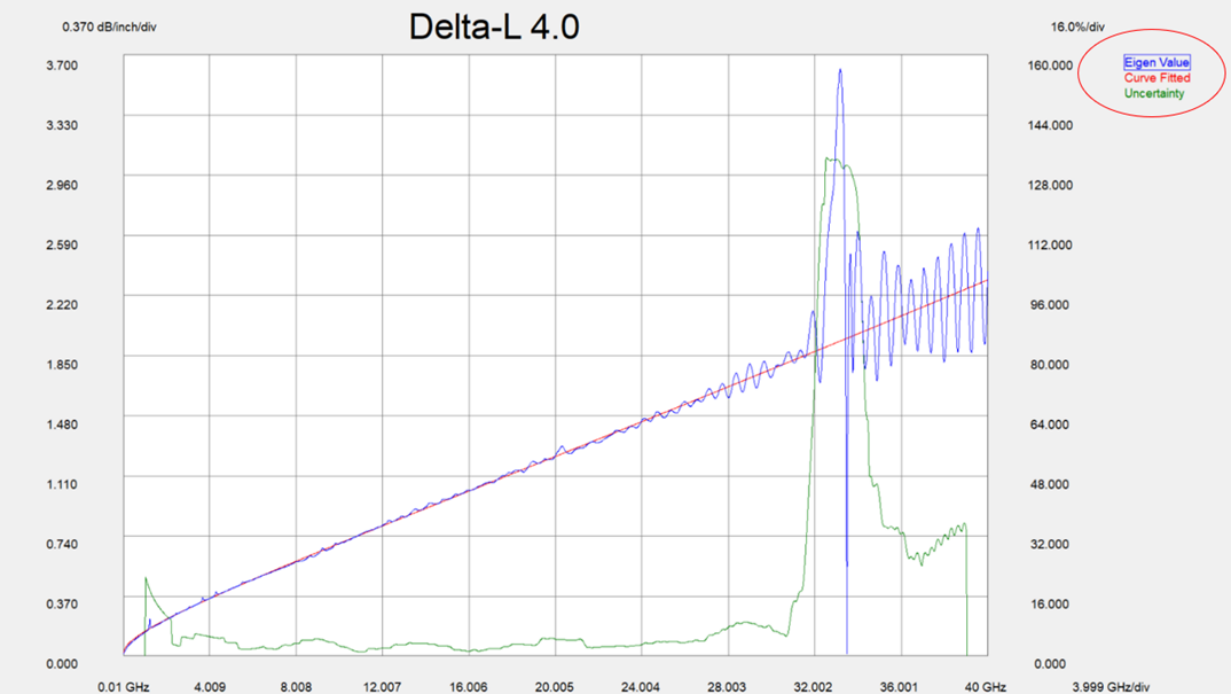
New Automatic Fixture Removal (AFR) enhancements:

Continuously upgraded software AFR algorithm includes:

- Fine Tune the Impedance Matching: Advanced algorithm to fixture impedance mismatching cases for better results
- New mode conversion algorithm
- Auto-Gating Span: Address large time-domain responses before time zero for better accuracy.
- Save/recall AFR advanced settings
- Refine PLTS gating impedance transformation steps
- AFR DUT gating can be used by just advanced calibration license

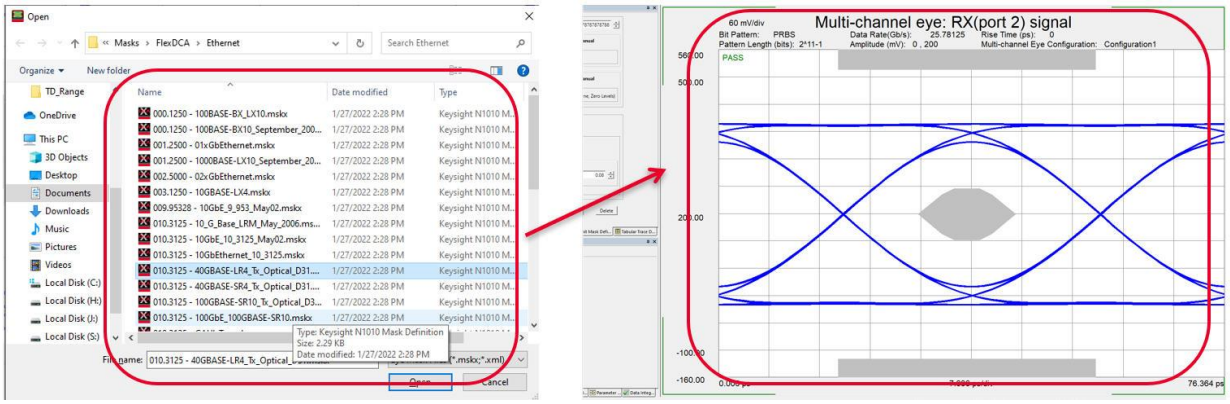
Delta-L (1L/2L/3L) methods of calculating insertion loss/inch

Advanced de-embedding tools such as Keysight's Automatic Fixture Removal (AFR) can achieve extracted models with unsurpassed accuracy. However, if a more simple de-embedding tool is desired, then Intel's Delta-L methodology can be easily used. As more PCB manufacturers integrate high-speed Tx/Rx chipsets onto their boards, the need to measure and control frequency-based losses increases. Measuring transmission line losses presents fabricators with a set of challenges very different from those for validating impedance. The Delta-L 1-line, 2-line and 3-line methodologies now included within the PLTS 2024 release is one of the industry standards utilized for simple and fast confirmation of printed circuit board performance at today's higher data rates.



Import FlexDCA eye mask for NRZ and PAM4

The Keysight Digital Communication Analyzer (DCA) oscilloscope has a large FlexDCA library of eye diagram masks that can now be easily leveraged and imported into PLTS 2024 eye diagram testing. Importing both NRZ and PAM4 eye masks can save precious time and money during the design validation cycle. Signal integrity engineers can now focus on more critical design challenges using this new feature.



Keysight enables innovators to push the boundaries of engineering by quickly solving design, emulation, and test challenges to create the best product experiences. Start your innovation journey at www.keysight.com.