Time Sync Analyzer — TimeSync

Ensure Robust Timing Infrastructure for 5G Success

Introduction

Timing and Synchronization has become essential to a variety of networks and industries. With the introduction of Ethernet-based fronthaul into the 5G Radio Access Network (RAN), the demand for synchronizing devices across RAN has become more stringent. ITU-T has enhanced G.827x recommendations and defined new Class-C and Class-D telecom grade clock. Many RAN devices now need to support Ethernet-based synchronization technologies with enhanced accuracy. It is critical to test the interoperability and to benchmark synchronization performance of RAN devices and the networks to ensure a robust Ethernet synchronization infrastructure for the successful 5G services delivery.

The Keysight Time Sync Analyzer (TSA) is a clock quality analytics platform, targeting 5G O-RAN, xHaul transport, as well as Data Center networks. Equally at home in the R&D lab as it is performing standardized qualifications, TSA tests synchronization performance of devices and networks, allowing users to analyze an array of digital clocks, packet clocks, and Ethernet PHY clocks. It is designed to address stringent synchronization demand, to enhance the test methodology with realistic network load, to monitor concurrently multiple network paths, and to increase the productivity with parallel test executions.

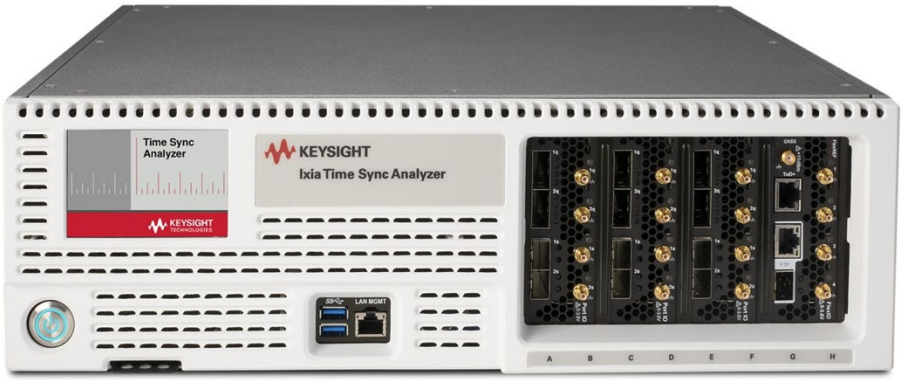


Figure 1. Time sync analyzer — High-performance DU Emulator and TimeSync tester

KEYSIGHT

Platform Overview

Time Sync Analyzer is available as a factory-assembled appliance with flexible configuration options. It includes a Timing card and up to three Ethernet line cards.

The timing card includes standard 10 MHz and 1 PPS reference clock input/output for system operation, driving external devices, and taking test input for measurement. It also provides integrated GNSS receiver, ITU-T standard ToD+ port, and optional Rubidium standard.

The Ethernet line card supports two multi-rate-capable Ethernet ports per line card, and multiple digital clock interface ports for associated signal analytics. Each Ethernet port can act as Precision Time Protocol (PTP) TimeTransmitter and TimeReceiver, generate SyncE clock, add clock impairment, and measure clock quality. Data traffic can be injected together with the PTP flows to assess the synchronization performance under realistic network load.

Time Sync Analyzer is driven by a convenient and intuitive Web-based UI, along with a comprehensive Python/REST automation interface. It offers a scalable multi-user architecture with minimum per Ethernet line card ownership, allowing up to three test users to share the system for parallel test execution.

Highlights

- High-density and high-performance clock quality analytic tool
- Analyzes an array of digital clocks, packet clocks, and Ethernet PHY clocks
- Emulates PTP and SyncE clocks with build-in impairment for realistic testing
- Measures clock quality per ITU-T recommendations and O-RAN specifications
- Analyzes multiple clock paths in parallel across devices and networks
- Flexible reference clock input/output options fit various lab timing infrastructure and fronthaul timing topologies
- Exercises and tests hybrid multi-drop networks from a single appliance
- Scalable multi-user architecture for sharing and parallel test execution
- Intuitive web-based user interface for system operation
- Comprehensive Python/REST test automation and easy-to-use

Key Features

- PTP TimeTransmitter/TimeReceiver supporting ITU-T G.8275.1/G.8275.2 and IEEE 1588v2-2008
- SyncE and ESMC with QL TLV and enhanced QL TLV per ITU-T G.8264
- Flexible standard-based noise profiles and custom noise profiles
- Clock quality analysis for PTP, SyncE, 1PPS, 10 MHz per ITU-T Recommendations and O-RAN specification
- Concurrent multi-path measurements for comparison and productivity
- Programmable digital low/high pass filter and flexibility of defining starting point of a measurement
- Frequency stability test with controlled frequency drift and adjustable FFO reference frequency
- Event Markers for correlating TE/TIE change to an event for analyzing potential impact
- Aligned Action for defining time aligned actions for tolerance, transient and holdover test
- Line rate bi-directional capture and flexible background traffic
- Ability of multi-day test run to access long duration synchronization performance
- Convenient web-based user interface for clock quality test and system timing source configuration
- Multiple user support (up to three test sessions, one per Ethernet line card)
- Python/REST API support for automation

PTP and ESMC Protocol Test

Time Sync Analyzer provides simple 'Quick Setup' for PTP configuration, as well as ESMC frame content control, which can be independent of the actual PHY clock. Users can customize the configuration grid and add more parameters for positive and negative testing. PTP and ESMC statistics view provides protocol details to help validate operation and to aid troubleshooting.

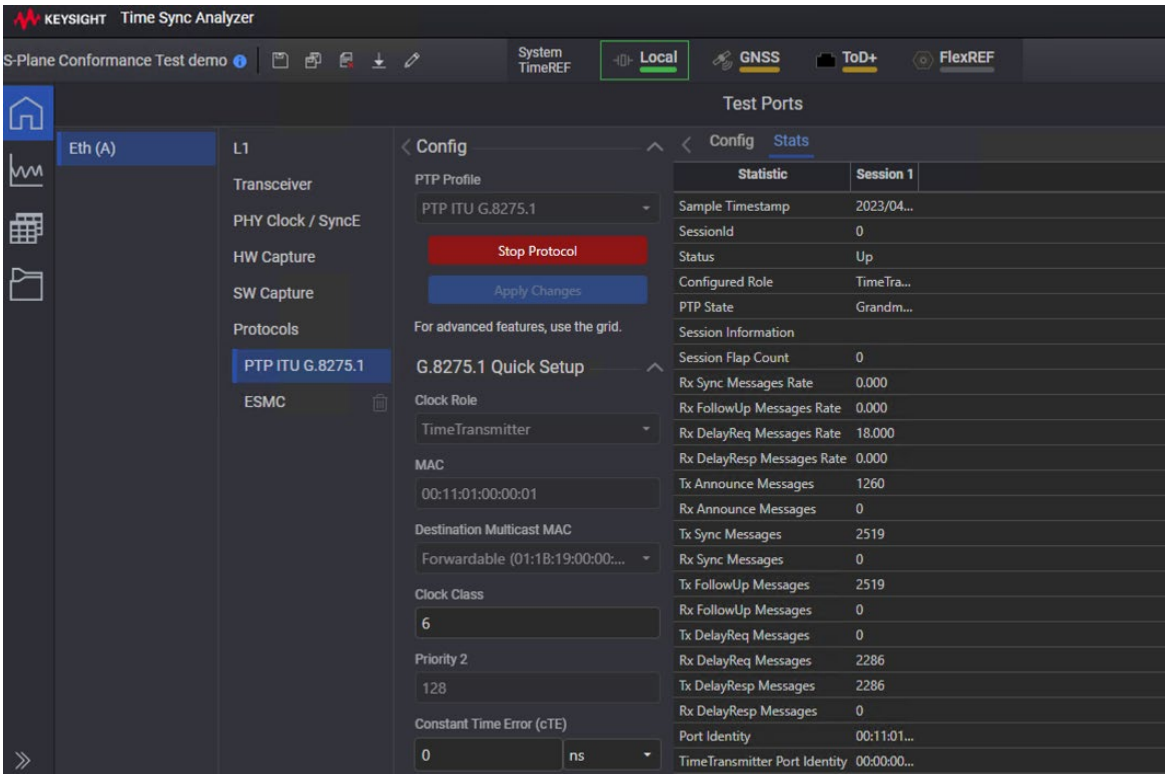


Figure 2. Time sync analyzer PTP protocol configuration and statistic

Clock Quality Analysis

Time Sync Analyzer provides Clock Quality Analysis (CQA) for PTP, SyncE, and digital clock input such as 1PPS or 10 MHz. It supports ITU-T based and O-RAN based conformance test. Users can select the desired metrics such as TE/TIE, MTIE and TDEV, and then evaluate pass/fail against standard-based masks or user-defined masks. Analysis can be performed with live measurement or with an offline data set. Multiple clock paths can be analyzed in parallel for comparison and correlation.

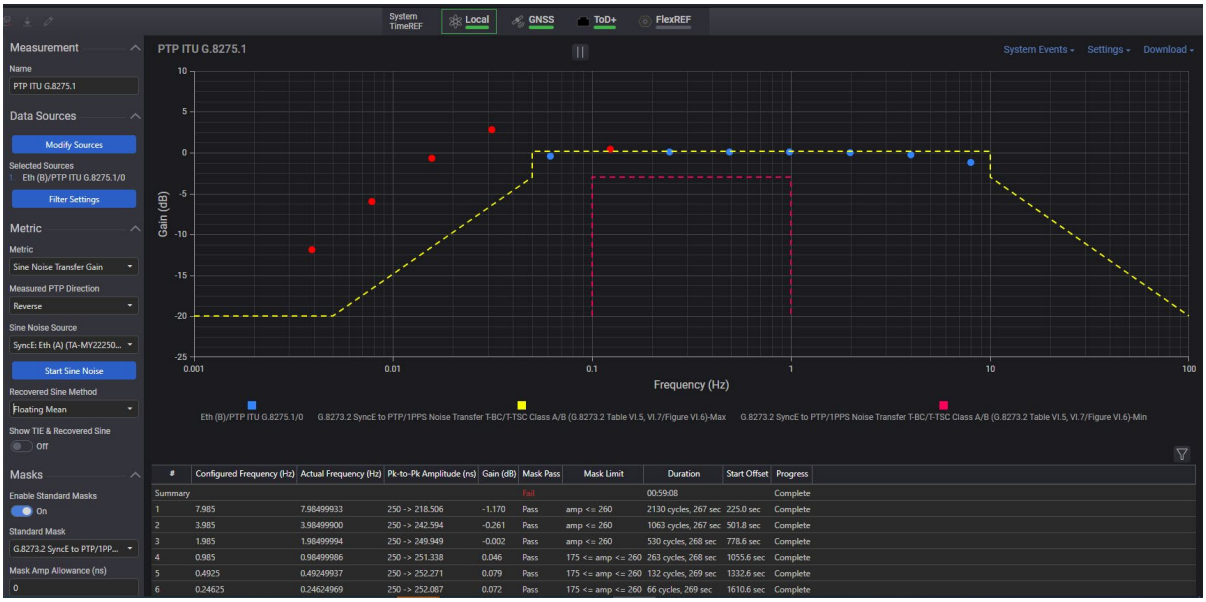


Figure 3. Time sync analyzer clock quality measurement

Analyzing PTP Clock

Precision Time Protocol (PTP), defined by the IEEE 1588v2 standard, provides highly accurate timing over a packet-based network by propagating frequency, phase, and time-of-day information. The precision and performance of 1588v2 (PTP) depends on the accuracy of timestamping, as well as the network performance between time source and receivers.

Time Sync Analyzer emulates Precision Time Protocol (PTP) TimeTransmitter and TimeReceiver. It tests PTP protocol and PTP synchronization performance of devices acting as ordinary clock, boundary clock or transparent clock per ITU-T G.8273.x recommendations.

Analyzing SyncE Clock

ITU-T Synchronous Ethernet (SyncE) provides a mechanism to ensure frequency synchronization over Ethernet networks. SyncE is a standard for the distribution of clock frequency over Ethernet links by using the Ethernet Synchronization Messaging Channel (ESMC) protocol.

Time Sync Analyzer supports flexible wander generation and measurement for Ethernet PHY clock to test SyncE wander generation, wander tolerance, and wander transfer per ITU-T G.8262/G.8262.1.

O-RAN S-Plane Test

O-RAN working groups define S-Plane test specification for RAN device and network, including O-RU, O-DU, transport switch and various networks.

Time Sync Analyzer supports O-RU S-Plane conformance test with integrated CUSM Plane in a single fronthaul system, provides a controlled and deterministic test environment fully compliant with WG4 Conformance test specification. It also provides advanced S-Plane test capabilities to help characterize synchronization performance of radio unit component blocks and end-to-end from Ethernet to RF.

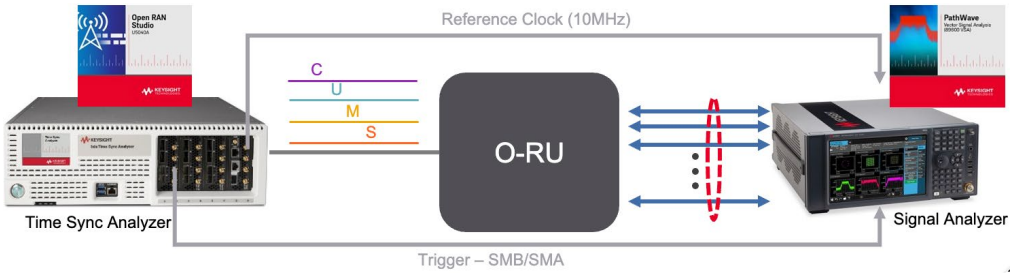


Figure 4. Time sync analyzer O-RU S-Plane conformance test solution

Time Sync Analyzer supports O-DU S-Plane conformance test per O-RAN spec covering various synchronization topologies. It generates PTP and SyncE clock, models noise pattern in different sync topology, and measures PTP/SyncE/1PPS for functional and performance test per O-RAN WG4 CONF spec.

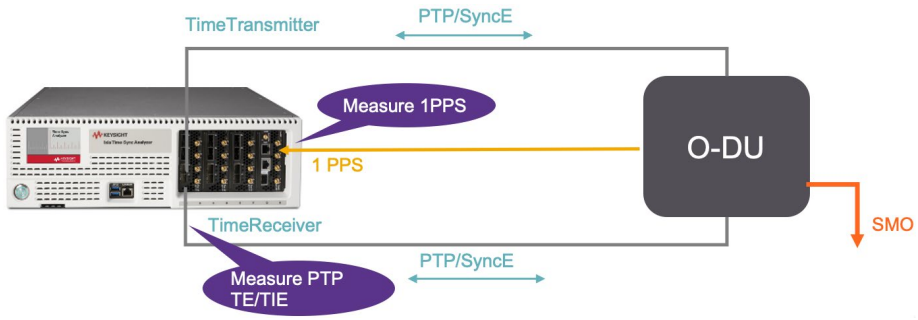


Figure 5. Time sync analyzer O-DU S-Plane conformance test solution

Time Sync Analyzer supports S-Plane test for transport devices and transport networks per ITU-T recommendation and O-RAN WG9 test specification. It emulates PTP TimeTransmitter and TimeReceivers surrounding transport devices or end-to-end networks to analyze synchronization performance of transport network paths.

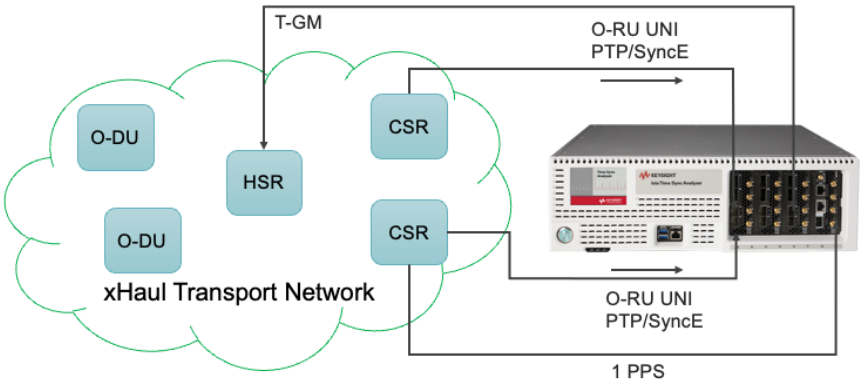


Figure 6. Time sync analyzer to test S-Plane for 5G xHaul transport network

Flexible Architecture for Increased Productivity

Time Sync Analyzer is designed with flexible factory configuration and multi-user architecture. It supports one test user per line card and up to three test users per system, allows sharing of the system for parallel test execution, saves rack space and power. Customer has the flexibility to use the system to its full capacity with one user for multi-drop network test or to share among multiple users to analyze multiple clocks in parallel.

Time Sync Analyzer Specifications

Key Specifications	Details
Modular appliance	• Time sync analyzer appliance • 1 Timing card with optional Rubidium option • Up to 3 Ethernet line cards, factory configured
Timing card	• Internal reference clock (with Rubidium): ◦ Frequency stability over temperature < 1 x 10^{-10} ◦ Short term stability (10s Tau, TDEV): 30ps or better (typical) ◦ Long term stability (1000s Tau, ADEV): < 1 x 10^{-12} • FlexREF 1 & 2 SMB ports ◦ Frequency and Phase reference input: 10 MHz and 1PPS • FlexIO 1 ~ 4 SMB ports ◦ Frequency reference output: 2.2 Hz to 10 MHz ◦ Phase (1PPS) reference output ◦ Test input: 1 PPS or 0.9 Hz to 10MHz • FlexIO inputs: +0.1 V to +3.3 V; 50 Ohm input impedance • FlexIO outputs: +1.65 V square into 50 Ohms • Embedded multi-constellation capable GNSS receiver (GPS, GALILEO, QZSS) • ToD interface with RJ48 connector, supports ITU-T G.8271 format data
Ethernet line card	• 2 x Ethernet ports per line card with SFP28 and QSFP28 • Supporting 1GE (Fiber), 10GE, 25GE, and 100GE speeds • Speed option licensed per card • Independent speed and operation across line cards
1588v2 (PTP)	• Emulate TimeTransmitter and TimeReceiver supporting PTP G.8275.1/G.8275.2/1588v2-2008 • Dynamic update of PTP clock class • Generates Time Error impairment • PTP statistics with session state and protocol information
SyncE	• Generate ESMC (SSM) messages per ITU-T G.8264 ◦ Configurable MAC and VLAN ◦ Support QL TLV and extended QL TLV with user configurable Quality Level • PHY Clock Phase and Frequency Offset control • Generate and measure wander per ITU-T G.8262/G.8262.1
Capture	• Capture buffer per port: Tx 512M, Rx 512M • Bi-direction hardware and software capture • Capture and decode PTP and ESMC protocol messages
Statistics	• Port Stats • PTP Stats • ESMC Stats
Measurement	• Measure PTP, SyncE, 1PPS and frequency • Built-in standard-based mask and user-defined mask • Programmable digital low pass filter and high pass filter • Multiple parallel clock quality measurement lines

Key Specifications	Details
	• Metrics: TE, TIE, MTIE, TDEV, MDEV, OADEV, MATIE, cTE, PE, FFO • PTP TE Generation and measurement accuracy: 1ns or better typical
General	• Web-based user interface • Automation API: Python/RestAPI
Chassis	• Rack mount and desktop mounting hardware included • Dimensions: 3RU 17.27 in (438 mm) x 14.61 in (371 mm) x 5.21 in (132 mm) • Weight: 29.9 lbs / 13.6 kg (with a maximum load of 3 line cards) • Noise Level: 60 dBA normal operation, 70 dBA max • Thermal ◦ Operating temperature: 5 °C to 40 °C (41° F to 104 °F) ◦ Operating humidity: 10 % to 85 % (RH), non-condensing ◦ Storage temperature: -40 °C to 70 °C (-40 °F to 158 °F) ◦ Storage humidity: 5 % to 95 % (RH), non-condensing • Input power ◦ 100–127 Vac / 200–240 Vac, 10 / 5A, 50/60 Hz (x2) or ◦ 100–127 Vac / 200–240 Vac, 10 / 5A, 50/60 Hz (x1) • Power consumption: ◦ 1-line card system – Max 380W, typical 268W ◦ 2-line card system – Max 540W, typical 328W ◦ 3-line card system – Max 700W, typical 388W
Safety	• UL 62368-1 / CSA C22.2 No. 62368-1 • EN 62368-1 / IEC 62368-1
Emissions and immunity	• FCC Part 15B, Class A • CAN ICES-003(A)/NMB-003(A) • EN 55032 Class A / EN 55035 / EN 61000-3-2 / EN 61000-3-3 • AS/NZS CISPR 32 Class A • KS C 9832 Class A / KS C 9835 / KS C 9610-3-2 / KS C 9610-3-3 • VCCI – CISPR 32 Class A
Regulatory approvals	• CSA (USA, Canada) • CE (Europe) • UKCA (United Kingdom) • RCM (Australia) • KCC (Korea) • VCCI (Japan)
Environmental	• RoHS Directive 2011/65/EU; Annex II, Directive (EU) 2015/863 • WEEE Directive 2012/19/EU • China RoHS

Product Ordering Information

Time sync analyzer hardware appliance

Part Number	Description
941-0120	Keysight Time Sync Analyzer Appliance (941-0121 and Base Software (930-7300); Rack mountable 3U unit, INCLUDES: Keysight Timing Sync Analyzer Appliance, Keysight Time Sync Analyzer Base Software which enable timing reference input/output of 10MHz and 1PPS, and timing reference input of GPS and TOD+, 2 power supply modules, 1 Rackmount kit, and 1 Ship kit; REQUIRED: 1 Timing card and minimum 1 Ethernet line cards; NOTE: Additional hardware accessories can be purchased separately for increased system availability or for backup
944-1801	Keysight Time Sync Analyzer TIMING Card (944-1801); Enable system timing control and distribution with internal and external time source, output timing source to external system, support test input/output and trigger input/output
944-1802	Keysight Time Sync Analyzer TIMING Card with Rubidium (944-1802); Enable system timing control and distribution with internal and external time source, output timing source to external system, support test input/output and trigger input/output
944-1811	Keysight Time Sync Analyzer 2-port Ethernet Line Card (944-1811); Support 2 Ethernet ports with SFP28 and/or QSFP28 physical interface; REQUIRES: Minimum one Speed option to be purchased

Time sync analyzer software options

Part Number	Description
930-7200	Keysight Time Sync Analyzer Ethernet Line Card 100G Speed Enablement (930-7200); Enable QSFP28 100G speed for exact one Ethernet Line Card
930-7201	Keysight Time Sync Analyzer Ethernet Line Card 25GE Speed Enablement (930-7201); Enable 25GE speed for exact one Ethernet Line Card
930-7202	Keysight Time Sync Analyzer Ethernet Line Card 10GE/1GE Speed Enablement (930-7202); Enable 10GE speed for exact one Ethernet Line Card
930-7301	Keysight Time Sync Analyzer Advanced Software (930-7301); Enable digital clock impairment and measurement, and Clock Quality Analysis; REQUIRES: 930-7300 Keysight Time Sync Analyzer Base Software Package
930-7302	Keysight Time Sync Analyzer IEEE 1588v2 (PTP) Generation and Measurement (930-7302); Enable PTP TimeTransmitter and TimeReceiver emulation for testing G.8273.x Boundary Clock, Transparent Clock, and Ordinary Clock; Enable TIE collection and clock quality analysis of derivative metrics; REQUIRES: 930-7301 Keysight Time Sync Analyzer Advanced Software
930-7303	Keysight Time Sync Analyzer SyncE Clock Generation and Measurement (930-7303); Enable ESMC generation and analysis for EEC and enhanced EEC clock per ITU-T G.8264, Enable TIE collection and clock quality analysis of all derivative metrics; REQUIRES: 930-7301 Keysight Time Sync Analyzer Advanced Software
930-7305	Keysight Time Sync Analyzer O-RU S-Plane Conformance Test for O-RU (930-7305); Enable O-RU S-Plane Conformance test for functional and performance test cases per O-RAN WG4 S-Plane Conformance specification; REQUIRE: 930-7300 Keysight Time Sync Analyzer Base Software
930-7306	Keysight Time Sync Analyzer Custom Traffic Generation (930-7306); Enable Custom Traffic Generation to assess synchronization performance; REQUIRE: 930-7301 Keysight Time Sync Analyzer Advanced Software

Notes: 930-7305 enables feature set for O-RU S-Plane conformance test, which is a subset of 930-7302 + 930-7303.

Optics and cables

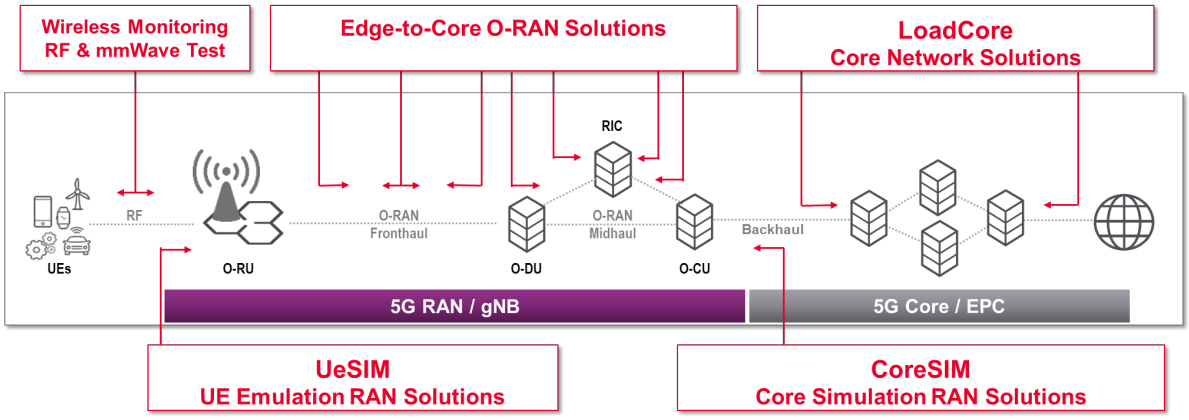
Part Number	Description
SFP28-SR-XCVR	SFP28 Dual-Rate 25GBASE-SR 25GE and 10GBASE-SR 10GE pluggable optical transceiver
SFP28-LR-XCVR	SFP28 Dual-Rate 25GBASE-LR 25GE and 10GBASE-LR 10GE pluggable optical transceiver
QSFP28-SR4-XCVR	QSFP28 100GBASE-SR4 100GE pluggable optical transceiver, MMF (multimode), 850nm, 100m reach (948-0036)
QSFP28-LR4-XCVR	Ixia, QSFP28 100GBASE-LR4 100GE pluggable optical transceiver, SMF (single mode fiber), 1310nm, 10km reach (948-0038)
SFP-PLUS-SR-XCVR-D-T	SFP+ 10/1GBASE Dual Rate SR pluggable optical transceiver, MMF (multimode fiber), 850nm, 300m reach, LC
SFP-PLUS-LR-XCVR-D-T	SFP+ 10/1GBASE Dual Rate LR pluggable optical transceiver, 1310nm, MMF (single mode fiber), 10km reach, LC

Keysight 5G Solutions

Keysight's industry-first 5G end-to-end design and test solutions enable the mobile industry to accelerate 5G product design development from the physical layer to the application layer and across the entire workflow from simulation, design, and verification to manufacturing, deployment, and optimization.

Keysight 5G Radio Access and Core Network Test Portfolio

Keysight Open RAN Architect (KORA) Solutions



Keysight offers common software and hardware platforms compliant to the latest 3GPP standards, enabling the ecosystem to quickly and accurately validate 5G chipsets, devices, base stations, and networks, as well as emulate subscriber behavior scenarios. Additional information about Keysight's 5G solutions is available at www.keysight.com/find/5G

Keysight enables innovators to push the boundaries of engineering by quickly solving design, emulation, and test challenges to create the best product experiences. Start your innovation journey at www.keysight.com.

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