

N5991DP2A

DisplayPort 2.1 receiver test automation software

The screenshot displays the DisplayPort N5991 ValiFrame software interface. The main window is titled "DisplayPort - DP2.1" and shows a hierarchical test configuration tree on the left. The tree includes sections for DP1.4 Calibration, DP2 Calibration, and various tests like Jitter Tolerance Test, Bit Error Rate Testing, Common Mode Interference, Crosstalk, DPCD, Jitter, Link Training, Pattern, Sequencer, and Spec Values. The right pane shows the configuration details for the selected test, "Jitter Tolerance Test 1 MHz PJ UHBR13_5 Lane 0 (TP2)". The bottom pane shows a log of test results, including progress messages and error counter test results.

DisplayPort N5991 ValiFrame

NEW LOAD SAVE EXPORT RESET START PAUSE ABORT

DisplayPort - DP2.1

- DP1.4 Calibration
 - RBR
 - HBR
 - HBR2
 - HBR3
 - Aggressor Lane
- DP2 Calibration
 - Aggressor DP2
 - TP1
 - Channel Loss
 - Insertion Loss Calibration 10G
 - Insertion Loss Calibration 13p5G
 - Insertion Loss Calibration 20G
 - TP3
 - Lane0
 - UHBR10
 - RX EQ Adaptation and Eye Diagram Calibration 1MHz
 - RX EQ Adaptation and Eye Diagram Calibration 2MHz
 - RX EQ Adaptation and Eye Diagram Calibration 10MHz
 - RX EQ Adaptation and Eye Diagram Calibration 50MHz
 - RX EQ Adaptation and Eye Diagram Calibration 100MHz
 - Calibration Summary @TP3
 - UHBR13.5
 - UHBR20
- DP1.4 Sink Tests
- DP2 Sink Tests
 - Lane 0
 - TP2
 - AUX Communication and Link Setup Checking
 - UHBR10
 - Jitter Tolerance Test 1 MHz PJ UHBR10 Lane 0 (TP2)
 - Jitter Tolerance Test 2 MHz PJ UHBR10 Lane 0 (TP2)
 - Jitter Tolerance Test 10 MHz PJ UHBR10 Lane 0 (TP2)
 - Jitter Tolerance Test 50 MHz PJ UHBR10 Lane 0 (TP2)
 - Jitter Tolerance Test 100 MHz PJ UHBR10 Lane 0 (TP2)
 - Jitter Tolerance Test Summary UHBR10 Lane 0 (TP2)
 - UHBR13_5
 - Jitter Tolerance Test 1 MHz PJ UHBR13_5 Lane 0 (TP2)

Jitter Tolerance Test 1 MHz PJ UHBR13_5 Lane 0 (TP2)

Offline	True
Software Version	1.4.0.8
Calibration Data Version	Unknown
Compliant	False
Non-compliance reason(s)	Procedure offline; Required cal not
Tested Lane Eye Height	700 mV

Bit Error Rate Testing

Allowed Number of Errors	100
Observation Time	16 s

Common Mode Interference

AC CM Set Value	225 mV
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Crosstalk

Aggressor Clock Divider	4
Aggressor Set Amplitude	486 mV

DPCD

Extra DPCD	Before Generator Programming
Extra DPCD Order	Before Generator Programming
Clearing DPCD Register Before	False

Jitter

Total Jitter	360 mUI
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Link Training

Max injected error count during	10
Run Frequency Lock Phase	True

Pattern

BERTestPattern	PRBS31
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Sequencer

Procedure Error Case Behavior	Abort Sequence
Procedure Failed Case Behavior	Proceed With Next Procedure
Repetitions	0

Spec Values

AC CM Amplitude Target	100 mV
Aggressor Lane Voltage	340 mV

Repetitions

Severity	Message	Date
Progress	Try to lock frequency (#1)	01/22/2024 12:02:00 PM
Progress	Frequency locked	01/22/2024 12:02:02 PM
Progress	Try to achieve symbol lock (#1)	01/22/2024 12:02:02 PM
Progress	Symbol lock achieved	01/22/2024 12:02:02 PM
Info	Injecting errors for ErrorCounter test	01/22/2024 12:02:02 PM
Info	Error counter test passed: 9 error(s) injected => CTS allows 9 to 11 errors. The error counter shows a value of 9	01/22/2024 12:02:05 PM
Info	Error count during test was 0, allowed limit is 100	01/22/2024 12:02:10 PM

Ready

Warnings: 0 SW Maintenance License is OK Completed

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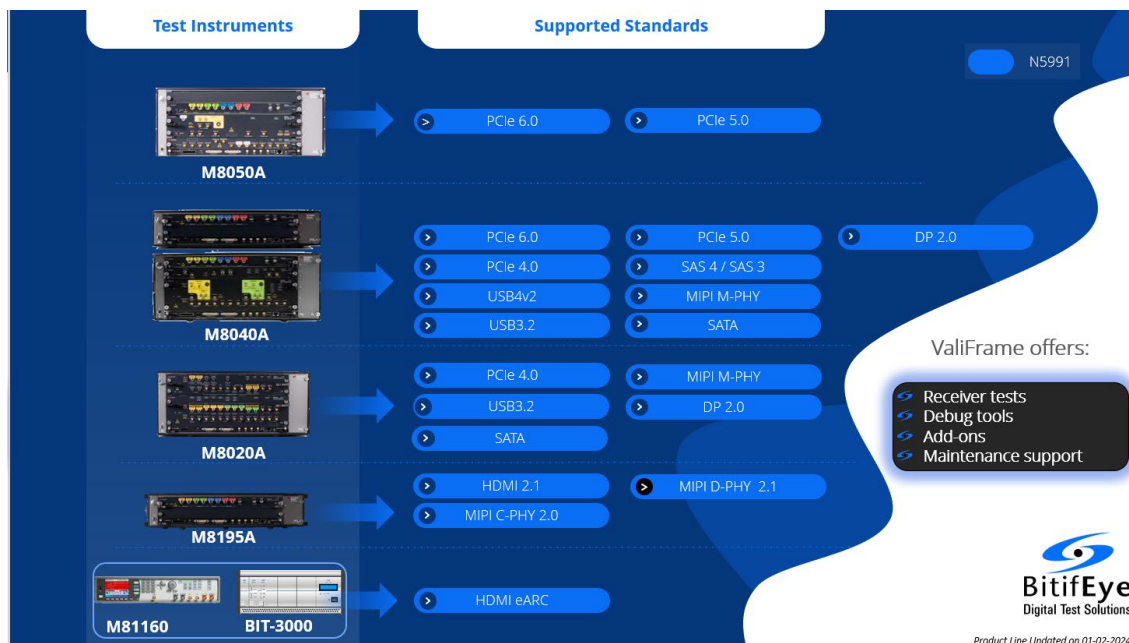
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At a Glance

High-speed digital standards are quickly evolving to keep pace with emerging technologies such as 5G, Internet of Things (IoT), artificial intelligence (AI), virtual reality (VR), and autonomous vehicles.

Each generational change introduces new test challenges for your digital designs. You need to test your high-speed digital designs across all product development stages — from design and simulation, analysis, debug, and compliance test. The N5991 software solution anticipates test challenges, optimizes performance, and accelerates time-to-market of your high-speed computing interfaces, data center connections, and consumer electronics

- Supported standards, which include PCIe, SAS, SATA, USB, HDMI, DisplayPort, and MIPI M-PHY / C-PHY / D-PHY. Other standards will be continuously added with the requirements for higher data-speed testing
- Guided setup with automated fast stress signal calibrations and compliance measurement functions
- Modern look and feel with enhanced functionalities
- System modularity allows the user to enable only required functionalities
- HTML test reports
- Node-locked and transportable licenses
- Characterization mode for in-depth testing
- Single and multi-lane device testing



Turn your instruments into a solution

An efficient test strategy is a proven competitive advantage. The Keysight Technologies N5991 test automation software platform combines the performance of your instruments with the convenience of your PC. The system's software provides unprecedented test integration, high-throughput, and ease-of-use for a wide range of stimulus and response systems, providing a level of control that transforms a collection of instruments into a universal, user-friendly, and highly productive test solution.

Standardize your tests

The N5991 receiver-test options provide dedicated receiver compliance tests for popular and emerging digital buses. The user can choose compliance mode for fast reassurance, or characterization mode for in-depth analysis. The Receiver Test Automation Platform's compliance testing capabilities have been repeatedly proven at interoperability workshops ("plug fests"). The N5991 builds on the success of previous generations to deliver significant gains in productivity. Like its predecessor, the N5990A, the new system makes it easy to test multiple buses by using the same interface for all available standards. It delivers additional gains by using familiar HTML for reporting results.

Test selection and test results

The test automation software platform lets you select tests from an intuitive tree structure with multiple levels of detail. Select the tests you want to run, as well as the number of repetitions. Test results are provided in HTML format. When you measure a parameter range, it delivers a specific graph and a related data table (see Figure 1).

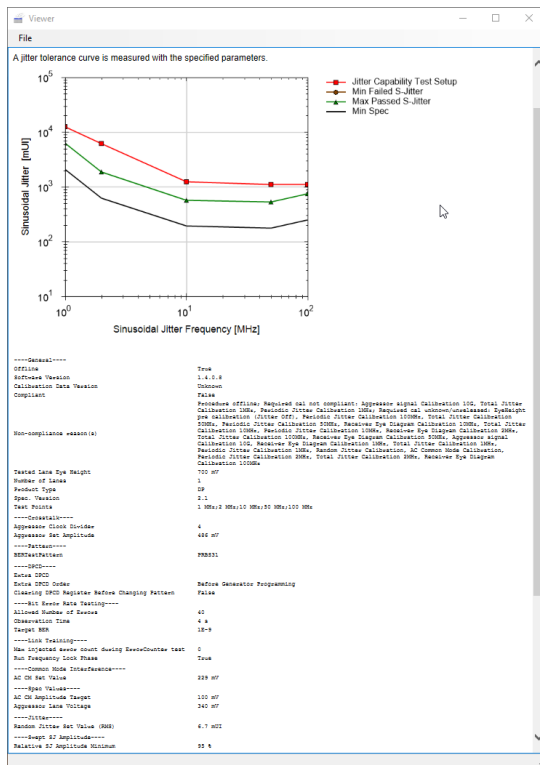


Figure 1. Jitter Tolerance Characterization test report

N5991DP2A DisplayPort 2.1 Receiver Test

DisplayPort™ 2.1 is the next generation of VESA's (Video Electronics Standards Association) specification for digital display and audio data transmission. Built on top of DisplayPort 1.4a, this new revision of the protocol has numerous additions and is backward compatible with existing products. Focusing on the physical layer, DisplayPort 2.1 supports three new main link data transfer speeds: UHBR10, UHBR13.5 and UHBR20, running at 10, 13.5 and 20 Gb/s per lane, respectively. Instead of 8b/10b coding, the UHBR bitrates use 128b/132b coding, providing a net data transfer efficiency of 97%, as opposed to 80%. With that, the maximum net data transfer rate increases from 25.92 Gb/s with HBR3 over 4 lanes to 77.57 Gb/s with UHBR20 over 4 lanes.

With DisplayPort designs becoming more complex, ensuring the conformance to the specification and the interoperability with the broad ecosystem of devices is the key to a successful product. Do not let the complexity of validation and characterization affect your schedule and meet your time to market without delays with the N5991DP2A DisplayPort 2.1 Receiver Test software. Use N5991DP2A to debug, characterize and validate the physical layer of your DisplayPort Sink designs in a fast, reliable way, following VESA's DisplayPort PHY Compliance Test Specification or CTS.

At a high level, the validation of a DisplayPort Sink product consists of two steps. First, the test station is calibrated to achieve the required test conditions. Second, the test conditions are applied to the Device Under Test (DUT) and its performance is evaluated. The following sections cover the steps mentioned in more detail.

Calibrations

The DisplayPort PHY CTS test conditions consist of an impaired DisplayPort signal transmitted over the worst-case passive channel injected on the receiver lane under test. The signal impairments include random jitter, sinusoidal jitter, common-mode interference, inter-symbol interference (ISI) and others that are finely adjusted to achieve a certain eye opening and amount of total jitter. In addition, if the DUT supports two-lane or four-lane Main Link configurations, additional signals are injected at the neighbor lane(s) to induce crosstalk.

The adjustment of the stress signal is an arduous task that if not followed accurately leads to invalid test conditions, and thus invalid test results. With an intuitive interface, the N5991DP2A software guides the user through the complex calibration process, providing clear steps and detailed connection diagrams and instructions. The calibration procedures are sorted by bitrate and test point for an easy selection and an optimal sequence order to minimize the human interaction with the setup.

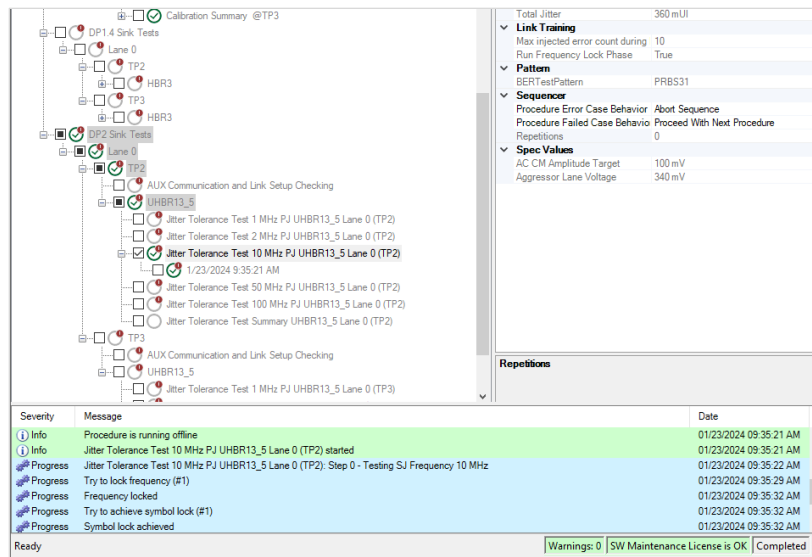


Figure 2. Test station calibration procedures

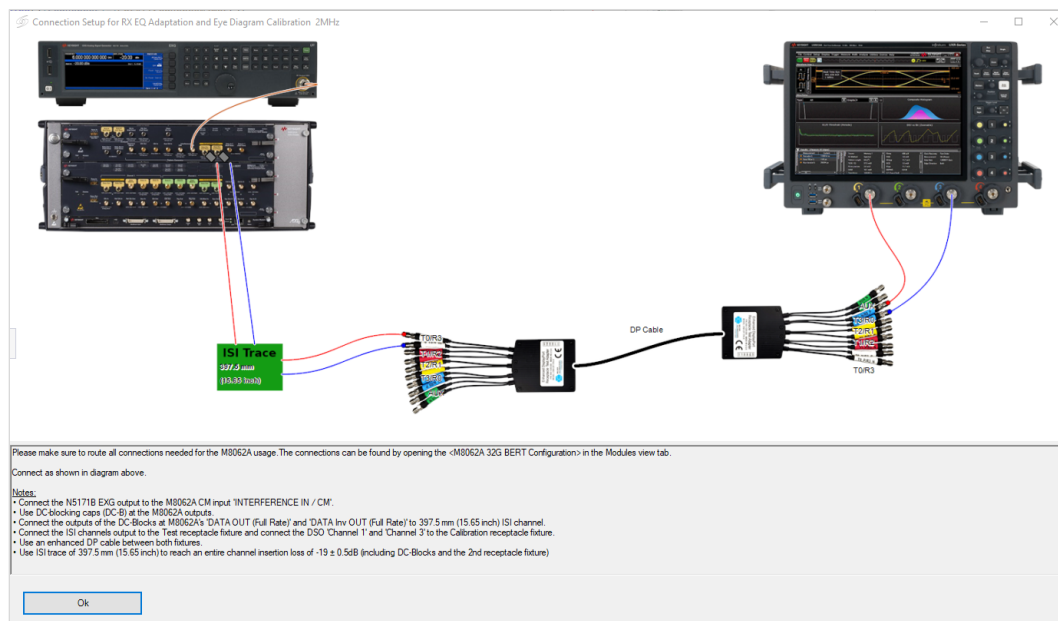


Figure 3. Connection setup for UHBR10 calibration at test point TP3

Receiver Tests

When a DP Source and Sink are connected, the first that happens is link training. Led by the Source, link training consists of the discovery of the Sink capabilities, the negotiation of a common link configuration (number of lanes and bitrate), the adjustment of the Source drive settings and the tuning of the Sink receiver equalization. This involves the transmission of link training patterns on the high-speed lanes of the DP Main Link and numerous read/write operations with the DPCD (DisplayPort Configuration Data) register space via Auxiliary (AUX) Channel transactions. Once link training is complete, the actual DP data transmission starts.

The process in a PHY test environment is similar, with two key differences: there is no DP Source involved and the DP data transmission is replaced by a symbol error test. The role of the DP Source is played by two components: the stress signal generator and a so-called “reference Source”. The stress signal generator transmits calibrated, impaired link training patterns on the high-speed lanes, and the reference Source communicates with the DP Sink under test over the AUX channel allowing to configure the Sink as the test requires. Upon link training completion, the symbol error test starts: the stress signal generator transmits a test pattern for a pre-defined observation time and the reference Source is used to access a built-in symbol error counter that all DP Sink products are required to implement for PHY testing purposes.

In summary, DP Sink testing is extremely complex and error prone, as it involves the control of test equipment and the access to the DPCD register space of the DUT to perform the link training and reset/read the symbol error counter. Do not let this complexity affect your schedule and use N5991DP2A. After just a few configuration steps, the N5991DP2A software takes over the entire test process, making it consistent and repeatable so you can focus on what really matters: your product and the test result.

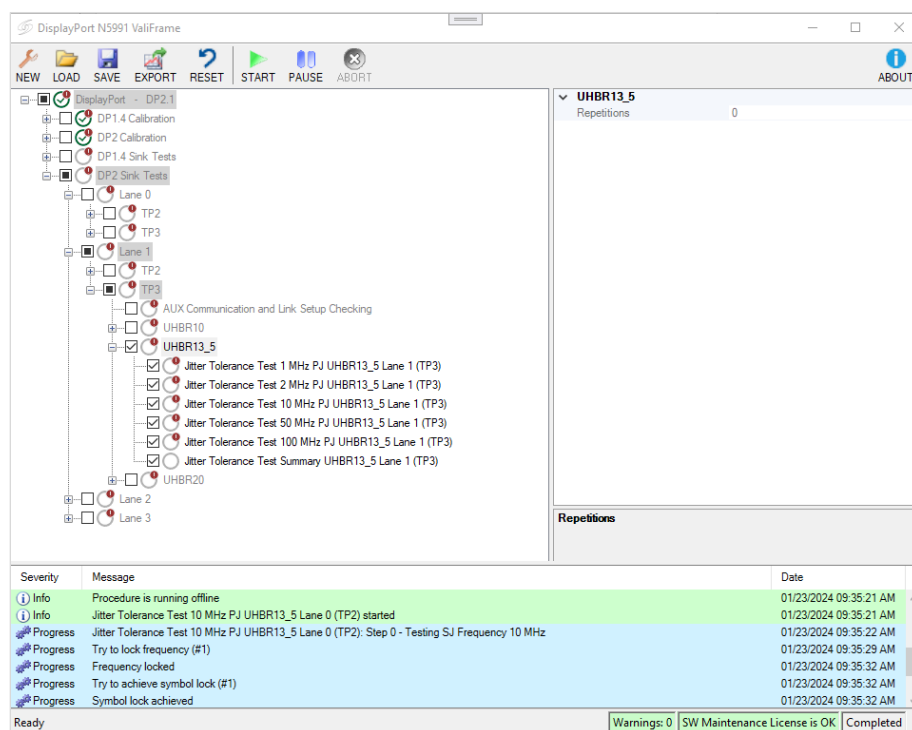


Figure 4. DisplayPort Sink tests sorted by tested lane, test point and bitrate

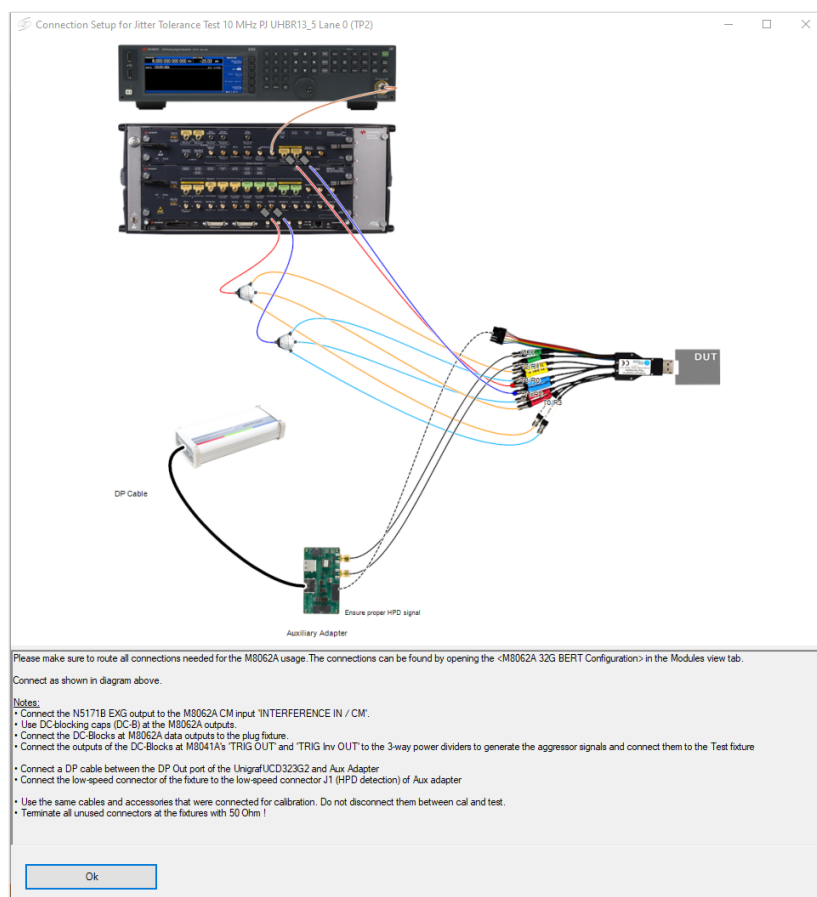


Figure 5. Connection setup for the jitter tolerance test at UHBR10

Expert Mode

By default, the N5991DP2A runs in “Compliance Mode”, which is intended for strict compliance testing, with reduced configurability and especially designed for Authorized Test Centers. But sometimes, compliance testing is not enough, and you want to know what the true performance of your product is. This is where “Expert Mode” becomes handy. Besides including additional jitter margining and receiver sensitivity tests, which are not covered by the DisplayPort PHY CTS, Expert Mode allows a greater degree of freedom to configure the software to further stress and characterize DP receivers. Expert Mode – for advanced, experienced users.

Add-ons support only DP1.4a data rates

N5991DPPX-ADD – DisplayPort Type-C PDO support

The USB Power Delivery (PD) specification enables two USB-C products to advertise voltage/current arrangements or options (PDOs) and negotiate the power transfer contract that will be used while the link operates, supporting power transfers of up to 100W. Furthermore, depending on the application, a given product may provide power to its link partner, or consume the power supplied by its link partner.

Use the N5991DPPX-ADD DisplayPort Type-C PDO Support add-on to be confident that your DP Sink product will be able to function properly under the different power delivery contracts that it supports. This add-on complements the entire test suite included with the N5991DP2A basic software package and automates the configuration of the DUT for a given PDOs. Combined with a Keysight N67xx series modular power supply system, it allows to test your product under acting as power provider or power consumer.

N5991DPSX-ADD – DisplayPort switch system

The N5991DP2A base software package can fully characterize and test a DisplayPort Sink product. But it still requires a certain amount of user interaction if testing a multi-lane product. Use N5991DPSX-ADD to take test automation to the next level by adding a switch system to the setup that will route the test signals through the test channel appropriately to interchange the victim/aggressor lane roles. The N5991DPSX-ADD software add-on is compatible with the BitifEye BIT-2100 series switch system. Please do not hesitate to contact Keysight or BitifEye if you have questions or would like to have more information about this powerful capability.

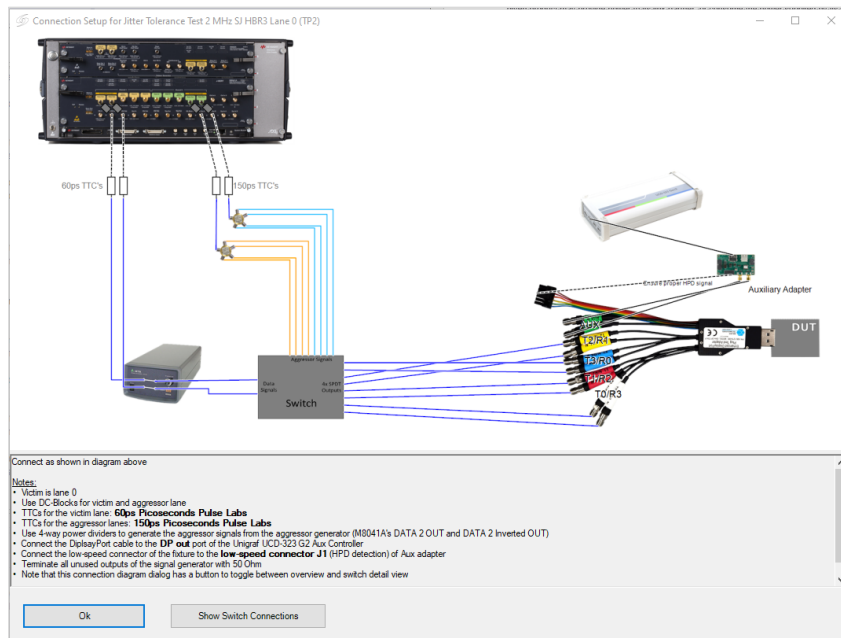


Figure 6. Connection setup for the jitter tolerance test at HBR3 with a switch system

The software provides a secondary connection diagram to show the connections to and from the switch in more detail.

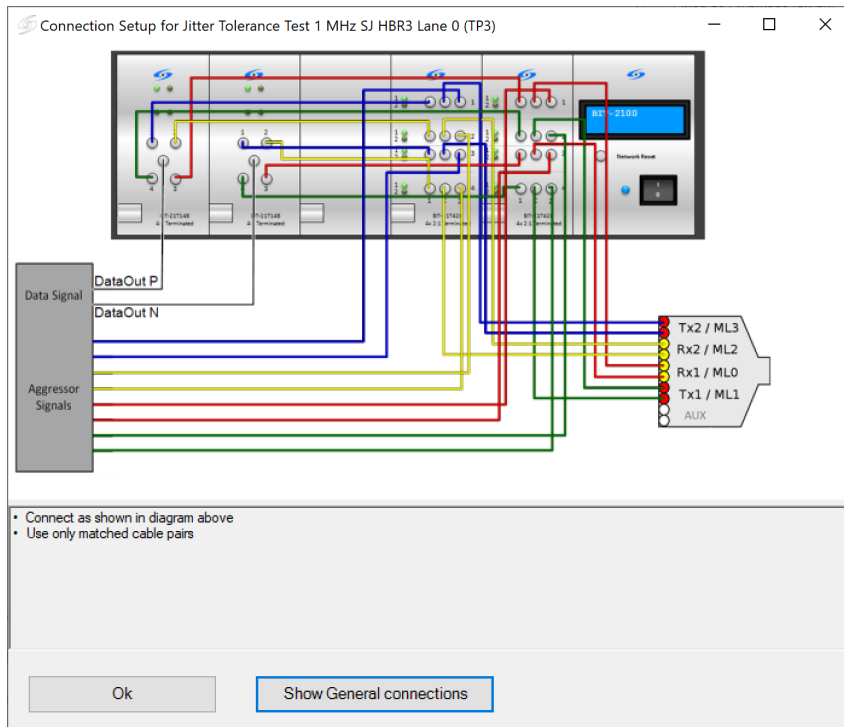


Figure 7. Detailed view of connections with a switch system

Ordering Information

N5991DP2A	DisplayPort 2.1 receiver tests
N5991DP2A-1FP	Perpetual, node-locked license
N5991DP2A-1TP	Perpetual, transportable license
N5991DP2A-SFM	Software maintenance, 12 months, node-locked license
N5991DP2A-STM	Software maintenance, 12 months, transportable license
N5991DP2A-SF3	Software maintenance, 36 months, node-locked license
N5991DP2A-ST3	Software maintenance, 36 months, transportable license

N5991DP2A	DisplayPort 2.1 receiver tests add-ons
N5991DPPX-ADD	DisplayPort Type-C PDO Support Add-on (Support only DP1.4a rates)
N5991DPSX-ADD	DisplayPort Switch System Support Add-on (Support only DP1.4a rates)

License types

Node locked

License can be used on one specified computer.

Transportable

License can be used on one computer at a time but may be transferred to another using the BitifEye License Manager.

Instrument Requirements

- Keysight M8020A or M8040A Series High-Performance BERT Platform
- Keysight UXR-Series Oscilloscope
 - At least 16 GHz for bitrates up to HBR3
 - At least 21 GHz for all bitrates covered by DisplayPort 2.1
- Unigraf UCD-323G2 Reference Source

Module	M8020A		M8040A
	M8041A	M8062A	M8045A
Data Rates			
RBR	Y	N	N
HBR	Y	N	N
HBR2	Y	N	N
HBR3	Y	N	N
UHBR10	N	Y	Y
UHBR135	N	Y	Y
UHBR20	N	Y	Y
Interference/AWG			
5182B MXG/5171B EXG	Y	Y	Y
81160A	Y	Y	Y
M8195A	Y	Y	Y

Y: Supported, N: Not-supported

Contact Keysight Technologies for more details about the supported instrument configurations.

System Requirements

Visit <https://www.bitfeye.com/download-n5991/> and read the changelog of the current software release for detailed information on software and hardware requirements.

Software

Requirements

- OS: Windows 10
- Microsoft .NET
- Keysight IO Libraries Suite
- Exact versions of software requirements are listed in the respective changelog file.

Recommendation

- Microsoft Office Excel, English version

Hardware

Requirement

- Connectivity hardware for instrumentation, depending on configuration e.g. USB3, Ethernet

Recommendations

- Multicore processor with 12 logical processors or more
- 32GB RAM or higher

Application Programming Interface (API)

The N5991 ValiFrame remote interface allows ValiFrame functionality (such as test setup information, calibration, and test procedures, and results) to be accessed from external programming environments. Remote interface does not need a special license to be used, it is included in the base product of particular standards. The remote interface can thus be used to control the N5991 with external software.

In typical use, a top-level external test sequencer takes advantage of ValiFrame functionality

Software Maintenance

The purchase of one -SFM maintenance license for -1FP product licenses or one -STM maintenance license for -1TP product licenses provides the ability to install updates for one year.

With the initial purchase of a product license, it is possible to purchase a 3-year software maintenance license. A -SF3 maintenance license covers a -1FP product license and -ST3 maintenance license covers a -1TP product license.

A software maintenance license is always valid for the respective RX test or Debug Tool e.g., Link Training Suite or Frame Generator product only.

Software Maintenance includes updates to newer instrument firmware as well as procedure and test limit changes for the test specifications covered by the products the software maintenance license belongs to. Upgrades to a different test specification are not covered.

All N5991 RX test or Debug Tool / Link Training Suite licenses which were purchased after November 30th, 2020 will no longer include an automatic Software Maintenance during the first year. Thus, it requires a respective software maintenance license to be able to install updates.

Products which do not have a software maintenance offering and are not an Add-On cannot be updated but are operational still when using the last version for which software maintenance was available.

Software without any extra software maintenance product associated with it, will have a maintenance expiration date of the license issue date + 14 days as a starting point. The software itself will still work, even if the maintenance is expired. If software maintenance has expired a new software maintenance license can be purchased for this product. But the new software maintenance will not grant coverage starting from the purchase date but from the date the previous software maintenance coverage expired. For example, the software maintenance expired on April 30th, 2020, and a new 1-year software maintenance is purchased on August 1st, 2020, the purchased coverage will take May 1st, 2020, and will end on April 30th, 2021.

Related Products

D9040DPPC DisplayPort Tx Test Software

D9042DPPC DisplayPort UHBR Tx Test Software

D9020USBC USB 3.2 Tx Compliance Test Software

D9040USBC USB4 Tx Test Software

D9050USBC USB4 Version 2.0 Tx Test Software

M8020A High-Performance BERT

M8040A High-Performance BERT

UXR The World's Most Advanced Oscilloscope

N5991 Receiver Compliance Test Automation Platform

N5991U32A USB 3.2 Receiver Compliance Test Software

N5991U42A USB4 Receiver Compliance Test Software

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