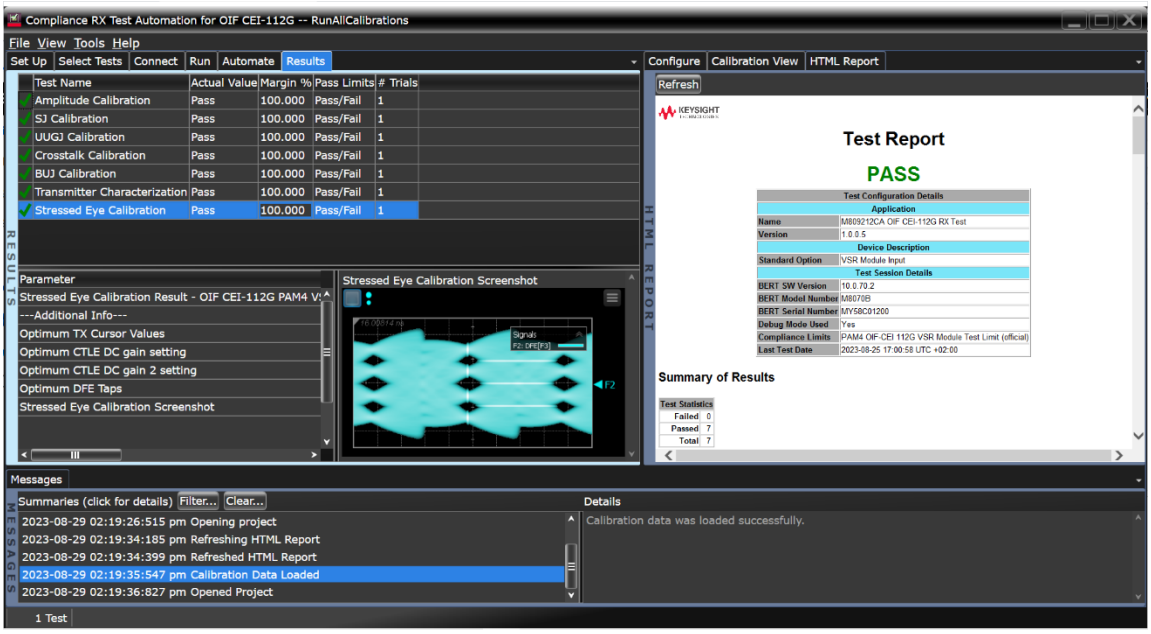
M809212CA

Electrical receiver conformance test application
for OIF-CEI 5.0

Introduction

The M809212CA electrical receiver conformance test application enables accurate and repeatable receiver test procedures following the OIF-CEI 5.0 recommendations to ensure interoperability between datacom interfaces with a lane rate of 112 Gbps. The test procedures are based on the Channel Operating Margin (COM) method for Medium Reach (MR) and Long Reach (LR) interface testing and on the stressed eye method for Very Short Reach (VSR) interface testing.



KEYSIGHT

Key Features

- Interface testing following recommendations from
  - OIF-CEI 5.0: CEI-112G-MR-PAM4 Medium Reach
    - 26.3.2.4 Receiver Interference Tolerance
    - 26.3.2.5 Receiver Jitter Tolerance
  - OIF-CEI 5.0: CEI-112G-LR-PAM4 Long Reach
    - 27.3.2.4 Receiver Interference Tolerance
    - 27.3.2.5 Receiver Jitter Tolerance
  - CEI-112G-VSR-PAM4 Very Short Reach Interface
    - 23.3.11.3 Host and Module stressed input test
    - 23.3.12 Input Overload Voltage Tolerance
- HTML test report
- Remote control & data analytics
- Choose between node-locked, transportable, network, USB-dongle perpetual license

Description

The M809212CA electrical receiver conformance test application is designed to assist and simplify the stressed signal calibration used for testing the inputs of OIF-CEI 5.0 — very short, medium and long reach electrical interfaces (VSR (MR/LR) using a Keysight M8050A 120Gbd High-Performance BERT combined with a Keysight Digital Communication Analyzer (DCA)) time-equivalent oscilloscope or Infiniium UXR real-time oscilloscope. It reduces user interaction to a minimum and performs all required calibration routines and compliance testing automatically by remote control of all required instruments. At the same time, it offers flexibility to test different scenarios within or beyond the standard recommendations.

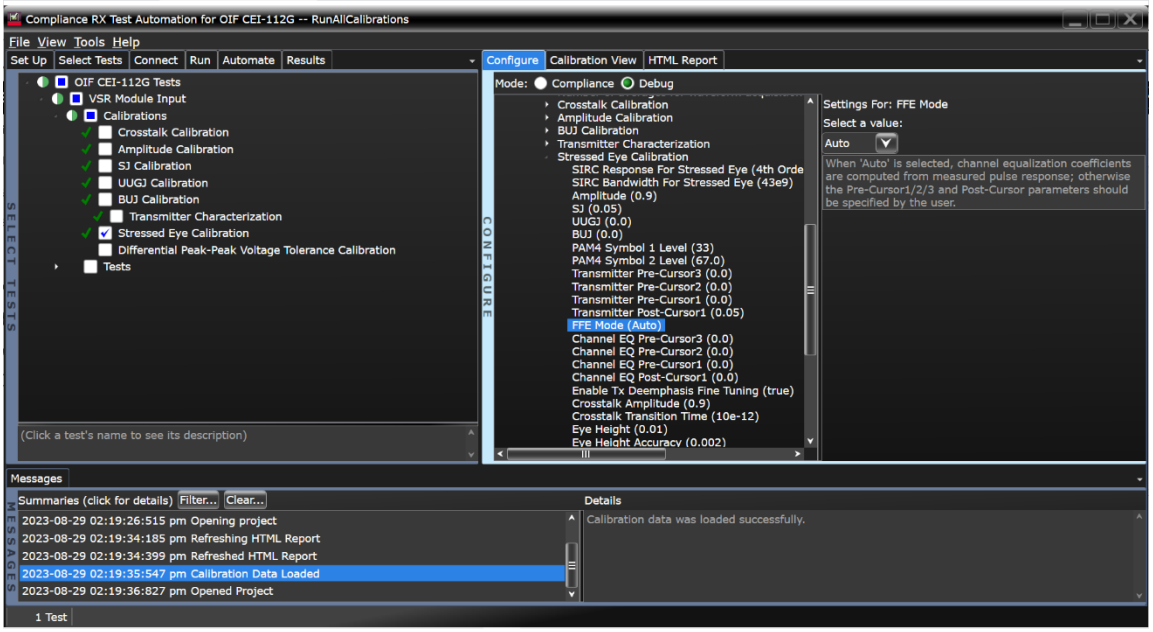


Figure 1. Graphical user interface of the M809212CA conformance receiver test application

The test application utilizes the same framework as other Keysight conformance test applications, thus reducing the training time and offering the functionalities remote control, scripting, and automated pdf or HTML-based test report generation. The user is guided by means of diagrams as well as text to minimize errors. Results of the individual calibration steps and tests are presented in tabular form as well as graphical form, where appropriate. Calibrations and test results can be stored in projects and recalled later.

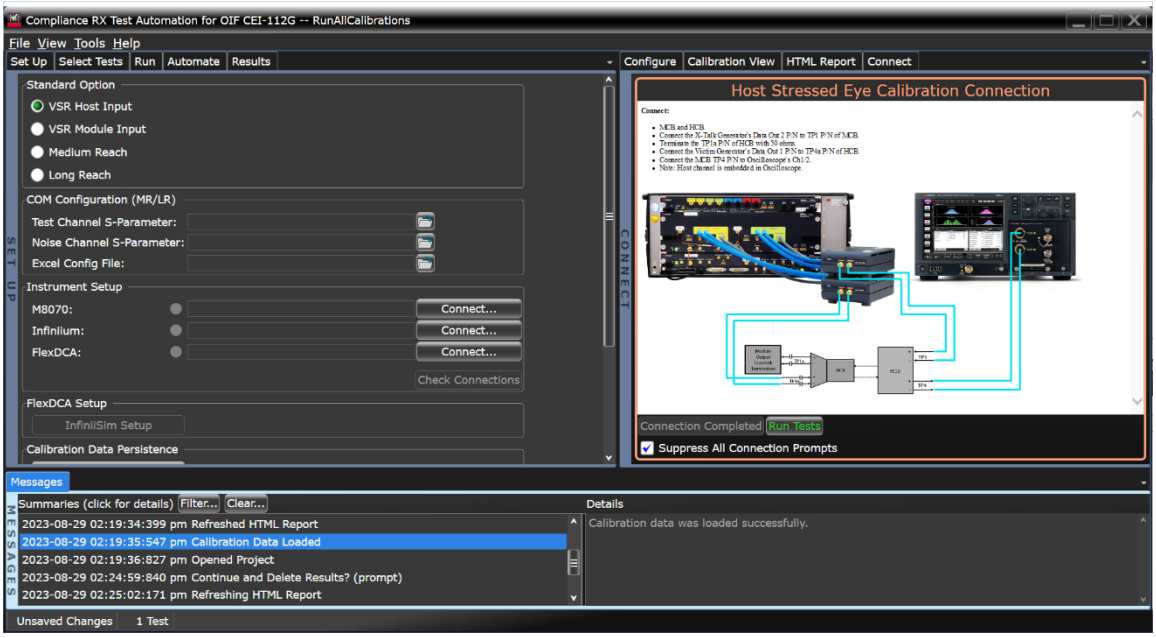


Figure 2. Connection diagram for Very Short Reach, VSR host stressed input test calibration

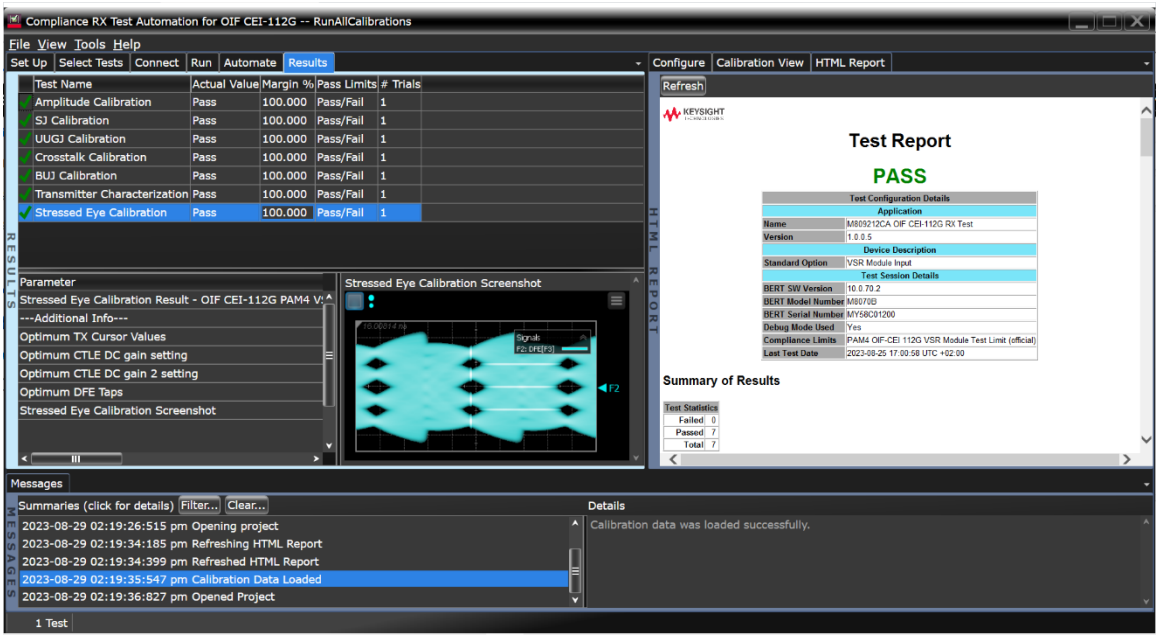


Figure 3. Results of a VSR stressed input test signal calibration

Parameter	Value
Transmitter Measurements - OIF CEI-112G PAM4 VSR Module TP0a	Pass
---Additional Info---	
Transition Time	10 ps
Output Jitter Measurement	(See image)
Linear Fit Pulse Response(Np=200)	(See image)
Transmitter Measurements	

Measurement Name	Status	Measured Value	Margin %	Pass Limits
Jrms	Pass	19.0 mUI	17.4 %	<= 23.0 mUI
J4u	Pass	101.5 mUI	14.0 %	<= 118.0 mUI
Level mismatch ratio RLM	Pass	0.96	1.1 %	>= 0.95
Signal-to-noise-and-distortion ratio(Np=200)	Pass	36.40 dB	12.0 %	>= 32.50 dB

Parameter	Value
Stressed Eye Calibration Result - OIF CEI-112G PAM4 VSR Module TP1a	Pass
---Additional Info---	
Optimum TX Cursor Values	(0,0.03,-0.14,0.73,0.1)
Optimum CTLE DC gain setting	-3.0 dB
Optimum CTLE DC gain 2 setting	-1.0 dB
Optimum DFE Taps	(0.1,0.05,0.025,0.0125)
Stressed Eye Calibration Screenshot	(See image)
Stressed Eye Calibration Results	

Standard Parameter	Status	Target	Measured	Instrument Parameter	Nominal	Actual
EH6	Pass	10 mV	10 mV	Amplitude	900 mV	299 mV
VEC6	Pass	12dB	11.6dB	RJ	0.00000 UI	15.42 mUI
Eye Linearity	Pass	0.9	0.87	Lower PAM4 Eye Level	33%	32%
Eye Linearity	Pass	0.9	0.87	Upper PAM4 Eye Level	67%	68%

Figure 4. Results of the reference transmitter characterization (top) and stressed eye calibration for VSR Host Input (bottom)

Calibrations and Tests Covered by M809212CA

OIF-CEI 112G MR/LR-PAM4 (Medium and Long Reach)

OIF-CEI-112G-LR and -MR test procedures rely on the Channel Operating Margin (COM) method [1]. COM was first introduced to measure the performance margin of a channel and then extended to digital systems. Interoperability of a digital receiver can be expressed in terms of COM requirements. COM is calculated using channel 4-port S-parameters (for victim and aggressor lanes) as well as the noise and equalization functionality of the considered transmitter and receiver. The resulting COM metric is the ratio of the signal amplitude (after equalization) to the noise and crosstalk peak-to-peak amplitude measured during a time interval depending on the target BER (1e-6 for the considered interfaces).

OIF-CEI 112G-MR/-LR receiver test calibration procedure consists of three steps [2].

1. *System calibration*: Calibrate the equipment used to generate the victim transmitter and the broadband noise (once per setup configuration).
2. *Channel characterization*: S-parameter measurements using a Network Analyzer.

COM-related calibration: The following steps are performed to complete the COM model

   a. Verify channel compliance based on S-parameter analysis
   b. Measure transmitter characteristics (jitter & electrical characteristics), which can be adjusted to test different scenarios.
   c. Compute the amount of broadband noise required for a specific channel operating margin (usually 3dB) and inject it into the noise path to test the receiver (BER measurement for different levels of noise or jitter)

1 OIF-CEI 5.0
2 For more details on these standards, refer to OIF-CEI 5.0

After calibration, the MR/LR receiver interference tolerance test and receiver jitter tolerance test can be performed.

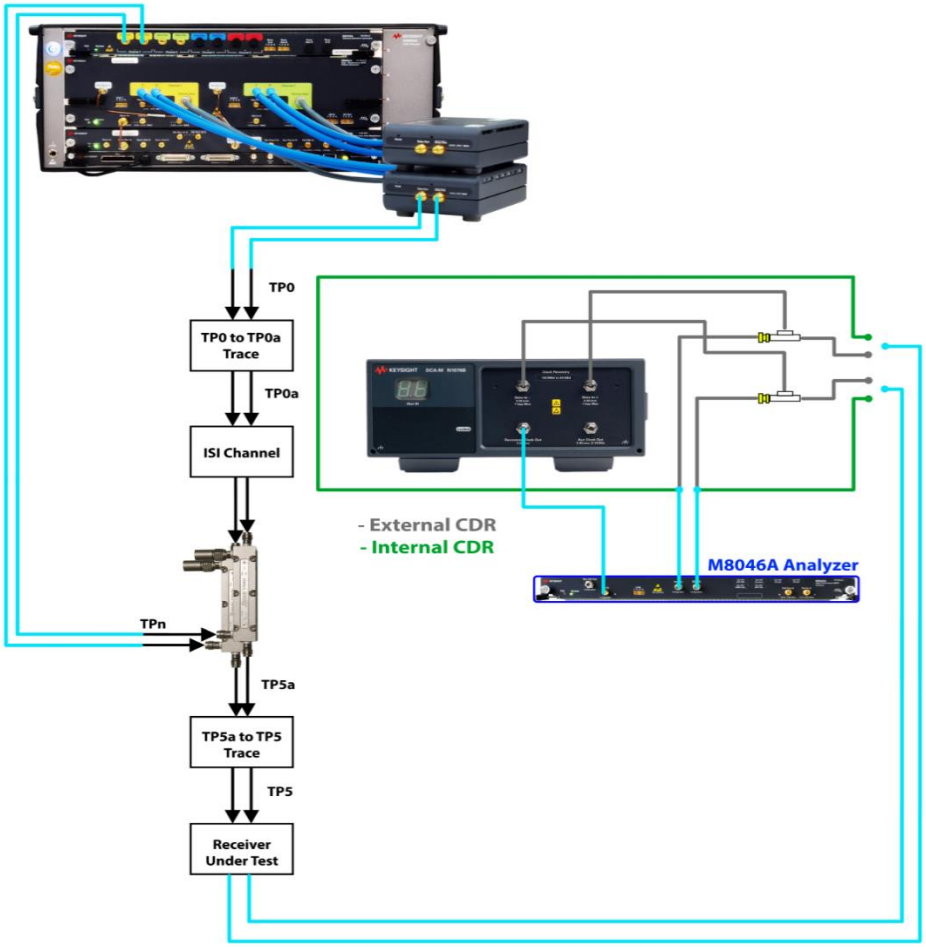


Figure 5. Setup configuration for MR/LR receiver interference tolerance test

Please note that this receiver conformance test application covers only the tests for Receiver Interference and Jitter Tolerance). Other test parameters such as baud rate, effective return loss and Differential to Common Mode Input Conversion can be carried out by the corresponding Keysight Transmitter Test solutions N109212CA listed in **Table 27-9** and **Table 26-9.**

OIF-CEI 112G-VSR-PAM4 (Very Short Reach)

The M809212CA implements both host and module stressed input test procedures defined in the 23.3.11.3 Host and Module stressed input test. The procedure is based on the stressed eye method, where the metrics of the test signal such as vertical eye opening (VEO) and vertical eye closure (VEC) are adjusted at the output of the mated host compliance board (HCB) or module compliance board (MCB) connection towards values defined in the standard by tuning the transmitter amplitude, de-emphasis, and jitter profile. When carried out manually, this calibration procedure is very time-consuming. The M809212CA receiver test application performs this task automatically.

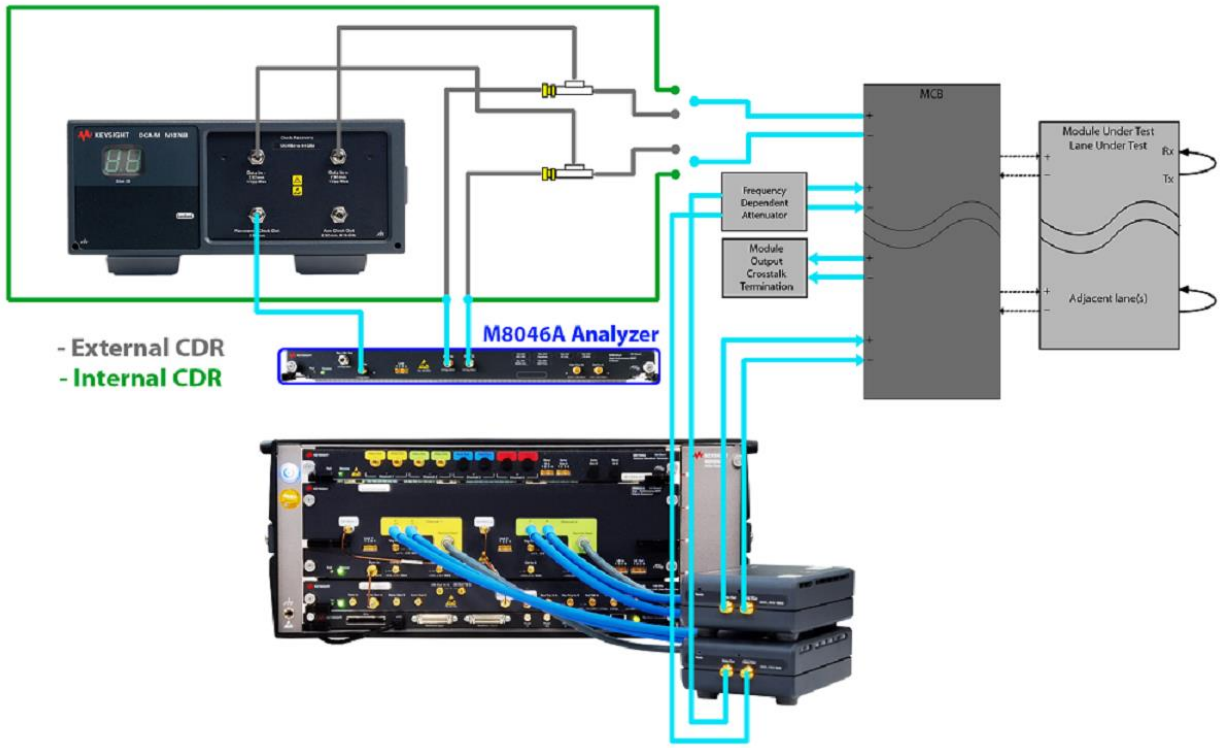


Figure 6. Setup configuration for VSR module stressed input test

OIF-CEI VSR receiver test calibration procedure consists of the following steps:

1. *Crosstalk* calibration 3: The aggressor lane slew time and amplitude are adjusted to meet the specified target. A third-party source can be used as an aggressor channel. In this case, the calibration must be carried out manually.

2. System calibration: Calibrate the amplitude and jitter (sinusoidal, BUJ, UUGJ) of the pattern generator used to generate the victim transmitter (optional, recommended once per setup configuration).

3. Transmitter characterization: In this step, the transmitter characteristics (rise time, SNDR, jitter profile) are measured and compared to the requirements for compliant transmitters. Note that different transmitter profiles can be used as starting points for the stressed eye calibration (optional, recommended once per setup configuration).

4. Stressed signal calibration: The transmitter de-emphasis and receiver equalizer are first optimized. This step is optional but highly recommended to ensure successful calibration. Otherwise, optimal Tx-de-emphasis settings must be provided by the user. After this, the signal amplitude and random jitter are adjusted to meet the target Vertical Eye Opening (VEO) (defined at 1e-6 probability) and Vertical Eye Closure (VEC) metrics.

3 The requirements of the Crosstalk Calibration for the Host and Module Stressed Inputs cannot be met with the M8045A pattern generator. Please refer to the Release Notes for more information and workaround.

Example setup for VSR Host input stressed eye calibration

Connect (for Host):

- MCB and HCB
- Connect X-Talk Generator's Data Out 2 P/N to TP1 P/N of MCB.
- Terminate TP1a P/N of HCB with 50 ohms.
- Connect Victim Generator's Data Out 1 P/N to TP4a P/N of HCB.
- Connect TP4 P/N of MCB to Oscilloscope's CH1/CH2.

Note: Host channel is embedded in the oscilloscope.

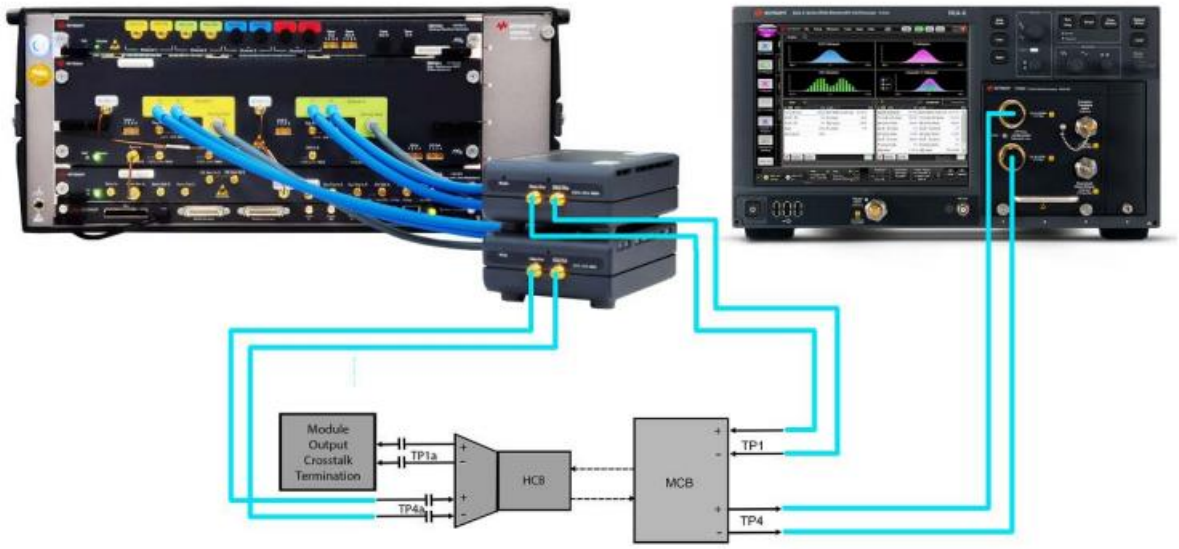


Figure 7. Setup configuration for VSR host stressed input test

VSR stressed input test calibration recommendations

VSR stress mix and calibration targets

	Module input test	Host input test
Sinusoidal Jitter (Refer to Table 23-7)	50 mUI	
Random Jitter (RJ) and Bounded Uncorrelated Jitter (BUJ)	inject if required to meet VEO and VEC targets	
VEC (refer to table 23-1)	12-12.5 dB	
EH (refer to table 23-4)	10 mV	15 mV (FarEnd); 20 mV (NearEnd)

Voltage tolerance test for VSR host input and VSR module input

The host and module voltage tolerance test procedures as defined in 23.3.11.3 Host and Module stressed input test validate the acceptance of the differential input peak-to-peak amplitudes produced by the extreme operating conditions from the transmitter.

Please note that this application covers only the host and module voltage tolerance test procedures as defined in “23.3.11.3 Host and Module stressed input test”. Other requirements listed in Table 23-2 and Table 23-5 (Common Mode Voltage, Differential Termination Resistance mismatch, Differential Mode to Common Mode Conversion and Effective Return Loss) can be verified using the corresponding transmitter application N109212CA from Keysight.

Configuration Guide

The table below shows the required equipment for each standard option under OIF-CEI 5.0. Required instrument configuration and required software options are listed in the following section.

Equipment type	VSR	MR/LR
Victim pattern generator	M8042A	M8042A
Crosstalk generator	2nd channel of /M8042A or third-party crosstalk generator	N.A.
Interference source	N.A.	M8054A or M8196A or M8194A
Victim error detector	M8046A or M8043A or DCI (DUT Control Interface available in M8070ADVB)	
Clock recovery	M8046A – 0A4/ 0A5 (internal CDR) or N1076B / N1078A	
Scope	DCA-X N1000A + N1060A or UXR-Series Oscilloscopes with 70GHz Bandwidth & above	

Minimum required instrument configuration

The options marked * are recommended but not mandatory.

M8000 BERT system

M8040A-BU2 or M8050A-BU2 or M8050A-BU4 [4]	Bundle consisting of one M9505A 5-slot AXIe Chassis with USB option Bundle consisting of one M9505A 5-slot AXIe Chassis with USB option Bundle consisting of two M9505A 5-slot AXIe Chassis with USB
M8070B	System software for M8000 Series of BER test solutions (version 10.0.160.6 or later)

M8050A BERT platform

		M8050A
M8042A		Pattern Generator Module 32/64/120 GBd, 2 or 3-slot AXIe Pattern Generator NRZ and PAM4, 1 Channel, 2-slot AXIe Modu (requires M8058A Remote Head)
◦	M8042A-0G1	
◦	M8042A-G64	Pattern Generator, 64 GBd for NRZ and PAM4, module-wide License
◦	M8042A-0G4	De-emphasis, module-wide License
◦	M8042A-0G2*	Pattern Generator NRZ and PAM4, 2 Channel, 3-slot AXIe Module (requires M8058A Remote Head)
M8058A		Remote Head, 32/64 GBd for M8042A Pattern Generator
◦	M8058A-801	Matched Cable Pair, 1.85 mm (m) to 1.85 mm (m), 2 ps, 0.15 m
M8009A		Clock Generator Module with Jitter Modulation, 60 GHz, 1 slot AXIe
◦	M8009A-061	
◦	M8009A-0G3	Advanced Jitter Modulation for up to two Channels, License

4 A two-chassis approach is required for the M8050A-based configuration covering VSR and MR/LR when an externa error detector is required.

Configure the error analyzer [5]

M8046A		Analyzer module, 32/64 Gbaud 1-slot AXIe
∘	M8046A-A64	Analyzer, one Channel, Data Rate up to 64 GBaud, NRZ
∘	M8046A-0A4*	Clock recovery for 32 Gbaud, License
∘	M8046A-0A5*	Clock recovery for Extension up to 64 Gbaud License
∘	M8046A-0P3	PAM-4 decoding up to 32 GBaud, License
∘	M8046A-0P6	PAM-4 Extension up to 58 GBaud, License
∘	M8046A-0A3	Equalizer License
∘	M8046A-802*	Matched cable pairs, two matched cable pairs are required
∘	M8046A-801	Cable 2.92 mm (m) to 2.92 mm (m), 0.5 m for clock input, Qty 1
M8043A		Analyzer Module 32/64 Gbaud, NRZ and PAM4 2-slot AXIe
∘	M8043A-A64	Analyzer, one Channel, Data Rate up to 64 GBaud, NRZ and PAM4
∘	M8043A-0A3	Equalizer License
N1076B/N1078A [6]		
∘	N107xx-264	Supported input rates 125 MBd to 64 GBd
∘	N1076B-CR1	Clock Recovery Phase Matching Kit for N076B Electrical
∘	N1076B-2PB	Microwave Pick-off Tee 1.85 mm connectors, matched pair
∘	11900B	2.4 mm female to 2.4 mm female adapter
∘	83059A	Coaxial Adapter, 3.5 mm Male-Male

Select an interference source for the MR/LR application

M8194A		120 GSa/s Arbitrary Waveform Generator
∘	M8194A-001	Arbitrary Waveform Generator, 1 Channel 120 GSa/s
M8196A		92 GSa/s Arbitrary Waveform Generator
∘	M8196A-001	Arbitrary Waveform Generator 1 Channel 92 GSa/s
M8054A		Interference Source 32 GHz

Choose between DCA-X (recommended) and UXR platform

		DCA-X
N1000A		DCA-X Wide-Bandwidth Oscilloscope Mainframe
∘	N1000A-PLK	Pattern Lock Trigger Hardware Model
N1060A		Precision Waveform Analyzer
∘	N1060A-050	Two 50 GHz channels
∘	N1060A-EVA	Equalizer Integrated variable
∘	N1060A-264	Supported input rates 125 MBd to 64 GBd
∘	N1060A-PTB	Precision Timebase Ultra/Low Radom Jitter
∘	N1060A-JSA	Jitter Spectrum Analysis and Clock Recovery Emulation

5 Not required if internal error counters of the device under test are used.
6 Choose on external N107xx Clock Recovery if M8046A-A04/-A05 options not selected. Not required when DUT internal error counter is used.

UXR0702A or UXR0702B	70 GHz, 2-CH, Infiniium UXR-Series real-time Oscilloscope
D9020ASIA	Advanced Signal Integrity Software (EQ, InfiiniSimAdv, Crosstalk)
D9010PAMA	Pulse Amplitude Modulation PAM-N Analysis Software
D9020JITA	Jitter, Vertical and Phase Noise Analysis Software for 90000, V-, Z- and UXR-Series Oscilloscopes
Accessories & fixtures (recommended)	
M8195A-810	Cable, 2.92 mm (m) to 2.92 mm (m), length-0.85 m (for combining SI and RI)
M8195A-820	Coaxial termination 50 Ω DC to 26.5 GHz, 3.5 mm (male) (2 required)
SP0602A	Wilder OSFP 112G/800G MCB 1.85 mm Receptacle Test Adapter
SP0603A	Wilder OSFP 112G/800G HCB Plug 1.85 mm Test Adapter
SP0606A	Wilder QSFP-DD 112G/800G MCB 1.85 mm Receptacle Test Adapter
SP0607A	Wilder QSFP-DD 112G/800G HCB Plug 1.85 mm Test Adapter
M8045A-802 [7]	Matched directional coupler pair, 50 GHz, 13 dB, 2.4 mm
-	Wilder DCOM-ISI-112G-9CH-36F-1.85, Datacom ISI 112G 9-Channel Board (for VSR, MR low- and high-loss and LR low-loss)
M8067A-001	ISI Channel Board Three Traces 6.2, 11.7, and 17.1 inches, 1.85 mm Connectors (for VSR and MR high-loss)
M8067A-002	ISI Channel Board Three Traces 6.2, 11.7, and 17.1 inches, 1.85 mm Connectors (for LR low-loss and high-loss)
Software configuration	
M8070ADVB-1xx	Advanced Measurement Package for M8000 Series of BERT Test Solutions (node locked, transportable, floating or USB license, revisions 9.1 or later)
M809212CA-1xx	Conformance RX Test Automation for IEEE 802.3ck (node-locked, transportable floating or USB license)
N1010100A	Research and Development Package for FlexDCA-DCA-X mainframe minimum configuration [8]

7 For MR/LR application
8 Corresponding legacy DCA options: N1010AT-200/-201/-0EP/-SIM

Minimum PC configuration

The PC running the application should meet the following requirements

PC hardware requirements

- Operating system: Windows 10 (64 bit), Version 1809 or later
- Memory: 8 GB RAM minimum
- Monitor resolution: WXGA+ (1440 x 900) minimum

PC software requirements

- Microsoft Office 2019 or higher
- Microsoft .NET Framework 4.7.1 or newer
- Keysight IO Library Suite Rev. 18.1
- Keysight License Manager 5 and Keysight License Manager 6
- Keysight M8070B system software for M8000 series
  - Ver. 10.0.160.6
  - M8070ADVB Advanced Measurement Package for M8000 Series Ver. 1.6.180.2
  - M8194A soft front panel version 2.0.31.0 or later or M8196A soft front panel version 2.1.1.0
- Keysight DCA-X Oscilloscope FW rev. A.07.41.27
- Keysight UXR Oscilloscope FW rev. 11.50.00601
- MATLAB Compiler Runtime R2017a (9.2)

Remote Programming

The M809212CA Conformance Receiver Test Application for OIF-CEI 5.0 is part of Keysight's Digital Test Apps and can be programmed via ARSL, any .NET language. For more information, see www.keysight.com/find/rpi.

Data Analytics Enabled

This test application supports data exporting with support from the Keysight KS6800A Data Analytics Software. For more information see www.keysight.com/find/data-analytics.

Related products

The N109212CA Electrical TX Test Software for OIF-CEI 5.0 for the sampling oscilloscopes offers automated transmitted testing for OIF PAM-4 based electrical outputs.

The D9050CEIC Electrical TX Test SW for OIF-CEI-112G-PAM4 (VSR/MR/LR) for the real-time oscilloscopes offers automated transmitter testing for OIF PAM4-based electrical outputs.

The M8091CKCA Electrical Receiver Conformance Test Application for IEEE 802.3ck enables accurate and repeatable receiver test procedures following the IEEE 802.3ck Draft 3.3 recommendations to ensure interoperability between datacom interfaces with a lane rate of 106 Gbp

The N4917BSCB Optical Receiver Stress Test Application addresses test needs for optical input test of transceiver modules for IEEE 400GBASE-based optical interfaces.

The N19301B PLTS Base Analysis is the industry standard for signal integrity measurements and data post-processing of high-speed interconnects, such as cables, backplanes, PCBs and connectors.

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