M8091DJCA

Receiver Conformance Test Application for IEEE 802.3dj

Introduction

The M8091DJCA receiver conformance test application enables accurate and repeatable receiver test procedures following the IEEE P802.3dj/D2.0 recommendations to ensure interoperability between datacom interfaces with a lane rate of 200 Gbps. This solution covers the Chip-to-Chip (C2C), Chip-to-Module (C2M), backplane (KR), and twinaxial copper cable (CR) interfaces.

KEYSIGHT

Key Features

- Validation of digital receiver designs running at 106.25Gbaud PAM4 lane rate following the test procedure defined in IEEE P802.3dj/D2.0 *

Annex 176C 200GAUI-1 C2C

- 176C.6.4.2 Receiver amplitude tolerance
- 176C.6.4.5 Receiver interference tolerance
- 176C.6.4.6 Receiver jitter tolerance

Annex 176D 200GAUI-1 C2M

- 176D.8.11 Amplitude Tolerance
- 176D.8.12 Interference Tolerance
- 176D.8.13 Jitter Tolerance

Clause 178 200GBASE-KR1

- 178.9.3.3 Receiver amplitude tolerance
- 178.9.3.4 Receiver interference tolerance
- 178.9.3.5 Receiver jitter tolerance

Clause 179 200GBASE-CR1

- 179.9.5.2 Receiver amplitude tolerance
- 179.9.5.3 Receiver interference tolerance
- 179.9.5.4 Receiver jitter tolerance

- Guided setup, automated stressed signal calibration, and pre-conformance measurement
- HTML test report
- Remote control
- Choose between node-locked, transportable, network, or USB-dongle perpetual license

*** Note:**
The M8091DJCA electrical receiver conformance test application does **not support** *Auto-Negotiation* (Clause 73) or *Inter-sublayer Link Training* (Annex 178B). Instead, an alternative method is employed to optimise the pattern generator's de-emphasis coefficients prior to testing.

As the Device Under Test (DUT) may lack the capability to return error statistics required for estimating the *block error ratio* (Clause 174A.8), the compliance application reports the **raw Bit Error Rate (BER)** by default. If the DUT or an external error detector can provide block error ratio data, the BER target may be adjusted accordingly.

Description

The M8091DJCA electrical receiver conformance test application is designed to assist and simplify the stressed signal calibration used for testing the inputs of IEEE P802.3dj/D2.0 for Chip-to-Chip (C2C) and Chip-to-Module (C2M), backplane (KR), and twinaxial copper cable (CR) electrical interfaces using a Keysight M8050A 120Gbd High-Performance BERT combined with a Keysight Infiniium UXR real-time oscilloscope. It reduces user interaction to a minimum and performs all required calibration routines and compliance testing automatically by remotely controlling all required instruments. At the same time, it offers flexibility to test different scenarios within or beyond the standard recommendations.

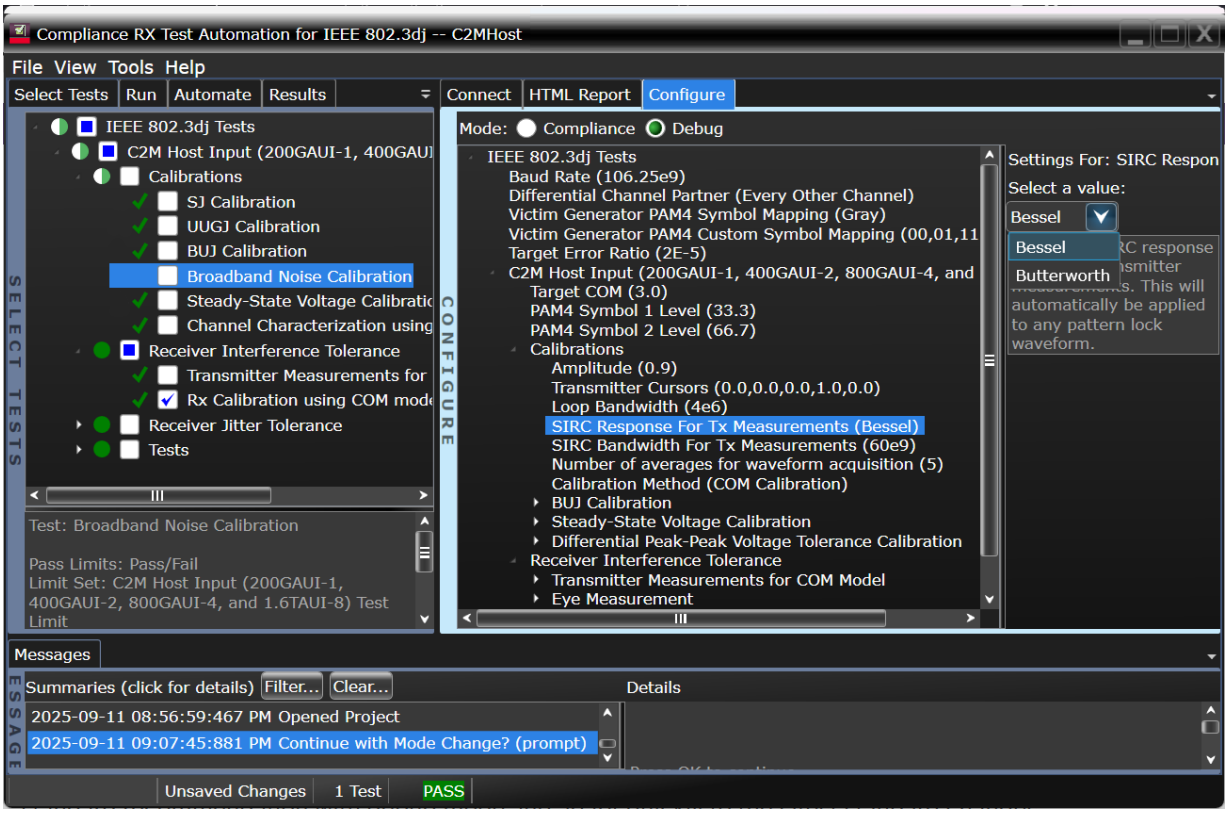

Figure 1. Graphical user interface of the M8091DJCA IEEE 802.3dj conformance receiver test application

The test application utilizes the same framework as other Keysight conformance test applications, thereby reducing training time and offering functionalities such as remote control, scripting, and automated PDF or HTML-based test report generation. The user is guided by means of diagrams as well as text to minimize errors. Results of the individual calibration steps and tests are presented in tabular form as well as graphical form, where appropriate. Calibrations and test results can be stored in projects and recalled later.

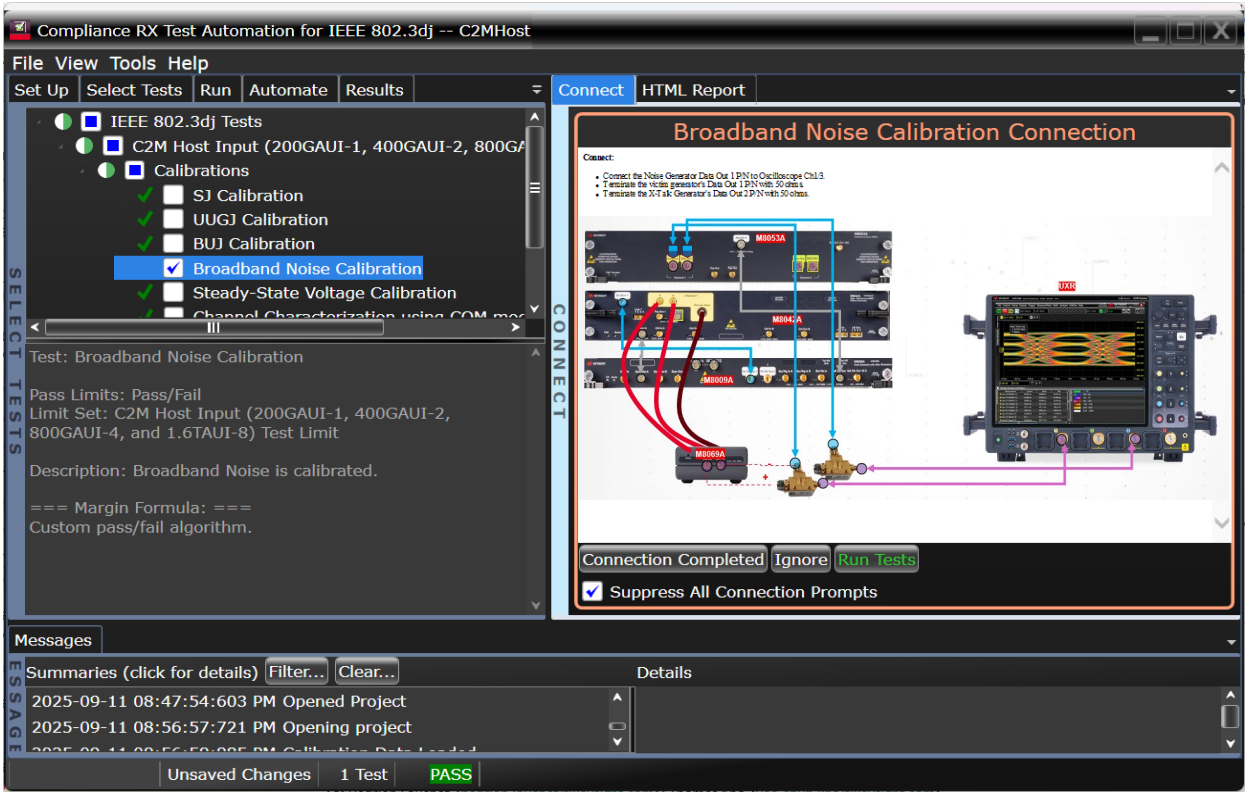

Figure 2. Connection diagram for C2M, broadband noise calibration

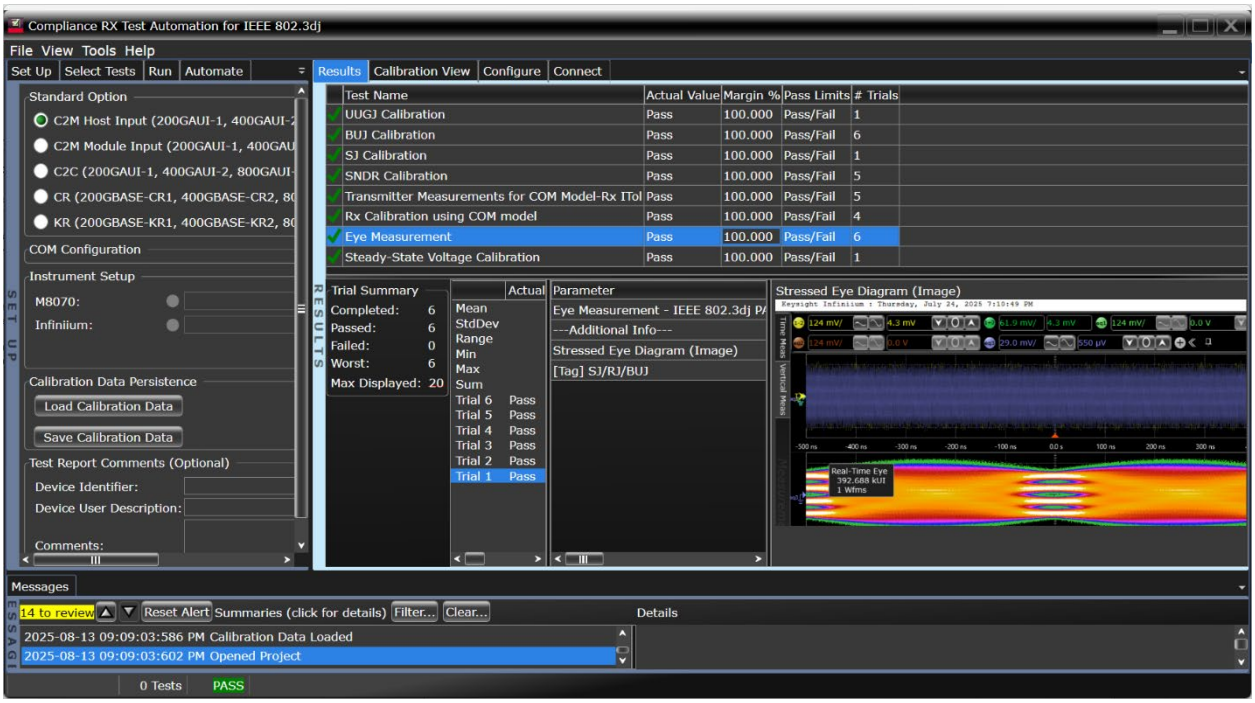

Figure 3. Results of a C2M Interference Tolerance calibration (Draft 1.4)

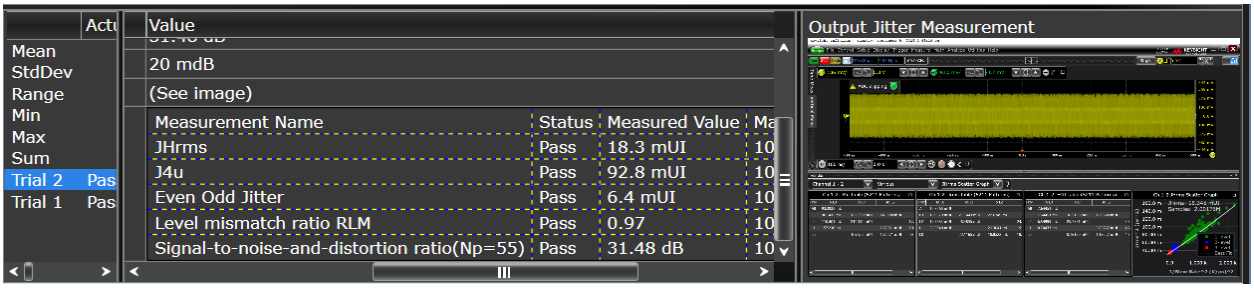

Figure 4. Results of the reference transmitter characterization

Calibrations and Tests Covered by M8091DJCA

200GAUI-1 C2C (Chip-to-Chip) and 200GBASE-KR1 (backplane)

The Chip-to-Chip (C2C) test procedures defined in IEEE P802.3dj/D2.0, Annex 176C rely on the Channel Operating Margin (COM) method [1]. COM was first introduced to measure the performance margin of a channel and then extended to digital systems. The performance of digital receivers can be expressed in terms of COM requirements. COM is calculated using channel S-parameters (as well as the noise and equalization functionality of the considered transmitter and receiver. The resulting COM metric is the ratio of the signal amplitude (after equalization) to the noise and crosstalk peak-to-peak amplitude measured during a time interval depending on the target BER.

The IEEE 802.3dj C2C receiver test calibration procedure for the Interference Tolerance Test consists of the following steps [2].

1. *System calibration*: Calibrate the equipment used to generate the victim transmitter and the broadband noise (once per setup configuration).
2. *Channel characterization*: S-parameter measurements using a network analyzer. This is done once per setup configuration for both signal and noise (optional) paths.
3. *Channel and transmitter characterization*: Verify channel compliance based on S-parameter analysis. This is achieved by estimating the COM of this specific channel, assuming reference transmitter and receiver designs.
4. Characterize the actual transmitter (rise-time, SNDR[3], Jitter[4], linearity[5]), which can be adjusted to test different scenarios.
5. *COM-based calibration*: Based on 3.a) and 3.b), compute the amount of broadband noise to be injected at the receiver input (TP5a) required to meet a target channel operating margin (typically 3dB).

1 IEEE Standard for Ethernet, IEEE 802.3, Annex 93A.
2 For more details on these standards, refer to IEEE Standard for Ethernet, IEEE 802.3, Annex 176C.
3 Signal-to-Noise-Distortion-Ratio
4 J_{RMS}, $J4u_{03}$, (see clause 179.9.4.6.1)
5 Level separation mismatch ratio, R_{LM}

For the receiver interference tolerance test, the broadband noise is injected into the noise path, and the receiver performance (bit error rate or, if available, the “block error ratio”) is retrieved from the Device Unter Test (DUT) internal error checker.

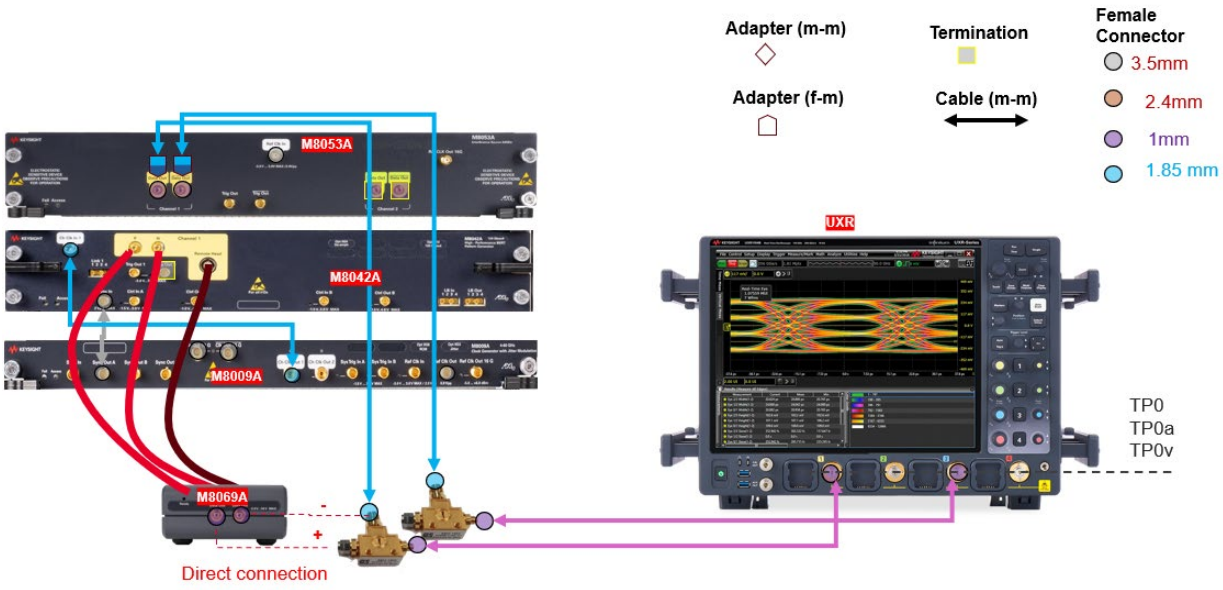

Figure 5. Setup configuration for the C2C receiver interference tolerance test

While the backplane (KR) interface (clause 178) has different loss targets for the test channel than C2C, it follows a similar test procedure. Different parameters are used in the COM model to calculate the Channel Operating Margin.

200GAUI-1C2M (Chip-to-Module) and 200GBASE-CR1 (Coaxial Copper)

The M8091DJCA implements the *amplitude, interference, and jitter tolerance tests* [6] for both module and host, following the procedures defined in IEEE P802.3dj/D2.0, annex 176D.

Legacy C2M interfaces such as IEEE 802.3ck (100G per lane) rely on stress eye calibration, where eye metrics such as Eye Height and Vertical Eye Closure are adjusted at the output of the test channel by tuning the transmitter amplitude, de-emphasis, and jitter profile to meet the limits defined by the standard.

Instead, for 200G lane rate interfaces, the IEEE 802.3dj standard recommends inserting broadband noise at the transmitter side to adjust the link channel operating margin (COM) towards 3dB. The amount of noise to be injected depends on the actual test channel and transmitter characteristics such as SNDR, jitter profile, and eye linearity.

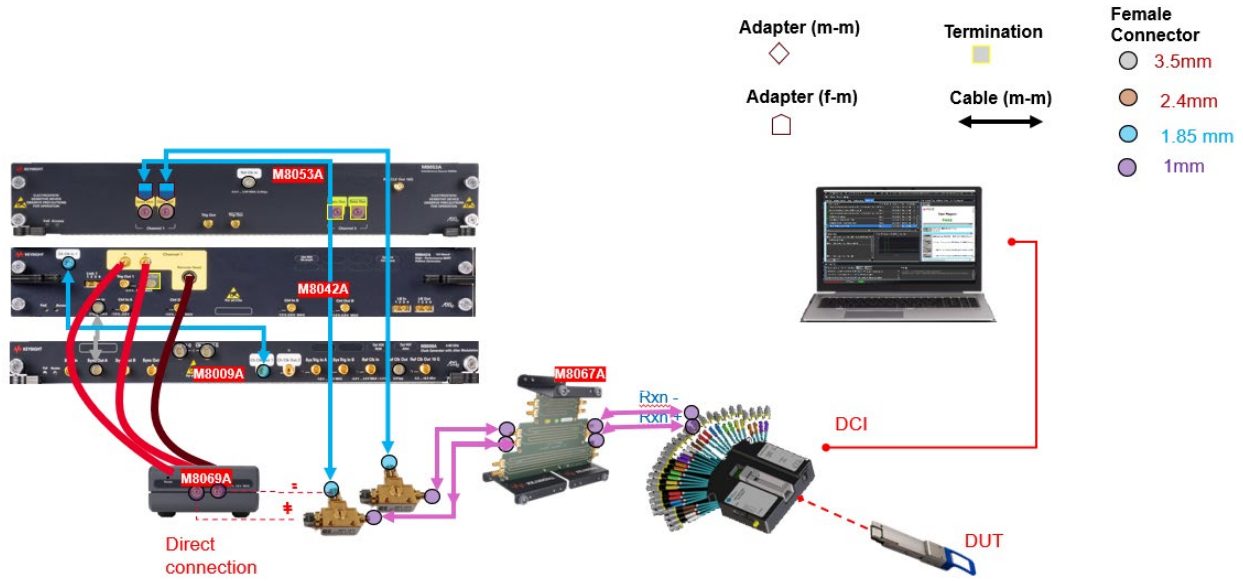

Figure 6. Setup configuration for C2M module stressed input test

6 Repeat the limitation w.r.t to ILT and block error ratio

The M8091DJCA supports two different approaches for stress signal calibration. The procedure detailed in IEEE P802.3dj/D2.0 is similar to the C2C, but with a different test channel and with the noise injected at the transmitter side (TP0v) [7]: The second approach described in IEEE P802.3dj/D1.4 consists of the following steps:

1. *System calibration*: Calibrate the equipment used to generate the victim transmitter (once per setup configuration)
2. *SNDR calibration*: Measure the Signal-to-Noise-Distortion-Ratio (SNDR) for varying broadband noise amplitude after the channel
3. *Link characterization*: Measure the transmitter SNDR, jitter, RLM, and pulse response after the channel
4. *COM-based calibration:* Using results from steps 2 and 3, determine the broadband noise amplitude needed to achieve the SNDR required to meet a 3 dB COM for the combined actual transmitter and test channel.

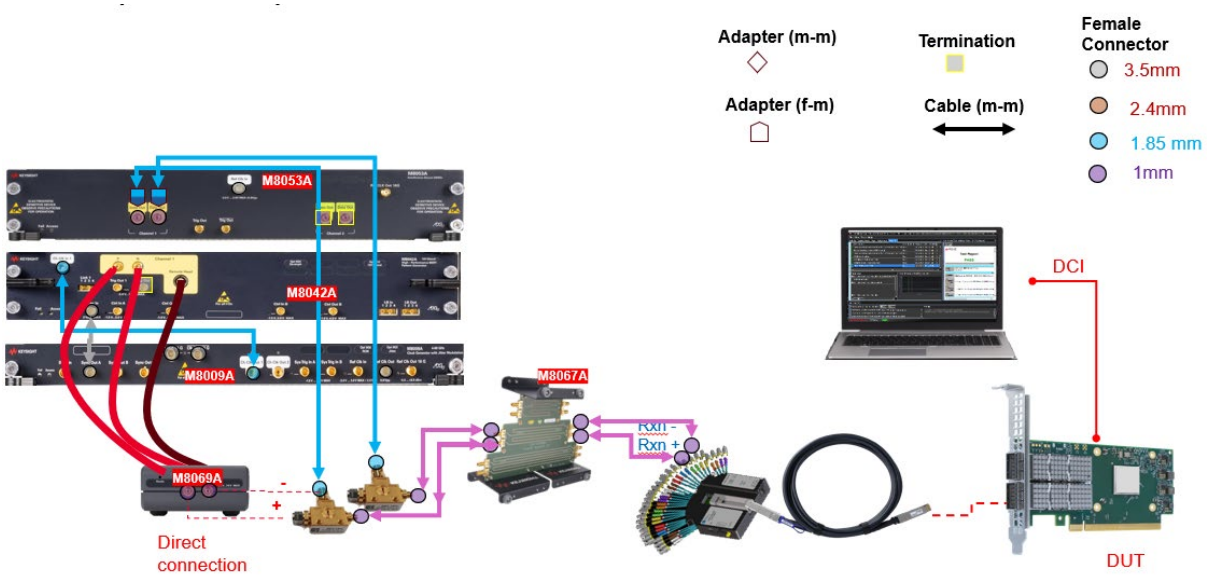

Figure 7. Setup configuration for the CR receiver interference tolerance test

While the backplane (CR) interface (clause 179) has a different test channel than C2M, it follows a similar test procedure. Different parameters are used in the COM model to calculate the Channel Operating Margin and the amount of broadband noise to be injected at the transmitter side.

7 For more details, refer to the M8091DJCA User Guide

Overview of Test and Calibration Channels

The channels used for receiver validation have different mechanical characteristics depending on the interface being tested. In principle, any channel can be used as long as it meets the requirements defined in the specification for a compliant test channel. In particular:

- The insertion loss at the Nyquist frequency [8] must fall within a specified range (see table below).
- The Effective Return Loss (ERL) must be below a defined threshold.
- The Channel Operating Margin (COM) must be greater than 3 dB.

Note that the COM of a given channel will vary depending on the interface, as each has different requirements.

Test channel characterization is typically performed using a Vector Network Analyzer (VNA), such as the Keysight PNA series, as illustrated in Figure 8.

Interface	Calibration Channel	Test Channel Insertion Loss (dB)
C2C	ISI trace + cable	10,22.5 & 26 ±0.5
KR	ISI trace + cable	15, 30.5 & 34 ±0.5
C2M – host & module (low-loss) C2M – module (high loss)	HCB [9] + MCB (ISI trace) + MCB + HCB	9 ±2 32 ±0.5
CR	(ISI trace) + MCB + DAC cable + MCB	16,27, 32 & 37±0.5

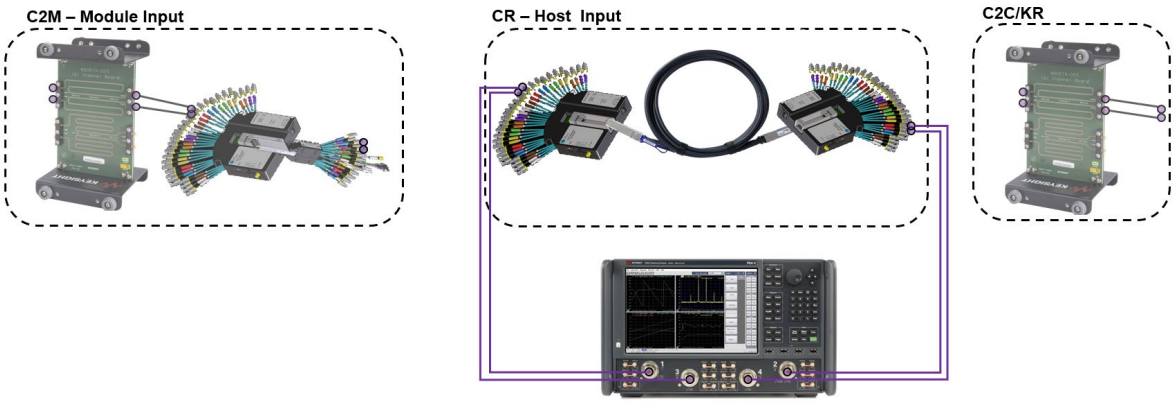

Figure 8. Calibration channels for C2M, CR and C2C/KR

8 Nyquist frequency = Baudrate/2 (53.125GHz)
9 A test fixture consists of a Host Compliance Board (HCB) and a Module Compliance Board (MCB) following the requirements of Annex 179B

Receiver Amplitude and Jitter Tolerance Tests

The purpose of the Jitter Tolerance Test is to test the ability of the receiver's clock and data recovery (CDR) to track and compensate for both low- and high-frequency jitter. No broadband noise is added for the jitter tolerance test, but the frequency and amplitude of the sinusoidal jitter are varied according to Table 179–12.

Case	A	B	C	D	E	F	G
Frequency (MHz)	0.04	0.1333	0.4	1.333	4	12	40
Jitter amplitude (UI pk-pk)	5	1.5	0.5	0.15	0.05	0.05	0.05

The Amplitude *Tolerance Test*, as defined in IEEE P802.3dj/D2.0, Annex 120G, validates the acceptance of the differential input peak-to-peak amplitudes produced by the extreme operating conditions from the transmitter. For the Amplitude Tolerance Test, no broadband noise is added, but the signal steady-state is set to the maximum allowed value specified in Table 176C–4.

Note:

Please note that the M8091DJCA receiver conformance test application does not cover additional receiver tests, such as *receiver signaling rate* (176C 6.4.1), *receiver difference ERL* (176C 6.4.3), *and receiver differential-mode to common-mode return loss* (176C 6.4.4). The dERL (Annex 176C.6.4.3 & clause 178.9.3.6) can be measured using the D90203DJC IEEE802.3dj Electrical Transmitter Test software, which applies the same ERL methodology and references the IEEE802.3dj specification.

Configuration Guide

The table below shows the required equipment for each standard option under IEEE 802.3dj Annex 120F (Chip-to-Chip, C2C) and 120G (Chip-to-Module, C2M). The required instrument configuration and software options are listed in the following section.

Equipment Type	
Victim pattern generator	M8042A
Interference source	M8053A
Victim error detector	DCI (DUT control interface available in M8070ADVB)
Oscilloscope (calibration)	UXR-series oscilloscopes with 90 GHz bandwidth and above (recommend BP model)

Minimum Required Instrument Configuration

The options marked * are recommended but not mandatory.

M8050A BERT Platform

M8050A-BU2	Bundle consisting of one M9505A 5-slot AXIe Chassis with USB option
M8042A	Pattern generator module 32/64/120 GBd, 2 or 3-slot AXIe
M8042A-0G1	Pattern generator NRZ and PAM4, 1 Channel, 2-slot AXIe Module
M8042A-G12	Pattern generator, 120 GBd for NRZ and PAM4, module-wide license
M8042A-0G4	De-emphasis, module-wide license
M8069A [10]	Remote Head, 120 GBd for M8042A Pattern Generator
M8059A-801	Matched cable pair 1.0 mm (m) to 1.0mm (m), 150 mm
M8009A	Clock Module
M8009A-062	Clock generator module with jitter modulation, 60 GHz, 1 slot AXIe
M8009A-0G3	Advanced jitter modulation for up to two channels, license

Interference Source

M8053A	64GHz interference source

UXR

UXR0702/4BP[11]	Infiniium UXR-Series real-time oscilloscope, 70GHz bandwidth, 2 or 4 ports
N2157A-017/8	Bandwidth upgrade 2/4 Ch Infiniium UXR real-time oscilloscope 70 to 80 GHz 1mm model (License Only)
N2129BU-111/7	Bandwidth upgrade – 2/4 Ch Infiniium UXR real-time oscilloscope – 80 to 90 GHz
D9320ASIA	Advanced signal integrity software (EQ, InfiiniSimAdv, crosstalk)
D9320PAMA	Pulse amplitude modulation PAM-N analysis software
D9320JITA	Jitter, vertical, and phase noise analysis software for 90000, V-, Z-, and UXR-series

10 M8059A Remote Head is supported as well but may not have enough amplitude range to cover some use-cases.
11 UXR B model upgrade is possible as well

Accessories and Fixtures [11] (Recommended)

M8053A-801	Matched cable pair, 1.85mm, length 850 mm, matching 1 ps (for combining SI and RI)
M8053A-803	Coupling path: bandwidth 64 GHz, coupling loss 14 dB, 1.85 mm. Through path: bandwidth 110GHz, 3.5 dB, 1.0 mm
M8053A-804	Adapter 1.0 mm (m) to 1.85 mm (f) (x2)
-	Wilder OSFP 224G/1.6T MCB 1mm Connectors
-	Wilder OSFP 224G/1.6T HCB 1mm Connectors
-	Wilder QSFP 224G/1.6T MCB 1mm Connectors
	Wilder QSFP 224G/1.6T HCB 1mm Connectors
M8067A-003	ISI Channel Board Two Traces 1.4 and 4.3 inches, 1.0 mm Connectors (for KR low loss)
M8067A-004	ISI Channel Board Two Traces 2.9 and 5.8 inches, 1.0 mm Connectors (for C2C low loss)
M8067A-005	ISI Channel Board Two Traces 7.3 and 8.8 inches, 1.0 mm Connectors (for C2M, C2C, and KR high loss)

Software Configuration

M8070ADVB	Advanced measurement package for M8000 Series of BERT test solutions (node locked, transportable, floating or USB license, revisions 9.1 or later)
M8091DJCA	Receiver conformance test application for IEEE 802.3dj (node-locked, transportable floating, or USB license)

11 Due to copper cable variability, Keysight cannot recommend any test channel for CR interfaces.

Minimum PC Configuration

The PC running the application should meet the following requirements

PC hardware requirements

- Operating system: Microsoft Windows 11 or Windows 10 (64-bit), Version 1809 or newer
- Memory: 8 GB RAM minimum
- Monitor resolution: WXGA+ (1440 x 900) minimum

PC software requirements (please refer to the software release note for version/ revision info)

- Microsoft Office
- Microsoft .NET Framework
- Keysight IO Library Suite
- Keysight License Manager 5 and Keysight Software Manager Utility
- Keysight M8070B system software for M8000 series
- M8070ADVB Advanced Measurement Package for M8000 Series
- Keysight UXR oscilloscope FW
- MATLAB Compiler Runtime

Remote Programming

The M8091DJCA Receiver Conformance Test Application for IEEE 802.3dj is part of Keysight's Digital Test Apps and can be programmed via ARSL, any .NET language. For more information, see www.keysight.com/find/rpi.

Related Products

The D90203DJC IEEE 802.3dj Electrical Transmitter Compliance Test Software for real-time oscilloscopes.

The N4917DJCA 1.6T Optical Receiver Stress Test Application for 800G and 1.6T transceiver modules.

The M8091CKCA Receiver Conformance Test Application for IEEE 802.3ck for testing Chip-to-Chip (C2C) and Chip-to-Module (C2M) interfaces