M5200A

PXIe High-Speed Digitizer

4 Channels / 2 GHz / 4.8 GSa/s / 12-bit

The M5200A is a high-speed, four-channel, 12-bit digitizer in a single-slot PXIe form factor with optional streaming capability. Designed for demanding applications in aerospace/defense, quantum computing and RF communications, it delivers exceptional measurement fidelity and phase coherence. With real-time sequencing, FPGA programmability, and scalable channel density, the M5200A enables advanced signal processing in compact, high-performance systems.



KEYSIGHT

Overview

Product Description

The M5200A is a single-slot PXIe digitizer featuring four DC-coupled 2 GHz channels with 12-bit resolution and a sampling rate of 4.8 GSa/s. Designed for high-definition signal capture in aerospace and defense, quantum computing and wireless applications, it offers 1 GS/channel acquisition memory and real-time processing via PathWave FPGA enabling HIL (Hardware In the Loop) applications. When paired with Keysight's PathWave VSA software, the M5200A delivers advanced multichannel signal analysis in a compact, scalable form factor.

Example Applications

- Radar and satellite communication
- Antenna array calibration/test
- Passive radar and multi-band SATCOM monitoring
- Quantum control systems
- Emerging standards (6G) R&D in massive MIMO, or multi-channel baseband IQ
- RF measurements and component testing
- Particle physics experiments (i.e. beam position monitoring)
- Medical imaging research

Key Product Features

- Four independent 2 GHz channels
- High-speed 4.8 GSa/s sampling rate
- 12-bits of resolution for high-definition sampling
- Ability to create custom IP and processing algorithms in the FPGA
- Data transfer over the PCIe backplane
- PathWave FPGA and PathWave Test Sync Executive compatible

Hardware Platform

Hardware Overview

The M5200A is a flexible modular digitizer engineered for precision analog-to-digital conversion across four independent channels. Each channel supports up to 2 GHz analog bandwidth and delivers 12-bit resolution at a sampling rate of 4.8 GSa/s. The digitizer integrates a high-speed ADC front end with programmable gain amplifiers and low-noise signal conditioning circuitry optimized for dynamic range and signal fidelity. Data acquisition is managed by a real-time sequencing engine and user-programmable FPGA allowing deterministic control and custom processing workflows. The module interfaces with the PXIe backplane via a x8 Gen 3 PCIe link ensuring high-throughput data streaming to host systems.

When used with the QS1 option on the M9046A chassis, featuring an embedded high performance 2.4 GHz reference clock, the module achieves minimal phase noise and jitter across the system, critical for high-speed digitization and coherent signal acquisition. Additionally, as part of Keysight's M5000 modular platform, the M5200A can be used with PathWave Test Sync Executive [1], PathWave FPGA, and Keysight System Sync modules for unparalleled scalability.

Block Diagram

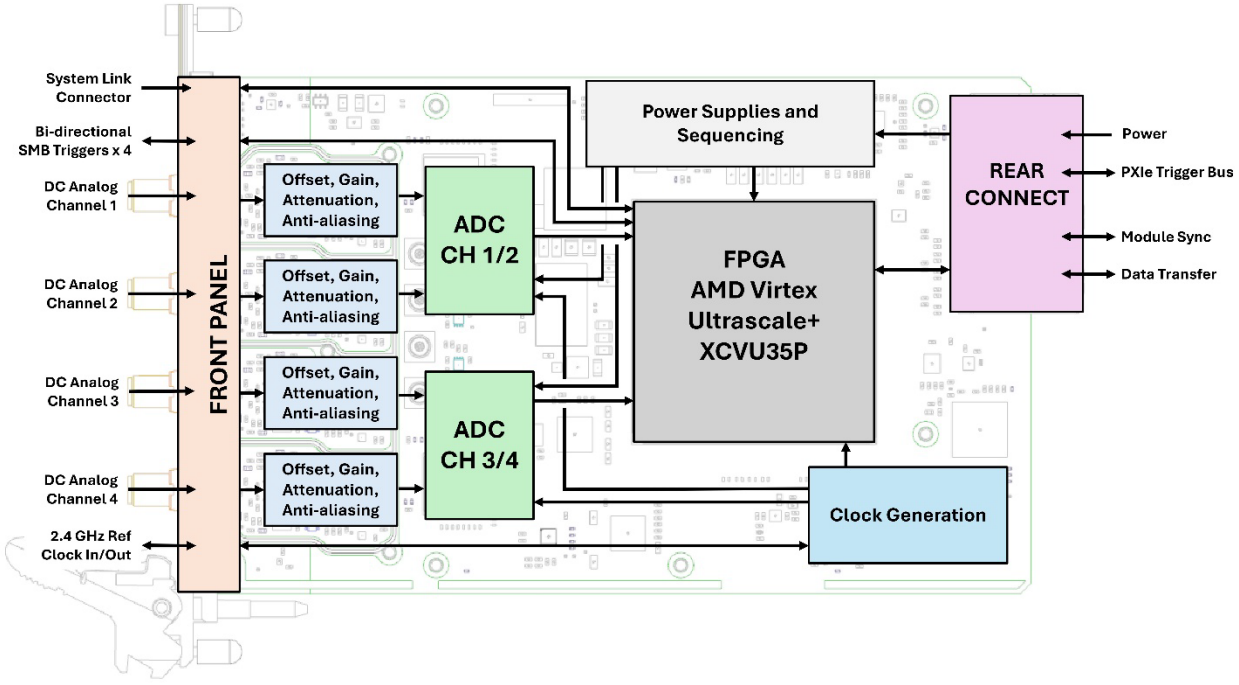

Figure 1. Block diagram representation of the M5200A Digitizer module

1 To use PathWave Test Sync Executive, a system requires an M9032 or M9033 System Sync Module.

On-Board Real Time Processing

The M5200A uses a Virtex UltraScale+ FPGA, allowing for fast, distributed processing. The FPGA configurable region utilizes AMD's FPGA partial reconfiguration technology to design and configure a defined section of the FPGA without the need to power down or reboot the card or host computer. FPGA capabilities are further enhanced when used in tandem with PathWave FPGA.

Software Platform

I/O Libraries

Keysight IO Libraries Suite offers fast and easy access to the M5200A digitizer using a standardized interface and ensuring compatibility and upgradability of the software application.

The Keysight IO Libraries Suite displays all the modules in each system. From here, one can view information about the installed software or launch the modules' soft front panel directly from Keysight Connection Expert (KCE). In addition, KCE offers an easy way to find the correct driver for any instrument.

Drivers

The M5200A comes with IVI.NET, IVI-C, IVI-COM and LabVIEW™ drivers to enable easy integration into common test development environments. A Python interface is also provided with the module.

Software Integration

To help users get started and complete complex tasks quickly, the M5200A digitizer is supplied with a comprehensive portfolio of module drivers, documentation, examples, and software tools.

Compliance

The M5200A is PXI Express compliant, designed to be compatible and integrated with Gen 3 PXIe modular chassis products. [2]

Software Applications

Soft Front Panel

The M5200A has a Soft Front Panel (SFP) that provides a simple interface to the digitizer module. It covers the basic operation of the instrument and is useful for getting acquainted with the

2 Keysight only supports M5000 modules in the high-power M9046A chassis.

module's functionality before software programming is started. The SFP also gives users the ability to debug the system and monitor driver calls.

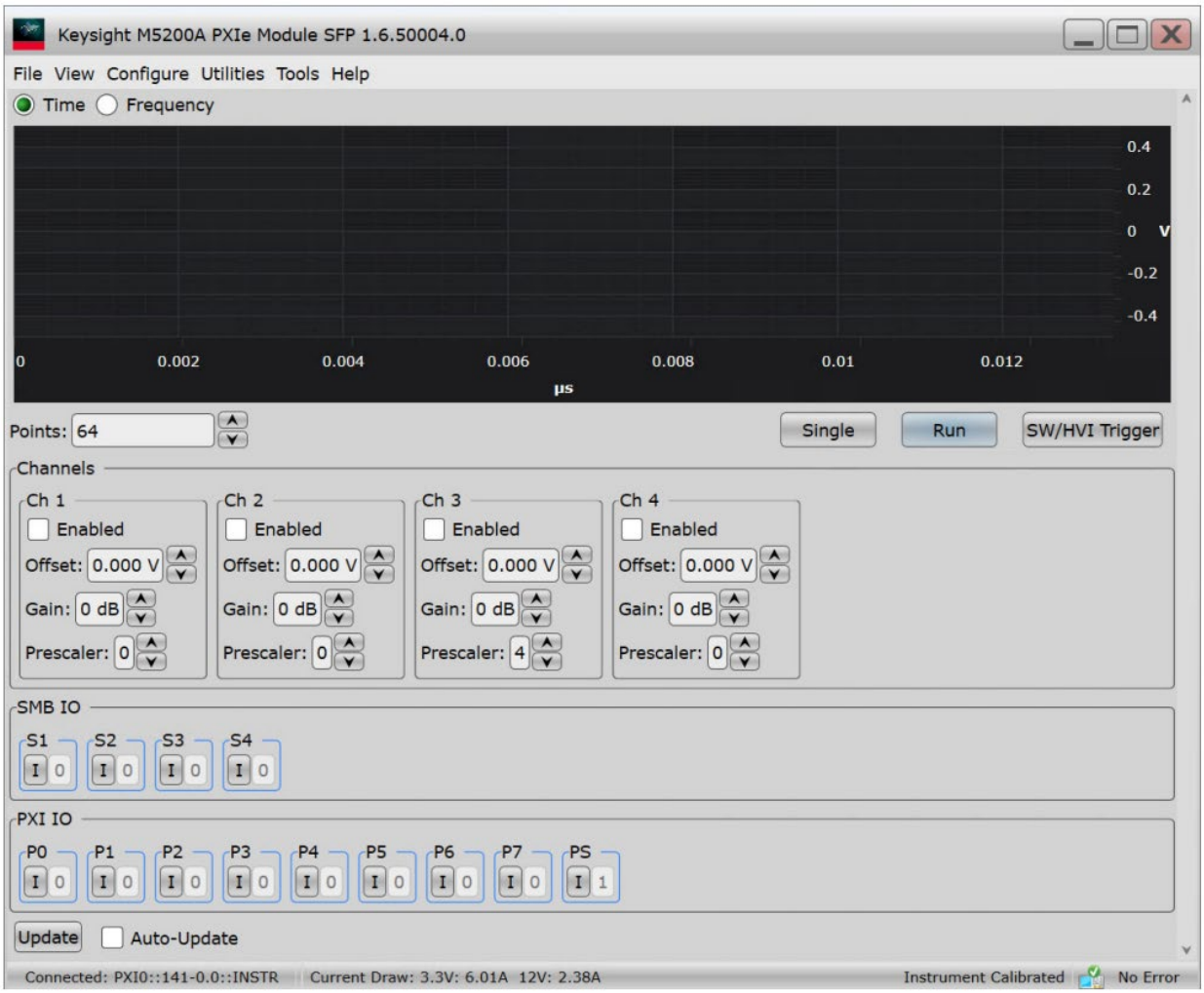

Figure 2. Default view of the M5200A SFP in connected mode.

PathWave Test Sync Executive

PathWave Test Sync Executive (TSE) enables rapid development of high-performance, multi-channel, multi-instrument, real-time synchronous solutions. This powerful software tool is critical in solutions requiring tight synchronization and feedback, such as radar applications, communication systems, quantum control and more. When used with the M5200A, data acquisition can be synchronized across modules and chassis down to the nanosecond scale; TSE also enables real-time processing on the data acquired. It is enabled on the M5200A with a PathWave license and has seamless interaction with PathWave FPGA.

Test Sync Executive features:

- Transparent multi-mode synchronization by precisely time aligning multiple channels in the same module or across several modules
- Real-time synchronous execution including sequencing, branching, and looping
- Time-deterministic hardware-based execution

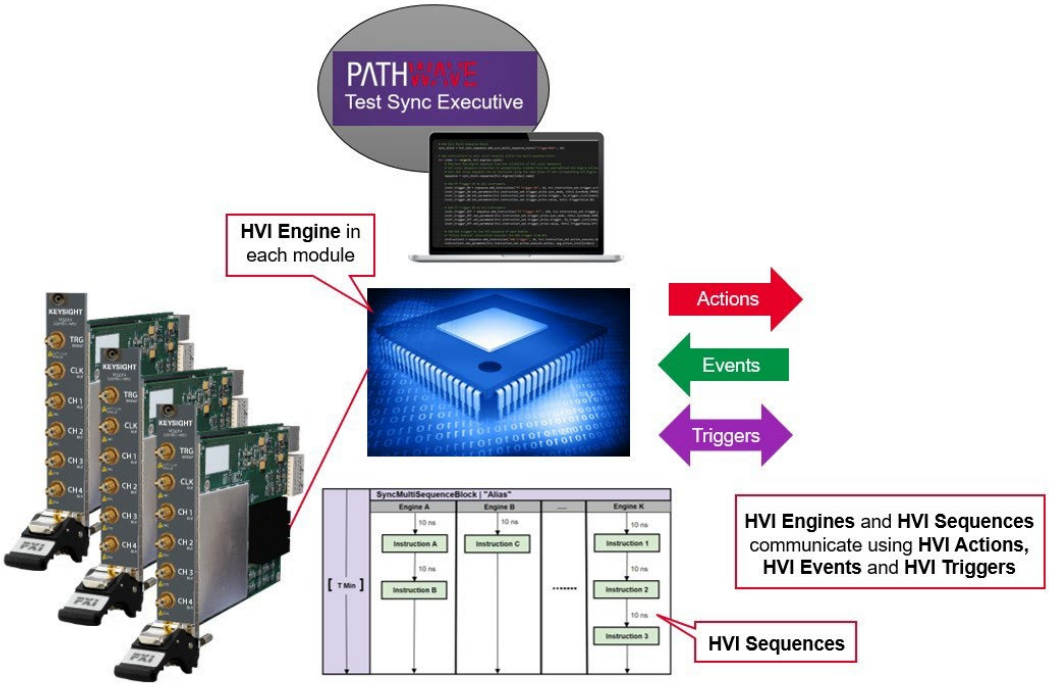

Figure 3. PathWave Test Sync Executive workflow visualization

PathWave FPGA

PathWave FPGA is a graphical environment that enables rapid development of FPGA designs for the M5200A. When combined with a PathWave FPGA license, the user has access to the user-programmable FPGA and can insert custom logic into the instrument. An IP library includes logic/math, memory, and DSP blocks that can be included in an FPGA design. PathWave FPGA supplies components to create custom design flows to go quickly from schematic to bitfile generation with the press of a button.

PathWave FPGA ships with a rich set of built-in library elements that can be dropped into a schematic. The default template can easily be modified by importing Vivado IP, HDL IP, or by using the PathWave FPGA IP library.

Key benefits:

- Visualize application flows and insert custom blocks
- Streamline the design process with full native FPGA-code compatibility
- Quickly compile the bit file to program the FPGA model embedded in the instrument
- Easily target different instrument FPGAs using Board Support Packages (BSP)

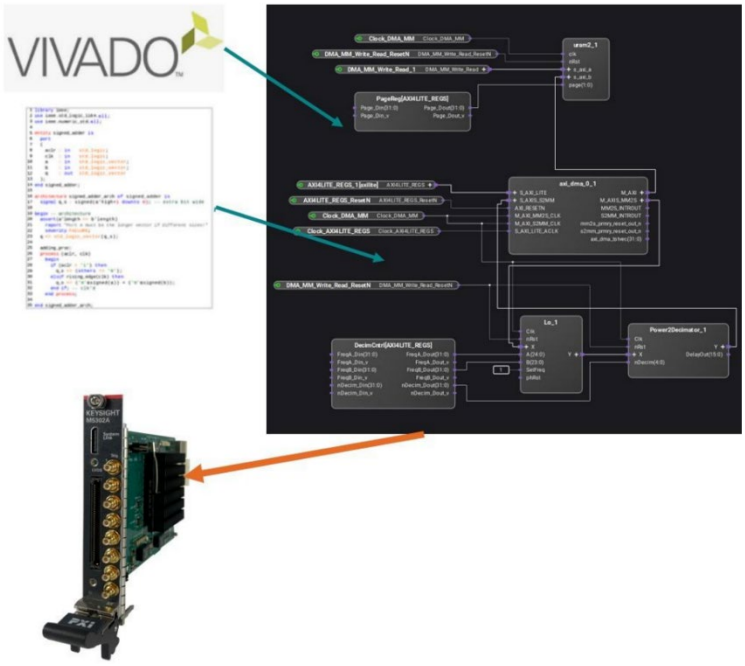

Figure 4. PathWave FPGA interface example

Configurable Options

-BPS Backplane Streaming Option for RF Digitizer

The –BPS Backplane Streaming Option for RF Digitizer enables the Peer-to-Peer (P2P) streaming feature on the M5200A digitizer. P2P streaming moves a continuous stream of data between modules. In the M5000 Series Modules, P2P streaming refers to the transfer of data between modules installed within specific segments of a single chassis. Users can configure the hardware to operate in several data path modes. [3]

The –BPS option for the M5200A can be added via the M5200A-BPS configuration option at time of purchase or through the M5000AU-002 upgrade after purchase. The M5000AU-002 license is supported by the M5200A driver to enable P2P streaming for version 1.7.50103.0 and newer. The license is also supported with the SFP for version 1.4.50301.0 and newer.

Bandwidth and Channels Supported for P2P Data Streaming

Channel number used	Bandwidth	Sample Rate	M5200A Decimation Factor	M5300A DAC Interpolation
1 (CH1)	+- 480 MHz (~1 GHz)	1.2 GSa/s for I 1.2 GSa/s for Q (2.4 GSa/s)	4 for I 4 for Q	16
2 (CH1 and CH2)	+- 240 MHz (~500 MHz)	600 GSa/s for I 600 GSa/s for Q (1.2 GSa/s)	8 for I 8 for Q	32
4 (CH1, CH2, CH3, & CH4)	+-120 MHz (~250 MHz)	300 GSa/s for I 300 GSa/s for Q (600 GSa/s)	16 for I 16 for Q	64

-480 Reduced Bandwidth and Sample Rate

The –480 Reduced Bandwidth and Sample Rate (480 MHz with 960 MSa/s) [4] option offers reduced bandwidth and sampling rate on the M5200A digitizer. The –480 option is offered for driver version 1.6.50005.0 and newer. With this package, the FPGA versions offered are expanded to include ‘non-IVL tandem’ and ‘non-IVL non-tandem’ to accommodate the reduced sample rate configuration. [5]

3 For more information on P2P streaming, see the M5200A User Guide, Section 6.
4 The M5200A with option –480 does not have IVL export restrictions.
5 Without the –480 option, the FPGA versions offered include ‘tandem’ and ‘non-tandem’. For more information, see the M5200A Release Notes.

Technical Specifications and Characteristics

Analog I/O

Number of channels		4 (SMA)
Impedance		50 ± 1 Ω
Coupling		DC
Gain		-6 dB to 26 dB[6]
Gain accuracy		± 2%
Voltage offset[7]		± 450 mV
Voltage offset accuracy		± 1.5%
Input Characteristics (Typ)		
Input frequency range		DC to 2 GHz
Input voltage max full-scale range		900 mV_{pp}
Input voltage min full-scale range		23 mV_{pp}
Input range/gain settings[8]	Gain	Input voltage full-scale range
	@ -6 dB	900 mV_{pp}
	@ -3 dB	636 mV_{pp}
	@ 0 dB	450 mV_{pp}
	@ 3 dB	319 mV_{pp}
	@ 6 dB	226 mV_{pp}
	@ 12 dB	113 mV_{pp}
	@ 18 dB	57 mV_{pp}
	@ 22 dB	36 mV_{pp}
	@ 26 dB	23 mV_{pp}
Time Skew Characteristics (Typ)		
Channel-to-channel skew [9]	Within the same ADC pair (e.g., CH1 to CH2)	< 3 ps
	Not sharing the same ADC (e.g., CH1 to CH3, or across modules); with TSE alignment	< 75 ps
	Not sharing the same ADC (e.g., CH1 to CH3 or across modules); w/out TSE alignment	< 145 ps
Channel-to-channel skew stability	vs. Frequency [10]	< 3 ps
	vs. Temperature [11]	< 2 ps
	Overall [12]	< 5 ps

6 Adjustable in 1 dB increments.
7 Offset voltage is applied to the input signal prior to the gain adjustment stage.
8 Table shows a selection from the 33 possible gain settings.
9 Custom single-point deskew can reduce channel-to-channel skew to <1 ps at the calibrated frequency and temperature; away from that point, alignment is limited by skew stability specifications. Frequency- and/or temperature-dependent multi-point deskew can improve wideband alignment.
10 Skew variation across 0.5-1.75 GHz at 22.5 °C ambient.
11 Skew variation across 5-40 °C ambient at 1 GHz.
12 Skew variation across 0.5-1.75 GHz and 5-40 °C ambient.

Effective Number Of Bits (ENOB) [13]					
	Input frequency				
	105 MHz	390 MHz	1.15 GHz	1.53 GHz	2.1 GHz
SINAD (dBFS)	50.7	51.4	50.9	50.6	50.4
ENOB (bits)	8.1	8.2	8.2	8.1	8.1

Performance Characteristics (Typ)		
RMS noise		< 800 uV
Spurious free dynamic range (SFDR)	50% full-scale	65 dBc
	80% full-scale	65 dBc up to 1 GHz 40 dBc up to 2 GHz
Total harmonic distortion (THD) [14]	@ 500 MHz	0.4%
	@ 1 GHz	0.1%
	@ 2 GHz	0.2%

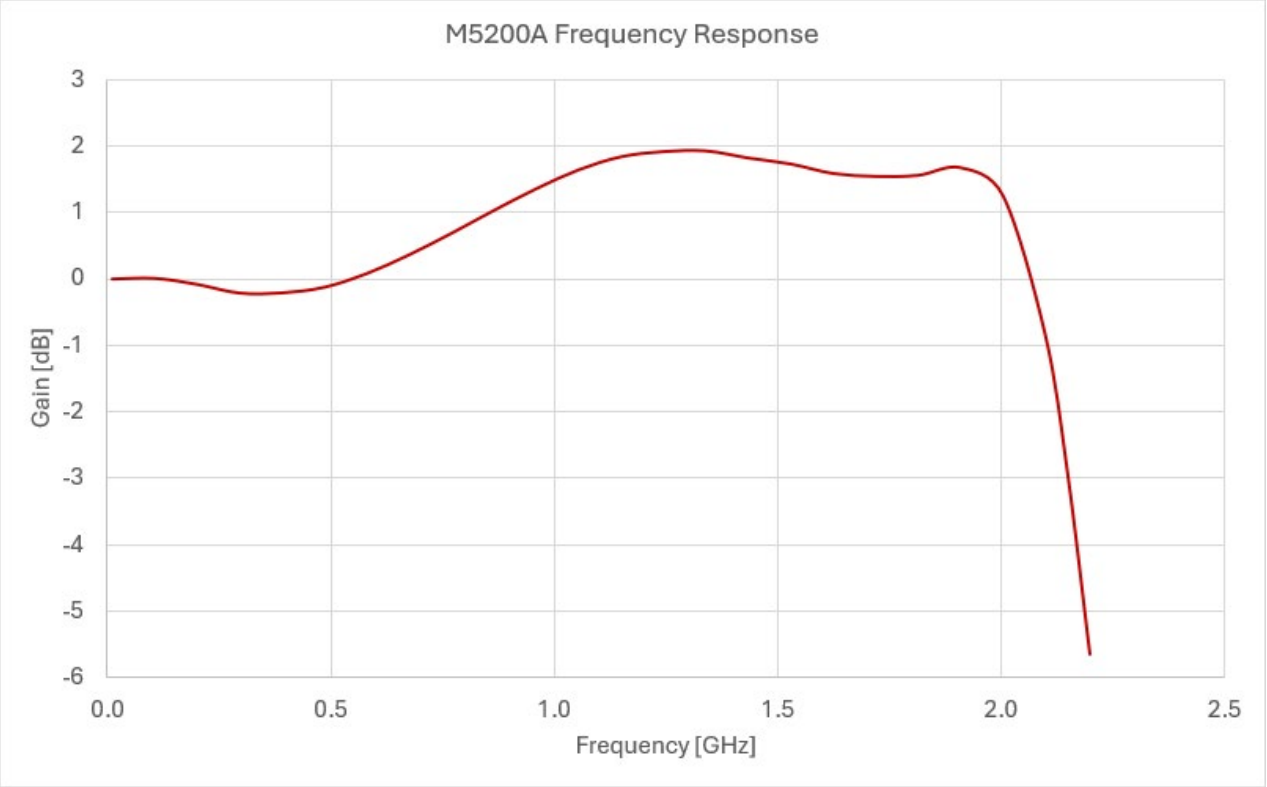

Figure 5. M5200A frequency response, flatness uncorrected. [15]

13 Typical values measured from production units at 80% FSR, 0 dB gain setting.
14 Typical values measured from production units using input power of -2 dBm (~0.5 Vpp).
15 Plot uses typical values measured from production units.

Clock and I/O Characteristics

Digital Conversion		
Sampling rate		4.8 GSa/s
Resolution		12-bit
Memory depth		1 GSa/Ch
Module Reference Clock		
Clock sources		Front panel, PXI_CLK100
Front panel clock frequency		2.4 GHz
Nominal input clock power		+ 15 dBm
Module self-clocking		Yes
Accuracy		Chassis-dependent
Input/Output Triggers		
Trigger sources		Software, PXI_TRIG, PXI_STAR, front panel I/O
Trigger destinations		PXI_TRIG, front panel I/O
Trigger polarity		Active high or active low (programmable)
Max PXI trigger toggle rate		100 MHz

Trigger Channel Characteristics

Number of channels		4 (SMB)
Channel type		Single-ended, bidirectional, ground reference
Default state		1 MΩ nominal, input
Output Characteristics (Typ)		
Output voltage	50 Ω load	0 V – 1.6 V
	High impedance load	0 V – 3.2 V
Maximum output channel toggle rate		150 MHz
Input Characteristics (Typ)		
Input voltage range		0 – 5 V
Maximum low voltage threshold		0.8 V
Maximum high voltage threshold		2 V
Load impedance		1 MΩ
Maximum input channel toggle rate		75 MHz

FPGA Characteristics

FPGA type	AMD Virtex Ultrascale+ (XCVU35P)
User-accessible sandbox resources (approx.)	479844 CLB registers
	235567 CLB LUTs
	719 RAMB18 (13 Mb)
	240 URAM (71 Mb)
	1872 DSP
Timebase frequency	300 MHz (phase-locked to 100 MHz chassis clock)
Timebase source	PXI_CLK100, DSTARA

System Specifications

General Specifications

Bus interface and compatibility		PXIe peripheral module (x8 Gen 3)	
Number of slots		1	
PXIe chassis compatibility		M9046A	
Module Power Requirements			
Total power dissipation		45 W	
Supply voltage		+3.3 V	+12 V
Supply current		5.8 A	2.2 A
Mechanical Characteristics			
Front panel connectors	RF input connectors	SMA (4)	
	Trigger I/O	SMB (4)	
	2.4 GHz in	MCX	
	2.4 GHz out	MCX	
Size		3U/1-slot PXIe standard 130.1 x 21.7 x 210 mm; includes connectors and handle extensions	
Weight		419 g (0.9 lb)	

Environmental Characteristics

Operating and Storage Conditions	Operating	Storage
Temperature	0 °C to 40 °C	-40 °C to 70 °C
Altitude	Up to 10,000 ft (3048 m)	Up to 15,000 ft (4573 m)
Humidity	Type-tested at 95%, +40 °C (non-condensing)	
Warm-up time	30 minutes	
Vibration		
Operating random vibration	Type-tested at 5 to 500 Hz, 0.21 g rms	
Survival random vibration	Type-tested at 5 to 500 Hz, 2.09 g rms	

Configuration and Ordering Information

Software Information

Software Infrastructure Requirements	
Supported operating systems	Widows 10/11, 64-bit
Keysight IO libraries suite	See M5200A driver release notes for required I/O Libraries Suite version recommendation
Chassis slot compatibility	PXIe [16]

Related Products and Accessories

Model	Description
M5000 Series Modules	
M5201A	PXIe Down Converter: 4 channels, 2-16 GHz RF, 0.01-2.4 GHz IF
M5300A	PXIe RF AWG: 4 channels, DC-16 GHz RF, 2 GHz IBW, 14-bit
M5301A	PXIe Precision AWG: 4 channels, 400 MHz, 14-bit
M5302A	PXIe Digital I/O: 28 LVDS channels, 8 trigger channels
Required Equipment	
M9046A	PXIe Chassis: High power, 18 slots, 24 GB/s, requires Option -QS2
M9032A	PXIe System Synchronization Module, 2-port
M9033A	PXIe System Synchronization Module, 5-port
M9038A	PXIe Embedded Controller
M9048B	PCIe Host Adapter: Single port (x8), Gen 3
M9049A	PCIe High-Performance Host Adapter
M9022A	PXIe System Module: Single port (x8), Gen 3
M9023A	PXIe High-Performance System Module: Dual port (x16), Gen 3
Cabling	
Y1202A Y1203A	PCIe cable: x8, 2.0 m PCIe cable: x8, 0.5 m
Y1326A Y1327A Y1329A	System Sync/Link cable, x8-x8, 0.5 m System Sync/Link cable, x8-x8, 1.0 m System Sync/Link cable, x8-x8, 2.0 m
Y1330A Y1331A Y1332A	MCX(m) to MCX(m) cable, phase stable [17], 0.3 m MCX(m) to MCX(m) cable, phase stable, 1.0 m MCX(m) to MCX(m) cable, phase stable, 2.0 m
Y1333A	SMA(m)-SMP(f) cable [18], 0.3 m
Cat-5	RJ-45 connectors (to interconnect chassis) [19]

16 The M9046A chassis is the Keysight tested and recommended chassis for the M5000 Series modules.
17 Used to distribute high-performance reference clock from M9046A-QS1/-QS2/-QS3 chassis to individual modules. All distribution paths must be the same length to preserve clock synchronization.
18 Used to connect high-performance reference clock from M9046A-QS1/-QS3 chassis to M9032A/M9033A System Sync Module.
19 The RJ-45 connector is used for multi-chassis power-sequencing.

Ordering Information

Model	Description	
M5200A	PXIe Digitizer, 4 channels, 2 GHz, 12-bit	
	Base order includes:	M5200A PXIe Digitizer KeysightCare Assured First Year Support Return to Keysight Warranty – 1 year

Configurable Options

Item	Description
M5200A-480	Performance 480 MHz with 960 MSa/s sample rate
M5200A-BPS	Backplane streaming option for RF digitizer

Services

KeysightCare Upgrades	
R-55A-001-2/3/5	KeysightCare Assured – Extend to 2/3/5 years (includes Return to Keysight Extended Warranty)
R-55B-001-1	KeysightCare Enhanced – Upgrade 1 year (Upgrades the Tech Support and Repair TAT in year 1)
R-55B-001-2/3/5	KeysightCare Enhanced – Extend to 2/3/5 years (includes KeysightCare Assured Services, Return to Keysight Extended Warranty and Calibration)
R-55C-001-2/3/5	KeysightCare Calibration – calibration of choice and technical support with priority TAT – 2/3/5 years
Warranty	
R-51B-001-C	Return to Keysight Warranty – 1 year
R-51B-001-3/5C	Extended Warranty – Return to Keysight -3/5 years
Recalibration Service Plans	
R-50C-011-3/5	Calibration Plan – Return to Keysight – 3/5 years

Instrument Upgrades

Upgrade number	Description
M5000AU-002	Upgrade – Backplane streaming option for RF digitizer

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