DATA SHEET

M8085 MIPI D-PHY 2.1

Receiver Conformance Test Automation Platform
M8085DC1A and M8085DE1A

The M8085Dx1A is a software plug-in for M8070B Bit Error Ratio Test system software within the M8000 series of BER test solutions. The M8085DxA software plug-in controls an M8195A Arbitrary Waveform Generator (AWG) to create D-PHY standard conformant test signals. Depending on the provisions for error detection implemented in the DUT receiver (RX) the plug-in provides the option to connect to your DUT built-in receiver via the so-called IBERReader interface, which is based on a user provided DLL, to read the bit error counter and display the result in the M8085DC1A user interface.

Key Benefits

- Fast characterization of digital D-PHY receivers through easy test signal generation
- Editor enabling set-up of all PHY-parameters in application terms
- Reliable and automated calibration of signal parameters
- Complete and conformant RX test procedures for single lane enabling automated, unattended test
- Can be operated manually or through program control via customer or N5990A Keysight test sequencer

KEYSIGHT TECHNOLOGIES

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Mobile Applications, Challenges for Testing D-PHY Receivers and Solutions

While modern mobile products are designed for high speed data transmission and processing (e.g. HD camera or video applications), they are often in a mode where these high speed data capabilities are not needed and they preferably are operating in a mode consuming less to nearly no power in order to extend battery life. Mobile standards are designed accordingly featuring such power saving modes.

High speed mode: Differential signaling, 100 Ω termination, source synchronous double data rate clocking

Low power mode: Unterminated, not differential, clock embedded within data

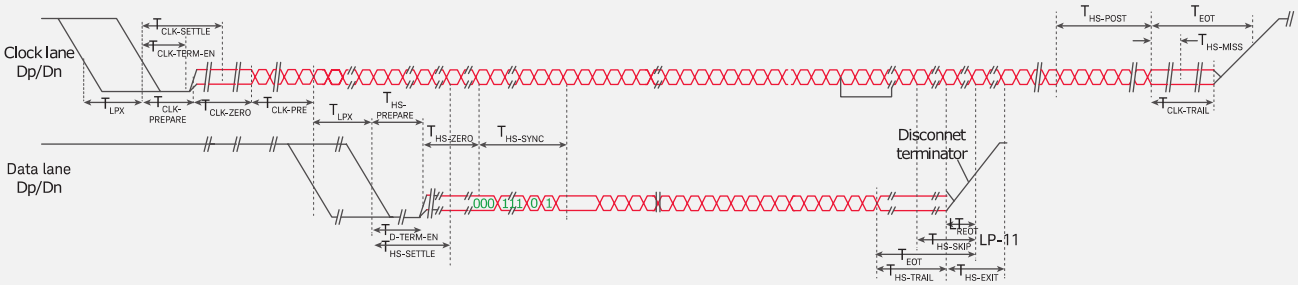


Figure 1. Timing Diagram of D-PHY showing transitions from Low Power Mode to High Speed Mode and back.

As depicted in Figure 1 above, the MIPI D-PHY standard which supports the applications CSI (for Camera) and DSI (for Display), uses different signaling levels and data formats in Low Power (LP) and High Speed (HS) mode. In LP mode the two wires are not terminated and used as independent single ended wires. For HS data transmission, D-PHY uses differential signaling with NRZ format 100 Ω termination. It is obvious that the generation of test patterns used for receiver testing is a real challenge. Traditional BERTs using NRZ pattern format cannot generate such 4-level D-PHY signals. AWGs can generate any signal; however, customers may not want to deal with the necessary generation of the waveform (vector) files.

MIPI Receiver Test Solutions

The next level of integration

The M8000 Series of BER test solutions for digital RX characterization with its modular AXI-HW architecture and its Plug In SW-concept allows composing the required BERT consisting of Pattern Generator (PG) and Error Detector (ED) building blocks using a Keysight M8195A AWG as PG and the M8070B System Software. The M8070B SW furthermore hosts the application specific test automation SW Plug-Ins M8085DC1A and M8085DE1A as depicted below in Figure 2 below, which in turn hosts the IBERReader interface providing the connection to the error detector that needs to be provided by the DUT.

The functionality is visualized in the software block diagram.

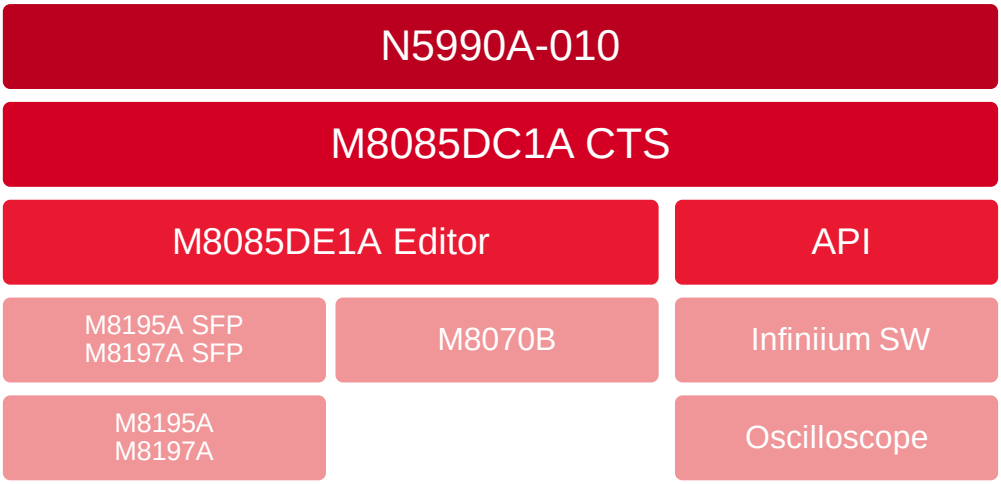


Figure 2. Architecture of application specific solutions within the M8000 System.

Building blocks of a complete RX test

An RX test is used to determine an RX's capability to properly detect the digital signal content, even for worst-case impaired input signals. For this testing

- A Bit Error Ratio Tester's (BERT) Pattern Generator (BERT PG) is used to emulate a system's TX plus channel thus generating a data signal containing the impairments to be expected at the RX input when it is operating in a target system.
- This signal has to be calibrated according to the specification / conformance test suite (CTS)
- The RX is set into test mode and the input of the RX under test is stimulated with the calibrated test signal
- Proper detection of the digital content is monitored in a suitable fashion to determine performance according to target BER

These tasks are depicted in the functional block diagram Figure 3 below. The functionality is delivered by separate SW blocks allowing the user to tailor the solution according to his needs.

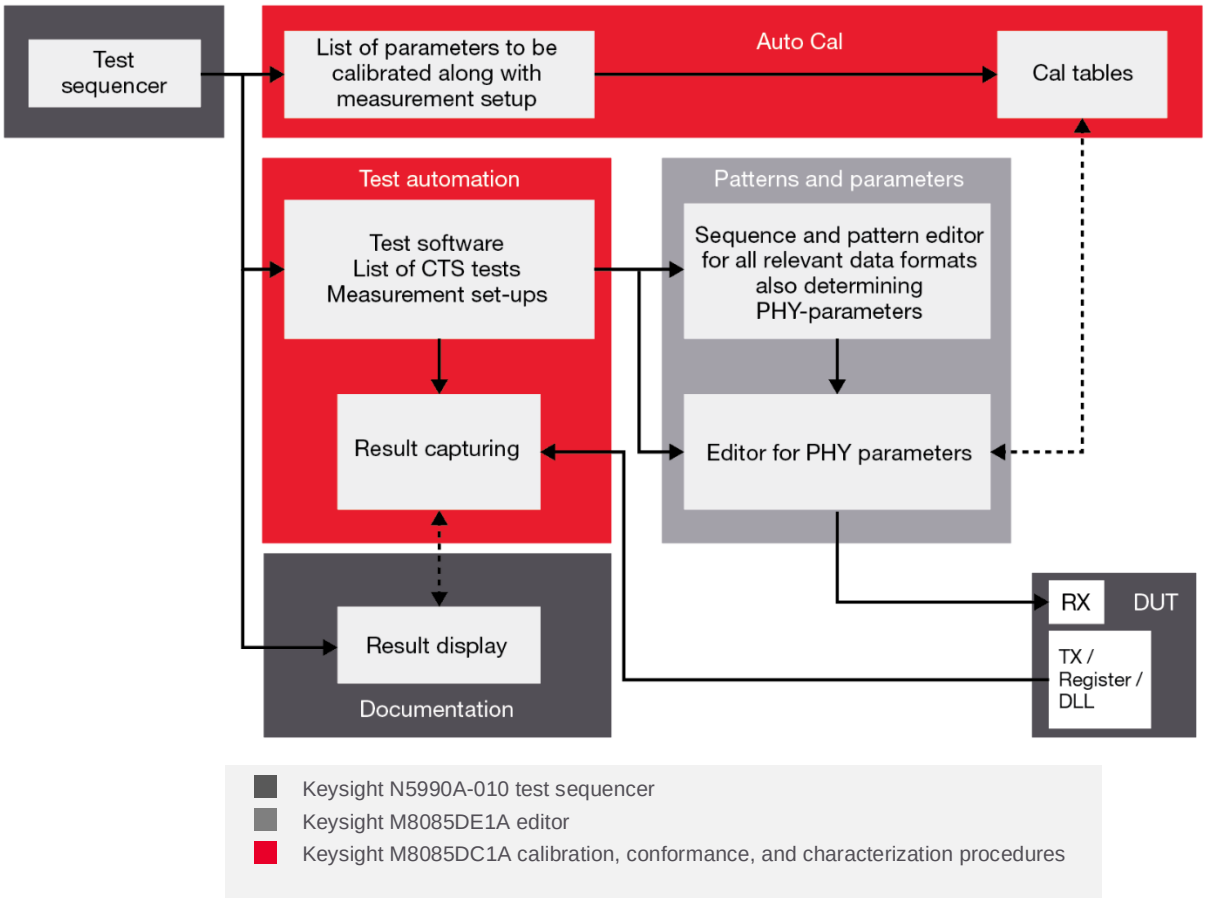


Figure 3. Building blocks of an RX Test and Related SW Products using Plug-Ins for the M8000 System SW M8070B.

1. The Editor allows direct setup of PHY parameters and data content (local from GUI or remote under program control via SCPI commands)
2. Automated calibration, conformance and characterization procedures can be started individually from GUI or a remote program
3. In case the customer does not want to generate his own remote control program or use his own test sequencer the test sequencer from the Keysight N5990A Test Automation Software Platform provides complete automated control of all the calibration and tests in addition to test result documentation.

M8085Dx1A Products

The M8085Dx1A products address the D-PHY standard. The SW which includes editor as well as CTS features is available as a perpetual, transportable or network license.

Product No.	Option	Description
M8085DE1A	-1TP	MIPI D-PHY 2.0 Editor for M819xA AWG, Transportable, Perpetual License
	-1NP	MIPI D-PHY 2.0 Editor for M819xA AWG, Network/Floating, Perpetual License
M8085DC1A	-1TP	MIPI D-PHY 2.0 Calibration, Conformance and Characterization Procedures for M819xA AWG, transportable, perpetual License
	-1NP	MIPI D-PHY 2.0 Calibration, Conformance and Characterization Procedures for M819xA AWG, Network/Floating, Perpetual License
M8085DUEA	-1TP	Upgrade D-PHY Editor from M8085A-DT1 to D-PHY 2.0, Transportable, Perpetual License
	-1NP	Upgrade D-PHY Editor from M8085A-DN1 to D-PHY 2.0, Network/Floating, Perpetual License
M8085DUCA	-1TP	Upgrade D-PHY Editor plus Calibration, Conformance and Characterization Procedures from M8085A-DT1 and M8085A-DTA to D-PHY 2.0, Transportable, Perpetual License
	-1NP	Upgrade D-PHY Editor plus Calibration, Conformance and Characterization Procedures from M8085A-DN1 and M8085A-DNA to D-PHY 2.0, Network/Floating, Perpetual License

Benefits

Key features of the M8085DE1A editor

As already mentioned above, the test stimulus used for D-PHY receiver test is created by the AWGs. These instruments generate their output signal from a vector memory that contains the digitized waveform information. Usually the waveform vectors must be generated by the user utilizing waveform synthesis tools such as MATLAB or equivalent. With the M8085DE1A editor SW, these instruments can be operated from the familiar user interface that the M8070B SW provides for the J-BERT M8020A - with the addition of application specific parameters as shown below in Figures 4 to 6 for the D-PHY application.

HS pattern can be set up as bursted, bursted with continuous clock, pure HS or Frames using

- hexadecimal data or predefined PRBS in HS section
- hexadecimal data in LP section

Automatic transition between HS and LP using programable protocol parameters

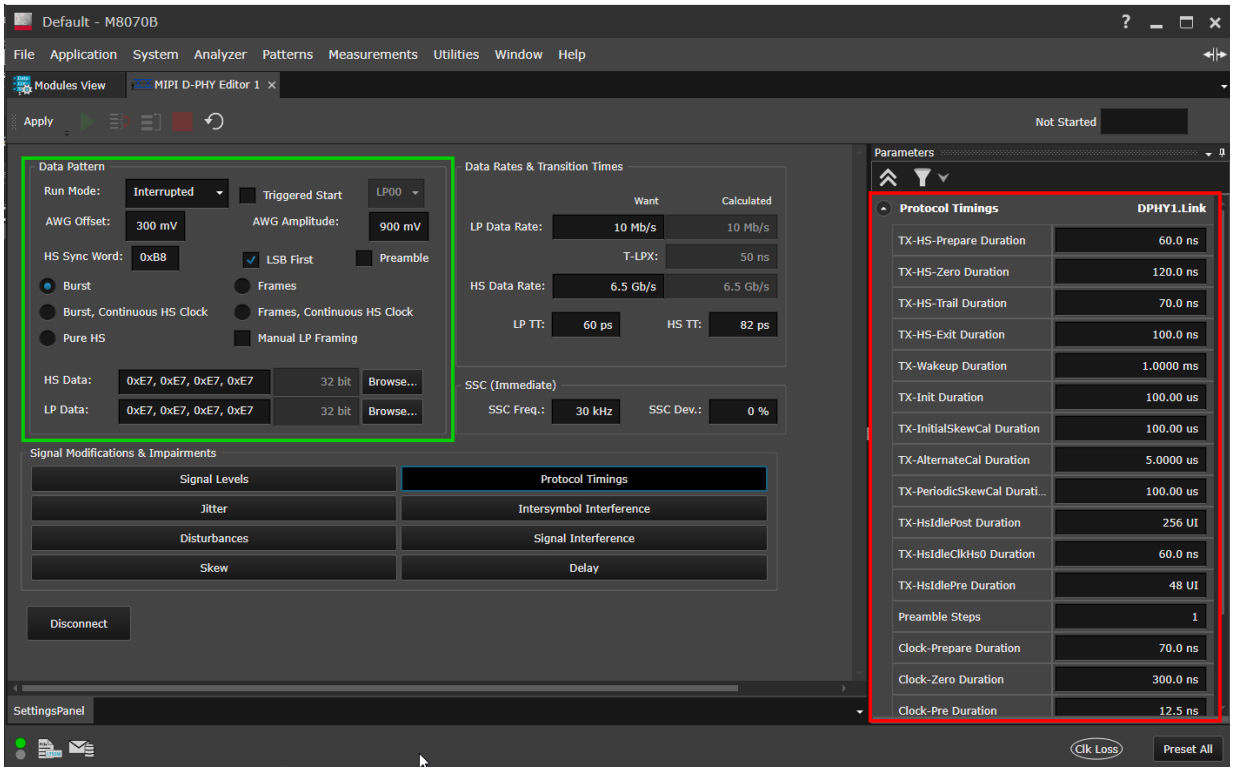
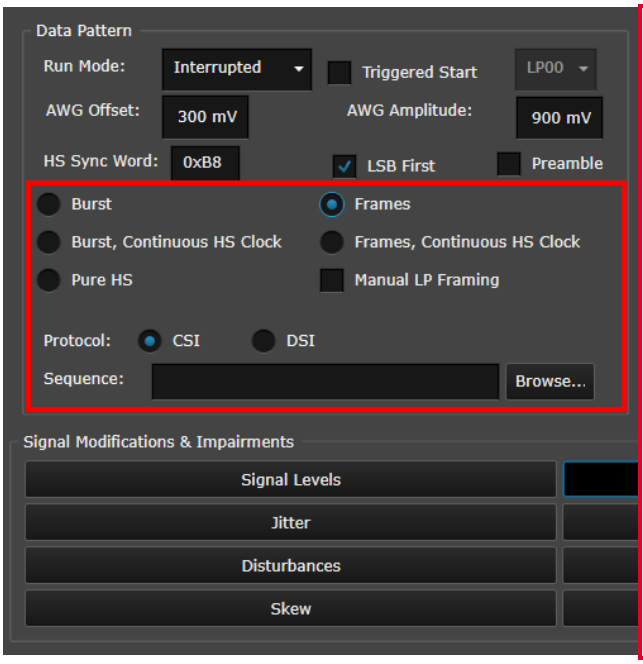


Figure 4. D-PHY editor showing GUI for Data set-up




```
HSFreq: 158 MBit/s;

Blocks:

FrameStart: C000000,LP11E10880;

Blanking: LP11E10880;

Video: C2B"Raw10_256x200.dat",LP11E10880;

FrameEnd: C010000,LP11E10880;

Sequence:

1. FrameStart,1;

2. Blanking,1;

3. Video,1;

4. Blanking,2;

5. FrameEnd,1;
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Figure 5. D-PHY editor showing GUI for CSI or DSI data set-up

Set up of parameters like HS impairments in a BERT-like fashion

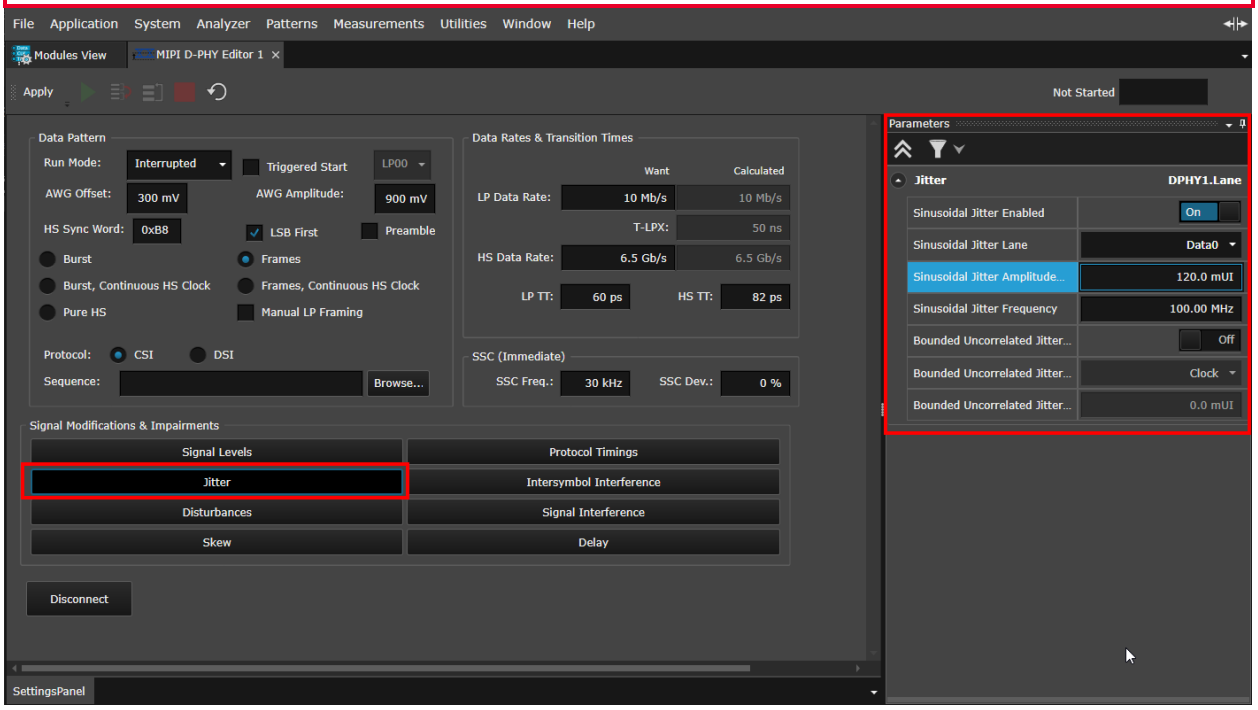

Figure 6. D-PHY editor showing GUI for HS impairment set-up

Key features of the M8085DC1A Calibration, Conformance and Characterization Procedures

A prerequisite for any RX test is to stimulate the RX with well-calibrated test signals. As the test set-ups often differ from those used to perform the factory calibration of the generators and influence the parameter values it is necessary to do an in-situ calibration. The Conformance Test Suite (CTS) for D-PHY specifies the different test set-ups and by this indirectly also the calibration procedures.

Furthermore, the CTS contains quite a few tests to verify the conformance or characterize the margins of the respective HS and LP receivers, in addition to tests verifying proper behavior during mode transitions. To unburden the user from having to study the CTS and maybe the specification itself and translate the insights into test set-ups, calibration and test procedures. Keysight provides the M8085DC1A containing these calibration, test and characterization procedures.

Below is listed which tests are addressed by the above mentioned SW.

List of D-PHY test procedures provided by the M8085DC1A	
GROUP 1: LP-RX VOLTAGE AND TIMING REQUIREMENTS	
Test 2.1.1 – LP-RX Logic 1 Input Voltage (VIH)	√
Test 2.1.2 – LP-RX Logic 0 Input Voltage, Non-ULP State (VIL)	√
Test 2.1.4 – LP-RX Input Hysteresis (VHYST)	√
Test 2.1.5 – LP-RX Minimum Pulse Width Response (TMIN-RX)	√
Test 2.1.7 – LP-RX Interference Tolerance (VINT and fINT)	√
Test 2.1.8 – LP-CD Logic Contention Thresholds (VIHCD and VILCD)	√
GROUP 2: LP-RX BEHAVIORAL REQUIREMENTS	
Test 2.2.1 – LP-RX Initialization period (TINIT)	√
Test 2.2.2 – ULPS Exit: LP-RX TWAKEUP Timer Value	√
Test 2.2.3 – Clock Lane LP-RX Invalid/Aborted ULPS Entry	√
Test 2.2.4 – Data Lane LP-RX Invalid/Aborted Escape Mode Entry	√
Test 2.2.5 – Data Lane LP-RX Invalid/Aborted Escape Mode Command	√
Test 2.2.7 – Data Lane LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits	√
Test 2.2.8 – Data Lane LP-RX Escape Mode Unsupported/Unassigned Commands	√
GROUP 3: HS-RX VOLTAGE AND SETUP/HOLD REQUIREMENTS	
Test 2.3.1 – HS-RX Common Mode Voltage Tolerance (VCMRX(DC))	√
Test 2.3.2 – HS-RX Differential Input High Threshold (VIDTH)	√
Test 2.3.4 – HS-RX Single-Ended Input High Voltage (VIHHS)	√
Test 2.3.5 – HS-RX Single-Ended Input Low Voltage (VILHS)	√
Test 2.3.6 – HS-RX Common-Mode Interference 50MHz - 450MHz (ΔVCMRX(LF))	√
Test 2.3.7 – HS-RX Common-Mode Interference Beyond 450MHz (ΔVCMRX(HF))	√
Test 2.3.8 – HS-RX Setup/Hold and Jitter Tolerance	√
GROUP 4: HS-RX TIMER REQUIREMENTS	
Test 2.4.1 – Data Lane HS-RX TD-TERM-EN Value	√
Test 2.4.2 – Data Lane HS-RX THS-PREPARE + THS-ZERO Tolerance	√
Test 2.4.3 – Data Lane HS-RX THS-SETTLE Value	√
Test 2.4.4 – Data Lane HS-RX THS-TRAIL Tolerance	√
Test 2.4.5 – Data Lane HS-RX THS-SKIP Value	√
Test 2.4.6 – Clock Lane HS-RX TCLK-TERM-EN Value	√
Test 2.4.7 – Clock Lane HS-RX TCLK-PREPARE + TCLK-ZERO Tolerance	√
Test 2.4.8 – Clock Lane HS-RX TCLK-SETTLE Value	√
Test 2.4.9 – Clock Lane HS-RX TCLK-TRAIL Tolerance	√
Test 2.4.10 – Clock Lane HS-RX TCLK-MISS Value	√
Test 2.4.11 – Clock Lane HS-RX TCLK-PRE and TCLK-POST Tolerance	√

Performing calibration and tests automatically

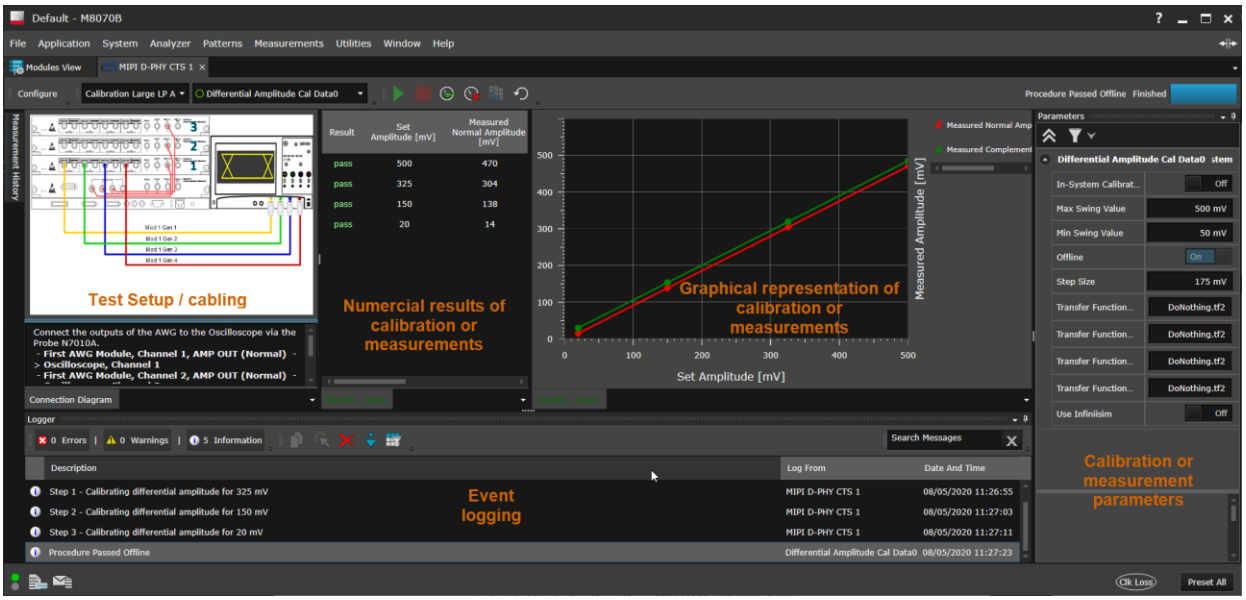

Figure 7 below shows how the M8085DC1A D-PHY calibration procedure guides the user through the connections of the oscilloscope with the AWG and the DUT. The result of the automated calibration is displayed in graphical form as well as with numerical values listed in a table.

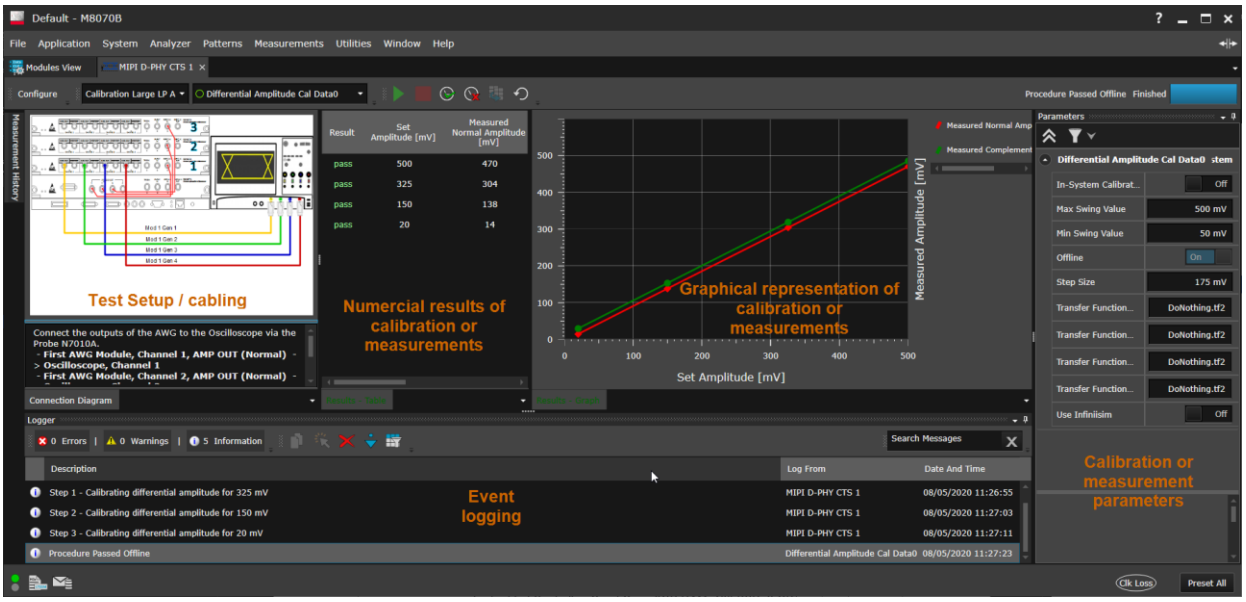

Figure 7. GUI of M8085DC1A. Calibration and test routines for D-PHY

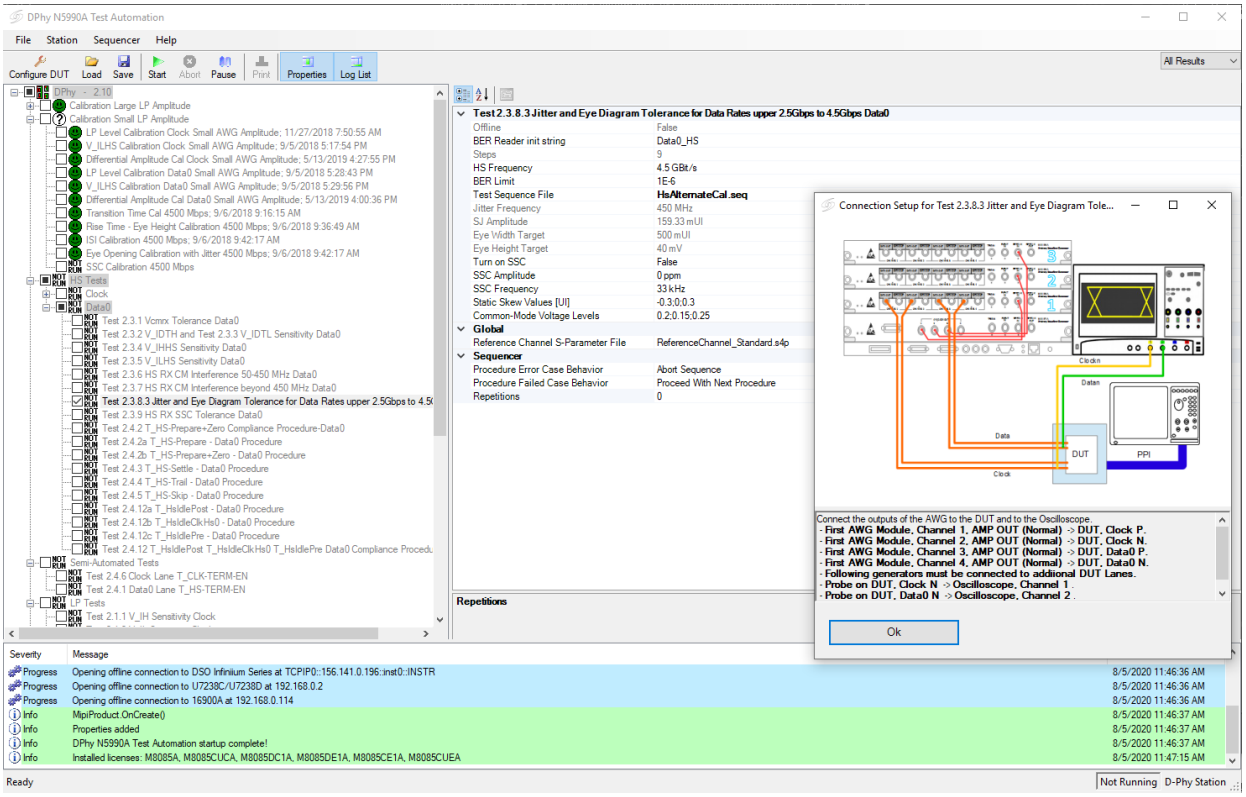

Figure 8. Using the N5990A-010 test sequencer

Recommended Instrument Configurations

Accessories are not listed

Complete n-Lane D-PHY Setup (HS, LP, and transitions, full compliance) using M8195A modules				
Number of D-PHY lanes		**1**	**2**	**4**
Option	**Description**	**Quantity**		
M8195A-BU1	AXIe Chassis: 5-slot with Integrated System Module plus Embedded Controller: Quad Core, 8GB RAM, 160 SSD, 2 GB/s	1	1	1
M8195A-004	Arbitrary Waveform Generator, 4 Channels, 65 GSa/s	1	1	2
M8195A-002	Arbitrary Waveform Generator, 2 Channels, 65 GSa/s	0	1	1
M8195A-001	Arbitrary Waveform Generator, 1 Channel, 65 GSa/s	0	0	0
M8195A-16G	Upgrade to 16 GSa Memory	1	2	3
M8195A-SEQ	Sequencer	1	2	3
M8197A	AWG synchcronisation module	0	1	1
M8195A-810	Matched Cable Pair for M8195A AWG, 2.92 mm	0	0	0
M8085DE1A-1TP	MIPI D-PHY 2.0 Editor for M819xA AWG, Transportable, Perpetual License	1	1	1
M8085DC1A-1TP	MIPI D-PHY 2.0 Calibration, Conformance and Characterization Procedures for M819xA AWG, transportable, perpetual License	1	1	1
M8085DE1A-1NP	MIPI D-PHY 2.0 Editor for M819xA AWG, Network/Floating, Perpetual License	0	0	0
M8085DC1A-1NP	MIPI D-PHY 2.0 Calibration, Conformance and Characterization Procedures for M819xA AWG, Network/Floating, Perpetual License	0	0	0
N5990A-010	Bitifeye Test sequencer for M8085DC1A	1	1	1

For more information: www.keysight.com/find/m8085a

System Requirements

Software

Requirements

- OS: Windows 10 - 64-Bit, English version
- Microsoft .NET Framework version 4.7.1 or higher
- Keysight IO Libraries Suite 18.1 or higher
- Keysight M8195A 65 GSa/s Arbitrary Waveform Generator firmware version 4.0.0.0 or higher
- Keysight M8197A Multi-Channel Synchronization Module for M8195A firmware version 4.0.0.0 or higher

Recommendation

- Microsoft Office Excel 2016 or higher, English version

Hardware

Requirements

- Connectivity hardware for instrumentation, depending on configuration e.g. USB3, Ethernet

Recommendations

- Multicore processor with 12 logical processors or more
- 16GB RAM or higher

Related Products

D9020DPHC MIPI D-PHY Compliance Test Software for Infiniium Oscilloscope

M8195A 65 GSa/s Arbitrary Waveform Generator

M8197A Multi-Channel Synchronization Module for M8195A

N5990A Automated Compliance and Device Characterization Tests

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