Keysight W1717
SystemVue Hardware Design Kit
From Algorithm to Implementation of Digital Signal Processing Systems

Data Sheet

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Unlocking Measurement Insights

Overview

The W1717 SystemVue Hardware Design Kit (HDK) is a hardware design flow personality that adds onto the core W1461 SystemVue core environment to accelerate the design and verification of digital signal processing (DSP) algorithms in communications and aerospace defense systems. It allows system architects and algorithm developers to create baseband models quickly and validate their performance at the system-level against RF models, test equipment, Standards references, and other signals and conditions.

The W1717 HDK enables a model-based design approach to FPGA rapid prototyping and integrates easily into mainstream design and verification flows. It includes a synthesizable fixed-point model library, and offers a rich set of example designs, ranging from basic filters to realistic communications physical layer design.

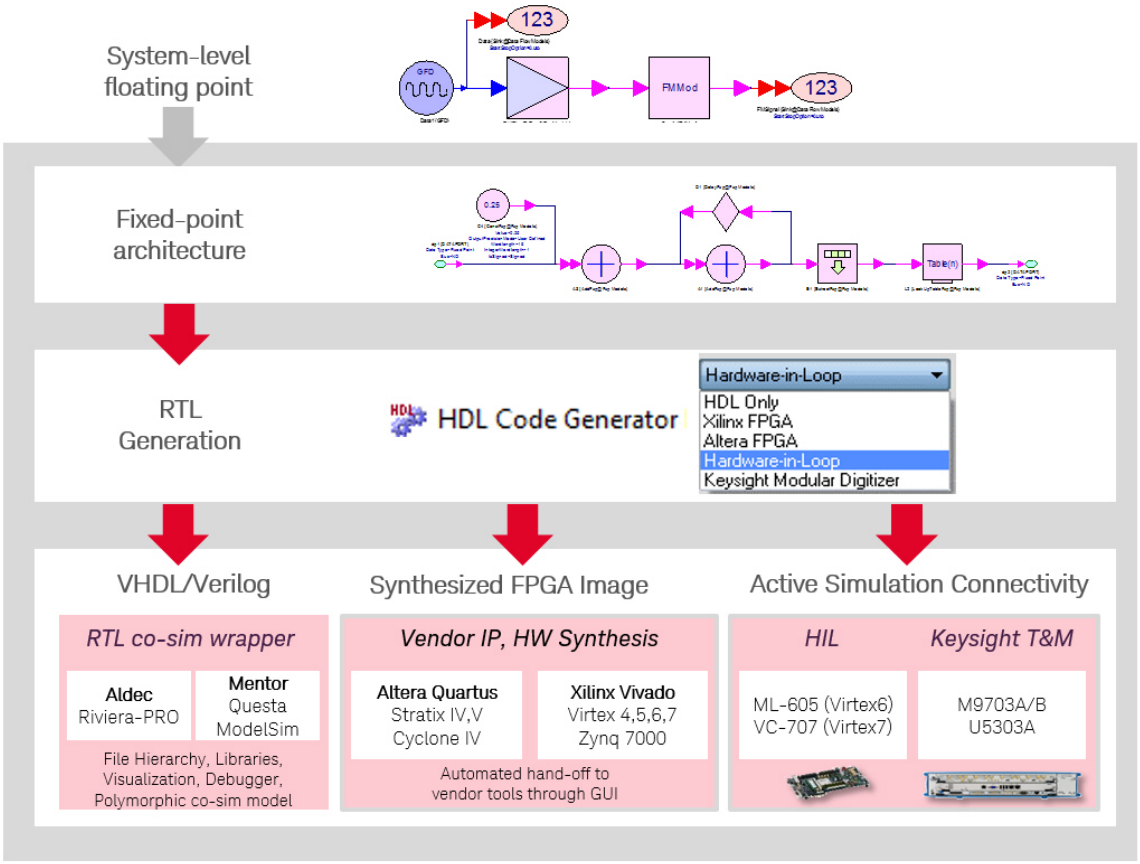


Figure 1. The W1717 Hardware Design Kit adds a fixed-point library, VHDL/Verilog code generation, and connectivity to popular vendor tools and platforms.

Key Features

Design and verification productivity

System-level modelers and verification engineers can take advantage of SystemVue's comprehensive integration into hardware design and verification flows. A fixed-point simulation library predicts hardware-like effects without committing to a targeted implementation, and generates synthesizable, hierarchical, RTL-level Verilog and VHDL that is bit-true and cycle accurate. This provides a path to implementation and creates a verification wrapper for polymorphic model-based design flows moving from algorithm to fixed point to RTL and to instantiated hardware. The ability to co-simulate with external hardware description language (HDL) simulators or real hardware is included free with the SystemVue core environment.

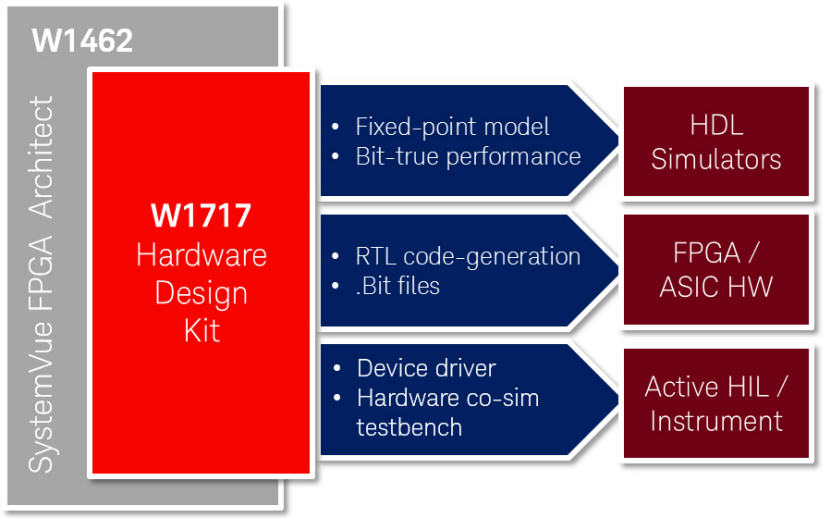


Figure 2.

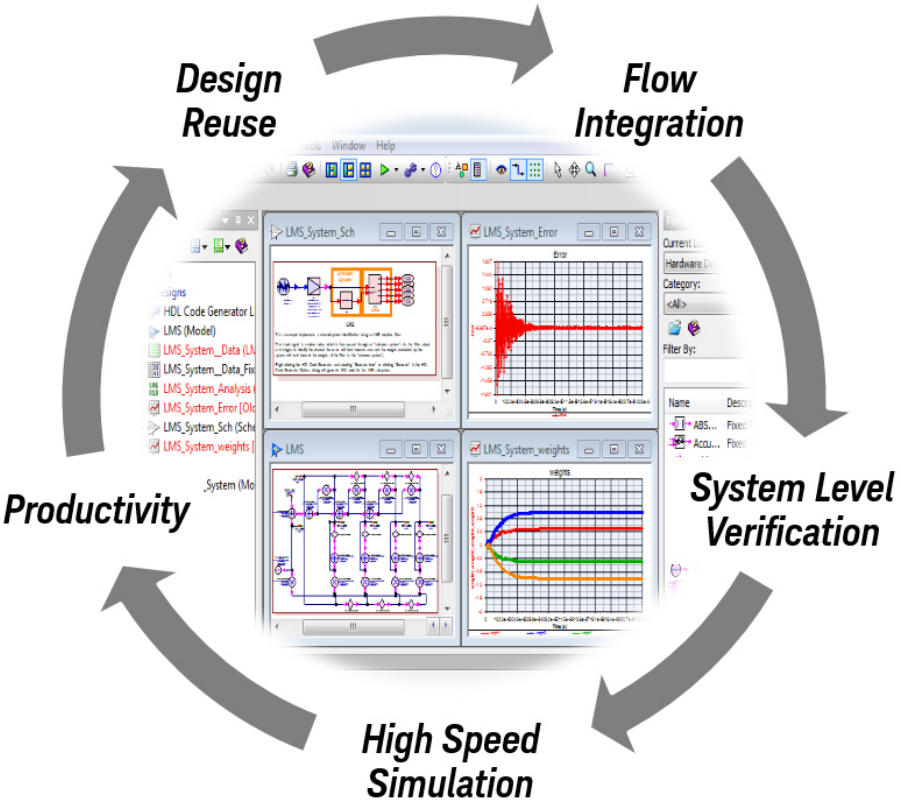


Figure 3. The HDK provides the fastest hardware design flow, enabling high performance and high productivity.

Fixed Point Design

Mapping signal-processing algorithms to dedicated hardware with fixed-point arithmetic is often an integral part of the algorithm design and analysis flow. Hardware Design Parts, available in the HDK, can be used to build, simulate and analyze fixed-point systems. A library of over 45 functions, from low-level logic elements to more advanced signal-processing parts such as filters and fast Fourier transforms (FFTs), is available.

The fixed-to-float and float-to-fixed conversion parts provide a means of interfacing fixed-point components with other SystemVue blocks. Hardware Design Parts can also be configured to automatically collect information on dynamic range, overflows and underflows. The parts can be shown in the Fixed-Point Analysis Table to help engineers with system optimization.

The SystemVue HDK supports use of standard-compliant IEEE 1666 SystemC fixed-point data types.

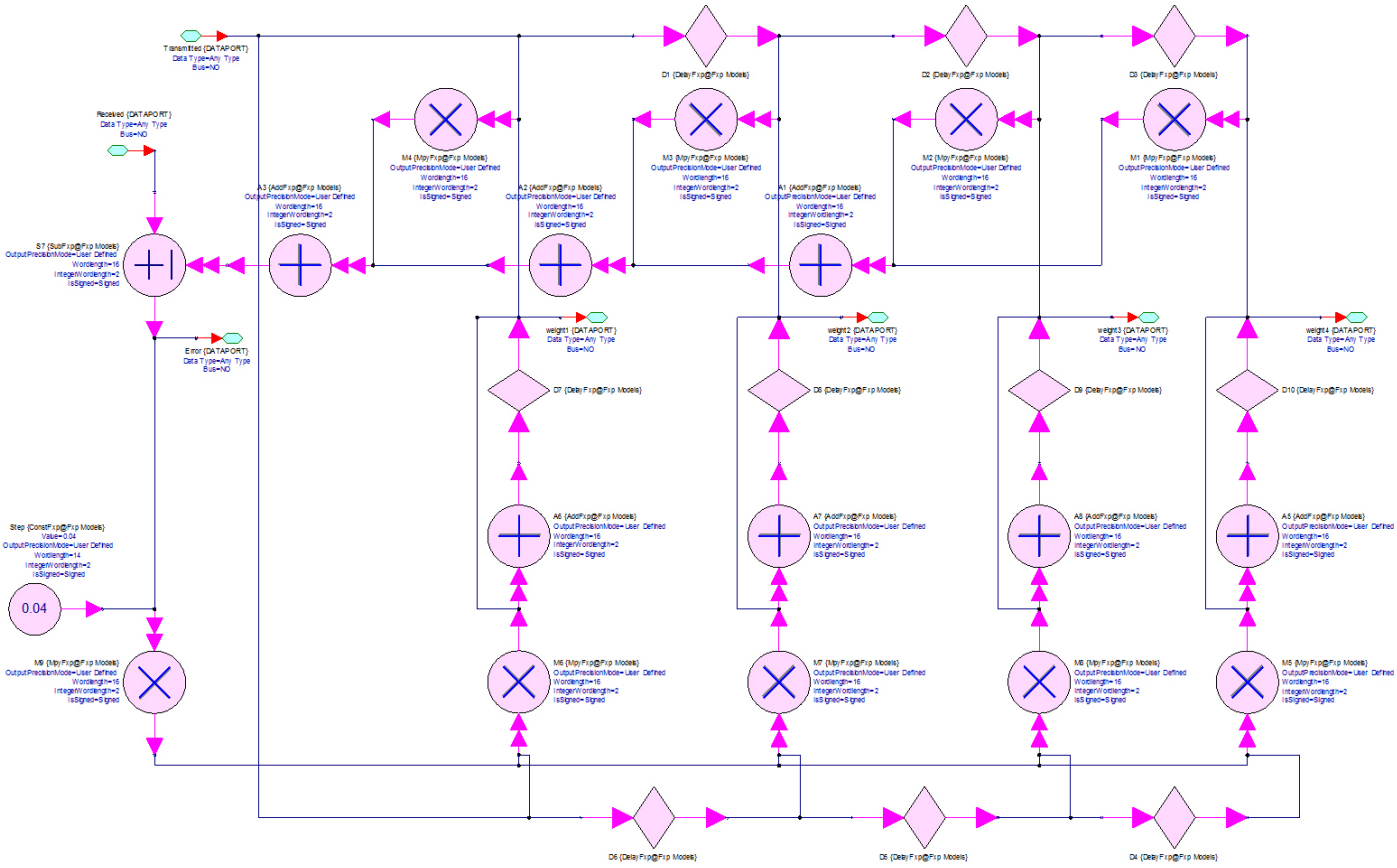
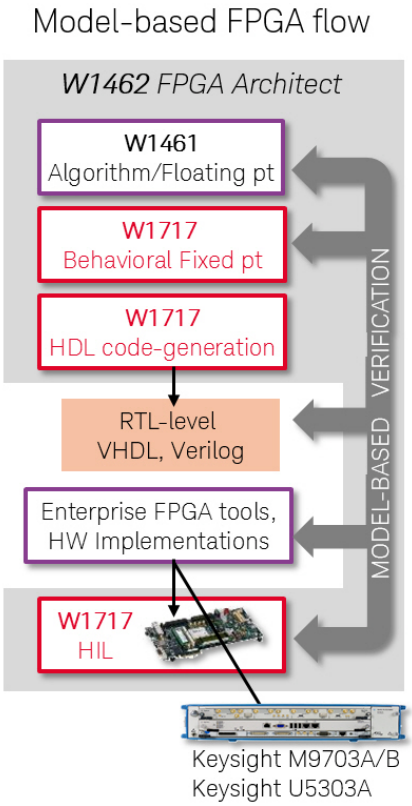


Figure 4. A cycle-accurate LMS transpose adaptive filter design using fixed-point generic primitive models.

Synthesizable HDL Code Generation

SystemVue's HDL Code Generation capability provides users an easy path from schematic design to hardware. A user-created SystemVue sub-network model, with only synthesizable fixedpoint parts from the HDK, can be used to generate VHDL/Verilog for the sub-network. For Xilinx's Virtex-4-7 and Zynq7000 FPGAs, SystemVue provides a path to configure the clock and reset the user's HDL design, as well as set up Vivado project or generate bit files directly. For Altera's Cyclone IV/Stratix IV/Stratix V FPGAs, SystemVue provides a similar path to set up a Quartus II project or generate programming files directly.



Simulation

VHDL/Verilog co-simulation

With the SystemVue HDL co-simulation feature, users can simulate components represented in a HDL, VHDL and Verilog, in the same schematic with other SystemVue components. This integrated capability provides complete design flexibility and complements other SystemVue features, including HDL generation.

HDL co-simulation also allows the user's existing HDL code to be included in system-level simulations, and integrated with local synthesizable fixed-point primitives. The HDL Code Generator connects the user's HDL code with other Hardware Design Parts to generate HDL codes for the whole design. It then runs the Xilinx/Altera automatic implementation flow to generate the programming file.

The ability to design all portions of a communications product in one integrated environment eliminates design errors resulting from disconnects among different design teams. By co-simulating with HDL designs, users can easily incorporate existing HDL intellectual property (IP) into new designs, or even co-simulate with SystemVue-generated HDL. SystemVue integrates well with the Mentor ModelSim/Questa or Aldec Riviera-PRO HDL simulators via two simulation modes, either direct simulation from the SystemVue user interface or hierarchical HDL project generation, for full interaction and debugging using the external development environments.

Hardware co-simulation

The SystemVue Hardware-in-Loop (HIL) co-simulation engine allows the dynamic use of FPGA hardware to accelerate computational tasks in a multi-threaded software environment. Effectively, it circumvents traditional bottlenecks where the accelerator hardware would only be usable by a single thread at a time. The engine provides both the hardware implementation and dynamic partial reconfiguration on /7 to implement functions or measurements in FPGA hardware. Programming and run-time simulation connectivity is also supported for the Keysight wideband digitizer families M9703A/B and U5303A. This allows real-time T&M personalities to be prototyped in simulation, then used for custom measurement personalities.

Hardware co-simulation requires a great deal of data stream exchange between processors and FPGA cards. It can be streamed via the PCI Express® bus. In theory, an eight-lane PCI Express Gen 2 bus offers a peak throughput of 500 MB/s. Even though PCI Express suffers from latencies inherent in device drivers and operating system interrupt handling, there are clear advantages to performing hardware co-simulation with a FPGA board using a PCI Express connection to the host processor.

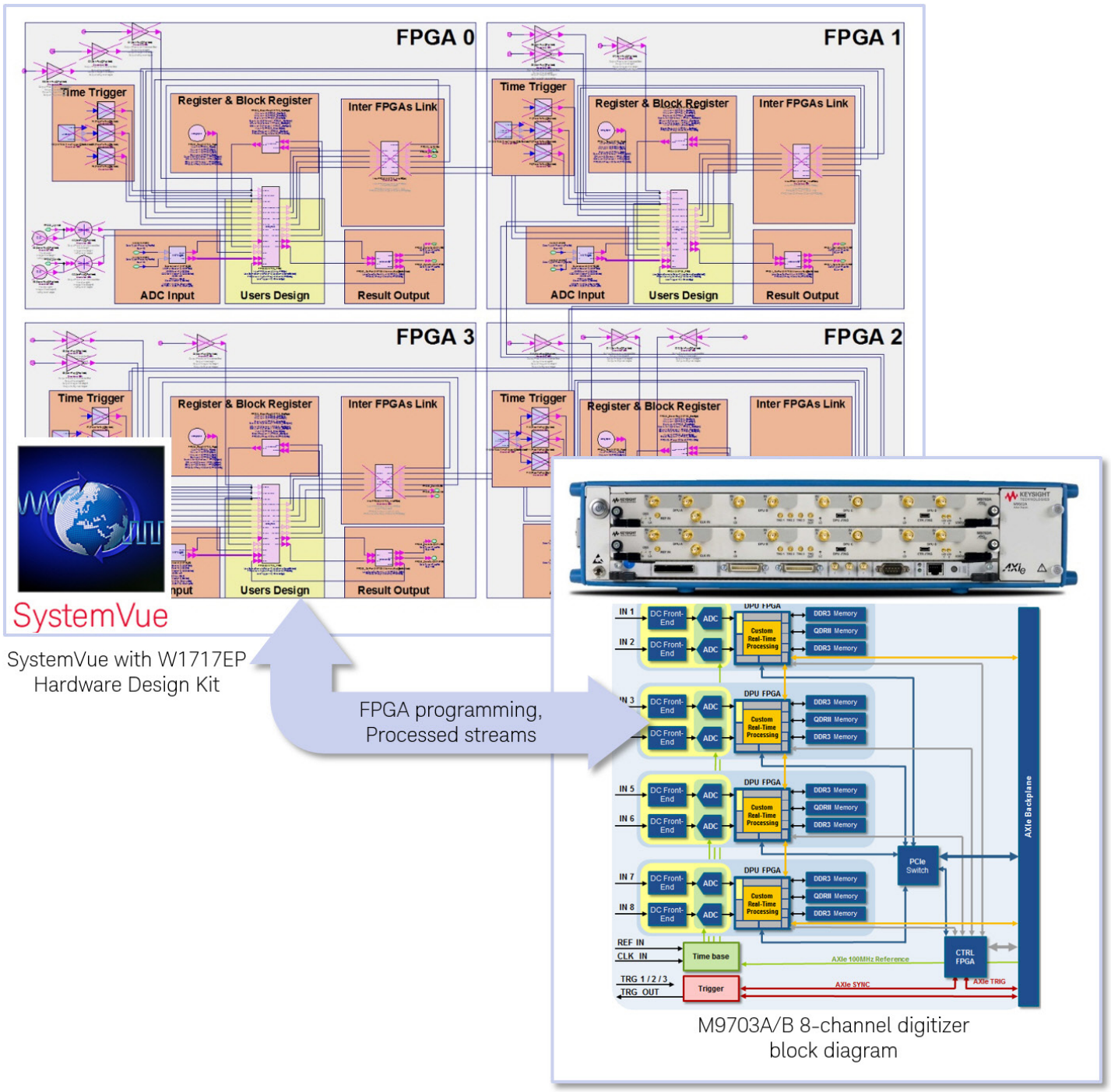


Figure 6. SystemVue connects to the M9703A/B wideband multi-channel digitizers through a special interface included with the W1717 HDK. This allows custom high-performance algorithms (such as filtering, beamforming, or real-time corrections) to be programmed into the instrument, to run at the true measurement speed. Processed measurement data can also be used in SystemVue simulations, in an HIL configuration over PCIe.

Design Reuse

Design reuse is part of the growing Electronic Design Automation (EDA) industry trend toward repeated use of previously designed components. SystemVue provides two efficient methods for carrying IP into the system-level design environment.

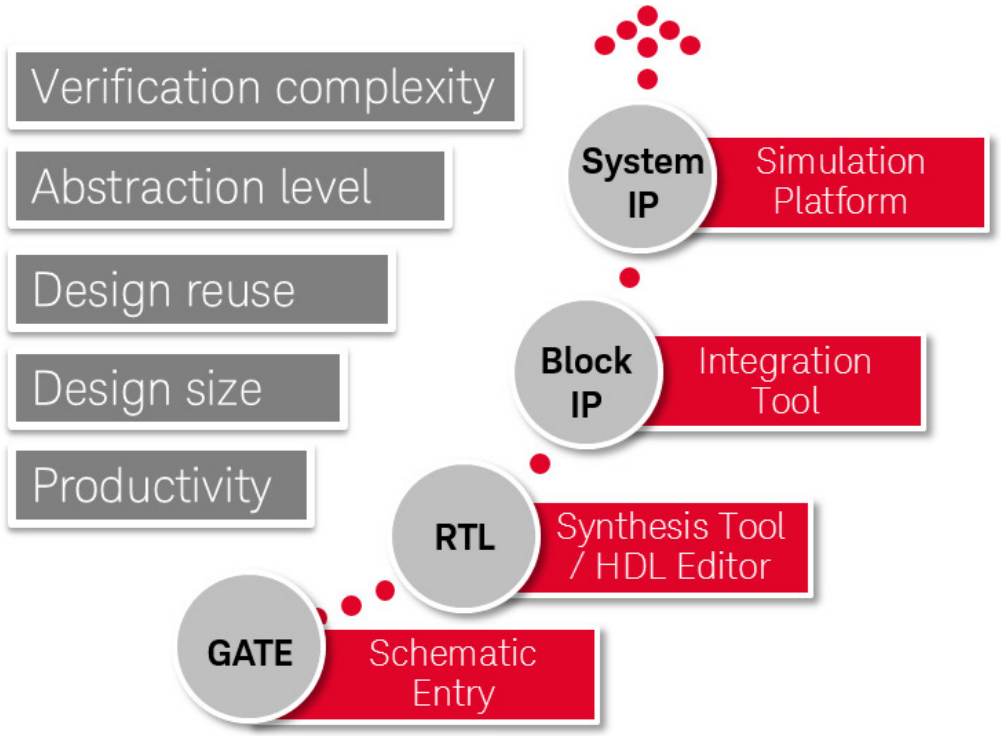


Figure 6. SystemVue HDK improves design productivity by allowing engineers to design at a higher abstraction level and reuse their designs.

The SystemVue environment provides the primary method for design re-use, using sub-network models. SystemVue subnetworks are portable and easily inserted into other design workspaces (e.g., via a copy and paste function). Within SystemVue, they are known as “design” objects, and contain a symbol, schematic, equation, parameters, and notes. Sub-networks can include fixed-point schematics built using the graphical UI, or external HDL code that is instantiated in SystemVue using the HDL co-simulation block.

A second method of design re-use is facilited by the W1717 HDK’s XilinxIPIntegrator model. This model allows Xilinx CORE Generator IP cores to be co-simulated using external HDL simulators. Furthermore, SystemVue can combine these external Xilinx CORE Generator IP cores with native SystemVue fixed-point designs and other external HDL blocks, and then use HDL Code Generation to create a hierarchical HDL for the overall design. SystemVue’s XilinxIPIntegrator model supports most of the Xilinx IP cores needed for communications signal processing including: Base IP, Basic Elements, Communication and Networking, Digital Signal Processing, Math Functions, and Memory & Storage Elements.

After HDL code generation is complete, SystemVue can be configured to invoke Xilinx’ automatic FPGA implementation tools to generate a programming (“.bit”) file and add a polymorphic model choice for the HIL model, all in a single step, from the SystemVue GUI.

Benefits

The W1717 HDK provides a number of key benefits for baseband algorithm developers and communications and radar system architects, including:

- **Fidelity**
  Quickly account for bit-true hardware effects prior to targeting, while still at the architecture level, for better baseband-RF partitioning.
- **Productivity**
  Integrate your proprietary, hand-optimized HDL blocks or import IP cores from external sources, such as Xilinx CORE Generator IP.
- **Vendor-neutrality**
  Generate target-neutral RTL that is transportable between hardware vendors.
- **Tool connectivity**
  Rapid-prototyping with direct integration to Xilinx Vivado, Altera Quartus II and other synthesis tools.
- **Real-time verification**
  Verify and accelerate algorithms with HIL cosimulation with Xilinx Virtex-6 families (such as the ML-605 and VC-707 development boards) over a PCI Express interface.
- **Cross-domain model-based design**
  Verify and debug algorithms at every level of FPGA hardware abstraction, in the presence of models from other domains, such as RF EDA models, test and measurement waveforms, and simulation-based wireless Standards references.

Included with the W1717 HDK

- **Fixed-point library** containing 45 bit-true, cycle accurate models. Enables fixed-point data type and simulation mode with block-level/pin-level, fixed-point histograms and “red-x” overflow/underflow analysis.
- **Integration of custom libraries** of handgenerated HDL and external IP cores, such as the Xilinx CORE Generator.
- **HDL code generation** of RTL-level VHDL/Verilog, complete with design hierarchy, system-level test bench wrappers, test vectors, and intelligent creation of clock ready and enable signals.
- **Polymorphic model instantations** added for each installed HDL simulator, such as Aldec Riviera-PRO, or Mentor Questa/ModelSim SE, enabling easy model-based scripting and co-simulation, with verification-in-place.
- **Direct integration of synthesis tools** (such as Xilinx Vivado and Altera Quartus II) from the SystemVue GUI.
- **Hardware-in-the-Loop** co-simulation. Bring real-time acceleration into SystemVue using development boards such as the ML-605 or VC-707 over PCIe.

Configuration

The W1717 HDK can be added to any SystemVue environment. It is already included in both the W1462 SystemVue FPGA Architect and W1465 SystemVue System Architect bundles.

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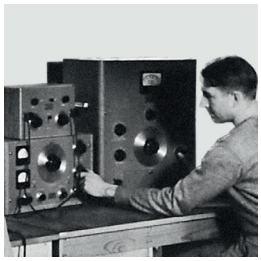

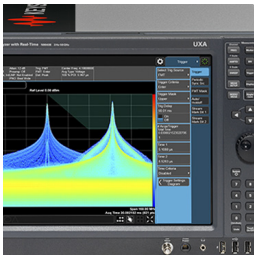

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