

Keysight Technologies

Triggering Wide-Bandwidth Sampling Oscilloscopes For Accurate Displays of High-Speed Digital Communications Waveforms

Application Note

Includes information on use of the
83496A clock recovery module

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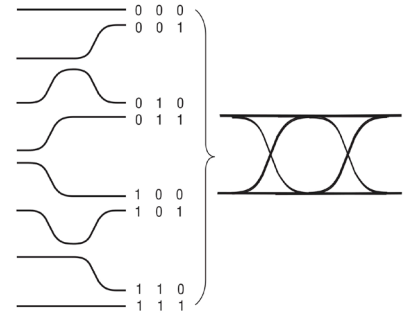
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Correct Triggering Is Essential For Accurate Waveform Displays

Virtually every test scenario for the design, development, and manufacturing of high-speed digital communications systems and components includes some method to observe the transmitter waveforms. A common tool for this is a wide-bandwidth sampling oscilloscope.

An oscilloscope displays the amplitude of a signal as a function of time. An important issue in setting up an 'amplitude versus time' display is to determine what the time axis of the oscilloscope represents. A fundamental requirement to acquire a signal using a wide-bandwidth sampling oscilloscope, such as the 86100 Infiniium Digital Communications Analyzer (DCA), is to provide a signal that is used to establish a timing reference. This signal is commonly known as a trigger. The time locations of all displayed amplitude information are determined by their position in time relative to the triggering signal. To correctly display and interpret a waveform, it is critical to understand the different triggering options and how they affect measurements.



The most common way to view high-speed digital communications signals is in the eye diagram format. The eye diagram provides an easy way to quickly check the overall quality of the signal. In one view, the many bit combinations of data patterns are overlaid in a composite waveform. Because the eye diagram represents a comprehensive view of the signal, it is easy to visually obtain the overall characteristics of the signal such as noise, jitter, distortion and signal strength.

Another possible way to display a digital communications signal is in the pattern display. In this display, the bits of the signal are shown in a sequential format. This is useful to see in great detail the shape and trajectories of the signal, which are often difficult to observe in the composite eye diagram. However, due to a limited time span of the oscilloscope it is difficult to show a large number of bits with high resolution.

Whether an eye diagram or a pattern waveform is displayed is dependent upon the type of signal that is used to trigger the DCA. To understand why this is true requires a basic understanding of how a widebandwidth sampling oscilloscope operates.

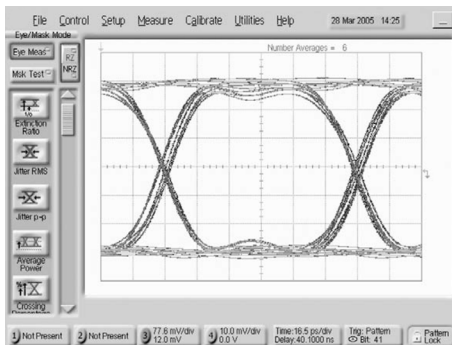


Figure 1: The eye diagram display

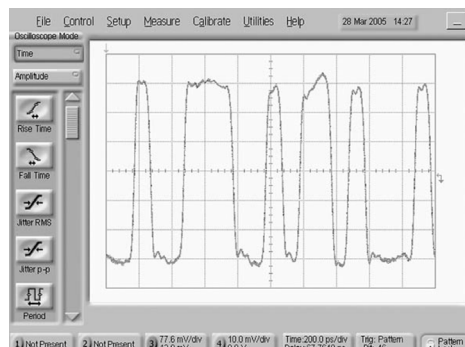


Figure 2: The pattern waveform display

Digital oscilloscope architectures

Two types of oscilloscopes can be used to view very high-speed signals. One is the wide-bandwidth sampling oscilloscope (sometimes referred to as an equivalent time scope) such as the DCA mentioned above, or a real-time sampling oscilloscope (sometimes referred to as a single-shot scope). In the simplest analysis, a real-time oscilloscope can be thought of as an ultra fast analog-to-digital converter. The sampling rate (as of 2005) can be as fast as 40 Giga-samples/second. The bandwidth of this type of oscilloscope is determined in large measure by the sampling rate and is approximately 13 GHz for a 40 Gsa/s architecture. At these sampling rates/bandwidths, signals as fast as 5 Gb/s can be accurately viewed. Higher speed signals can be observed, but with degraded accuracy. A wide-bandwidth sampling (equivalent-time) oscilloscope like the DCA can have a bandwidth in excess of 80 GHz. However, the sampling rate is under 1 Mega-samples/second. How can an instrument with a sampling rate several orders of magnitude below that of the real-time oscilloscope have a bandwidth several times higher? The answer lies in how the instruments are triggered.

As mentioned, the real-time oscilloscope samples data as fast as 40 GSa/s. Thus a large stream of data points are captured in one contiguous record. Something is needed to determine what portion of the data stream gets displayed. This is determined by the trigger. Generally, the trigger event is a feature of the data signal itself. The trigger can be as simple as when the input signal level crosses a certain amplitude level to as sophisticated as a complex series of logic events in the data stream. See Figure 3.

With its relatively low sampling rate, the DCA will acquire only one sample point for any triggering event. Also, the sampling architecture does not allow the triggering event to be some feature of the incoming signal. A trigger separate from the signal being observed is required to synchronize the sampling process. First, the DCA must be armed and waiting for the trigger event to occur. The armed DCA is triggered when the trigger signal crosses a defined voltage threshold. The trigger establishes the time reference and initiates the first sampled point. The sampling takes place a fixed delay time after the trigger event. The delay value must be controlled with extremely tight tolerance (under 100 fs in high-resolution configurations). This delay term is at least 24 ns. (It can be larger if the DCA timebase is configured to observe the signal at a delay value larger than the minimum instrument setting.) The DCA must rearm before another trigger signal can be accepted. The rearm time is approximately 25 μ s after a sample is taken. This is a critical concept to understand and has a significant impact on how signals are reconstructed. Once the DCA has rearmed, a second sample is taken when the next trigger event occurs. Like the first sample, the second sample takes place after the delay time has elapsed. However, to avoid sample two occurring at the identical time (relative to the trigger event) as sample one, a small incremental delay is added to the large delay term. The incremental or sequential delay term is dictated by the time span of the DCA and the number of points (record length) defined to reconstruct a waveform. For example, if the DCA time span is configured to be 1 ns wide (100 ps/division and a 10 division display) and 1001 points are going to be used to construct one waveform, the time between points, which is also the sequential delay term, will be 1 ps. A complete waveform record will be constructed and displayed when 1001 rearm and trigger cycles have taken place.

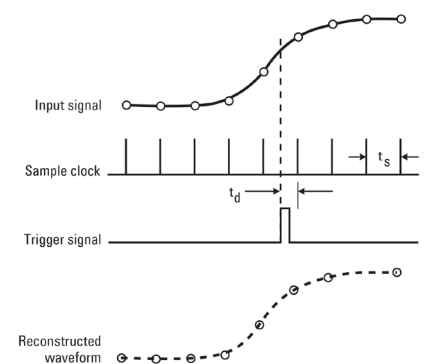


Figure 3: Waveform acquisition and triggering with a real-time oscilloscope

Pattern waveform or eye diagram?

The type of waveform displayed (a pattern waveform or an eye diagram) is dependent upon what type of trigger signal is used. The pattern waveform requires a data pattern that repeats and a triggering signal that occurs once every repetition of the pattern. The sampling process for the DCA when using a pattern trigger is shown in figure 4.

As described above, the first sample is taken once the DCA is armed and the trigger edge (indicating the start of the pattern) triggers the scope. The pattern trigger must always occur at the same exact time location relative to the data sequence. The scope will rearm and wait for the next pattern trigger edge. The trigger occurs at the same point in the data sequence. Due to the sequential delay added to the main delay, the second sample is taken at a point in the pattern adjacent to and slightly later in time than the first point. The process is repeated over and over again, with the sequential delay increasing and forcing the sampling to take place across the data pattern.

It is important to note the two critical requirements to observe the pattern waveform:

- 1) The data pattern or waveform must be a repeating signal
- 2) A trigger signal that occurs only once for N repetitions of the pattern
(N = 1, 2, 3...) and is always at the same relative location of the pattern

The above requirements are not always achievable. Fortunately, displaying signals in the eye diagram format is not bound to the requirements of the pattern waveform. Even if the signal is not repetitive, an eye diagram can be constructed. This is achieved with a clock (triggering signal) that is synchronous to the data. The sampling process is shown in figure 5.

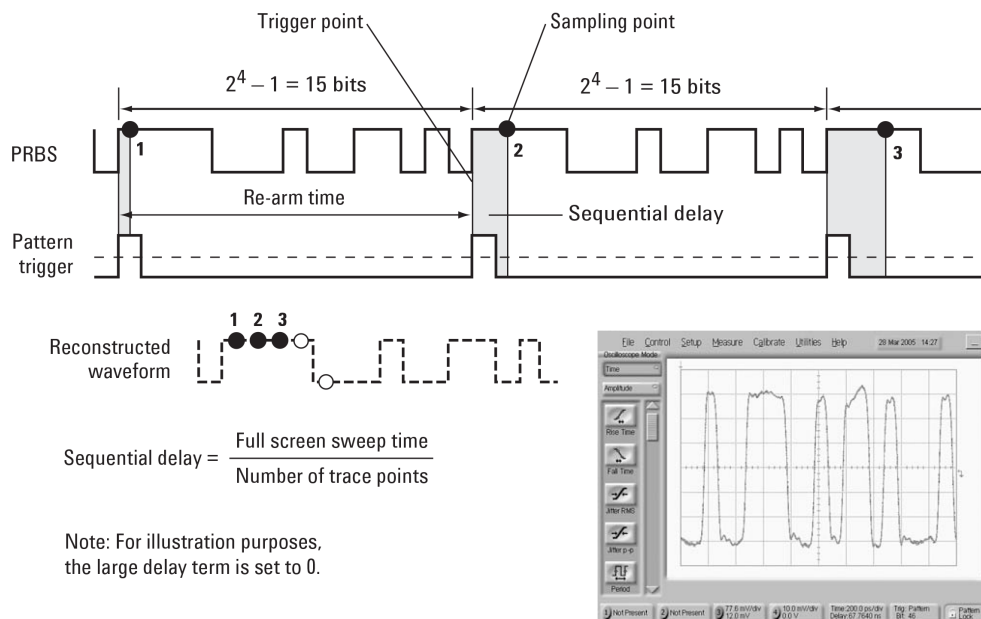


Figure 4: Sampling process for a pattern waveform

The sampling process is similar to that of the pattern waveform with the following exceptions. Clock triggers occur much more frequently than pattern triggers. Generally the DCA will be triggered more frequently with a clock (assuming the pattern repetition rate is slower than the rearm time of the DCA). Also, the rearm time is asynchronous to the data signal and trigger, so the time at which the DCA will accept triggers will occur at arbitrary locations in the data pattern. Thus samples are taken with high precision and synchronism to the data. The clock trigger ensures that the sampling is precisely aligned with the bits in the pattern. However, which specific bits are sampled in the data stream is uncontrolled. Thus two adjacent samples will be taken at completely unrelated locations in the data stream. If sample 1 is taken on a logic 1 level, sample 2 is equally likely to take place on a 0 level or a 1 level. The result is that the waveform record will have been acquired from many locations in the bit stream (many 1's, many 0's, as well as the transition regions) and all displayed on a common timebase. This is the eye diagram.

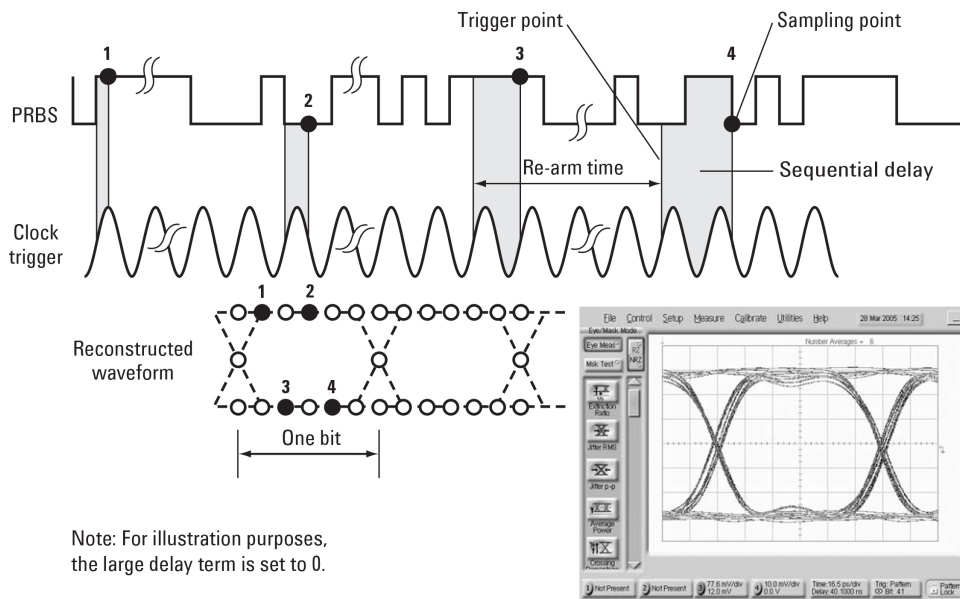


Figure 5: Eye diagram construction using a clock trigger

Divided clock triggers

There are some important details about the allowable characteristics of the clock trigger when constructing the eye diagram. Full rate clocks as well as divided clocks will generate an eye diagram. But there are some important considerations when using divided clocks. If the data pattern is repeating, and the length of the pattern is an even multiple of the clock divide ratio, the eye diagram will be incomplete. For example, if the data pattern is 64 bits in length, and a divide-by-8 clock is used, the samples will be taken on bits 1, 9, 17..., 49, 57. The time span of the DCA can be expanded to include the other bits in the pattern, but any one eye diagram displayed in this case will only include one-eighth of the data stream. On the other hand, a divide by 10 or divide by 6 clock will produce a complete eye for the 64 bit pattern.

(Note that the Keysight Technologies, Inc. 83496 clock recovery module, discussed later, provides a clock/8 trigger to the DCA. Thus data patterns that have lengths that are multiples of 8 will be observed as incomplete eye diagrams. This can be solved by using the front panel port of the 83496 connected to the DCA mainframe trigger input and selecting the front panel as the trigger source. The front panel trigger can have several clock divide ratios, including a full rate clock. However, above 7 Gb/s, the smallest divide ratio for the front panel clock output is 2).

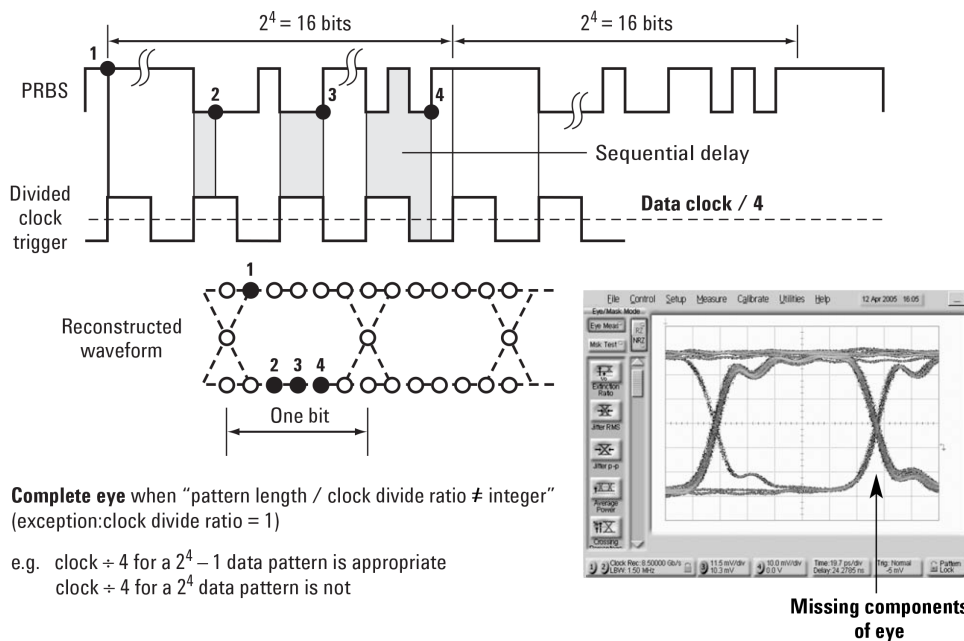


Figure 6: Divided clocks can lead to incomplete eye diagrams

Incoherent clock triggers

If a clock signal is at the same nominal rate as the data, but is not synchronous to the data, an eye diagram may be displayed. Any frequency drift in either the data or the trigger (relative to the other) violates the requirement of the clock being synchronous. This incoherence between the two signals will be viewed as a wander effect. The eye will appear to be smeared. The issue of data jitter, a specific type of frequency variation in the data, relative to the triggering clock, will be discussed in “Using clock recovery to derive a trigger”, page 9.

Triggering on the data directly

What if the data signal itself is used as a trigger? For example, what if the signal were split, half going to the DCA input port, the other half to the trigger input. The result will be an eye diagram. However, it will be an incomplete eye. Note that there must be a 0 to 1 or a 1 to 0 transition in the data to create a trigger event. The DCA can trigger off either case, but not both. If the DCA is configured to trigger on a rising edge the only two bit sequence that will generate a trigger is the 0, 1 sequence. The ‘0, 0’, ‘1, 0’, and ‘1, 1’ sequences will not produce triggers. The resulting eye from triggering on the data may look to be complete, but for random or near pseudorandom data approximately 75% of the possible bit sequences do not generate a trigger and are not observed. DCA trigger delay can help towards a more complete eye by taking samples downstream from the trigger event and including more of the possible pattern sequences. Triggering on the signal itself has some significant issues relative to how frequency instability (jitter) should be interpreted when the signal is being compared to itself. This will be discussed below under the topic of clock recovery, where in the case of a data trigger, all the jitter present on the data is also present on the trigger signal.

One case where triggering directly on the data stream is effective and accurate is when optical modulation amplitude (OMA) is being measured. OMA is the difference between the nominal 1 level and the 0 level of a digital communications signal. Communications standards typically suggest that the pattern for this measurement should be a run of n consecutive 1's followed by n consecutive 0's, where n is somewhere between 4 and 11. The 1 amplitude is found in the middle of the run of 1's and the 0 level is found in the middle of the run of 0's. If a clock signal is used to trigger the DCA, it is difficult to isolate the middle of the consecutive identical digits, unless the clock is a divide by n clock. However, if the DCA is triggered on the data stream directly, the ideal OMA display is achieved.

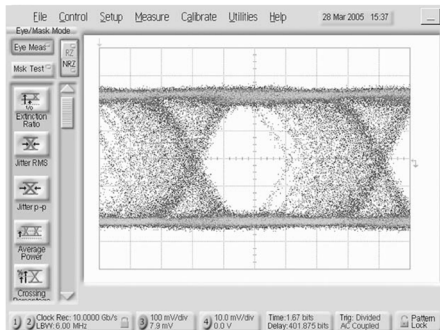


Figure 7: Triggering with an incoherent clock results in a degraded eye diagram

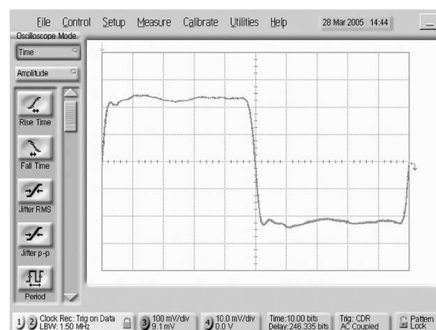


Figure 8: OMA square pattern is easily observed with a direct data trigger

Using Clock Recovery To Derive A Trigger

Finally, an important case exists for deriving a synchronous clock from the signal being measured. This is referred to as triggering using clock recovery. Several important issues arise when deriving the measurement timing reference from the signal being measured:

- How are waveforms to be interpreted if the timing is derived from the signal itself?
- Are jitter and eye-mask tests still valid compared to triggering with a stable, jitter free synchronous clock from a data pattern generator?
- Does the clock extraction process add any jitter to the displayed waveform?
- Can compliance testing to industry standards be performed?
- How does the design of the clock extraction circuit affect the waveform?
- Does the clock extraction process vary depending upon the data pattern?

Clock recovery basics

To answer these questions, some basic knowledge about clock extraction hardware is needed. Most clock recovery circuits are based upon some form of phaselocked loop (PLL). In a PLL there are three basic building blocks. A voltage controlled oscillator (VCO), a phase detector, and a gain/filtering stage between the two.

A small portion of the signal to be measured is tapped and routed to the input of the phase detector. The VCO is set to operate at a frequency close to the rate of the data stream. A portion of the VCO is routed to the phase detector. If the two inputs to the phase detector are not at the same rate, an error signal proportional to the difference is produced, tuning the VCO and forcing it to the same frequency as the incoming data rate. The VCO is then locked to the data stream. The VCO signal is also routed to the DCA as a trigger.

Clock recovery loop bandwidth

The VCO of the clock extraction circuit can be thought of as a flywheel that is kept spinning at the desired rate by incoming bit transitions. That is, whenever there is a change from a 1 to a 0 or a 0 to a 1, the VCO has something to synchronize to. It is important for the VCO to stay on frequency even when there are no transitions such as a long run of 0's or a long run of 1's. This is achieved by placing an effective low-pass filter between the output of the phase detector and the control input of the VCO. Although not an actual low pass filter, the effect is similar. Adjustment of the gain in the line leading to the tuning input of the VCO controls what range of frequencies on the error signal are attenuated and do not affect the VCO tuning. This provides stabilization to the VCO control signal and subsequently the VCO frequency. It would seem that the higher the stability, the better. But consider also that the filter controls how fast the data rate can fluctuate (jitter) and still allow the VCO track and follow. When the data signal has jitter, the error signal output of the phase detector will be an analog representation of the jitter. The phase detector is effectively a jitter demodulator. Since the error signal controls the VCO, the jitter from the data is transferred to the VCO. If the rate of jitter becomes fast enough (relative to the bandwidth of the control loop), the rapidly varying error signal from the PLL phase detector will be suppressed by the loop filter. High frequency jitter does not reach the VCO. Thus the PLL, and subsequently the clock extraction circuit using this PLL, will only follow data with jitter frequencies that are within the bandwidth of the loop filter. If the jitter is very fast, the VCO can stay locked to the data, but can only follow jitter within its bandwidth.

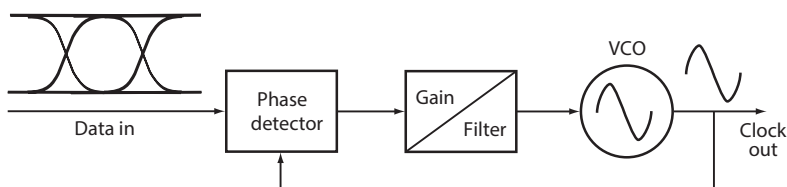


Figure 9: Basic clock extraction circuit

The effect of loop bandwidth on observed jitter

The fact that data jitter is transferred to the (VCO) DCA trigger signal has very important implications for what jitter will be seen on the signal displayed by the DCA. Remember that all measurements are made relative to the trigger signal. If the trigger signal were perfect (a single frequency with no fluctuation) the DCA would display how a data signal varied in its timing relative to this ideal trigger signal. All of the data jitter would be observed since the trigger is stable. But now the signal used as a reference has instability (jitter) similar to the signal being measured. The jitter of the data relative to the trigger is effectively zero. Now, even a data signal with large jitter can potentially appear to be jitter free as long as the jitter on the trigger and the jitter on the data are identical!

If the PLL loop bandwidth is very narrow, very little data jitter is transferred to the VCO. The VCO comes close to being jitter free, similar to the 'ideal' clean clock signal where all the jitter is observed. If the loop bandwidth is very wide, almost all of the jitter is

transferred to the VCO and very little jitter is observed. This indicates an unusual effect of the loop bandwidth control in the clock recovery PLL. This is effectively a low pass filter effect in the PLL. However, from the perspective of the observed jitter on the DCA, it has a high pass effect. Only jitter that is above the bandwidth of the filter is observed.

The jitter transfer function of a PLL clock extraction circuit is a measure of the jitter on the recovered clock compared to the jitter on the incoming data stream. It is a common method to describe the jitter bandwidth of a clock extraction circuit. It is sometimes used to describe what jitter will be observed on a DCA when the PLL is used as a trigger. However, a more precise description of what jitter is observed on the DCA would be "1-jitter transfer" which has the expected high-pass characteristics. The function is complex, and phase must be considered when constructing the response plot. This is shown in figure 10.

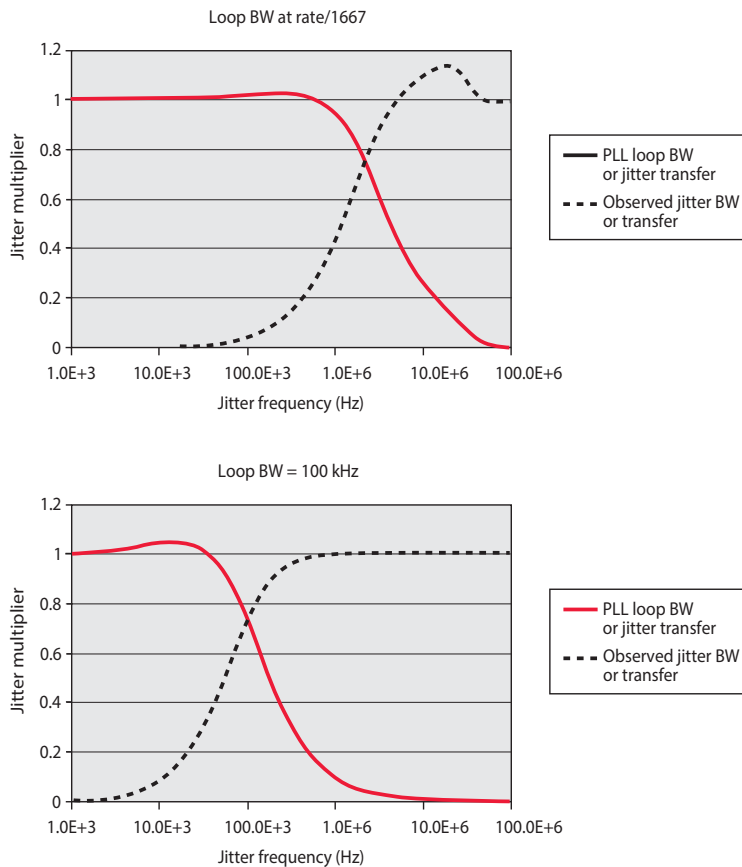


Figure 10: 83496A PLL jitter transfer and resulting range of jitter observed on the DCA

What is the ideal loop bandwidth?

When measuring a data signal, what should the loop bandwidth of the clock extraction circuit be? At first glance it would seem that the narrower the loop bandwidth the better, as this allows most of the jitter to be observed. However, a case can be made for having a wider loop bandwidth.

Consider that the transmitter being tested will eventually be paired with a receiver to create a communications link. The receiver includes a decision circuit to determine the logic levels of incoming bits. To make decisions at the optimal time, even when the data has jitter, the receiver will have its own clock extraction circuit. It must have a loop bandwidth wide enough to track out the expected jitter, but low enough to not be affected by low transition density (transition density being how frequently jitter edges occur at the transition from a one to a zero or a zero to a one, and a 100% transition density is achieved with a 1-0-1-0-1-0...pattern) data sequences. The VCO of the PLL ideally should stay in phase with the data stream even when there are few edges to keep it stabilized. With an optimal loop bandwidth the receiver is tolerant of jitter on the data, as long as the jitter is not too fast as well as runs of consecutive digits. If the receiver is tolerant of low frequency jitter, transmitters should not be penalized for their low frequency jitter performance. It would make sense to screen transmitters only for high frequency jitter. Thus a test system should display jitter that is above the loop bandwidth of the PLL in the receiver (that this transmitter will be paired with). This is achieved by setting the loop bandwidth of the trigger clock extraction circuit to be the same as that in the receiver. This is sometimes referred to in industry test standards as triggering with a “golden PLL”.

Figure 11 shows 2 eye diagrams. One was obtained using a wide loop bandwidth recovered clock trigger, the other with a narrow loop bandwidth. Less jitter is observed with the wide bandwidth, similar to what a real receiver decision circuit would encounter.

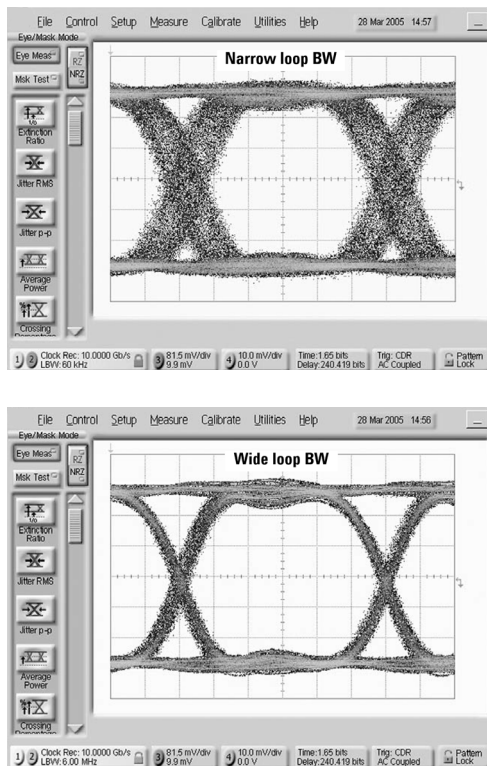


Figure 11: Data stream with 100 KHz jitter observed with a DCA with a narrow loop BW PLL and a wide loop BW PLL

In addition to eye-diagram measurements, jitter analysis using the DCA can also benefit from a PLL-based triggering scheme. When the various elements of jitter are analyzed, low frequency jitter is removed from the results when the DCA is triggered with a wide-bandwidth PLL. In Figure 12, note the change in the both the graphical and tabular results when using a wide loop bandwidth versus a narrow loop bandwidth PLL. Jitter components with low frequency spectra are suppressed, while high frequency jitter remains constant. Note that ISI is unchanged, RJ changes slightly, while asynchronous PJ changes dramatically.

This test approach is supported by a variety of communications standards. Given that receivers are tolerant of low-frequency jitter, transmitter costs can be reduced if they are not penalized for having low frequency jitter. Thus testing is specified to include the use of a clock extraction circuit. The PLL bandwidth is commonly specified to be data rate/1667 or data rate/2500. For example, 10 Gb/s Ethernet eye-mask tests are specified to be performed with a DCA trigger using a PLL with a bandwidth of 10.3125 Gb/s/2500 or 4.125 MHz.

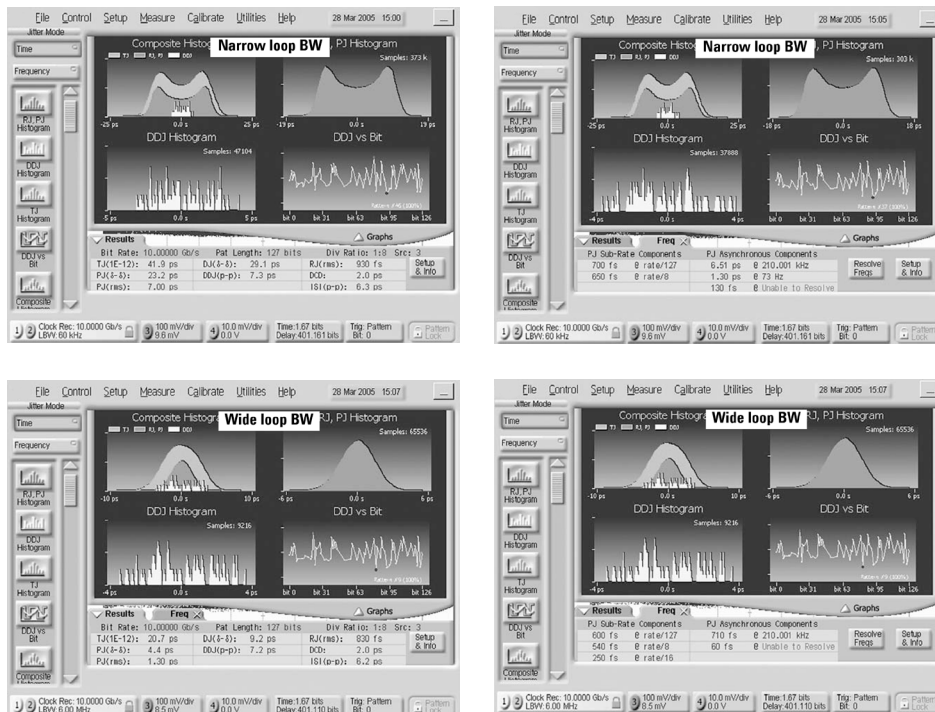


Figure 12: Jitter analysis with narrow and wide loop BW PLL trigger

The effects of data transition density

A subtle but important element of the test system golden PLL is that it needs to have a specific loop bandwidth for a variety of data patterns. Specifically, for consistent test results, the bandwidth should not change even if patterns with low or high transition densities are used. Thus the loop gain (which affects loop bandwidth) needs to monitor the pattern and adjust gain to match the data pattern transition density. In the 83496 clock recovery module, the transition density is measured and used to optimize the loop gain settings. This provides the correct loop BW for the given data pattern. It is important to note that if the transition density of the incoming data changes significantly, a “re-lock” process should be initiated by the user to assure the loop gain settings are updated to provide the expected loop bandwidth for measurements of that pattern.

The 83496 is designed to have optimal response for transition densities of 50%. That is, at 50% transition density there will be the widest range of adjustment of loop bandwidth. For transition densities significantly different than 50% but still between 25% and 100%, the 83496 should operate as expected, but with a slightly reduced range in loop bandwidth adjustment. For transition densities below 25%, performance is not documented.

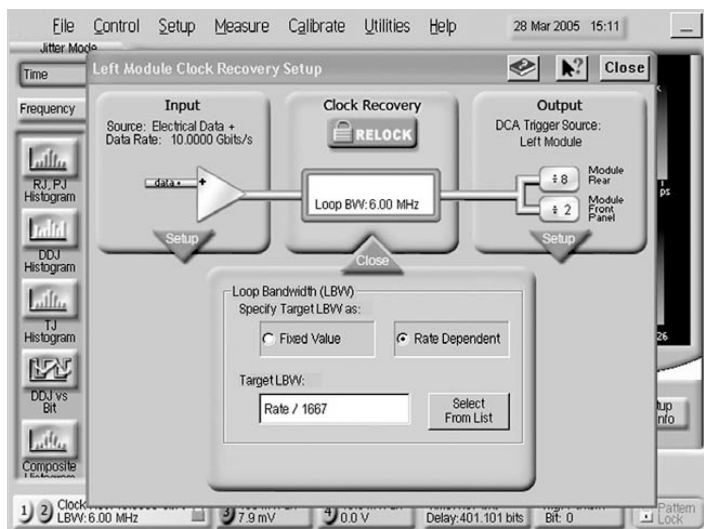


Figure 13: Control menu for the 83496 clock extraction module

The effect of timebase delay on observed jitter

Earlier the issue of timebase delay was discussed. Recall that the minimum timebase delay for the DCA is 24 ns. This presents a peculiar problem when characterizing data with high frequency jitter while the DCA is triggered with a recovered clock (or triggering directly on the data signal). Jitter is present on both the data and the trigger. What is the effect of having the trigger take place at one time and the sample take place a minimum of 24 ns later? It is like being on the ocean in a boat in rough seas and trying to throw a ball at a target on another boat some distance away. Assume both boats bob up and down in phase with each other. When the ball is thrown, both boats might be in the depth of a swell. By the time the ball reaches the other boat, it may have risen to the peak of the swell and the target is badly missed. It all depends on how long it takes to reach the target and how fast the ocean swells. In the case of the jitter measurement, problems occur if the rate of the data jitter is appreciable compared to the trigger-to-sample delay time. If the delay is set to the minimum value (24 ns), a worst-case scenario occurs when the jitter rate is at $1/(2 \times 24 \text{ ns})$ or 20.8 MHz. At this jitter frequency, if the DCA is triggered at one extreme of the jitter fluctuation, the sample will take place at the opposite extreme (a half period later). The reverse (opposite phasing) is also true. The net result is that the jitter will appear to be twice its actual value. Note that this is an extreme case and that the likelihood of the jitter being at or close to this worst-case frequency is very low. Also, jitter must be within the loop bandwidth of the PLL, with PLL bandwidth typically being less than 10 MHz. However, appreciable constructive interference can occur over a wide range of jitter rates, with significant spectra within the effective bandwidth of the PLL. 20 MHz represents the worst case for 24 ns of delay. If the delay is increased, the worst case scenario will be at a lower jitter frequency.

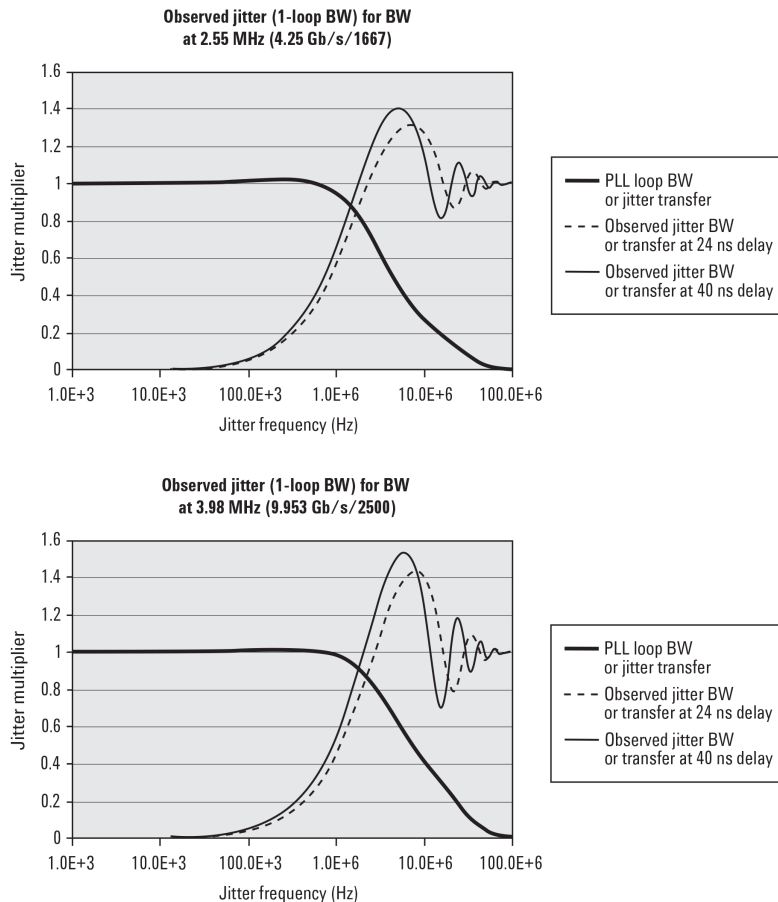


Figure 14. Jitter magnification as a function of DCA delay and jitter frequency

Reducing the trigger-to-sample delay term can mitigate the problem. Because the DCA delay value cannot be reduced below 24 ns, an alternative is to delay the data signal through adding cable delay prior to sampling. The added delay should be the same as the DCA timebase delay value. When using the 83496A Option 101 (optical clock recovery), a length of fiber is built in to the data path to align the trigger event and sampling instant. This will minimize the constructive interference problem that results through clock extraction when the trigger signal has common jitter with the data signal.

Jitter analysis through loop bandwidth adjustment

While the golden PLL solves the compliance test problem to screen out excessive high-frequency jitter, it can present a problem for someone trying to observe all or most of the jitter of a transmitter. A clean jitter free clock trigger allows all the jitter to be observed, but such a signal is not always available. This problem is also solved through a clock extraction circuit with an adjustable loop gain (which controls bandwidth). Reducing the loop BW allows more of the jitter spectrum to be observed. The 83496A clock recovery module has an adjustable loop bandwidth ranging from approximately 50 kHz to 10 MHz (dependent on the data rate). Thus a transmitter can be observed at several loop bandwidth values, allowing different ranges of jitter to be observed. Refer back to Figure 12.

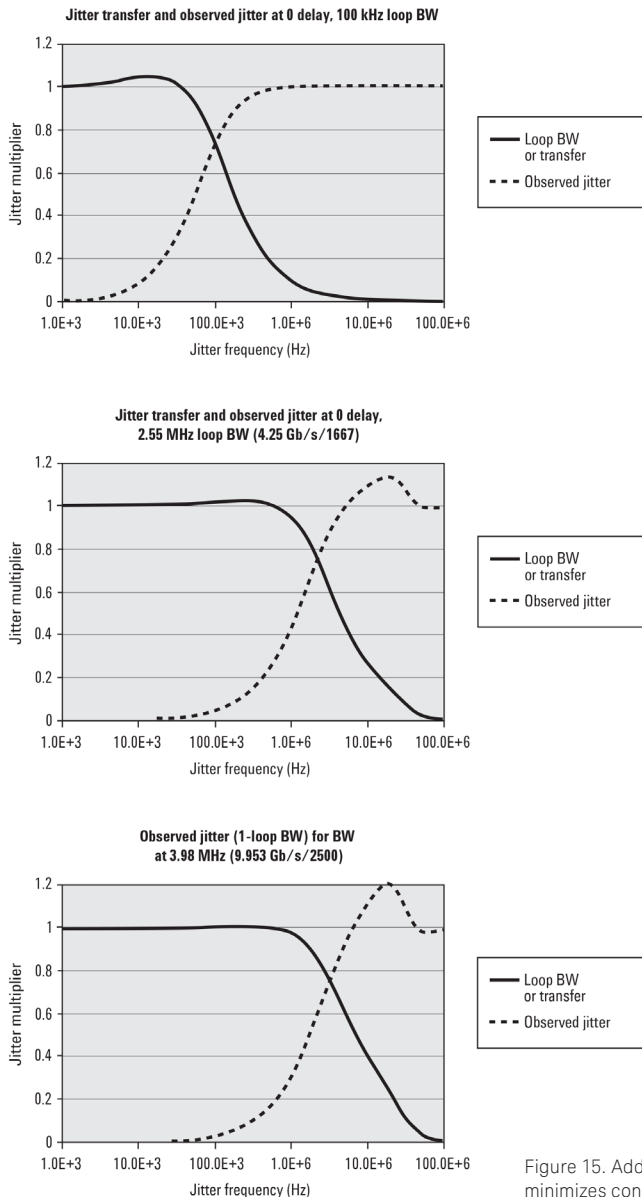


Figure 15. Adding delay in the signal path minimizes constructive interference

The interaction of loop bandwidth, data-dependent jitter, and pattern transition density

It is possible to observe an increase in data dependent jitter when going from a narrow band to a wideband PLL. This is related to the loop bandwidth of the PLL and how the PLL responds to changes in data pattern transition density. If the loop bandwidth is narrow, its response to changes in transition density will be slow. That is, once the PLL has locked to the data stream, it will remain stable even through long runs of ones or long runs of zeroes. The downside of this is a reduced range of periodic jitter that can be tracked out. If the loop bandwidth is increased, more periodic jitter can be tracked. But with a wider loop bandwidth, the PLL gain will self-adjust faster to changes in transition density. The VCO will be corrected to maintain a minimal phase error compared to the data. The 83496A has transition density compensation in its phase detector to minimize this effect.

From the perspective of jitter observed on the DCA, a critical issue is when this correction is applied in the data sampling process. If the delay between the trigger event and the sampling of the data is significant compared to the response time of the PLL (dictated by loop bandwidth), the phase correction may occur out of phase with when the data causing the correction is measured. Thus if there is significant data dependent jitter that fluctuates in its extremes at a rate similar to the fluctuation in transition density, the VCO correction may be applied out of phase with this jitter. The observed jitter may actually be magnified, similar to the effect discussed above for when periodic jitter is observed with sampling delays near the half period of the jitter. The period of the jitter in this case is the pattern length divided by the data rate. The amount of magnification or cancellation is a function of the PLL loop bandwidth, DCA sampling delay, the rate at which transition density fluctuates, and the rate at which the observed jitter manifests its earliest and latest edges. A delay line equal in path length to the DCA delay can help minimize the issue. (24 ns of delay is built in to the data path for the optical version of the 83496A)

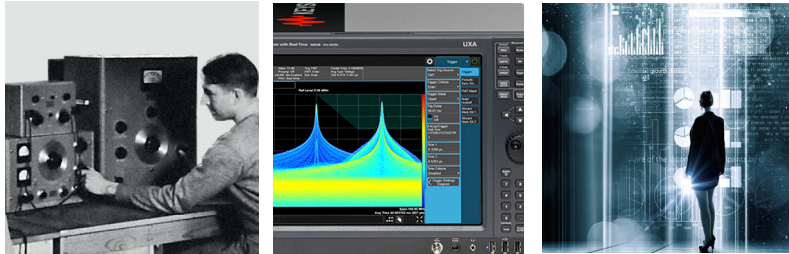
When using a clock extraction circuit for a trigger, the VCO in the PLL must also have extremely low phase noise. Oscillator phase noise and phase detector jitter will be manifested as trigger jitter on the DCA. This jitter is random and not common to the data signal. If the signal being measured were jitter free, it will appear to have jitter if the timing reference signal is corrupted. Using advanced microwave signal source technology, the 83496A VCO provides extremely low residual jitter that is far below 1% RMS of a bit period, even at data rates in excess of 10 Gb/s.

Using clock extraction circuitry provides an easy and effective method to examine high-speed digital transmitters. Depending upon the end use of the transmitter, deriving the clock from the test signal can actually provide a more appropriate test, as the test device can be examined from the perspective of the receiver it will be paired with. It is important to use care when selecting or configuring a clock extraction circuit, as it can have a significant impact on the test results.

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