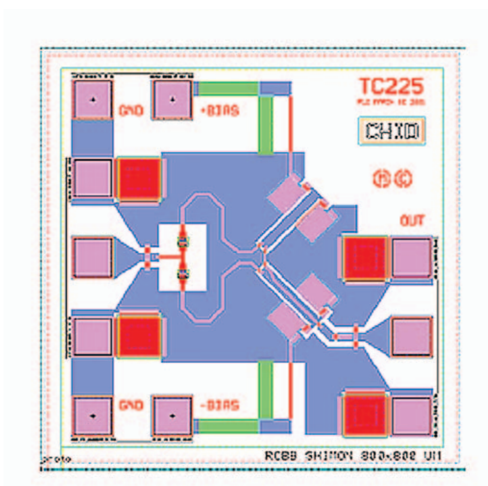
Keysight TC225
40–72 GHz Doubler
1GC1-8048

Data Sheet



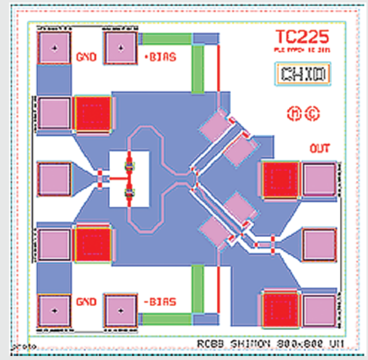
Features

- P_{IN} = + 15 dBm
- Wide Bandwidth:
  40–72 GHz
  Usable to 80+ GHz
- Low Conversion Loss:
  13 dB typical
- Low 1/2 and 3/2 spurs:
  –23 dBc typical

Description

The TC225 is a balanced diode frequency doubler consisting of two Schottky diodes and a coplanar balun structure. The doubler provides 15 dB conversion loss and –17.5 dBc 1st and 3rd order feedthru for input frequencies between 20 and 33.5 GHz.

This IC is fabricated in WPTC's InGaP/GaAs heterojunction bipolar transistor (HBT) process that provides excellent uniformity, reliability and 1/f noise performance.



Chip Size:
760 × 760 µm (29.9 × 29.9 mils)
Chip Size Tolerance:
± 10 µm (± 0.4 mils)
Chip Thickness:
127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:
80 × 80 µm (3.2 × 3.2 mils)

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Min.	Max.	Units
P_{IN}	Input Power:[2]			
	Voltage Bias, V_{dc} = ± 1.5 V		+15	dBm
	Voltage Bias, V_{dc} = ± 1 V		+15.5	dBm
	Current Bias, I_{dc} = ± 9 mA		+15.8	dBm
	Current Bias, I_{dc} = ± 6 mA		+16.3	dBm
V_{DC}	DC Voltage	–1.5	1.5	V
I_{DC}	DC Current	–9	9	mA
T_A	Backside Temperature[3]	–55	75	°C
T_{max}	Maximum Assembly Temperature[4]		300	°C
T_{stg}	Storage Temperature	–65	165	°C

1. Operation in excess of any one of these conditions may result in permanent damage to this device. T_A=25°C except for T_{max}, and T_{stg}.
2. Most doubler users operate the device at or near P_{max}. Therefore, we have given maximum power for voltage biasing and current biasing. See the notes for discussion of tradeoffs involved.
3. For MTTF> 10^6 hours. Operation in excess of T_A will degrade MTTF.
4. Sixty–second maximum.

DC Specifications/Physical Properties[1]

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
I_{DC+}	DC Current in Positive Port (+1V bias)	5.9	6.5	7.1	mA
I_{DC-}	DC Current in Negative Port (–1V bias)	–7.1	–6.5	–5.9	mA

1. Measured on wafer with T_{chuck} = 25°C, V_{DC+} = +1V, V_{DC} = –1V, Z_0 = 50Ω.

RF Specifications[1]

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units[2]
BW	Guaranteed Bandwidth (doubled frequency)	40		72	GHz
CL	Conversion Loss, F_{IN} = 20–32 GHz		13	15	dB
	Conversion Loss, F_{IN} = 36 GHz		14.2	16	dB
FT	Feedthrough (1/2) Suppression, F_{IN} = 20–32 GHz		–23	–20	dBc
	Feedthrough (1/2) Suppression, F_{IN} = 36 GHz		–20.8	–17.5	dBc
SP	3/2 Suppression, F_{IN} = 24 GHz		–24.5	–17.5	dBc

1. Measured on wafer with T_{chuck} = 25°C, V_{DC+} = +1V, V_{DC} = –1V, Z_0 = 50Ω.
2. dBc values referenced to P_{sat}.

Applications

The TC225 is a general–purpose frequency doubler IC suitable for a variety of millimeter–wave source applications.

Biasing

DC bias is applied to the diodes through two bias pads. A symmetric (±1V) scheme is preferred because it results in 0V at the dc–coupled input port. With the addition of an external coupling capacitor at the input port, an asymmetric (+2V, 0V) scheme is also acceptable for those applications that require a single–polarity supply. DC bias improves the conversion performance of the TC225 and greatly expands the range of input powers over which the doubler is approximately linear.

Designs requiring high input power may be interested in other biasing schemes. We have found that conversion loss ripple vs. frequency may be reduced by increasing to a ±3V bias, although there is some reduction in maximum allowed output power. To maximize output power, a current source at 6–9 mA may be used instead of the voltage source to reduce self–biasing. The value of the current source affects match, and can be chosen to minimize conversion loss ripple.

It is possible to maximize output power by eliminating DC bias altogether. This will affect input match at lower powers and reduce power linearity.

Operation

The TC225 consists of two identical Schottky diodes and a coplanar transmission–line balun oriented in an anti–parallel/ series configuration. The diodes' nonlinear I/V characteristics generate harmonics of the input signal. The balanced topology separates these harmonics by suppressing even harmonics at the input port and odd harmonics at the output port. This configuration results in good conversion performance and low 1/2 and 3/2 spurious levels without the need for external filtering. For best performance, the input signal should have low harmonic and sub–harmonic and sub–harmonic content.

Assembly Techniques

Epoxy die–attach using a conductive epoxy and solder die– attach using a fluxless gold-tin solder preform are both suitable assembly methods. The IC must be attached to an electrically conductive surface that forms DC and RF ground for the circuit. Gold wire mesh bonds (500–line/inch or equivalent) should be used at the RF input and output ports. These bonds must be kept as short as possible to minimize parasitic inductance. DC bias may be supplied through conventional 0.7–mil gold wire bonds. In both cases, thermosonic wedge bonding is recommended.

GaAs MMICs are ESD sensitive. MMIC ESD precautions, handling considerations, and die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Additional References

Keysight Technologies Application Note #54 (5991-3484EN), *"GaAs MMIC ESD, Die Attach and Bonding Guidelines*" provides basic information on these subjects.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications.

In this data sheet the term typical refers to the 50th percentile performance. For additional information contact Keysight WPTC Marketing at 1-707-577-4482.

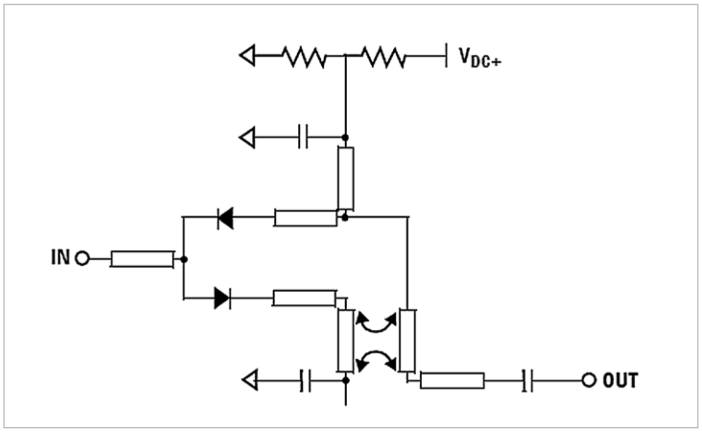


Figure 1. TC225 Schematic

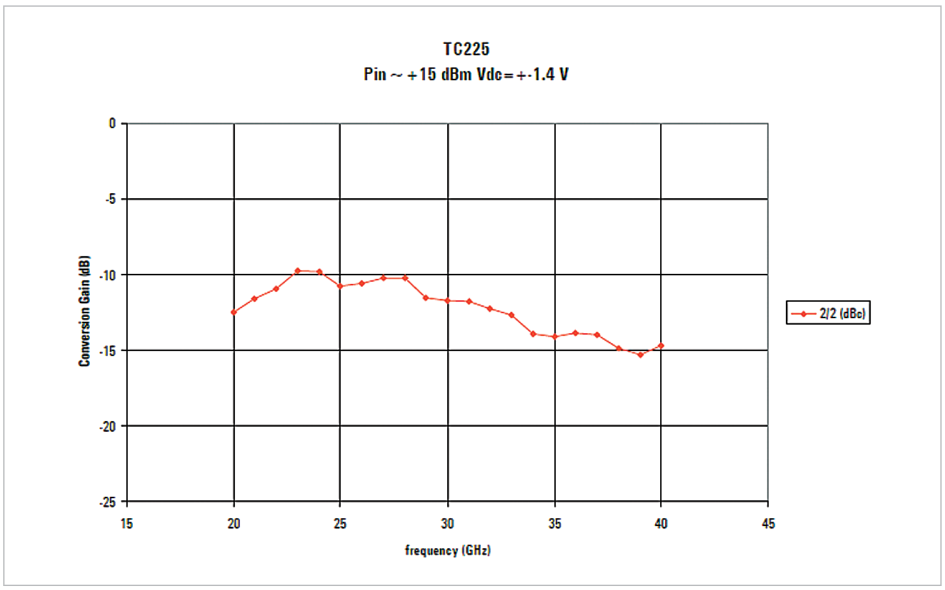


Figure 2. 1GC1-8048 Conversion Loss vs. Input Frequency

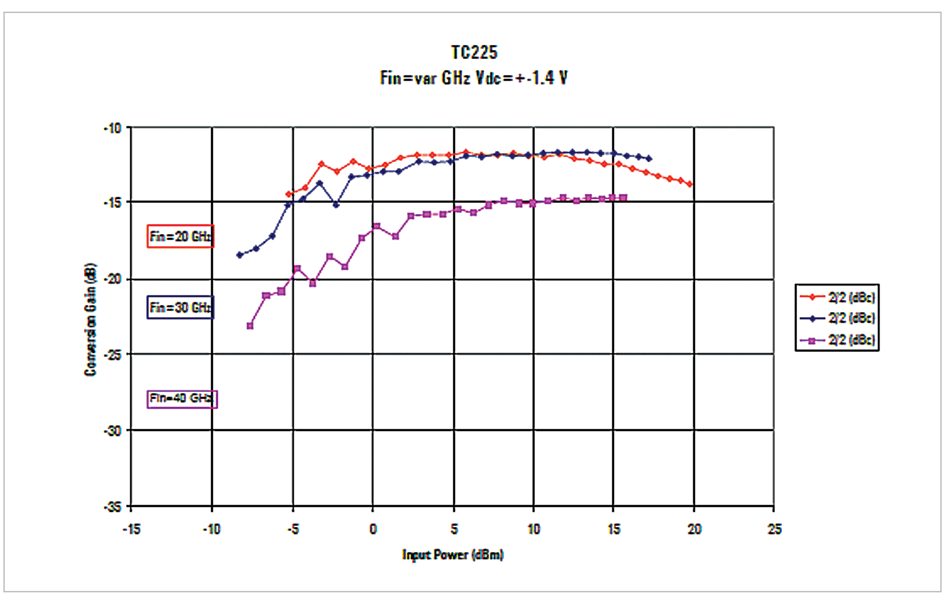


Figure 3. 1GC1-8048 Conversion Loss vs. Input Power

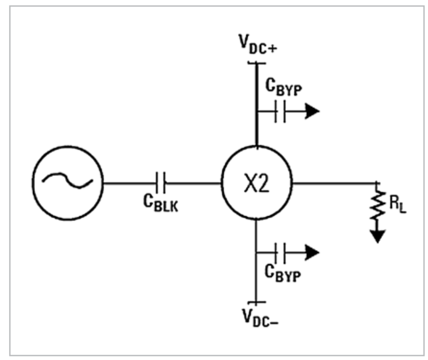
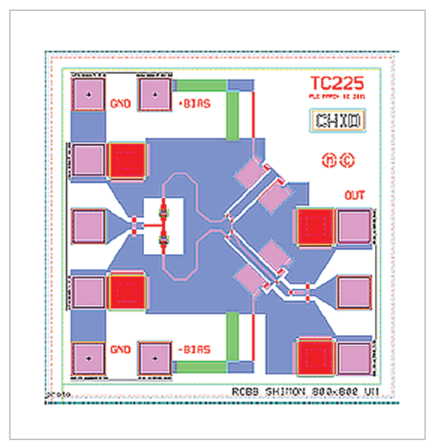


Figure 4. 1GC1-8048 Biasing



Pad Locations

	X	Y
IN	80	380
OUT	680	230
V_{DC+}	230	680
V_{DC-}	230	80

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