CASE STUDY

Wire Bond Integrity Tester for Post-Mold Inspection in High-Volume Semiconductor Assembly

Keysight s8050 inline wire bond validation and defect screening, optimized for IDM and OSAT production lines

KEYSIGHT

Introduction

In the rapidly evolving semiconductor industry, wire bond deformations pose risks to Integrated Circuits (ICs), particularly in mission-critical applications where failure is not an option. The Keysight s8050 Electrical Structural Tester (EST) is designed to screen post-molded packages for wire bonding deformation using a capacitive testing approach mainly targeting QFP and QFN type of packages. It introduces a high-volume production tester compatible with third-party handlers, including both Strip and Pick-and-Place (PNP). This enables the electrical screening of physical deformations in wire bonding in a high-throughput manner for the assembly line with extended capability for SECSGEM integration.

The customer is an advanced semiconductor and test manufacturing service provider, specializing in testing, assembly, and packaging. They encountered issues with defective ICs bypassing traditional open and short tests due to wire bonding defects, such as near-shorts and sagging wires. This issue led to multiple lots being put on hold. To address this problem, Keysight has collaborated with the customer to integrate the s8050 into their assembly process, enhancing their screening yield.

Organization

- A globally renowned independent provider of semiconductor manufacturing services.
- Specializes in packaging, assembly, and testing.
- Houses thousands of wire bonders for the assembly line.

Challenges

- Defective ICs escaping the assembly inspection.
- Inability to detect near-shorts, wire sag, and other wire bond deformations.
- Mainly Quad Flat Package (QFP) with a single die, ranging from simple to complex bond wire configurations.

Solutions

- s8050 Electrical Structural Tester
- Post-mold s8050 inspection

Results

- Seamless integration and compatibility with strip and PNP handlers with modifications to the change kit.
- High test throughput of up to 5,000 to 6,000 UPH.
- Fast test development and automated limits generation.
- SECS/GEM MES Integration of the s8050 into existing production workflows.

Test Challenges

For many decades, few technologies in IC assembly have endured as reliably as wire bonding. Generally, assembly defects account for 12% to 15% of semiconductor customer returns in the automotive chip market. (Meixner, 2022) Studies further indicate that 25% to 33% of package failures are attributed to wire bonding issues. (Zhou et al., 2023).

The customer, a manufacturer that specializes in assembly and testing services, is currently facing challenges related to wire bond defects. To meet the industry's growing demand for faster, smaller, and higher-performance chips, the manufacturer has consistently prioritized the structural reliability of its packages. However, they are struggling with a volume of post-Mold ICs that exhibit wire bonding deformation, which hinders their escape from the assembly line. Undetected IC deformation, such as near-shorts and wire sag, often goes undetected in traditional detection procedures, leading to costly latent failures and ultimately increasing Customer Returns (CRs).

The common screening process for detecting these defects includes Open and Short (OS) testers and Automated X-ray Inspection (AXI) systems. Despite their widespread use, a significant number of lots still fail during final functional testing or are returned by customers, indicating that current detection methods may not adequately identify wire bond deformations. OS testers are unable to detect physical structural defects in wire bonds, as these types of deformations cause minimal changes in electrical parameters. The inconsistency in defect detection, especially for near-shorts and wire sag, increases the risk of undetected issues that can compromise the functionality and reliability of semiconductor devices. The industry's heavy reliance on a sampling approach using AXI means that not all ICs undergo testing. Consequently, there is a higher probability that defects will escape this screening process, leaving the manufacturer vulnerable to latent failures in their products, unless they establish a full lot AXI at the expense of a subsequent increase in Cost per Unit.

The Solution

Given the importance of this gap in today's screening process, the customer has recognized the need for a post-mold wire bonding screening process. Deploying the s8050 post-assembly and prior functional testing is essential for identifying alterations in the overall metallic structure, such as vertical sag wires, offset lead frame, and paddle. These defects, which may go unnoticed by X-ray inspection and other testing methods, fall within the s8050's specialized detection capabilities.

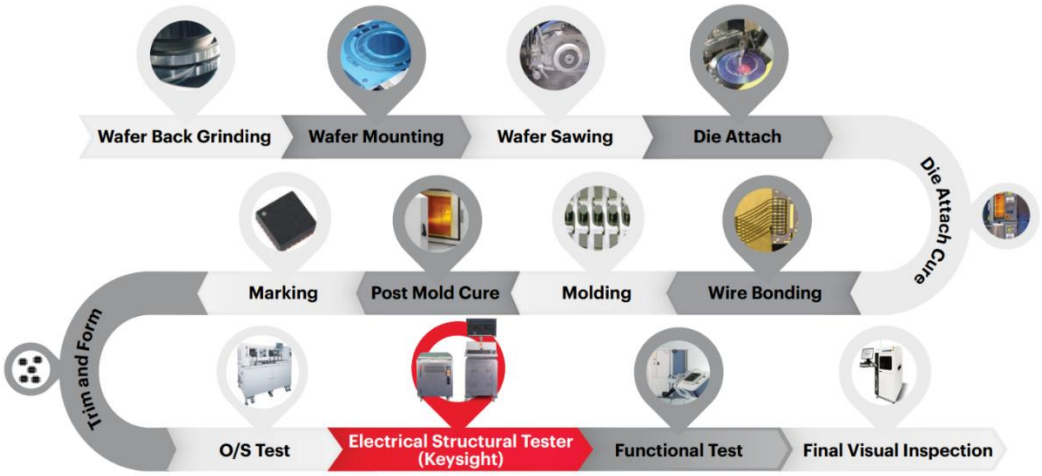

Figure 1. The EST is a post-mold electrical testing process designed to ensure assembly integrity by detecting deformations following the open and short testing phase.

The s8050 is designed as a screening station with high parallelism, optimized explicitly for high-volume wire-bonded package testing using nVTEP technology, enabling the rapid detection of regions in the DUT with massive wire-bonding deformations. For cases where defect classification is required, X-ray inspection provides an additional layer of analysis by closely examining pins that exceed their specified limits, complementing the s8050's precise defect detection capabilities.

How does the s8050 EST capture wire bond defects?

The s8050 Electrical Structural Test System utilizes the Nano Vectorless Test Enhanced Performance (nVTEP) technology, a non-destructive capacitive tester designed for high-volume testing to rapidly detect regions in the device under test (DUT) with significant wire bonding deformations. The s8050 utilizes a capacitive coupling principle to detect electrical outliers, which can be categorized as near-shorts, sagged wires, swept wires, and other defects in wire-bonded packages. With fast test time for scanning each IC pin, the s8050 is an ideal post-mold screening station within the assembly line. Its high-throughput capability allows for the testing of up to 20 sites in parallel, achieving a test time of just 0.9 seconds per site, evaluated with each site having a 100-pin DUT. When constrained by a handler index time of approximately 3 seconds, the s8050 can scale up to an exceptional 18,000 Units Per Hour (UPH) in an optimal setup.

Handler compatibility

The s8050 is compatible with various handler vendors, such as strip and pick-and-place handlers, through the incorporation of an nVTEP sensor plate within its change kit. The s8050 system interfaces with the handler driver via the General-Purpose Interface Bus (GPIB) protocol, enabling operational control while supporting the SEMI Equipment Communication Standard (SECS/GEM), which establishes a connection to the Manufacturing Execution System (MES) throughout the entire production process. Keysight provides field engineering support to facilitate overall integration and collaboration with handler vendors, ensuring a higher success rate for sensor plate integration.

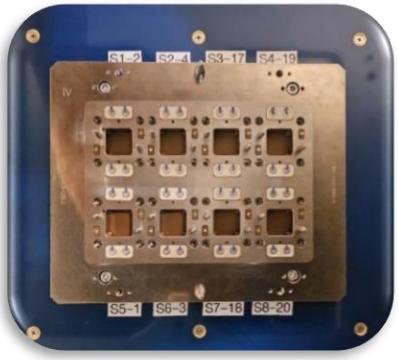

Figure 2. High-Density Test Site: Designed for parallel testing of multiple semiconductor devices to enhance throughput and efficiency.

One of the key features of the s8050, **Automated Test Program Generation**, reduces test development time by automatically assigning test resources sequentially based on the hardware configuration and generating test blocks without requiring Object-Oriented Project coding expertise, thereby enhancing operational adaptability.

Figure 3. nVTEP Measurements Chart: Monitoring electrical structural test data to detect anomalies and ensure compliance with test limits.

Its **Automated Limits Generation** algorithm, **Auto Debug,** utilizes Six Sigma methodologies and requires only a minimum of 10 Known Good Units (KGUs), although Keysight recommends 100 KGUs for more accurate limits. All 100 KGU must be free of wire bonding defects. This method is time-efficient for characterizations and initial limit setting. Users can remove failing data points within the s8050 environment. Advanced users can use Standard Test Data Format (STDF) tools for data processing and then reimport the STDF into s8050 to generate limits based on the selected data points.

Enhancing production yield with adaptive statistical testing (DPAT, RPAT, and MaRT)

The Dynamic Part Averaging Test (DPAT) algorithm in the s8050 plays a crucial role in identifying abnormal wire bond variations that may indicate electrical or non-electrical defects in ICs. The system employs continuous statistical analysis to monitor production, establish dynamic limits, and identify outliers in each lot, utilizing either the traditional mean and standard deviation or the AECQ-001 Robust Sigma approach. The user can configure the number of deviations for which DPAT limits will be applied for both upper and lower limits.

Figure 4. Real-time Part Averaging Test (RPAT) in Action: Adaptive statistical analysis optimizing test limits to improve yield and detect outliers.

A further enhancement, the Real-time Part Averaging Test (RPAT), modifies DPAT by continuously adjusting test limits in real-time as testing progresses, enabling more adaptive and precise control of the test process. Another feature, the Marginal Retry Test (MaRT), applies a one-sided hysteresis to test limits, effectively creating a guard band to handle marginal test results and retest them immediately without the need for replunging the device. This minimizes false failures by allowing transient or borderline cases additional opportunities to pass, improving overall test accuracy and yield.

The user can define the limits based on the lot characterization of Known Good Units (KGU). These units are those without any wire bonding deformations. Any measurement outliers indicate a physically displaced wire positioned farther from the central region of the KGU distribution. This shift can originate from the measured pin or an adjacent one, typically resulting in wire bond deformations such as sagging or sweeping. The lot-to-lot variations are negligible; however, if there are significant changes within the wire bonding recipe, this will be reflected in a measurement shift, failing to meet the established limits.

Production Integration

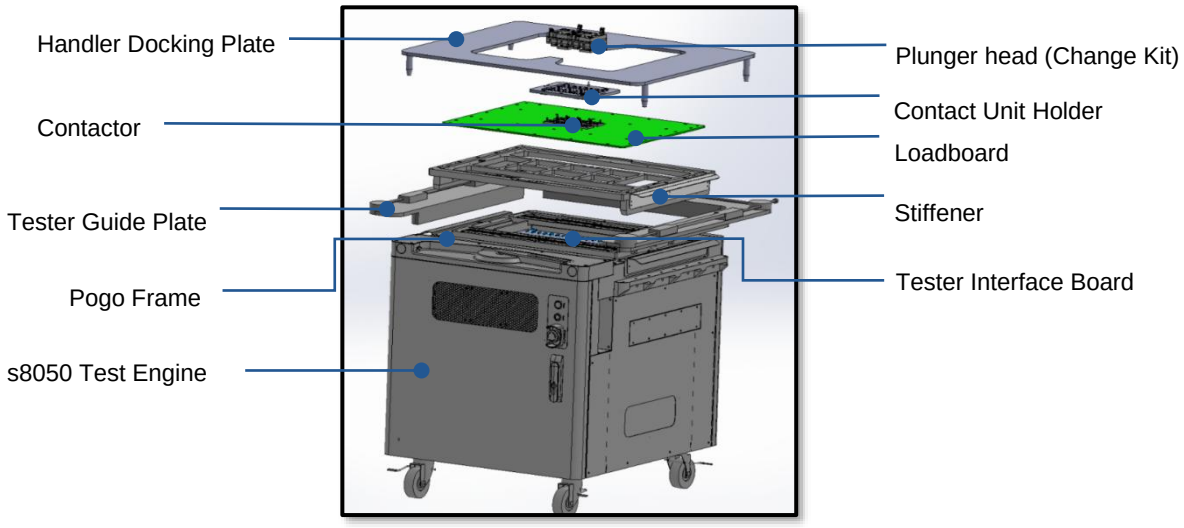

Figure 5. s8050 stack-up

An overall system integration for both the s8050 tester and the handler was deployed in a production environment as a screening station for post-mold IC assembly testing. The integration began with a Gage Repeatability and Reproducibility (GRR) evaluation to ensure measurement consistency and validate the system's reproducibility before it was released to manufacturing.

Upon receiving all the required fixtures listed in the s8050 stack-up, the evaluation began with manual testing to debug and verify the functionality of each fixture. With a set of correlation units, all fixtures passed the manual test evaluation. However, challenges emerged during handler testing in achieving an acceptable GRR. It was found that although instrument variation remains within a stable measurement, the setup variation intermittently failed. Root cause analysis shows an inconsistency in measurements taken from repeatedly testing the same DUT through multiple re-plugins with the same chuck or plunger head.

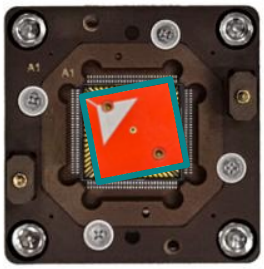

Figure 6. The misalignment between the DUT and the socket.

The team has successfully addressed this issue by stabilizing the design of the plunger head. At this point, GRR was successfully achieved across all 8 sites, effectively minimizing the setup variations and improving reproducibility. To define test limits, a set of Known Good Units (KGU) was run, and the limits were generated using the Auto Debug feature. As a final validation step, a mini bulk run was conducted before transitioning to full-scale production. The s8050 achieved an average throughput of approximately 5,500 units per Hour (UPH).

The Result

The post-mold s8050 implementation reduced the lot rejection rate from 32% to 1% in five months and eliminated 75% of field returns related to package structural faults. This improvement highlights the s8050's effectiveness in optimizing screening yield, enhancing manufacturing efficiency, and improving product reliability.

Feedback and impression

The customer is highly satisfied with the system's ability to conduct comprehensive testing on all sites, ensuring a thorough evaluation of the product before it progresses to the next stage. The high-speed performance of the s8050 enables rapid testing, allowing for the quick identification of wire bond defects as either pass or fail, by reducing testing times, increasing throughput, and processing larger volumes of components without sacrificing accuracy.

Summary

The s8050 Electrical Structural Tester is a highly efficient screening solution tailored for high-volume manufacturing. Optimized for testing wire-bonded packages leveraging nVTEP technology. When paired with an octal site PNP handler, UPH can easily range between 5,000 and 6,000 UPH. The design of a stable nVTEP Sensor Plate integration is pivotal to enabling an acceptable GRR.

The s8050 enables the rapid identification of regions in the DUT with significant wire bonding deformations. For cases where defect classification is required, X-ray inspection provides an additional layer of analysis by closely examining pins that exceed their specified limits, complementing the s8050’s precise defect detection capabilities. This new approach in screening post-Mold ICs as early as assembly testing will help enable a higher yield in the production process.

Reference

Meixner, A. (2022, June 7). *The Race To Zero Defects In Auto ICs. Semiconductor Engineering*. https://semiengineering.com/the-race-to-zero-defects-in-auto-ics/

Zhou, H., Zhang, Y., Cao, J., Su, C., Li, C., Chang, A., & An, B. (2023). *Research Progress on Bonding Wire for Microelectronic Packaging*. *14*(2), 432–432. https://doi.org/10.3390/mi14020432

For more information

Ready to discover more about Keysight's electrical structural tester? Go to www.keysight.com/find/EST

To learn more about wire bond testing, check out the Wire Bond Electrical Structural Test Methodologies white paper.