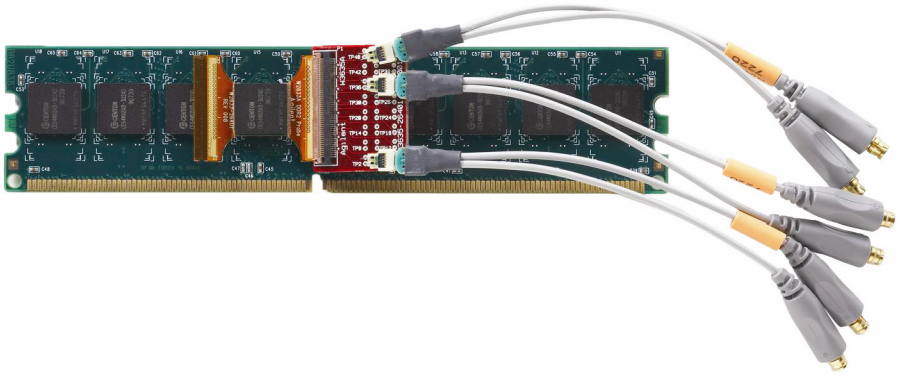
Keysight Technologies

DDR Memory Design and Test Overview



KEYSIGHT TECHNOLOGIES

Double Data Rate (DDR) Synchronous Dynamic Random Access Memory (SDRAM) is being implemented broadly in computing platforms and embedded applications. The overwhelming concern for developers of these products is interoperability. It starts with the physical layer where the data is transferred on both the rising and falling clock edges, to the functional test of read-to-write timing. Tools to validate the parametric and protocol aspects of these designs are required to understand if your design is in compliance, and how close design performance is to specification. DDR technology is implemented in several forms today -- DDR (also called DDR1), DDR2, DDR3, DDR4, and low-power DDR (LPDDR1, LPDDR2, and LPDDR3) targeted for mobile devices. Specifications are defined by the Joint Electronic Devices Engineering Council (JEDEC), but it's up to designers to guarantee compliance.

Key tasks

DDR design can be segmented into four areas: interconnect design, active signal validation, protocol validation, and functional test. While JEDEC defines the specifications, you are required to verify compliance. With no formal verification labs or test centers, you must decide the appropriate procedures, methods and equipment to perform these compliance tests. Keysight Technologies, Inc. offers solutions in each area for electrical physical layer, protocol layer, and functional test.

Keysight Gets Involved, You Benefit

Keysight's solutions for digital applications are driven and supported by Keysight experts that are involved in the various international standard committees. We call it the Keysight Digital Test Standards Program. Our experts are active in the Joint Electronic Devices Engineering Council (JEDEC), PCI Special Interest Group (PCI-SIG®), Video Electronics Standards Association (VESA), Serial ATA International Organization (SATA-IO), USB-Implementers Forum (USB-IF), Mobile Industry Processor Interface (MIPI) Alliance, and many others. Our involvement in these standards groups and their related workshops, plugfests, and seminars enables Keysight to bring the right solutions to the market when our customers need them.

DDR standard	DDR1	LPDDR1 or mobile DDR1	DDR2	LPDDR2 or mobile DDR2	DDR3	LPDDR3 or mobile DDR3	DDR4
Specification	JESD79E	JESD209	JESD79-2E, JESD208	JESD209-2B	JESD79-3C	JESD209-3	JESD79-4
Operating voltage	1.5 - 3.3V	1.8V	1.8V	1.6B	1.5V	1.2V	1.2V
Clock frequency	100 - 200 MHz	100 - 200 MHz	200 - 400 MHz	100 - 533 MHz	400 - 800 MHz	667 - 800 MHz	800 - 1600 MHz
Data transfer rate	200 - 400 MT/s	200 - 400 MT/s	400 - 800 MT/s	200 - 1066 MT/s	800 - 1600 MT/s	1333 - 1600 MT/s	1600 - 3200 MT/s
Package type	This Small Outline Package (TSOP)	Fin Ball-Grid Array (FBGA)	Fin Ball-Grid Array (FBGA)	Fin Ball-Grid Array (FBGA)/ POP	Fine Ball-Grid Array (FBGA)	POP	Fine Ball-Grid Array (FBGA)
Package size	x4, x8, x16, x32	x16, x32	x4, x8, x16	x16, x32	x4, x8, x16	x16, x32	x4, x8, x16
Bacward compatibility	No	Yes, with DDR	No	Yes, with DDR2	No	No	No

Table 1. DDR technologies and key JEDEC specifications

Physical Layer: Active Signal Validation

Validating DDR performance involves characterizing the clock and data signals. A big challenge is separating the read and write signals on the bidirectional bus. The ability to trigger properly will allow you to analyze the complex traffic on the DDR data bus.

Measure with confidence

Keysight's Infiniium 90000 Series oscilloscopes provide the lowest noise floor, jitter noise floor, and trigger jitter in the industry, enabling more accurate characterization of your design. InfiniiScan provides zone triggering, enabling the oscilloscope to separate read and write cycles based on the distinctive pattern of the waveform.

Automate complex tasks

The Keysight DDR electrical performance
compliance software runs on the 90000 Series oscilloscopes, simplifying set up and performing compliance tests. With versions for DDR1, DDR2 and DDR3, the software provides busy engineers quick, accurate answers.

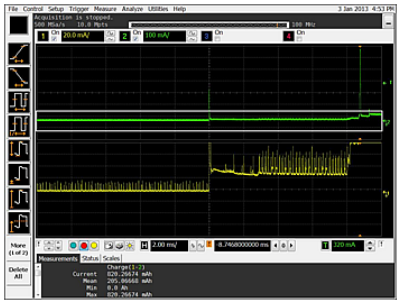


Figure 1: Make tests quickly with the Keysight DDR electrical test software.

Physical Layer: Interconnect Design

As data rates increase, designers need to minimize signal integrity problems. To avoid signal attenuation, rise-time degradation, and jitter caused by long trace lengths, designers need tools like those used by high-frequency engineers.

Accurate impedance measurements

The Keysight 86100C Infiniium DCA-J with the 54754A differential TDR/TDT module makes quick work of interconnect analysis. It utilizes a unique calibration process to remove the effects of cabling, allowing you to isolate your device from the test system and view results in time or frequency mode.

Predict interconnect performance through simulation

The Keysight Advanced Design System (ADS) has several features optimized for high-speed digital design. Design guides provide a quick vehicle to start a DDR design. Analyze complete serial links by simulating at the circuit or system level. Make analyses quickly with oscilloscope-like displays.

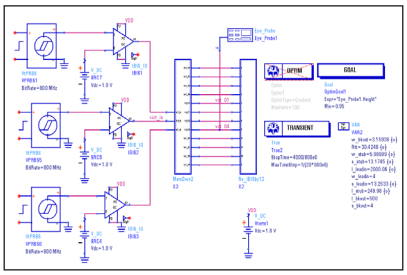


Figure 2: Simulate for optimum performance using ADS.

Protocol Layer

You want to validate that your system is sending the correct DDR commands, that memory banks are addressed properly, and find any protocol violations. You will need to view read and write data signals at several levels of abstraction – from binary to protocol.

Decoding DDR signals

The Keysight U4154A logic analyzer allows the read and write data to be sampled at different times, and viewed separately. With the B4621A memory bus decoder, you can trigger on system attributes like burst length, CAS, and chip selects to decode key bus signals. The intuitive results display provides quick interpretation.

Automate complex tasks

The Keysight protocol compliance protocol compliance and analysis tool complements the 16900 Series logic analyzer by simplifying set-up and performing protocol decode and compliance tests. It runs on the logic analyzer, and produces quick, accurate answers.

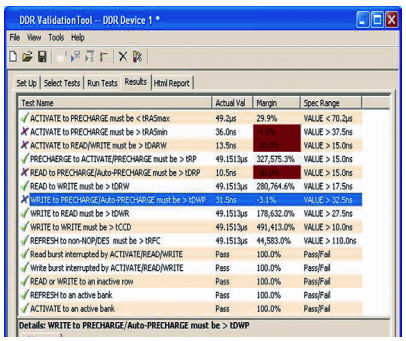


Figure 3: Automate protocol tests with the B4622A software.

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Functional Test

Validating system performance requires properly triggering on the data bus or a specific memory address to ensure there are no timing, state or protocol violations. You need to analyze the DDR system behavior – are some commands being executed too often?

Validating system performance

The Keysight DDR protocol compliance and analysis tool automates deep DDR bus trace acquisition and analysis of the Keysight 16900 Series logic analyzer to quickly identify timing and protocol problems. It checks timing and state violations, then produces an HTML report and margin analysis to determine how close you are to the specification.

How robust is your design?

You meet all the timing and protocol specifications, but how does your design tolerate errors? The Keysight B4622A DDR2/3 protocol compliance and analysis tool provides a quick overview of DDR bus performance with statistic and histogram views for bus optimization.

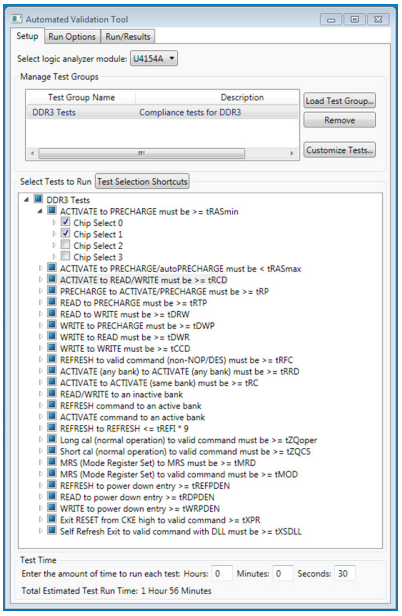

Figure 4: Analyze bus utilization of read and write commands with the B4622B software.

Probing DDR Memory

When you characterize or validate your DDR design, are you measuring the right signal? The JEDEC standards apply only at the BGA balls of the DRAMs, but in many cases these are difficult to access since many vias do not go through the board.

Probing specific signals

The Keysight InfiniiMax active probes are high-impedance, low capacitance probes that are minimally invasive to your signals. The solder-in probe head lets you easily solder to vias and quickly look at a signal.

Probing the data bus

To do a complete functional test, you need to measure the DDR bus. The Keysight Soft Touch logic analyzer probes can be used by just routing the traces in a specific manner. Their unique design makes solid contact with the traces without a connector.

Or use the Keysight DDR slot interposer, connecting directly to the standard DDR DIMM connector. The non-intrusive design lets you measure the full command, address, control and data bus signals.

A better way – BGA probe adapters

Probe all DDR signals right at the BGA balls using the Keysight DDR2 and DDR3 BGA probe adapters. The BGA signals are routed to the top of the adapter, so oscilloscope and logic analyzer probes can access them. The traces have the same length to reduce skew issues. Using an oscilloscope and logic analyzer, perform parametric and functional measurements using the same BGA probe.

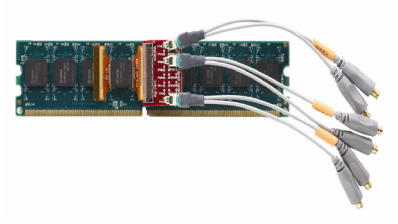

Figure 5: Using an InfiniiMax active differential solder-in probe.

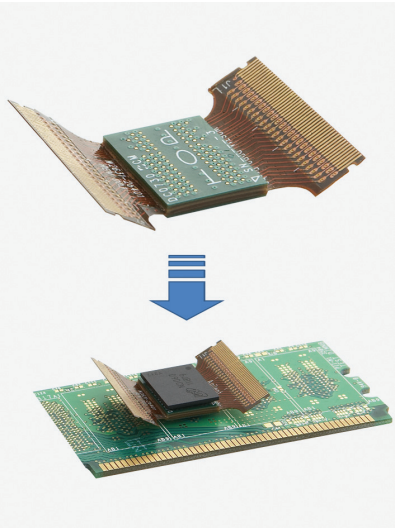

Figure 6: Using a DDR2 BGA probe adapter.

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Keysight DDR Design and Test Solutions

Table 2. Keysight DDR solutions by DDR technology (* Supported by FuturePlus Systems Corporation)

Product	Description	Technology supported				
	Physical layer	**DDR2**	**DDR3**	**DDR4[1]**	**LPDDR2**	**LPDDR3[1]**
DSA90254A or DSO9254A	2.5 GHz Infiniium oscilloscope					
DSA90404A or DSO9404A	4 GHz Infiniium oscilloscope	X			X	
DSA90804A	8 GHz Infiniium oscilloscope	X	X	X	X	X
U7233A	DDR1 electrical compliance test application					
N5413B	DDR2 and LPDDR2 electrical compliance test application	X			X	
N6462A	DDR4 electrical compliance test application			X		
U7231A	DDR3 electrical compliance test application		X			X
N5414A	InfiniiScan event identification software	X	X		X	
1131A	3.5 GHz InfiniiMax differential probe amplifier					
1132A	5 GHz InfiniiMax differential probe amplifier	X			X	
1134A/1168A/1169A	7/10/13 GHz InfiniiMax differential probe amplifier	X	X	X	X	X
W2212B	ADS Design Software bundle (ADS Core, Transient Convolution, Layout, Momentum G2, EMDS, Ptolemy)	X	X		X	
86100C, 54754A	DCA-J Infiniium oscilloscope with TDR module	X	X		X	
	Protocol/functional test	**DDR2**	**DDR3**	**DDR4[1]**	**LPDDR2**	**LPDDR3[1]**
16902B	Logic analyzer mainframe	X	X	X	X	X
16950B or 16951B	68-channel, 667 MHz, logic analysis module	X		X	X	
16962A	68-channel, 2 Gb/s, logic analysis module	X	X	X	X	X
B4621B	DDR2/3/4 memory bus decode software	X	X	X		X
B4622B	DDR2/3/4 and LPDDR2/3 protocol compliance and analysis tool	X	X	X		X
B4623B	LPDDR2/3 protocol compliance and analysis tool					
N4834A or N4835A	DDR3 midbus probe or advanced slot interposer		X			X
	BGA probes	**DDR2**	**DDR3**	**DDR4[1]**	**LPDDR2**	**LPDDR3[1]**
W2631A or W2633A	DDR2 x16 BGA command and data probe for logic analyzer and oscilloscope	X		X		
W2632A	DDR2 x16 or x8 BGA data probe for logic analyzer and oscilloscope	X		X		
W2634A	DDR2 x8 BGA data probe for logic analyzer and oscilloscope	X		X		
W2635A or W2636A	DDR3 x8 or x16 BGA oscilloscope probe		X			X
W2637A or W2638A	LPDDR x16 or x32 BGA probe for oscilloscope and logic analyzer					
W2639A	BGA oscilloscope probe adapter board	X	X	X		X
W3631A or W3633A	DDR3 x16 or x4/x8 BGA probe for logic analyzer and oscilloscope		X			X

Note 1: Please contact Keysight representative for LPDDR2, LPDDR3, DDR4 BGA probe information.

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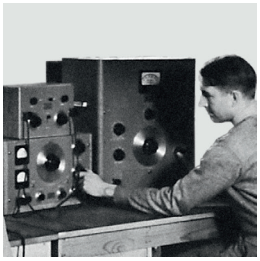

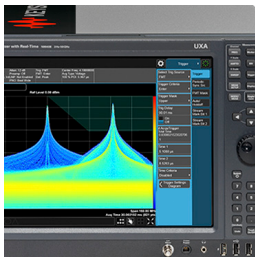

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