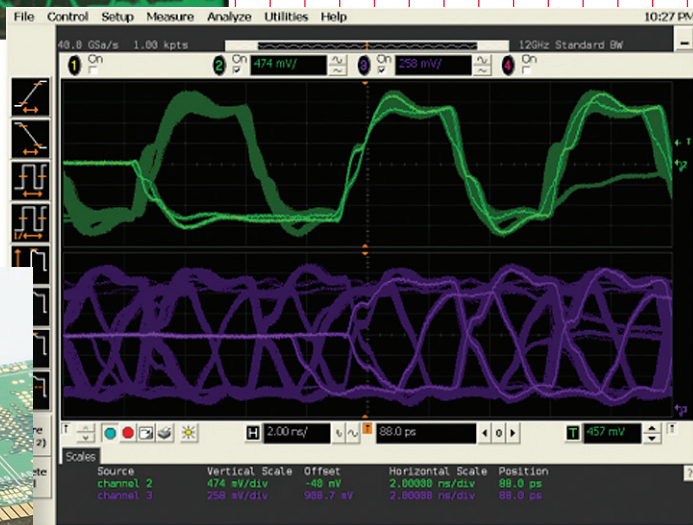
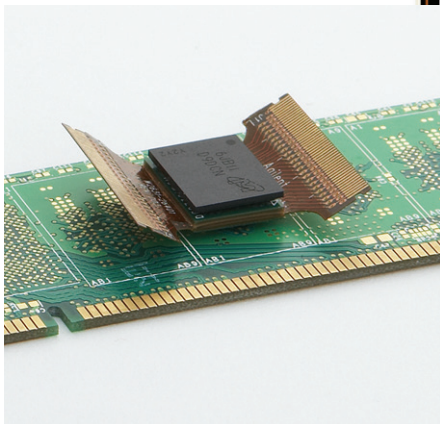
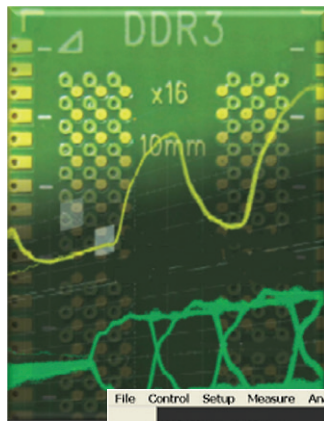


Keysight Technologies

DDR Memory Design and Test – A Better Way

Thoroughly Characterize and
Validate DDR Memory Designs



New Challenges

Double data rate (DDR) memory is being implemented broadly in computing platforms and embedded applications. The overwhelming concern for developers of these products is interoperability. It starts with the physical layer where the data is transferred on both the rising and falling clock edges, to the functional test of read-to-write timing. You need tools to validate the parametric and protocol aspects of your designs to make sure your design is in compliance, and to see how close design performance is to specification.

When you can gain insight to your design early in the design cycle, you can take

corrective action quickly to make sure you meet product quality and time-to-market goals. Keysight Technologies, Inc. design and test solutions can provide these insights to help you make the right decisions at key moments.

DDR technology is implemented in several forms today -- DDR (also called DDR1), DDR2, DDR3, DDR4, and low-power DDR (LPDDR1, LPDDR2, and LPDDR3) targeted for mobile devices. Specifications are defined by the Joint Electronic Devices Engineering Council (JEDEC) (see Table 1), but it's up to you to guarantee compliance.

With each advance of DDR, the rising data rates bring new design and test challenges. The higher clock frequencies increase signal integrity symptoms like reflections and crosstalk, causing signal degradation and logic issues. A shorter clock cycle means a smaller jitter budget, so reducing jitter is far more complex. The higher bandwidth requirements need quality probing techniques to ensure the probe isn't significantly degrading the signal. And lower voltage swings require measurements to be made with very low noise.

Table 1. DDR technologies and key JEDEC specifications

DDR standard	DDR1	LPDDR1 or mobile DDR1	DDR2	LPDDR2 or mobile DDR2	DDR3	LPDDR3 or mobile DDR3	DDR4
Specification	JESD79E	JESD209A	JESD79-2E, JESD208	JESD209-2B	JESD79-3C	JESD209-3	JESD79-4
Operating voltage	1.5-3.3V	1.8 V	1.8 V	1.6B	1.5 V	1.2V	1.2V
Clock frequency	100-200 MHz	100-200 MHz	200-400 MHz	100-533 MHz	400-800 MHz	667-800 MHz	800-1600 MHz
Data transfer rate	200-400 MT/s	200-400 MT/s	400-1066 MT/s	200-1066 MT/s	800-1600 MT/s	1333-1600 MT/s	1600-3200 MT/s
Package type	This Small Outline Package (TSOP)	Fin Ball-Grid Array (FBGA)	Fin Ball-Grid Array (FBGA)	Fin Ball-Grid Array (FBGA)/POP	Fine Ball-Grid Array (FBGA)	POP	Fine Ball-Grid Array (FBGA)
Package size	x4, x8, x16, x32	x16, x32	x4, x8, x16	x16, x32	x4, x8, x16	x16, x32	x4, x8, x16
Backward compatibility	No	Yes, with DDR	No	Yes, with DDR2	No	No	No

Key tasks

DDR design can be segmented into four areas: interconnect design, active signal validation, protocol validation, and functional test. While JEDEC defines the specifications, you are required to verify compliance. With no formal verification

labs or test centers, you must decide the appropriate procedures, methods and equipment to perform these compliance tests. Keysight offers solutions for electrical physical layer, protocol layer, and functional test (see Figure 1).

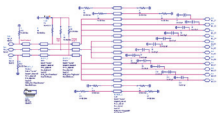
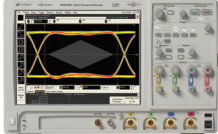
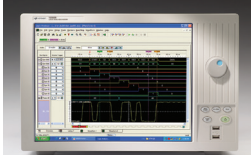
Physical layer: interconnect design	Physical layer: active signal validation	Protocol validation	Functional test
 – ADS design software  – 86100C DCA-J/TDR	 – 90000 or 9000 Series oscilloscope – DDR electrical compliance software – InfiniiScan, EZJIT Plus and Serial data analysis software – InfiniiMax probes – BGA probes	 – 16900 Series logic analyzer – DDR decode and compliance software – Soft Touch probes – BGA probes	 – 16900 Series logic analyzer – DDR decode and compliance software – Soft Touch probes – Slot interposers – BGA probes

Figure 1. Keysight DDR design and test solutions

Applying expertise

When it comes to quality digital measurements and signal integrity, Keysight has decades of experience in RF and protocol engineering. We understand the reflections, insertion and return loss, jitter budget, timing margins, compliance and other issues that digital designers have to face in high data rate standards. As an active member of JEDEC, with consistent participation in workshops and specification issues, Keysight has a solid background in the physical layer, protocol layer and functional test of DDR memory.

Keysight has a long history of collaborative innovation with industry leaders. It puts Keysight in a position to develop tools that meet the physical challenges, are customized to the needs of the standard, and are relevant to the way designers and developers need to use them.

Complete, reliable test coverage

But what makes Keysight design and test solutions so compelling is that they are the best tools, in every category, to meet the challenges presented by DDR memory. We developed these tools to match the application's specific needs – real-time and sampling oscilloscopes to verify signal integrity and jitter, probes for low-invasive high accuracy measurements (see Figure 2), pattern/protocol generators to create the necessary stimulus signals, time-domain reflectometer (TDR) and a vector network analyzer (VNA) to characterize impedance, and EDA software to simulate designs.

The quality of Keysight solutions is the key to easier, faster and more confident testing of your DDR designs. Accurate results reduce the number of design cycles to help you get to market faster, and they ensure robust products that uphold your hard-won lead in the market.

Keysight gets involved, you benefit

Keysight's solutions for digital applications are driven and supported by Keysight experts that are involved in the various international standard committees. We call it the Keysight Digital Test Standards Program. Our experts are active in the Joint Electronic Devices Engineering Council (JEDEC), PCI Special Interest Group (PCI-SIG®), Video Electronics Standards Association (VESA), Serial ATA International Organization (SATA-IO), USB-Implementers Forum (USB-IF), Mobile Industry Processor Interface (MIPI) Alliance, and many others. Our involvement in these standards groups and their related workshops, plugfests, and seminars enables Keysight to bring the right solutions to the market when our customers need them.

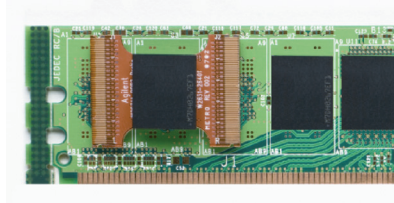


Figure 2. The Keysight W2631B DDR2 x16 BGA command and data probe offers a unique, high accuracy measurement approach

Physical Layer: Active Signal Validation

Validating DDR performance involves characterizing the clock signal, and the data read and write signals. For the clock, key parameters are the rising edge, falling edge, and jitter. For data, the challenge is separating the read and write signals on the bidirectional bus to verify the DQ and DQS waveform parameters. The ability to trigger properly will allow you to analyze the complex traffic on the DDR data bus.

Measure with confidence

Whether you are troubleshooting, capturing contiguous waveforms, ensuring correct operation, or proving compliance, an oscilloscope with low noise, low jitter, and high probe accuracy is critical for measurement accuracy. Eye diagram tests examine the minimum eye opening for adequate operation. Separating the read and write signals on the bidirectional data bus requires a sophisticated triggering system to overcome the limitations of simply triggering on the read/write preamble or signal amplitude.

Key Feature:

Keysight's Infiniium 90000 Series oscilloscopes provide the lowest noise floor, jitter noise floor, and trigger jitter in the industry

Keysight's Infiniium 90000 Series oscilloscopes provide the lowest noise floor, jitter noise floor, and trigger jitter in the industry, enabling you to more accurately characterize your design. The InfiniScan capability provides zone triggering, enabling the oscilloscope to separate read and write cycles based on the distinctive pattern of the waveform (see Figure 3). This is accomplished by drawing zones on the oscilloscope screen to visually determine the event identification condition – whether the waveform intersects or does not intersect the zones.

Automate complex tasks

The Keysight DDR electrical performance compliance and validation software complements the accuracy of the 90000 Series oscilloscopes by simplifying setup and performing compliance tests (see Figure 4). With packages for DDR1, DDR2 and DDR3, the software runs on the oscilloscope itself, using a test framework that has proven value to busy engineers who want quick, accurate answers. The software has the most complete set of DDR tests to evaluate device performance.

The software brings together Keysight's intimate knowledge of the oscilloscope and careful interpretation of the specifications to ensure the best results, high repeatability with minimal effort. The software produces an HTML report, complete with screenshots, which makes it easy to share your results. It also provides a margin analysis that shows how close your design is to the specification (see Figure 5).

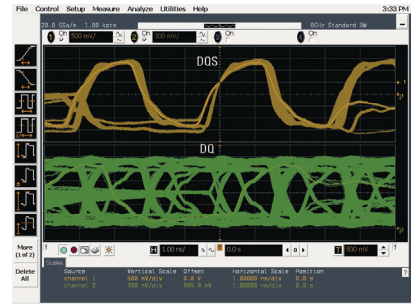


Figure 3. Separate DDR read/write signals quickly with Infiniium oscilloscopes and InfiniScan

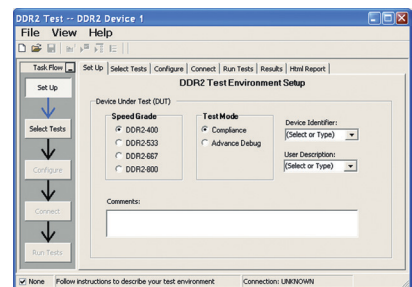


Figure 4. Keysight DDR electrical test software saves you time by selecting tests, configuring tests, setting up the connection, running the tests, and displaying the results

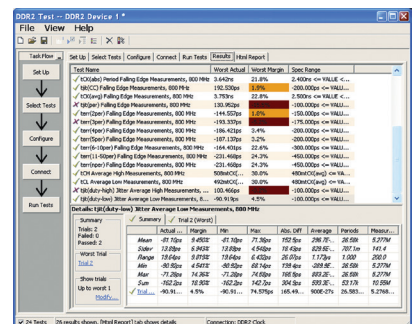


Figure 5. Keysight DDR electrical test software quickly generates a summary report for your device including waveforms and the margin of the result

Physical Layer: Interconnect Design

As data rates increase, you need to pay special attention to your board design to minimize signal integrity problems. Long trace lengths cause signal attenuation, rise-time degradation, and jitter. Impedance transitions between a trace and via can cause reflections and crosstalk. You need to use tools that are more commonly used by high frequency engineers – a time-domain reflectometer (TDR), a vector network analyzer (VNA), and high-frequency simulation software.

Accurate impedance measurements

For quick impedance measurements, a TDR is commonly used. By injecting a fast pulse into your design, the TDR measures the reflected signal to determine impedance versus time, which is easily converted to the distance domain. Likewise, measuring the signal at the far end of the circuit defines the insertion loss profile. TDR displays are intuitive, the measurement setup is easy, and the calibration approach is simple.

Key Feature:

To improve accuracy, the 86100C TDR utilizes a unique calibration process that removes the effects of cabling, allowing you to isolate your device from the test system

The Keysight 86100C Infiniium DCA-J with the 54754A differential TDR/TDT module makes quick work of interconnect analysis. To improve accuracy, it utilizes a unique calibration process that removes the effects of cabling, allowing you to isolate your device from the test system. By switching to frequency mode, you can also examine the S-parameters for transmission and impedance performance of channels, cables, and connectors (see Figure 6). Digital engineers, already familiar with oscilloscopes, can quickly see the relationships between frequency and time effects without having to purchase and learn new equipment.

Predict interconnect performance through simulation

High-frequency engineers commonly use RF simulation tools to predict the effects of transitions, connectors, and traces. Digital designers instead rely upon SPICE-based simulators to account for analog effects. These simulators can sometimes include high-frequency S-parameter data, but rarely match an RF simulator in accurately predicting the high-frequency impact of every element in their circuit.

The Keysight Advanced Design System (ADS) has several features optimized for the high-speed digital designer. Design guides provide a quick vehicle to start a DDR design. You can analyze complete serial links by co-simulating individual components, each at its most appropriate level of abstraction: link, circuit or physical level (see Figure 7). Import measured S-parameters as circuit elements for more accuracy. Make analyses quickly with a user interface leveraged from Keysight oscilloscopes to display eye diagrams and jitter analysis, thereby reducing product design cycles.

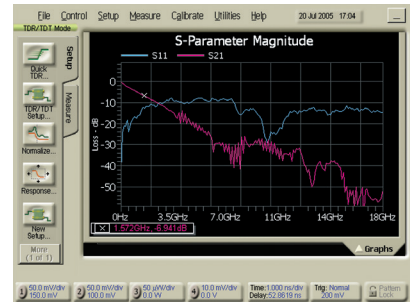


Figure 6. S-parameters can be automatically generated from the 86100C Infiniium DCA-J TDR measurement

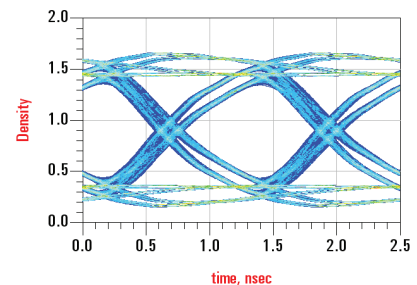


Figure 7. Simulate the impact of crosstalk and line lengths with ADS. After optimizing several trace parameters, you see the optimized eye measurement

Protocol Layer

After inspecting individual DDR signals, you will want to validate that your system is sending the correct DDR commands, that memory banks are getting addressed properly, and check for any protocol violations. Your logic analyzer will need to separate read and write data signals, then display them at several levels of abstraction – from binary to protocol – to validate performance.

Decoding DDR signals

To look at DDR memory bus transactions, a logic analyzer with flexible triggering and decode capability is crucial. The read signals are aligned with the leading edge of the clock, while the write signals are aligned with the center of the clock. The logic analyzer needs to be able to sample at different times, then show the read and write signals separately. You'll want to trigger on key system attributes to start capturing data for analysis.

The Keysight 16900 Series logic analyzer has a dual sample architecture that allows the read and write data be sampled at different times and viewed in separate windows. With the B4621B memory bus decoder, you can trigger on system attributes like burst length, CAS, additive latency, and chip selects to decode key bus signals. The resulting display lists the transaction type, address, data and command conditions. The software also supports user-defined symbols that can be easily added to the state listing display. Eliminate the tedious task of reviewing waveform traces, and view DDR bus transactions quickly with this intuitive display (see Figure 10).

Key Feature:

The Keysight U4154A logic analyzer has a dual sample architecture that allows the read and write data be sampled at different times and viewed in separate windows

Automate complex tasks

The Keysight protocol compliance and analysis tool complements the flexibility of the 16900 Series logic analyzer by simplifying the set up and performing protocol decode and compliance tests (see Figure 8). It runs on the logic analyzer and uses a proven Keysight test framework to produce quick, accurate answers. The software offers a large set of timing and protocol tests to evaluate device performance.

The software brings together Keysight's intimate knowledge of the logic analysis and careful interpretation of the specifications to ensure the best results and high repeatability with minimal effort. It produces an HTML report, complete with screenshots, which makes it easy to share your results. It also provides a margin analysis to show how close your design is to the specification (see Figure 9).

Real time protocol violation tests

DDR Memory measurement and debug work has become more complex and time consuming over the years as data rates increase and the architecture becomes more advanced. The B4622B provides four software tools in one toolset covering:

- Automated real-time compliance violation capture
- Post process compliance violation detection on captured traces
- Performance measurements
- Physical address trigger creation

These four tools help to quickly identify protocol problem areas and also give an overview of system performance.

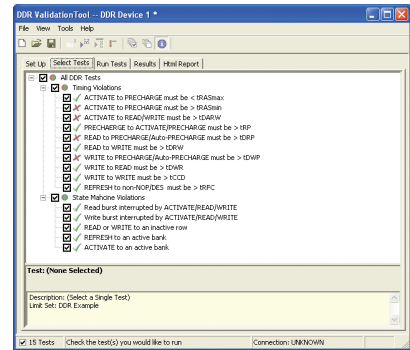


Figure 8. B4622B DDR2/3/4 protocol compliance and analysis tool saves you time by selecting tests, configuring tests, setting up the connection, running the tests, and displaying the results

Physical Address	DDR Bus Decode	Cycle Type
	Deselect	Idle
		Idle
D29 5C00	Read CS-0 BA-3 Row Address = 0x34a5 Col Address = 0x100 Burst Type = Interleave	Read Command
D29 5C00	mem read 0x-----00	*
D29 5C04	mem read 0x-----00	*
D29 5C08	mem read 0x-----00	*
D29 5C0C	mem read 0x-----aa	*
D29 5C10	mem read 0x-----55	*
D29 5C14	mem read 0x-----cc	*
D29 5C18	mem read 0x-----00	*
D29 5C1C	mem read 0x-----ff	*
	Clock is disabled	0000 0100
	Deselect	Idle

Figure 9. B4623B LPDDR2/3 protocol compliance and analysis tool generates a summary report for your device quickly, including waveforms and the margin of the result to provide further insight

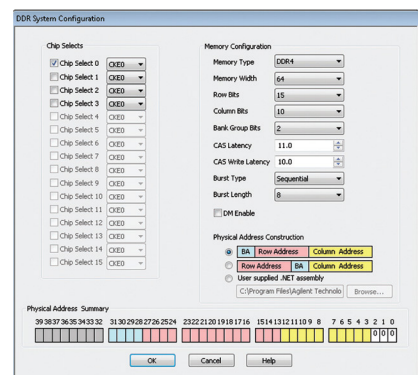


Figure 10. Get a quick, intuitive, view of bus transactions with the 16900 Series logic analyzer and B4621B memory bus decode software

Functional Test

Validating system performance of your DDR design requires properly triggering on the data bus or a specific memory address. You must ensure that there are no timing, state or protocol violations. For robustness, you want to analyze the DDR system behavior. Are some commands being executed too often, or is a memory bank or location being accessed more than others?

Validating system performance

Characterizing a DDR system requires acquiring multiple DDR bus transfers at speed, then analyzing these deep memory waveforms. This can be time consuming and complex to set up, analyze and verify. Key timing tests such as active/read/write-to-precharge, read-to-write and write-to-read require unique triggering setups. Key state tests such as read or write to an inactive row or refresh to an active bank also require unique setups. Automating any portion of these tests saves significant time and gives you a quicker overview of system performance.

Key Feature:

Keysight DDR protocol compliance and analysis tool automates the deep DDR bus trace acquisition and analysis of the Keysight 16900 Series logic analyzer

The U4154A protocol compliance and analysis tool automates the deep DDR bus trace acquisition and analysis of the Keysight U4154A logic analyzer so that you can quickly identify timing and protocol problems. A trigger wizard lets you automatically create a trigger on a specific physical address (see Figure 11). The software checks numerous timing and state violations against the JEDEC specification. It produces an HTML report, complete with screenshots, which makes it easy to share your results.

How robust is your design?

You meet all the timing and protocol specifications, but is your design robust enough to tolerate errors? Is it inefficient in accessing memory? Are there redundant commands or access cycles that increase power consumption? Interoperability requires anticipating these issues to increase fault tolerance and optimal performance.

The Keysight protocol compliance and analysis tool provides a quick overview of the DDR bus performance with statistic and histogram views for bus optimization purposes. The bus statistic report helps you analyze the behavior and activity of your DDR bus (see Figure 12). The histogram view report helps you improve optimization by controlling the number of accesses across the address bus (see Figure 13).

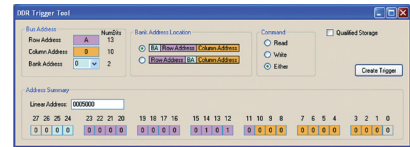


Figure 11. Trigger on a specific physical address for quick analysis using the 16900 Series logic analyzer and B4622B DDR2/3/4 protocol compliance and analysis tool

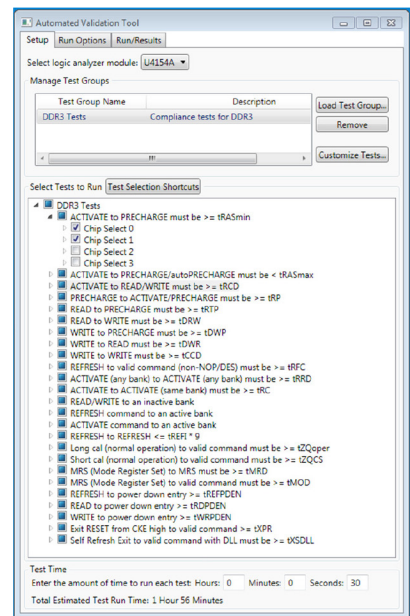


Figure 12. B4622B DDR2/3/4 protocol compliance and analysis tool automates timing and state violations checks

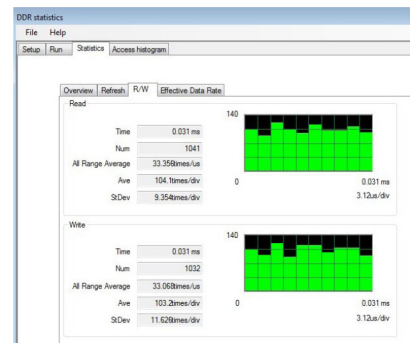


Figure 13. B4622B DDR2/3/4 protocol compliance and analysis tools' bus statistic view provides bus utilization information on read and write commands

Probing DDR Memory

When you need to characterize or validate your DDR design, are you measuring the right signal? The JEDEC standards apply only at the BGA balls of the DRAMs, but in many cases these are difficult to access since many vias do not go through the board. Traces with different lengths will have timing skew and long traces significantly degrade the signal due to high-frequency effects.

Probing specific signals

The easiest approach is to use an active differential probe to look at DDR signals. Your probe needs to have adequate bandwidth so it doesn't limit the signal. For DDR2, you need at least 4 GHz of probe bandwidth. For DDR3 and DDR4, you need 8 GHz. Measuring low voltage, differential signals, requires low probe noise to minimize errors and low input capacitance to reduce the probe loading effect.

The Keysight InfiniiMax Active Probes are high-impedance, low capacitance probes that are minimally invasive to your signals. The solder-in probe head lets you easily solder to vias and quickly look at a signal (see Figure 14).

Probing the data bus

To do a complete functional test, you need to measure the data and address bus, or multiple signals all at once. Traditional logic analyzer probes require you to modify the board layout to accommodate the socket. When you remove the socket after debug, these trace remnants can cause signal integrity problems.

The Keysight Soft Touch logic analyzer probes are one solution. You can use them without connectors by just routing the traces in a specific manner (see Figure 15). Their unique design makes solid contact with the traces without a connector.

The Keysight DDR slot interposer is another solution, connecting directly to the industry's standard DDR DIMM connector (see Figure 16). The non-intrusive design lets you measure the full command, address, control and data bus signals.

A better way – BGA probe adapters

The optimum approach is to probe all DDR signals right at the BGA balls. One solution is to place a thin fixture between the DRAM and the board to access all DDR signals. This is a high-frequency design challenge that few designers want to tackle.

Key Feature:

You can perform parametric and functional measurements using the same BGA probe

The Keysight DDR2 and DDR3 BGA probe adapters address these needs. The BGA signals are routed to the top side of the BGA probe adapter, so oscilloscope and logic analyzer probes can access them (see Figure 17). You can perform parametric and functional measurements using the same BGA probe. The traces have the same length to reduce skew issues. Embedded resistors minimize signal loading.

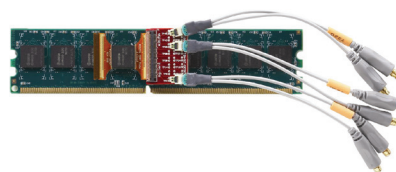


Figure 14. Using an InfiniiMax active differential solder-in probe

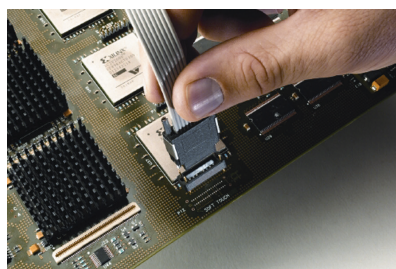


Figure 15. Using a Soft Touch non-invasive probe

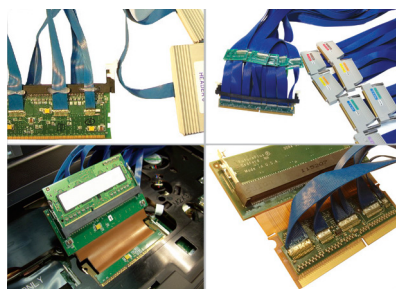


Figure 16. Using the N4835A Advanced DDR3 slot interposer

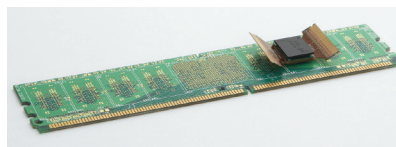
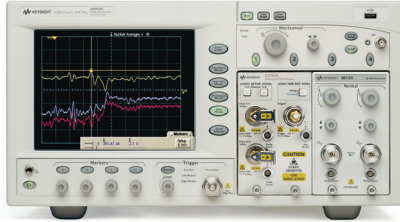


Figure 17. Using a DDR2 BGA probe adapter

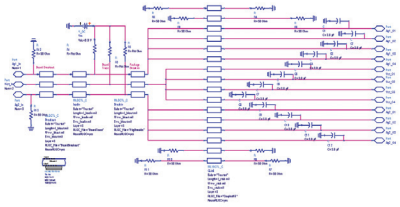
Keysight DDR Solutions

86100C Infiniium DCA-J wide-bandwidth oscilloscope with TDR



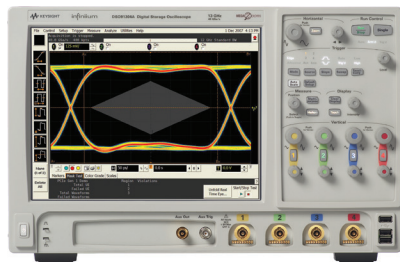
The Keysight 86100C Infiniium DCA-J can view electrical waveforms with bandwidths up to 93 GHz. The DCA-J is an ideal tool for making signal integrity and jitter measurements for high speed signaling standards. Complete jitter analysis is simplified – a one-button press allows you to review the random and deterministic jitter components. With the Keysight 54754A Differential TDR/TDT module, you can characterize impedance and crosstalk in channels and view the results in either the time-domain or as S-parameters in the frequency domain.

Advanced Design System (ADS)



With a complete set of simulation technologies ranging from frequency-, time-, numeric and physical domain simulation to electromagnetic field simulation, ADS lets designers fully characterize and optimize designs. The single, integrated design environment provides system, circuit, and electromagnetic simulators, along with schematic capture, layout, and verification capability – eliminating the stops and starts associated with changing design tools in mid-cycle.

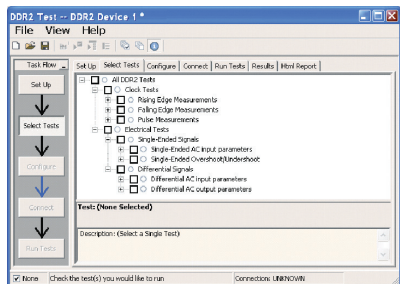
90000 Series Infiniium 13 GHz bandwidth oscilloscope



The Keysight 90000 Series Infiniium oscilloscopes are the highest performance real-time measurement system available. The Infiniium 90000 Series offers the industry's lowest noise floor, jitter noise floor, and trigger jitter, making it the ideal tool for signal integrity and jitter measurements. Models are available from 2.5 GHz to 13 GHz, and they can be upgraded in bandwidth for future needs. The N5414A InfiniiScan event identification software provides a unique combination of hardware and software triggering to capture hard to find events.



U7233A/N5413B/U7231B/N6462A DDR1/DDR2 & LPDDR2/DDR3 & LPDDR3/DDR4 electrical compliance test software



The Keysight electrical performance validation and compliance software for the Infiniium 90000 Series oscilloscope provide a fast and easy way to verify and debug your DDR designs. The DDR electrical test software allows you to automatically execute DDR electrical checklist tests and displays the results in a flexible report format. In addition to the measurement data, the report provides a margin analysis that shows how closely your design passed or failed each test.

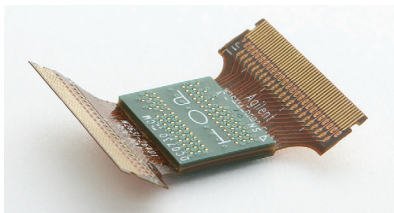
Keysight DDR Solutions

1130/1160 Series InfiniiMax active differential probes



The InfiniiMax probing system offers the highest performance available for measuring differential and single-ended signals, with flexible connectivity solutions for today's high-density ICs and circuit boards. High-input impedance active probes minimize loading, support differential measurements and DC offset, and can compensate for cable loss. Six different InfiniiMax probe amplifiers from 1.5 GHz to 13 GHz are available for matching your probing solution to your performance and budget requirements. Probe heads are available in solder-in, ZIF, socket, browser and SMA connections.

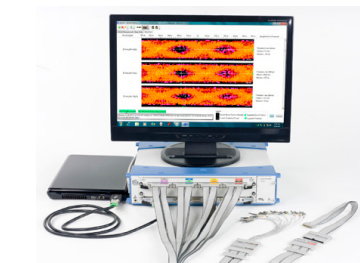
W2630 Series DDR2/LPDDR/DDR3 and W3630 Series DDR3 BGA probes



The Keysight W2630 Series DDR2/LPDDR/DDR3 and W3630 Series DDR3 BGA probes for logic analyzers and oscilloscopes enable viewing of data traffic on DRAMs with the Keysight 16900 Series logic analyzer and Infiniium 90000 Series oscilloscope. The BGA probes are used with the 46 channel single-ended ZIF probe which connects to the 90-pin logic analyzer cable. For use with the Infiniium oscilloscopes, use either the ZIF probe heads or the W3635A probe adapter for solder-in probe heads, with the InfiniiMax probing system. Contact Keysight representative for LPDDR2/3 and DDR4 probes.



U4154A 4 Gb/s AXIe-based Logic Analyzer Module



The Keysight U4154A AXIe logic analyzer system combines reliable data capture up to 136 channels with powerful analysis and validation tools to enable you to quickly and confidently validate and debug high-speed digital designs operating at speeds up to 4 Gb/s. Confidence in the state mode captures, and bus-level signal integrity insight, make the U4154A logic analyzer the ideal tool for DDR memory measurement and debug work.

"Best in test finalist" image from 2012 from webpage www.keysight.com/find/u4154A

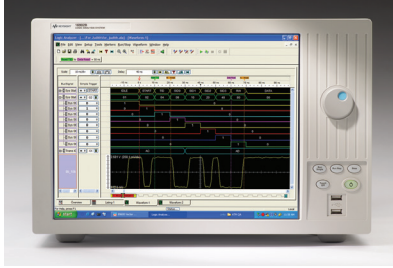
U4154A

Physical Address	DDR Bus Decode	Cycle Type
	Deselect	Idle
		Idle
D29 5C00	Read CS-0 BA-3 Read Command	
	Row Address = 0x345	*
	Col Address = 0x100	*
	Burst Type = Interleave	*
D29 5C00	mem read 0x-----00	*
D29 5C04	mem read 0x-----00	*
D29 5C08	mem read 0x-----00	*
D29 5C0C	mem read 0x-----aa	*
D29 5C10	mem read 0x-----55	*
D29 5C14	mem read 0x-----cc	*
D29 5C18	mem read 0x-----00	*
D29 5C1C	mem read 0x-----ff	*
	Clock is disabled	0000 0100
	Deselect	Idle

Accelerate your time to insight using the B4623B bus decoder for LPDDR, LPDDR2, or LPDDR3 debug and validation. The B4623B provides complete protocol decode of memory transactions using a Keysight logic analyzer as the analysis execution engine. The B4623B protocol-decode software translates acquired signals into easily understood bus transactions showing associated data bursts, for all LPDDR, LPDDR2, or LPDDR3 data rates. Valid Read and Write commands are decoded to include Row and Column Addresses and the complete data burst associated with the command. The B4623B bus decode software anticipates key system attribute inputs (Burst length, CAS Latency and CAS Write Latency, Chip Selects) from default LPDDR, LPDDR2, or LPDDR3 probing configurations and/or DDR Setup Assistant tool to accelerate decode of LPDDR, LPDDR2, or LPDDR3 bus signals.

Keysight DDR Solutions (continued)

16900 Series modular logic analysis system for DDR1 and 2



The Keysight 16900 Series logic analysis system provides high-performance, system-level debugging of digital designs. Customize this system for your specific needs with innovative probing, high-performance measurement modules, and post-processing analysis tools. Use the EyeFinder software to analyzer the read and write data valid windows to ensure accurate sampling position of data for protocol decode. The B4621B memory bus decode software translates acquired signals into easily understood bus transactions at full bus speed.

B4622B DDR2/3/4 protocol compliance and analysis tool

Test Name	Actual Val	Margin	Spec Range
✓ ACTIVATE to PRECHARGE must be < tRASmin	49.0ns	25.0%	VALUE < 79.0ns
✗ ACTIVATE to PRECHARGE must be > tRASmin	36.0ns	-4.0%	VALUE > 37.5ns
✗ ACTIVATE to READ/WRITE must be > tDQW	13.5ns	-24.0%	VALUE > 15.0ns
✓ PRECHARGE to ACTIVATE/PRECHARGE must be > tRP	49.151µs	327.575.3%	VALUE > 15.0ns
✗ READ to PRECHARGE/ACTIVATE must be > tCRP	10.5ns	-20.0%	VALUE > 15.0ns
✓ READ to WRITE must be > tDRW	49.151µs	280.764.0%	VALUE > 17.5ns
✗ WRITE to PRECHARGE/ACTIVATE must be > tDWP	13.5ns	-24.0%	VALUE > 15.0ns
✓ WRITE to READ must be > tDWR	49.151µs	178.632.0%	VALUE > 27.5ns
✓ WRITE to WRITE must be > tDWD	49.151µs	491.413.0%	VALUE > 10.0ns
✓ REFRESH to non-REFRESH must be > tRRC	49.151µs	44.263.0%	VALUE > 110.0µs
✓ Read burst interrupted by ACTIVATE/READ/WRITE	Pass	100.0%	Pass/Fail
✓ Write burst interrupted by ACTIVATE/READ/WRITE	Pass	100.0%	Pass/Fail
✓ READ or WRITE to an inactive row	Pass	100.0%	Pass/Fail
✓ REFRESH to an active bank	Pass	100.0%	Pass/Fail
✓ ACTIVATE to an active bank	Pass	100.0%	Pass/Fail

The B4622B DDR2/3/4 protocol compliance and analysis tool enables timing and functional validation measurement through the protocol compliance check capability. The software quickly sets up the complex test setups, acquires the data, and provides the test results with details of the test failure in HTML format for reporting purposes. The bus statistic report gives you an overview of the DDR bus utilization. The histogram view reports the number of accesses in specific memory locations to help you improve optimization.

Keysight DDR Design and Test Solutions

Table 2. Keysight DDR solutions by DDR technology (* Supported by FuturePlus Systems Corporation)

Product	Description	Technology supported				
		DDR2	DDR3	DDR4 ¹	LPDDR2	LPDDR3 ¹
DSA90254A or DS09254A	2.5 GHz Infiniium oscilloscope					
DSA90404A or DS09404A	4 GHz Infiniium oscilloscope	X			X	
DSA90804A	8 GHz Infiniium oscilloscope	X	X	X	X	X
U7233A	DDR1 electrical compliance test application					
N5413B	DDR2 and LPDDR2 electrical compliance test application	X			X	
N6462A	DDR4 electrical compliance test application			X		
U7231A	DDR3 electrical compliance test application		X			X
N5414A	InfiniiScan event identification software	X	X		X	
1131A	3.5 GHz InfiniiMax differential probe amplifier					
1132A	5 GHz InfiniiMax differential probe amplifier	X			X	
1134A/1168A/1169A	7/10/13 GHz InfiniiMax differential probe amplifier	X	X	X	X	X
W2212B	ADS Design Software bundle (ADS Core, Transient Convolution, Layout, Momentum G2, EMDS, Ptolemy)	X	X		X	
86100C, 54754A	DCA-J Infiniium oscilloscope with TDR module	X	X		X	
	Protocol/functional test	DDR2	DDR3	DDR4 ¹	LPDDR2	LPDDR3 ¹
16902B	Logic analyzer mainframe	X	X	X	X	X
16950B or 16951B	68-channel, 667 MHz, logic analysis module	X		X	X	
16962A	68-channel, 2 Gb/s, logic analysis module	X	X	X	X	X
B4621B	DDR2/3/4 memory bus decode software	X	X	X		X
B4622B	DDR2/3/4 and LPDDR2/3 protocol compliance and analysis tool	X	X	X		X
B4623B	LPDDR2/3 protocol compliance and analysis tool					
N4834A or N4835A	DDR3 midbus probe or advanced slot interposer		X			X
	BGA probes	DDR2	DDR3	DDR4 ¹	LPDDR2	LPDDR3 ¹
W2631A or W2633A	DDR2 x16 BGA command and data probe for logic analyzer and oscilloscope	X		X		
W2632A	DDR2 x16 or x8 BGA data probe for logic analyzer and oscilloscope	X		X		
W2634A	DDR2 x8 BGA data probe for logic analyzer and oscilloscope	X		X		
W2635A or W2636A	DDR3 x8 or x16 BGA oscilloscope probe		X			X
W2637A or W2638A	LPDDR x16 or x32 BGA probe for oscilloscope and logic analyzer					
W2639A	BGA oscilloscope probe adapter board	X	X	X		X
W3631A or W3633A	DDR3 x16 or x4/x8 BGA probe for logic analyzer and oscilloscope		X			X

Note 1: Please contact Keysight representative for LPDDR2, LPDDR3, DDR4 BGA probe information.

Related Keysight Literature

Publication title	Pub number
90000 Series Infiniium Oscilloscope and InfiniiMax Probing System Data Sheet	5989-7819EN
U7233A DDR1 Electrical Characterization and Compliance Software Data Sheet	5989-7366EN
N5413B DDR2 and LPDDR2 electrical compliance test application	5989-3195EN
U7231A DDR1 Electrical Characterization and Compliance Software Data Sheet	5989-7243EN
16900 Series Modular Logic Analysis System Data Sheet	5989-0421EN
B4622A DDR2/3 Protocol Compliance and Analysis Tool Data Sheet	5990-3300EN
W2630 Series DDR2 BGA Probes Data Sheet	5989-0421EN
W3630 Series DDR3 BGA Probes Data Sheet	5990-3179EN
86100C Infiniium DCA-J Wide Bandwidth Oscilloscope with TDR Brochure	5989-5235EN
Designing for Signal Integrity with Advanced Design System Data Sheet	5989-8392EN

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