Keysight Technologies
Changes in Test Coverage

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Changes in Test Coverage

DSPs, internal lead frames and high node count PCBs have forever transformed ICT.

TEST TECHNOLOGY HAS evolved a thousand-fold over the years, raising the question, Do manufacturers really have a choice of options, or is the status quo a result of having to use what they have in their manufacturing testing line to cut costs? This month we will attempt to uncover the mysteries behind in-circuit testing on a modern high-speed, high-complexity board to understand difficulties manufacturing has in defect detection.

All PCBs inside PCs, servers and telecom equipment are mainly driven by consumer demand for faster access to the Internet, cost, quality, and size. Behind all these state-of-the-art digital technologies are the increasing challenges to keep the cost of test low, while maintaining PCB quality. In-circuit test has been the workhorse of PCB testing, and EMS/ODMs maintain tens if not hundreds of ICTs on their manufacturing floors to keep pace with demand. But does ICT still do a good job of testing the components on a PCB?

Passive components. Passives comprise more than 90% of components on a PCB (FIGURE 1.) Passive development over the years was overshadowed by the advancement of digital technology. However, from the manufacturing perspective, passives still make up the majority of parts placed.

ICT measurement and testing requirements have not changed much over the years on passive components. Most advancements on the ICT's analog measurement capability are focused on enabling faster and more stable testing, something absent in older generations of ICTs. Here's a quick summary of the analog measurement advances in modern ICT:

- New analog measurement technology uses multiple microcontrollers and an analog and digital convertor (ADC) with digital-signal processing methods to enable faster simultaneous processing of the measured values. This improvement, along with software enhancements, translates to 20 to 40% throughput improvement.
- Capability to reliably test capacitors of 10 pF to 47 pF using high-frequency sources of 100 kHz to 200 kHz.
- Large capacitor measurements (1000 µF to 30 mF) using DC test method.
- Testing inductors and ferrite beads using high-frequency sources of 100 Khz and 200 Khz to detect shorted components. Older ICTs test low value inductors and ferrite beads as jumpers (resistor test), which does not detect shorts. Low-value inductors and low-Q ferrite beads are common on PCBs to filter power supply noise.
- High-voltage zener diodes (voltage rating 18 to 60V). The measurement circuit capable of measuring high-voltage zener diodes consists of a power switch and an over-current/over-voltage protection circuit, 70V boost power supply, adjustable voltage regulator, and zener test op-amp.

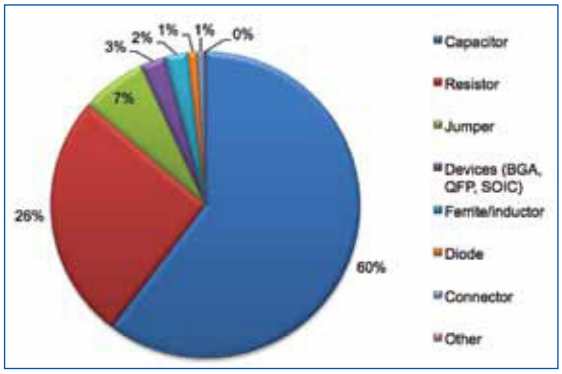

FIGURE 1. Component distribution on a large node count PCB (10k nodes).

Advanced capacitive vectorless testing. The capacitive vectorless test method consists of a sensor plate, a thin PC board cut to match the physical outline of the device under test and an electronics board that contains an amplifier. The measurement method uses an ICT analog source to drive a low frequency in Khz and low voltage in mV ranges, applied on a device pin, while the remaining device pins are tied to ground. The signal is coupled to the sensor plate by the capaci-

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TABLE 1. Coverage Comparison of Capacitive Vectorless Tests

	NO. DEVICES	NO. TESTABLE PINS	NO. PINS TESTED USING CAPACITIVE VECTORLESS	NO. PINS TESTED USING ADVANCED CAPACITIVE VECTORLESS
Board 1	10	686	686	634
Board 2	4	454	139	454
Board 3	12	1035	880	1033
Total	26	3315	2426 (73.18%)	3313 (99.94%)

tance between the device pin internal lead frame and the sensor plate. The signal received by the sensor plate is amplified by the electronics board and sent to the multiplexer card. The multiplexer card further amplifies and filters the signal before sending it to the ICT for further processing to identify if the pin is open or soldered to the PCB. The measurement typical value is 50 to 200 femptofarad (fF) for devices with internal lead frames such as QFP and SOIC, as well as connectors.

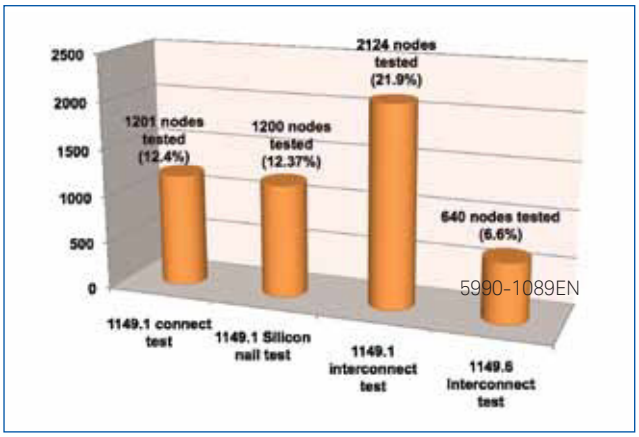

FIGURE 2. High-speed differential signal circuit testable using 1149.6 boundary scan test at ICT.

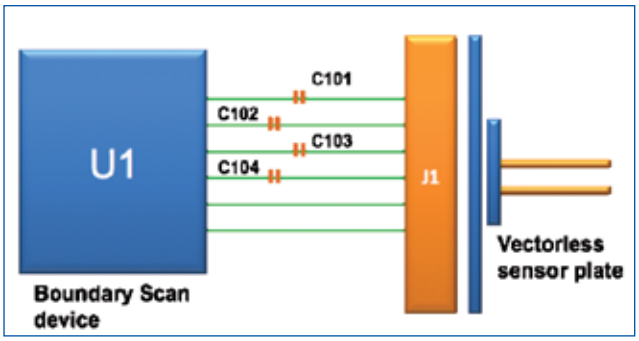

FIGURE 3. Powered vectorless combining boundary scan device and a capacitive vectorless.

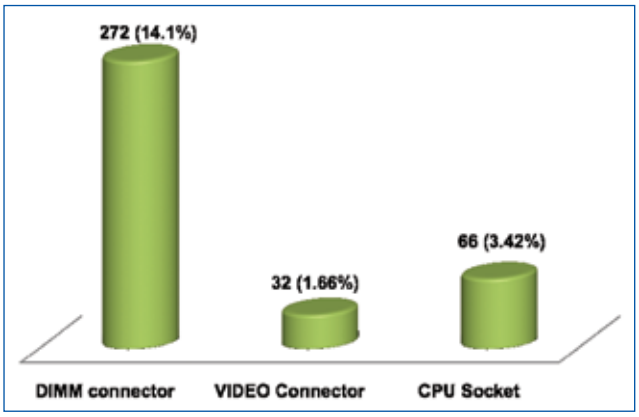

FIGURE 4. Powered vectorless test coverage on current notebook motherboard connectors/sockets.

In the case of advanced capacitive vectorless testing, a more sensitive amplifier is used along with an enhanced ICT measurement algorithm to test BGA devices without internal or little lead frame that measure below 20fF per ball. This test takes more accurate measurements compared to the capacitive vectorless tests seen on older ICTs (TABLE 1).

ICT boundary scan. The support of IEEE 1149.1 boundary scan test at ICT was implemented almost at the same time the IEEE 1149.1 standard was first released in 1990. However, during that time, there was no available PCB with devices that supported 1149.1. It took several years before the boundary scan device was adopted at PCB. Boundary scan at ICT is a limited access solution in which physical test access on probes is not needed to test the interconnection between devices. The ICT boundary scan test implementation minimizes cost of test at ICT, despite higher PCB node counts.

An important advance in ICT boundary scan testing today is the support of 1149.6, an IEEE standard for boundary scan testing of advanced digital networks. The 1149.6 boundary scan test enables ICTs to test high-speed differential signals commonly found on telecom, computers and server boards (FIGURE 2).

Implementation of boundary scan is no longer exclusive to high node count PCBs, as more medium-sized PCBs adopt the boundary scan strategy due to space constraint, in order to put test access and high-speed differential signal proliferation on consumer products such as laptops, netbooks, tablet PCs and smart phones. Although the majority of PCBs used are still on 1149.1 boundary scan, this is set to change as more devices support 1149.6 for high-speed differential signals.

Powered vectorless testing. By combining ICT vectorless test with boundary scan, this expands boundary scan and vectorless capability to test non boundary-scan devices, which includes non boundary-scan digital devices, connectors/sockets, passives and actives (FIGURE 3). This strategy is so promising that an IEEE standard 1149.8.1 is proposed to expand coverage on high-speed differential signals.

Consumer products are set to benefit from this technology, as products such as laptops, netbooks, tablet PCs and smartphones adopt boundary scan as part of their design to enable testing. The current notebook motherboard coverage shows a promising start to recover coverage at ICT (FIGURE 4). The powered vectorless test should set to improve further in the future, as more devices will be developed to support the 1149.1, 1149.6 and 1149.8.1 standards.

ICTs with upgraded hardware and software remain the best option to test PCBs in the manufacturing environment, helping manufacturers regain coverage older ICTs are no longer able to provide, as well as testing modern nodes and components no longer testable on older ICTs. CA