WHITE PAPER

UCIe vs. BoW: Practical Insights for Choosing the Right Chiplet Standards

KEYSIGHT

Executive Summary

The semiconductor industry is rapidly transitioning from monolithic System-on-Chip (SoC) designs to chiplet-based architectures to address escalating costs, yield challenges, and scaling limitations. As chiplets become mainstream, standardized die-to-die interconnect technologies are essential to enable efficient communication between heterogeneous dies. Two leading approaches have emerged: **Universal Chiplet Interconnect Express (UCIe)** and **Bunch of Wires (BoW).**

This whitepaper compares UCIe and BoW from a practical engineering perspective. It examines their architectural differences, signal-integrity methodologies, interoperability goals, and implementation complexity. A detailed channel case study is presented to evaluate how each standard addresses eye diagrams, channel loss, and crosstalk. The analysis highlights trade-offs between flexibility and cost efficiency (BoW) and standardization and robustness (UCIe). The paper concludes with signal-integrity insights for chiplet systems and discusses the growing importance of EDA tools in enabling reliable chiplet design.

From Monolithic Design to Chiplet Architectures

Integrated Circuit (IC) design traditionally follows a workflow that begins with schematic design, progresses to layout, and culminates in tape-out to wafer fabrication. Individual dies are then extracted from the wafer and packaged into final products.

Historically, most high-performance devices were built using a **monolithic design approach**, where all system functions were integrated onto a single large die. However, the increasing complexity of modern systems and the rising cost of advanced process nodes have made this approach less sustainable.

Chiplet-based architectures provide an alternative design methodology in which functionality is distributed across multiple smaller dies that are integrated within a single package.

Why Chiplets Are on the Rise

Chiplets are gaining momentum primarily due to their economic and manufacturing advantages.

Monolithic vs. Chiplet Yield

Traditional monolithic SoCs integrate all functions on a single die. While effective for many years, this approach faces increasing challenges:

- **Escalating costs** of advanced process nodes
- **Lower manufacturing yields** due to defects on large dies
- **Limited scalability** when different IP blocks require different optimal process nodes

Consider a monolithic die that integrates four required functional blocks into a single device. This approach assumes the full system depends on all four blocks being present on one die. When defects occur during wafer fabrication, any flaw in one block renders the entire die unusable, leading to yield loss.

Chiplet-based design addresses this limitation by partitioning the system into smaller, individual dies — each implementing one or more functional blocks. By decoupling the blocks, defects affect only the impacted chiplet rather than the entire system, significantly improving overall yield and reducing cost.

For example:

- 12 monolithic dies fabricated
- 4 defects present
- 8 usable dies produced
- Yield = 66.7%

In contrast, a chiplet design splits functionality across smaller dies. The same wafer defect density affects fewer complete systems.

For example:

- 16 chiplets fabricated
- 1 chiplet lost due to defects
- 15 usable chiplets produced
- **Yield ≈ 97.3%**

This demonstrates that chiplets significantly improve manufacturing yield and cost efficiency.

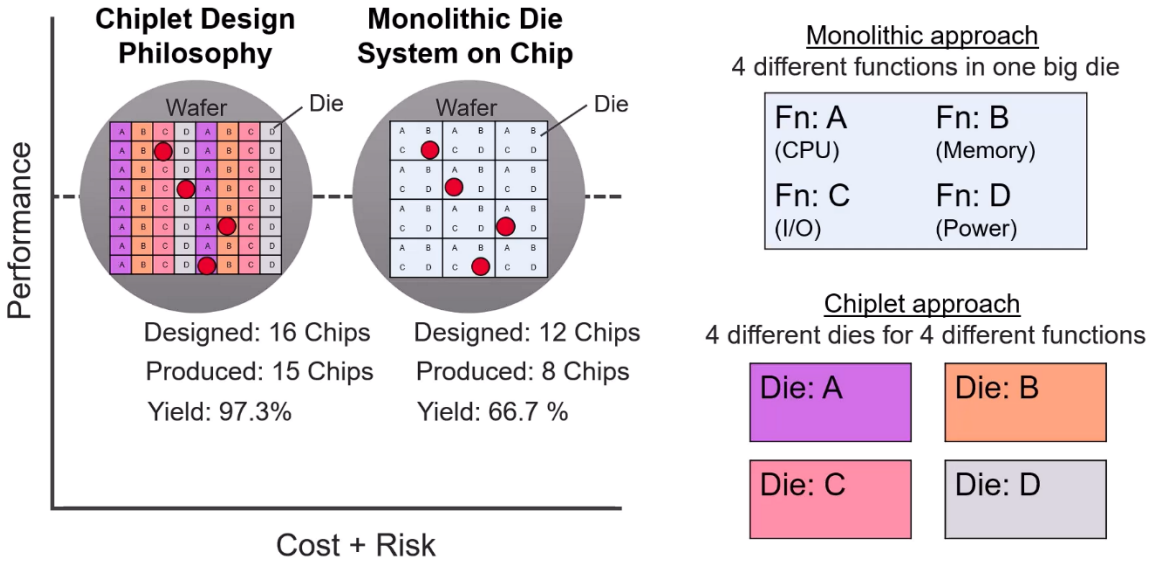


Figure 1. Chiplets Improve the Cost vs. Performance of Chip Production

Chiplets also enable heterogeneous integration, allowing designers to combine advanced-node logic dies, mature-node analog components, and specialized accelerators.

This flexibility can dramatically reduce costs. For example, industry analyses show that implementing certain processor configurations entirely on an advanced node can be twice as expensive as a chiplet-based design that partitions functionality.

The Interconnect Challenge

The key trade-off is that chiplets require high-speed die-to-die communication.

To address this requirement, industry standards have emerged, most notably:

- **UCIe (Universal Chiplet Interconnect Express)**
- **BoW (Bunch of Wires)**

These standards define the electrical and protocol layers that enable efficient communication between chiplets.

Although both UCIe and BoW are designed to enable die-to-die communication in chiplet architectures, they are built on fundamentally different philosophies. UCIe emphasizes interoperability and standardization, aiming to create a robust ecosystem in which chiplets from different vendors can work together. This is reflected in its structured approach to signal mapping, defined bump layouts, and tightly specified communication protocols.

In contrast, BoW takes a more flexible and implementation-driven approach. Rather than enforcing rigid mapping requirements, it allows designers to define their own wiring schemes, prioritizing simplicity and cost efficiency. This flexibility extends to its use of parallel data transmission, compared to UCIe's serial architecture, and its support for bidirectional communication within the same interface.

These architectural differences have direct implications for design complexity, performance scalability, and ecosystem compatibility. While UCIe offers a more comprehensive and future-proof framework, BoW enables faster adoption in cost-sensitive or application-specific designs where strict interoperability is less critical.

	Standards	
Feature	**UCIe**	**BoW**
Data transmission	Serial	Parallel
Basic design unit	Module	Slice
Directionality	Unidirectional	Can be Bi-directional
Signal mapping priority	Bump map	Wire order

Comparative Evaluation Framework

To meaningfully compare UCIe and BoW, it is useful to evaluate them through three practical lenses:

- Ease of implementation
- Signal Integrity (SI) specification coverage
- Interoperability

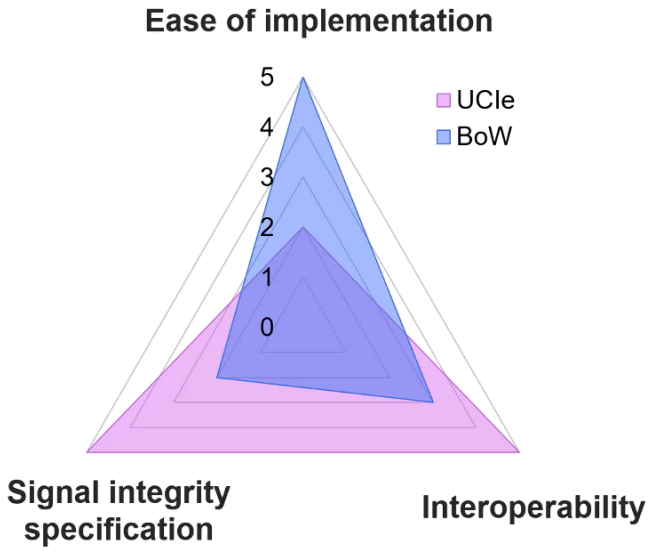
These criteria reflect the real-world concerns engineers face when selecting a chiplet interconnect standard.

From an implementation standpoint, BoW is generally easier to adopt due to its minimal constraints and flexible design rules. Designers are not required to adhere to rigid mapping or protocol structures, which reduces upfront complexity and accelerates development. UCIe, on the other hand, introduces additional design overhead due to its more comprehensive specification, requiring careful adherence to defined electrical and protocol requirements.

However, this added complexity in UCIe translates into significant advantages in signal integrity and interoperability. UCIe provides detailed and explicit SI guidelines, including well-defined eye masks, loss metrics, and crosstalk evaluation methods. These specifications enable more predictable system behavior and simplify validation. BoW, while functional, offers comparatively limited SI guidance, often leaving interpretation and validation methodologies to the designer.

Interoperability further distinguishes the two approaches. UCIe is explicitly designed to support a broad ecosystem, making it well-suited for plug-and-play chiplet integration across vendors and generations. BoW, by contrast, is more suited to tightly controlled environments where all components are designed within the same organization or for a specific application.

Radar Chart Assessment



Interpretation:

- **BoW** offers simpler implementation but fewer SI guidelines.
- **UCIe** provides comprehensive specifications but requires more design effort.

Use-Case Implications

- Plug-and-play ecosystems → UCIe preferred
- Cost-sensitive custom designs → BoW preferred

Channel Case Study: "What Would the Standard Say?"

To illustrate the practical differences between the standards, here's an example analysis of a representative chiplet channel.

Configuration

- Package-level interconnect
- Three adjacent data lines
- Data rate: **24 GT/s**
- Receiver eye diagrams evaluated

The analysis examined:

- Eye height and width
- Channel loss
- Crosstalk

Eye Mask Evaluation

UCIe defines explicit eye mask specifications based on data rate.

For a 24 GT/s link, the standard specifies:

- Eye height ≈ **40 mV**
- Eye width ≈ **0.65 UI**

BoW provides margin specifications in terms of:

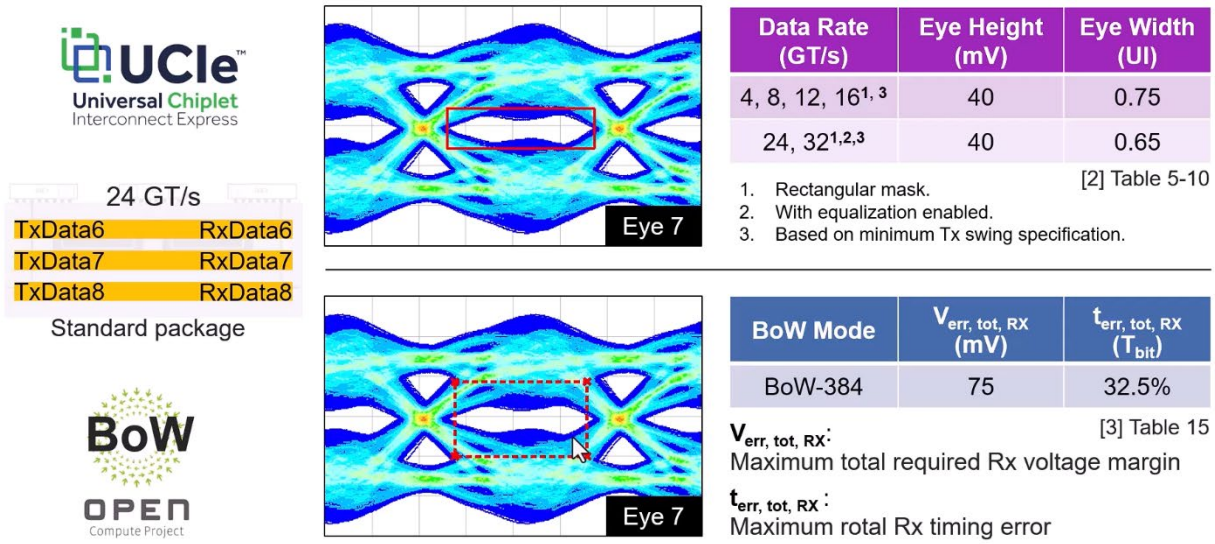
- Receiver voltage margin
- Timing error tolerance

However, these specifications must be interpreted to derive an equivalent eye mask.

Observation

- UCIe provides clear, directly usable SI metrics.

BoW requires interpretation and engineering judgment.



Data Rate (GT/s)	Eye Height (mV)	Eye Width (UI)
4, 8, 12, 16[1, 3]	40	0.75
24, 32[1,2,3]	40	0.65

[2] Table 5-10

1. Rectangular mask.
2. With equalization enabled.
3. Based on minimum Tx swing specification.

BoW Mode	$V_{err, tot, RX}$ (mV)	$t_{err, tot, RX}$ (T_{bit})
BoW-384	75	32.5%

[3] Table 15

$V_{err, tot, RX}$:
Maximum total required Rx voltage margin

$t_{err, tot, RX}$:
Maximum rotal Rx timing error

Figure 2. WWSS-Eye: Standards with different descriptions of the Eye

Channel Loss Evaluation

Channel loss is a critical factor in determining the performance of high-speed chiplet interconnects, and the way it is defined and evaluated varies significantly between UCIe and BoW. UCIe adopts a rigorous and highly structured approach through the use of the Voltage Transfer Function (VTF). This method models the channel as a complete system, incorporating source and receiver terminations, parasitic capacitances, and interactions across multiple transmission lines. By expressing loss as a frequency-dependent ratio between transmitted and received voltages, UCIe provides a precise and reproducible framework for evaluating signal degradation.

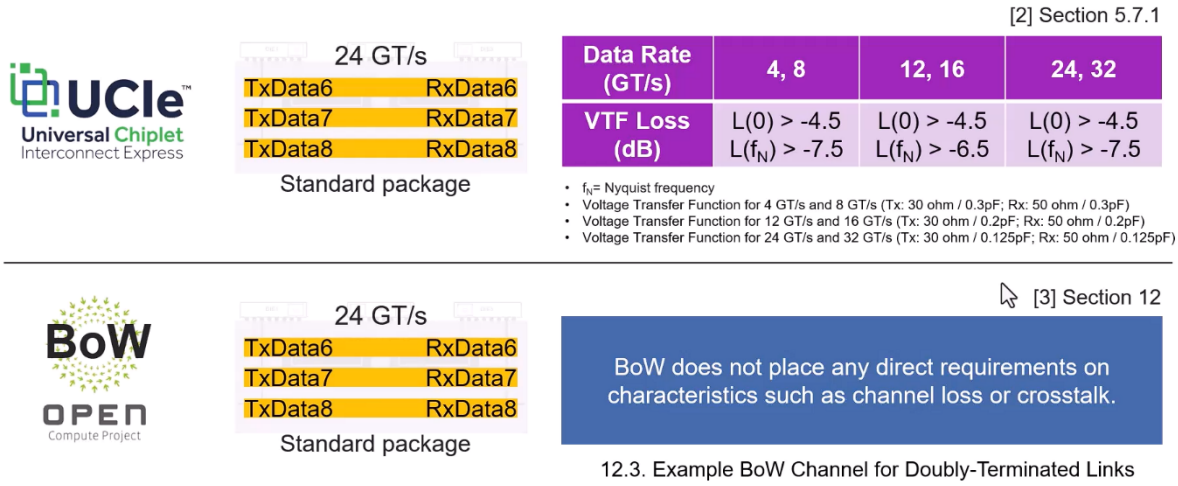


Figure 3. WWSS-Loss: Evaluate a channel's loss with the standards

This structured methodology allows designers to directly compare measured or simulated channel performance against clearly defined limits. As a result, pass/fail criteria are unambiguous, and compliance with the standard can be systematically verified.

In contrast, BoW does not impose strict requirements on channel loss characteristics. Instead, it provides general insertion loss guidelines, often illustrated through example channels. While these examples can serve as useful references, they lack the formal rigor and scalability of UCIe's approach. Designers may need to adapt or scale these guidelines to match their specific data rates and configurations, introducing additional uncertainty into the evaluation process.

In the case study presented in this paper, both standards ultimately identified the channel as failing due to excessive loss. However, the process of reaching that conclusion was notably more straightforward and transparent under the UCIe framework, highlighting the practical advantages of its more detailed specification.

Crosstalk Evaluation

UCIe Method

UCIe defines VTF-based crosstalk calculations across multiple lines. Crosstalk is computed by summing aggressor voltages relative to the source voltage.

This provides a precise quantitative limit across the frequency spectrum.

BoW Method

BoW provides general guidance:

- Crosstalk should typically remain below 35% of signal swing

While helpful, this guideline lacks detailed analytical methodology.

Result

- UCIe produced a clear failure result.

BoW analysis required assumptions and interpretation.

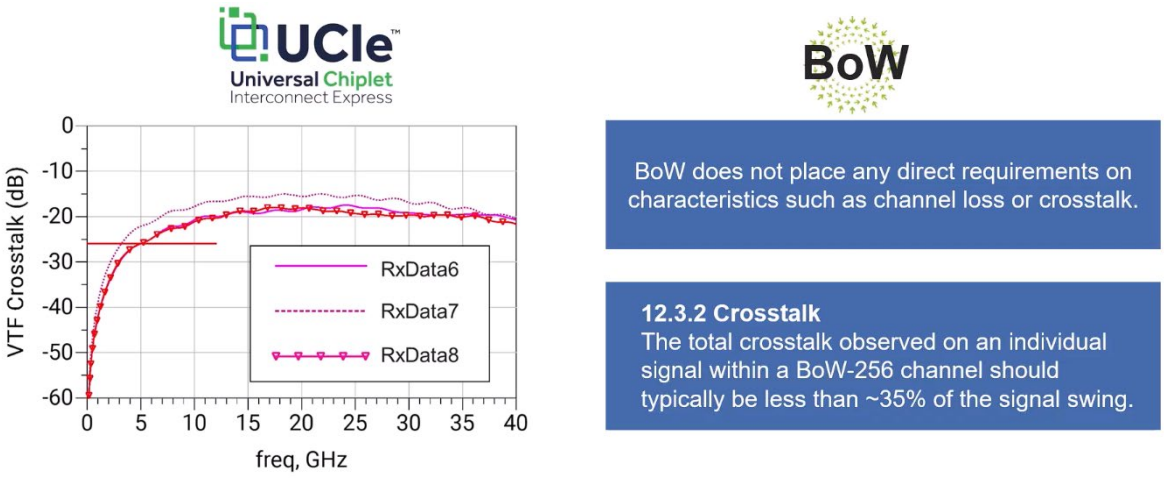


Figure 4. UCIe provides more consistent crosstalk metrics than BoW

Signal Integrity Insights from Eye Analysis

Analysis of the failing eye diagram revealed three primary degradation mechanisms.

Reflections (Impedance Discontinuities)

When a signal encounters impedance mismatches:

- Part of the signal transmits
- Part reflects back toward the source

Multiple reflections distort the received waveform, reducing amplitude and deforming the eye shape.

Mitigation

- Match impedance across interconnect interfaces
- Eliminate discontinuities in routing or packaging structures

Crosstalk

Crosstalk occurs when electromagnetic coupling between adjacent channels induces unwanted voltages.

Key observations:

- Larger spacing reduces coupling
- Closely spaced traces increase interference
- Unequal channel lengths shift crosstalk timing

When multiple channels of different lengths interact, crosstalk can cause **vertical eye collapse**.

Mitigation

- Increase channel spacing
- Maintain matched trace lengths

Frequency-Dependent Loss

Loss in high-speed channels increases with frequency due to skin effect and dielectric losses.

This behavior effectively creates a low-pass filter, degrading signal rise time and reducing both timing and voltage margins.

Mitigation

- Shorten channel length
- Apply equalization techniques
- Optimize interconnect materials

Reducing channel length directly improves eye opening.

Role of EDA in Chiplet System Design

As chiplet architecture becomes more complex, EDA tools are critical for signal-integrity verification.

An effective SI analysis platform should provide:

1. Standard-aware simulation
2. End-to-end chiplet system analysis
3. Efficient design workflows

Modern tools enable simulation of:

- transmitter and receiver behavior
- interconnect S-parameters
- eye diagrams
- VTF loss and crosstalk

This allows designers to detect performance issues early, before fabrication.

Future Directions

Both UCIe and BoW continue to evolve as the chiplet ecosystem matures, with each standard advancing along paths that reflect its core design philosophy and target applications.

For UCIe, future developments are largely focused on pushing performance boundaries and enabling more advanced integration techniques. This includes support for higher data rates and bandwidth densities, as well as tighter integration enabled by emerging packaging technologies. In particular, there is growing emphasis on 3D die stacking and advanced bump mapping strategies, which aim to improve interconnect density and reduce latency between chiplets. These advancements position UCIe to support next-generation high-performance computing and data-centric applications where scalability and interoperability remain critical.

BoW, on the other hand, is evolving toward broader applicability and increased flexibility across a wider range of use cases. Upcoming developments are expected to expand its scope beyond traditional electrical interconnects to include support for optical interfaces, enabling new possibilities for high-bandwidth and long-distance communication. Additionally, enhancements are being explored for memory integration and more flexible PHY implementations, allowing designers to tailor the interface to specific system requirements. A continued focus on cost-optimized architectures remains central to BoW's evolution, ensuring its relevance in applications where efficiency and simplicity are key priorities.

Enabling Chiplet System Analysis with Keysight's Chiplet PHY Designer

As chiplet architectures become increasingly complex, the need for accurate, system-level signal integrity analysis has grown significantly. Traditional design approaches, which often rely on fragmented simulations or late-stage validation, are no longer sufficient to ensure robust die-to-die communication. To address these challenges, Keysight Technologies provides **Chiplet PHY Designer**, a purpose-built solution focused on standard-driven chiplet system analysis.

Chiplet PHY Designer distinguishes itself by centering its methodology around industry standards, particularly UCIe. Unlike generic signal integrity tools, it is designed specifically to model and validate chiplet PHY behavior in compliance with standard-defined requirements. This includes support for advanced features such as forwarded clocking architectures, including quarter-rate clocking (QDR), which are essential for accurate UCIe simulations. By embedding these standard-specific capabilities directly into the workflow, the tool enables engineers to evaluate compliance and performance much earlier in the design cycle.

A key strength of Chiplet PHY Designer lies in its ability to perform comprehensive, end-to-end system analysis. Designers can model the complete signal path — from transmitter (Tx), through the interconnect, to the receiver (Rx) — within a unified environment. This holistic approach allows for early identification of performance bottlenecks, such as excessive loss, crosstalk, or timing margin violations, reducing the risk of costly design iterations later in the development process. The tool also automates complex calculations, including Voltage Transfer Function (VTF) analysis for both loss and crosstalk, which would otherwise require significant manual effort when dealing with multi-lane interfaces.

Ease of use is another important aspect of the platform. Chiplet PHY Designer incorporates guided setup workflows that streamline the configuration process, allowing users to quickly define key parameters such as the target standard, data rate, and package type. Signal selection and analysis setup are handled through intuitive interfaces, significantly reducing setup time compared to traditional simulation environments. Once simulations are complete, results — including eye diagrams, compliance masks, and performance metrics — can be generated into reports with minimal additional effort.

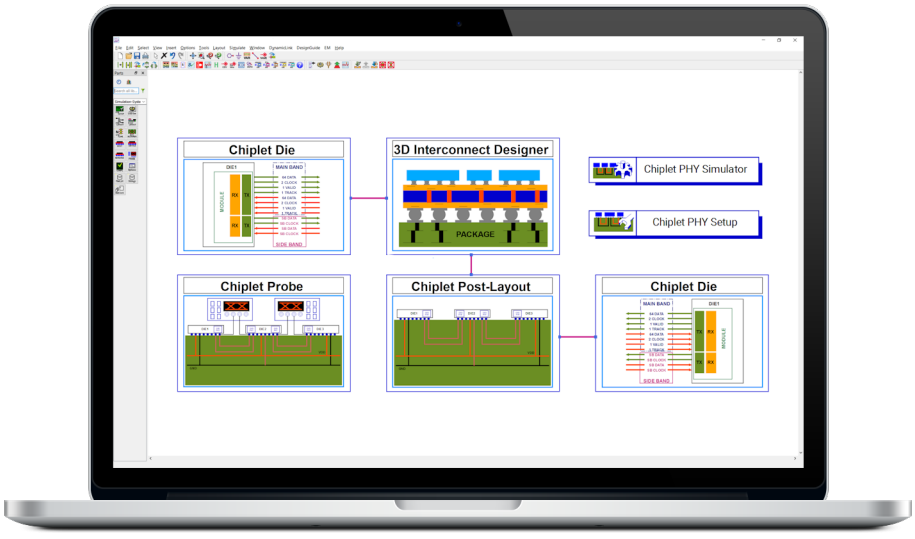


Figure 5. Chiplet PHY Designer interface

The tool also provides strong support for industry-standard modeling techniques. Designers can integrate IBIS-AMI models for both transmitters and receivers, enabling realistic behavioral simulation of high-speed links. For interconnect modeling, transmission lines and vias can be configured within a dedicated environment, while electromagnetic (EM) extracted data can be incorporated through S-parameter blocks. This flexibility ensures that both pre-layout and post-layout analyses can be performed within the same framework, maintaining consistency across the design flow.

Setting up a chiplet simulation within Chiplet PHY Designer follows a structured yet efficient process. Users begin by selecting the appropriate chiplet standard and system parameters through a configuration interface. Interconnect models are then incorporated, either through parameterized elements or imported EM data. Chiplet dies are instantiated using IBIS-AMI models, and connections between dies can be automatically generated, significantly simplifying multi-lane configurations. Measurement points are defined through probe components, allowing designers to evaluate key metrics such as eye diagrams and compliance against standard-defined masks. Once configured, simulations can be executed quickly, providing immediate insight into system performance.

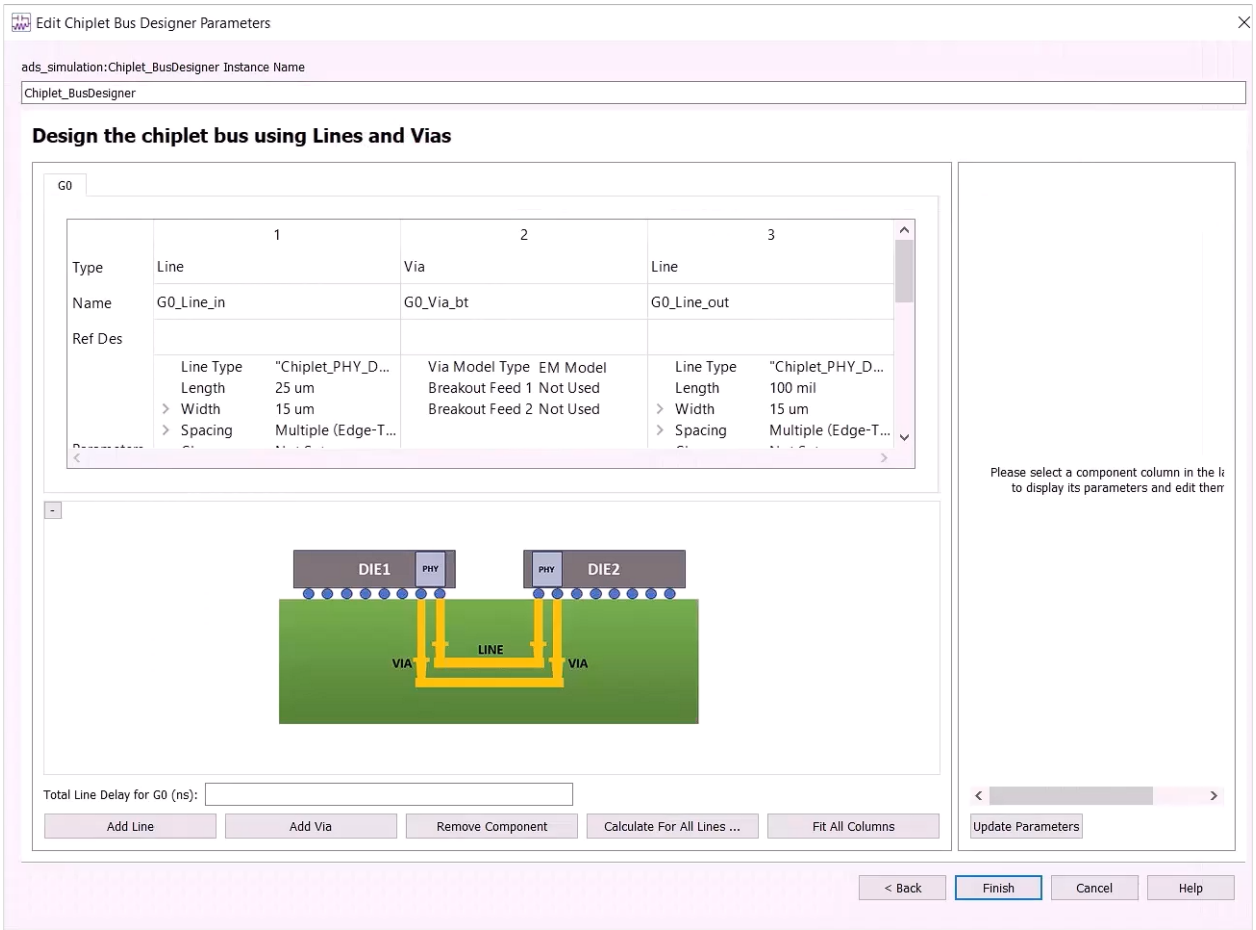


Figure 6. Designing the chiplet bus using Lines and Vias

In practice, this workflow enables designers to validate whether a given chiplet channel meets performance expectations before fabrication. For example, eye diagram analysis can be directly compared against UCIe-defined masks to determine compliance. The ability to predict system behavior early — before committing to silicon — represents a critical advantage in reducing development risk and accelerating time to market.

In summary, Chiplet PHY Designer provides a comprehensive and standard-aware platform for chiplet system analysis. By combining detailed signal integrity modeling, automated compliance evaluation, and an efficient user workflow, it enables engineers to confidently design and validate high-speed chiplet interconnects in an increasingly complex design landscape.

Conclusion

Chiplet architectures are fundamentally reshaping modern semiconductor design by offering a scalable and cost-effective alternative to traditional monolithic integration. By improving manufacturing yield and enabling heterogeneous integration, chiplets provide a compelling solution to the economic and technical challenges associated with advanced process nodes.

Within this context, UCIe and BoW represent two distinct approaches to solving the critical problem of die-to-die communication. UCIe prioritizes interoperability and robustness, providing a comprehensive framework with detailed signal-integrity specifications and clear compliance methodologies. This makes it particularly well suited for ecosystem-driven applications where compatibility across vendors and generations is essential.

BoW, in contrast, emphasizes simplicity and flexibility. Its lightweight structure and minimal constraints make it an attractive option for cost-sensitive designs and tightly controlled system environments. However, this flexibility comes at the expense of detailed guidance, particularly in the area of signal integrity, where designers must rely more heavily on their own analysis and validation techniques.

As chiplet systems grow in complexity and data rates continue to increase, the role of advanced design and verification tools becomes increasingly important. Solutions such as Chiplet PHY Designer enable engineers to perform standard-driven, end-to-end system analysis — from transmitter through interconnect to receiver — while automating complex tasks such as voltage transfer function calculations and compliance checking. By allowing designers to identify and resolve signal integrity issues early in the design cycle, these tools help reduce development risk and accelerate time to market.

Ultimately, the choice between UCIe and BoW depends on the specific priorities of the system being designed. Applications requiring standardization and long-term scalability will benefit from UCIe, while those focused on rapid implementation and cost optimization may find BoW to be the more practical solution. As chiplet adoption continues to accelerate, the importance of robust signal-integrity analysis and advanced EDA tools will only grow, reinforcing their role as essential components of successful chiplet system development.

To learn more, visit W3650B Chiplet PHY Designer | Keysight

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