

Mitigating Signal Integrity Challenges in High-Speed Chiplet Designs

Executive Overview

As system's data speed continues to increase, Signal Integrity (SI) impairments have become critical factors affecting reliable data transmission. High-performance systems require clean and error-free data communication between different functional blocks, engineers need a tool to qualitatively or quantitatively evaluate the system performance. An eye diagram provides a functional way to evaluate this performance. Ideally, an open and clean eye diagram represents error-free data transmission — the ultimate goal for any high-speed digital system design. However, real-world systems inevitably experience signal impairments that degrade performance and can lead to data errors.

This whitepaper explores common signal integrity challenges, their manifestations in eye diagrams, and practical methods to analyze and mitigate the impairments in modern chiplet-based systems. It also highlights the importance of the Universal Chiplet Interconnect Express (UCIe) standard for high-speed, multi-die architectures.

Signal Integrity Impairments

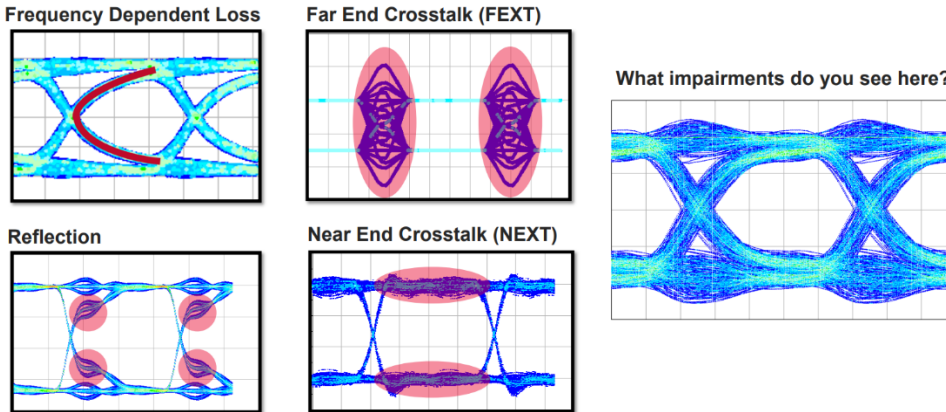
Signal impairments in high-speed systems can arise from a variety of sources, broadly categorized into material-related and design-related sources:

Material-related impairments: These include surface roughness, conductor losses and dielectric losses, which stem directly from the Printed Circuit Board (PCB) or package materials and manufacturing constraints.

Design-related impairments: These include crosstalk and reflections due to impedance mismatches. These can often be mitigated through careful layout and design adjustments, including routing, termination, and impedance control.

Common impairments and their signature to eye diagram:

- **Frequency-dependent loss:** Higher-frequency components of a signal are attenuated more than lower-frequency components, causing slopes in the eye diagram.
- **Reflections due to impedance mismatches:** Reflections distort waveform's rising and falling edges and appear as dips or ripples in the eye.
- **Far-end crosstalk (FEXT):** Noise originating from adjacent far-end channels at signal transitions. Sometimes it is shifted to the middle of eye in memory systems due to skew or half-UI clocking delays.
- **Near-end crosstalk (NEXT):** Typically manifests as plateau-like amplitude noise in the middle of eye, reducing eye margin and further degrading eye quality.



Diagnosing Crosstalk with Eye Diagrams

When it comes to identifying crosstalk issues, we can often spot them with a simple examination of the eye diagrams. For example, let's consider an 8-byte lane memory system. In this setup, we have 64 drivers on the data bus. All of these drivers are active, generating crosstalk — whether it's near-end or far-end — which degrades the overall eye performance. The closed eye in this diagram is a direct result of the cumulative effect of crosstalk from all these active drivers. While this observation is really helpful for evaluating the figure of merit of systems, including margin quality, it doesn't necessarily give us much insight into which specific drivers are the primary culprits responsible for that eye closure.

To pinpoint the root cause, engineers typically employ two key strategies:

Single-driver driven test: Make only one driver is active at a time while others are silenced. This isolates each driver's crosstalk contribution.

Accurate termination impedance: To make sure the termination impedances are properly set, the other silenced drivers impedance should be determined dynamically by using IBIS models than assuming a fixed termination. This provides a more accurate representation of the real system.

By repeating this process for all drivers, engineers can measure far-end and near-end crosstalk waveforms quantitatively and identify the dominant aggressors affecting the eye closure.

Advanced Crosstalk Analysis with Keysight EDA

To streamline this analysis, Keysight EDA provides the Crosstalk Analyzer within Chiplet PHY Designer and Memory Designer in ADS. This solution allows engineers to configure and simulate crosstalk scenarios using a structured and repeatable workflow.

Designers begin by enabling the Crosstalk Analyzer and configuring aggressors under single-driver conditions. Multiple aggressor modes are supported, including continuous switching, single-bit patterns, and step-rise or step-fall excitations. These modes allow engineers to model realistic switching behaviors and stress the channel in a controlled manner.

Once the aggressor is defined, its waveform propagates through the channel and interacts with victim signals. Victim behavior is modeled dynamically by selecting pull-up (high) and pull-down (low) states, each of which exhibits distinct impedance characteristics. Accurately capturing these differences is critical for realistic crosstalk analysis.

The probe component is then placed at key locations to measure crosstalk voltages independently of the data signal. Engineers can define pass/fail thresholds directly within the probe and automatically generate detailed HTML reports. These reports summarize results across all aggressors, providing a clear and actionable view of system-level crosstalk performance.

UCle Overview and High-Speed Chiplet Architectures

The **Universal Chiplet Interconnect Express (UCle)** standard is rapidly gaining adoption for multi-die packaging. Key advantages include:

- **High bandwidth:** Data rates up to 32 Gb/s per pin enables ultra-fast communication between chiplets.
- **Scalable architecture:** Mixed technology nodes (e.g., 40 nm with 5 nm) can interconnect using a standardized interface.
- **Interoperability:** Standardization allows components from multiple vendors to interoperate, reducing cost and enhancing design flexibility.

A typical UCle module includes:

- **TX side:** 16 single-ended data signals, a differential clock, TX valid, TX track, and two sideband signals (data and clock), totaling 22 signals.
- **RX side:** 16 single-ended data signals, a differential clock, RX valid, RX track, and two sideband signals, also totaling 22 signals.

Mitigating Crosstalk in UCle Multi-Die Systems

Modern chiplet designs feature hundreds of single-ended signals operating at 16 Gb/s, with 32 Gb/s and above expected in the near future. Accurate modeling of these dense interconnects is critical for reliable package design.

A robust workflow for crosstalk analysis includes:

- Accurate EM extraction of UCle channel model that represents a die-to-die interface.
- Compliance and link margin analysis such as VTF loss/crosstalk and eye diagram
- Perform the crosstalk analysis to identify the worst-case aggressor
- Optimize the layout to mitigate the crosstalk such as adding return vias to improve signal integrity.
- Verifying improvements via eye diagram analysis, ensuring high-quality data transmission.

This workflow supports the sign-off of advanced package designs for high-performance applications, such as data centers and aerospace systems, where bandwidth, density, and power efficiency are critical.

Case Study: Crosstalk Mitigation in a 16 Gb/s UCle Chiplet Package

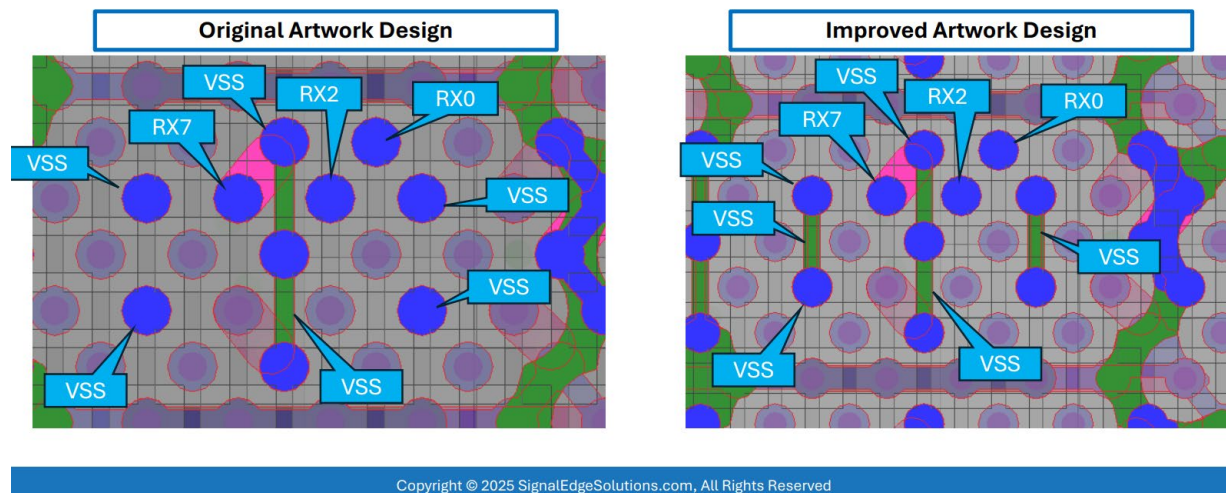
A 16 Gb/s UCle chiplet package with a 256-lane die-to-die interface was analyzed to address signal integrity challenges. The package uses a typical organic stack-up, and full electromagnetic (EM) extraction was performed using **Keysight ADS SIPro**, including copper roughness models to ensure realistic loss and coupling behavior. High-speed interconnects between chiplets can experience interference between signals, known as crosstalk, which can reduce signal clarity and potentially lead to data errors. The case study illustrates how systematic analysis and targeted layout adjustments can improve performance and ensure compliance with UCle standards.

Problem Identification

Initial analysis indicated that while overall signal loss in the package was within acceptable limits, several signals were affected by crosstalk. Time-domain evaluations using eye diagrams, a visual representation of signal quality, showed reduced eye margins on multiple data lines. These findings suggested that certain signals were affected by the crosstalk from adjacent data lines, which resulted in VTF crosstalk and eye margin compliance violation.

Analysis and Root Cause

A detailed review of the package layout and signal behavior revealed that the highest levels of interference occurred near the transition region of one die. To determine the worst-case aggressor, the Chiplet PHY Designer Crosstalk Analyzer was used. Single-pulse simulations were run to measure coupling into RX2 from neighboring signals. Specific signals were identified as contributing more heavily to the crosstalk, with one signal in particular producing the largest impact on neighboring lanes. This assessment allowed the engineering team to focus mitigation efforts on the most critical areas.



Mitigation Approach

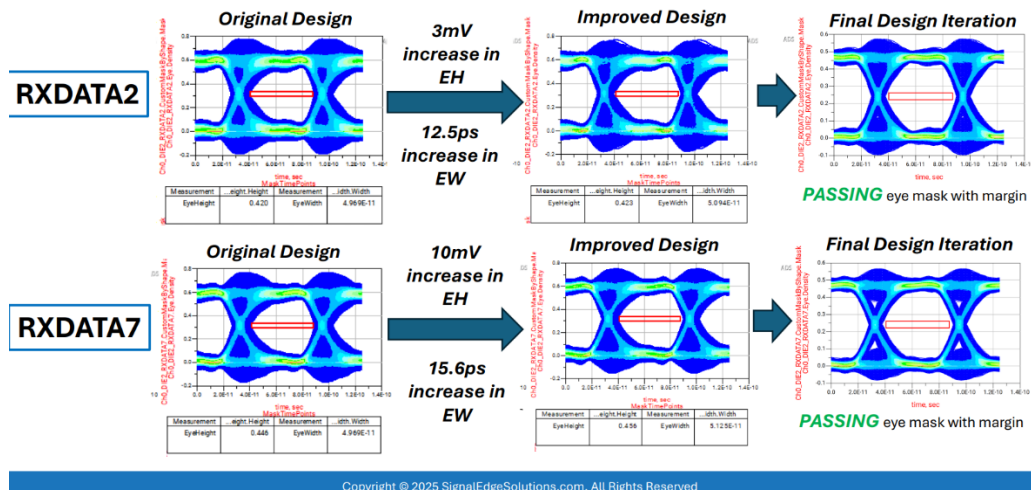
Targeted layout improvements were implemented to reduce signal interference. Additional grounding paths and return connections were strategically added near the affected signals to minimize coupling and improve current return paths. These changes were designed to address the crosstalk issue without requiring a major redesign of the package.

Results

Post-mitigation analysis showed significant improvements in signal quality:

- Crosstalk between critical signals was reduced.
- Eye diagrams for all affected lanes passed the UCle compliance mask.
- Key signal parameters, such as timing and voltage margins, increased, enhancing overall reliability.

For example, affected lanes demonstrated improved eye height and width, sufficient to restore signal integrity and meet compliance requirements.



The case study demonstrates that a methodical approach — identifying affected signals, isolating the primary sources of interference, and applying targeted layout enhancements — can effectively mitigate crosstalk in high-speed chiplet packages. This workflow ensures reliable operation and compliance without requiring extensive redesign, providing a practical methodology for advanced multi-die system designs.

Conclusion

No designer wants crosstalk in high-speed digital designs; however, completely eliminating it is often impractical. Crosstalk can nevertheless be effectively mitigated by understanding its underlying mechanisms and applying appropriate mitigation techniques, as demonstrated in the case study. Streamlined, automated crosstalk analysis enables engineers to pinpoint primary contributors early in the design process, helping to avoid costly last-minute design iterations.

High-speed chiplet systems demand careful attention to signal integrity to ensure reliable, error-free data transmission. By understanding the sources of signal impairments, leveraging eye diagram analysis, and applying advanced analysis tools such as Keysight EDA Crosstalk Analyzer, engineers can systematically identify and mitigate crosstalk, as demonstrated in the UCle case study.

To learn more, visit [W3650B Chiplet PHY Designer | Keysight](#)

To get a free evaluation visit [FREE Evaluation of ADS | Keysight Technologies](#)

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