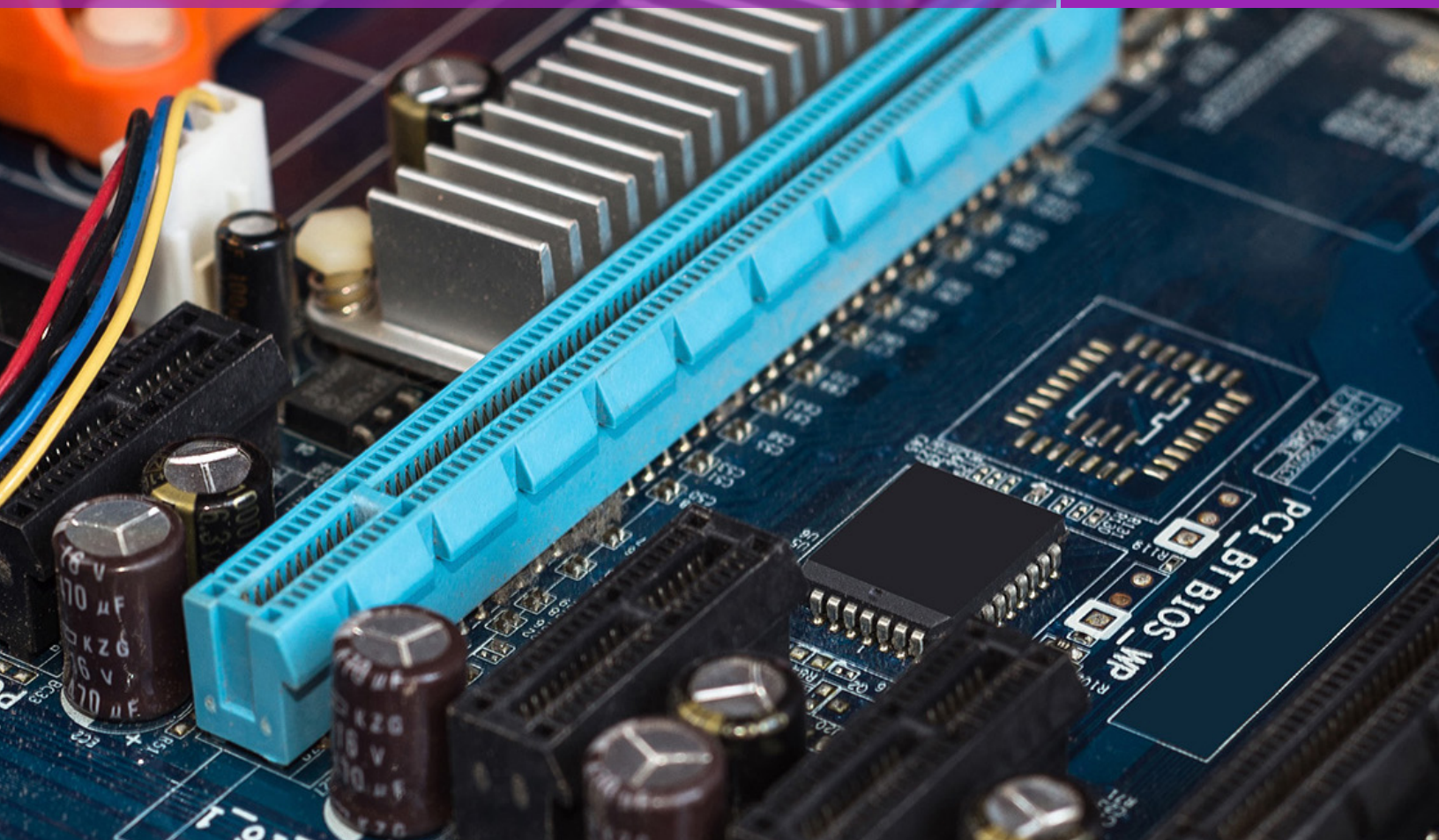




Essential Insights for Design PCIe® 6.0 Interconnects

Automate the setup and simulation for PAM4 PCIe systems
using a smart design environment

Table of Contents

Introduction..... 3

Design Challenges of PCIe 6.0 4

Accelerating Compliance: Simulation and Automation..... 7

Measurement Correlation: The Link Between Simulation and Reality 11

Optimizing Designs: Retimers and Equalization.....14

Shortening Test Time: Software-Driven Compliance.....17

Conclusion.....18

Introduction

PCI Express® (PCIe®) is a widely used serial communication protocol designed to deliver significantly more data than the existing PCI standard. Figure 1 illustrates the evolution of this technology across several generations, characterized by increasing data rates and incorporating new functionalities. In the latest version, PCIe 6.0, the data rate doubled to 64 GT/s, enabling up to 256 GB/s of bandwidth in an x16-lane configuration. PCIe 6.0 introduced technologies such as PAM4 signaling pulse-amplitude modulation, with four levels, and forward error correction (FEC) to achieve such high speeds while improving signal integrity and reliability.

However, PCIe 6.0 challenges the design and verification process, requiring more stringent specifications and tighter margins for the physical layer (PHY) and electrical and mechanical interfaces. At such high speeds and with denser circuitry, crosstalk, jitter, noise, and channel loss can degrade the performance and functionality of the PCIe link. Consequently, designers need to adopt effective strategies and tools to address these challenges and ensure the compliance and interoperability of their PCIe 6.0 devices and systems.

This white paper provides a comprehensive guide on how PCIe 6.0 can boost the efficiency of high-speed digital designs and address implementation hurdles. Learn how to overcome these challenges using sophisticated simulation and virtual prototyping tools.

PCIe evolution

Since its debut in 2003, PCI Express began with a data rate of 2.5 GT/s (gigatransfers per second). The throughput doubled with each version of PCIe, and the time between the introduction of these new versions has varied between two and seven years.

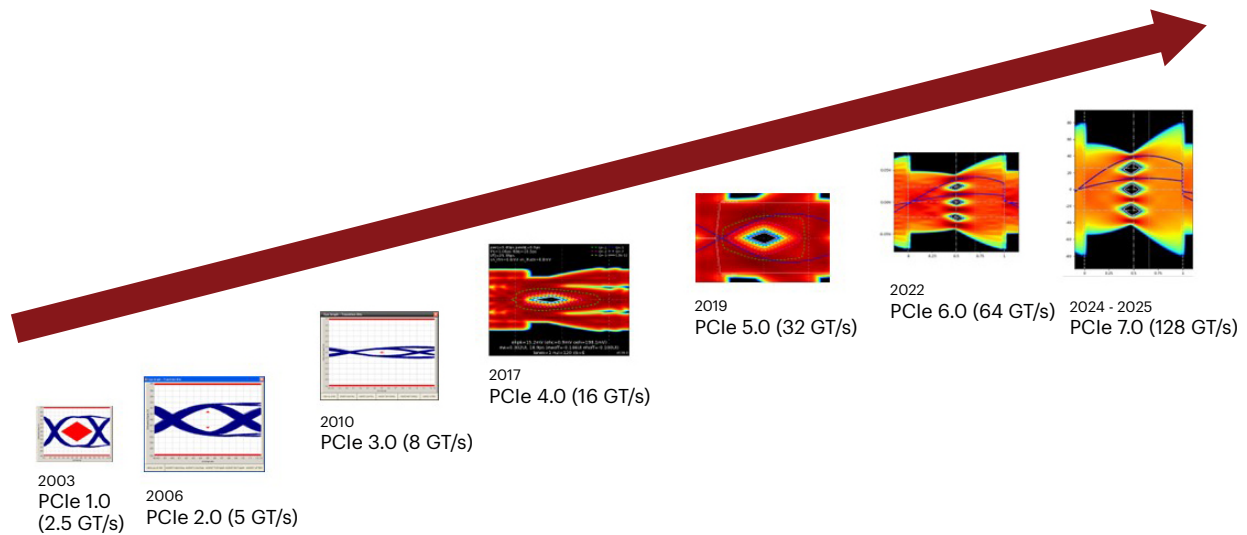


Figure 1. PCIe generations from 2003 to 2024

Design Challenges of PCIe 6.0

Adopting PCIe 6.0 presents several challenges and advancements in data transfer technology. The following is an overview of the key aspects of each respective area.

Signaling

The transition from non-return-to-zero (NRZ) signaling used in previous PCIe generations to pulse amplitude with four levels (PAM4) is one of the significant changes in PCIe 6.0. While NRZ uses two signal levels to represent binary data, PAM4 uses four levels, effectively doubling the data rate for a given baud rate. This shift enables PCIe 6.0 to achieve higher data transfer rates without increasing the channel bandwidth. However, it also introduces a higher bit error rate (BER) due to the smaller eye openings in PAM4 signaling, which makes it more susceptible to noise and errors.

NRZ versus PAM4

Non-return-to-zero is the encoding format used for earlier generations of PCIe signal lanes, and numerous other standards like gigabit Ethernet. PAM4 doubles the bandwidth by using four discrete logic levels instead of just two, as is the case with NRZ.

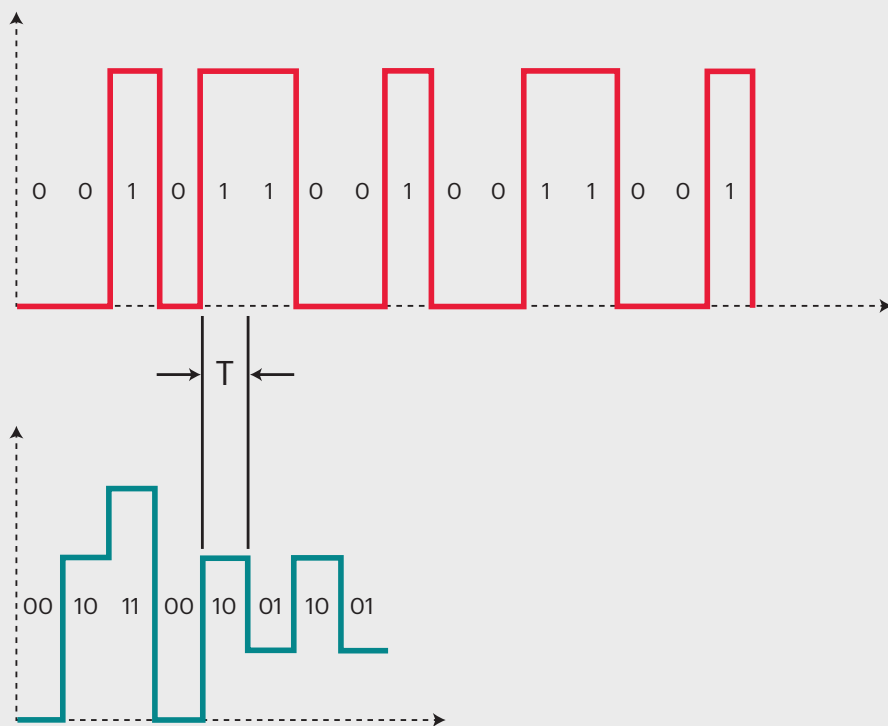


Figure 2. NRZ (top) versus PAM4 (bottom) encoding

Jitter

Jitter is the deviation from a signal's true periodicity. Because of the narrower eye openings of PAM4 signals, jitter is more critical in PCIe 6.0 than in previous generations. The transition to PAM4 requires tighter noise and jitter tolerances to ensure reliable data transmission.

Forward error correction

The PCIe 6.0 standard introduces a new feature, FEC, which addresses the elevated BER resulting from PAM4 signaling. Forward error correction works by adding redundancy to the transmitted data, enabling the receiver to detect and correct errors without retransmitting.

However, FEC algorithms can be complex, and their complexity increases exponentially with the number of bytes that require correcting. Validating these algorithms entails confirming their effectiveness in error correction, verifying that they do not introduce excessive computational overhead, and ensuring their harmonious integration with other PCIe 6.0 features, such as the cyclic redundancy check (CRC).

Decision feedback equalization

The decision feedback equalization (DFE) technique illustrated in Figure 3, uses a strategy to mitigate the effects of intersymbol interference (ISI). The DFE process uses feedback from past decision data to subtract the expected ISI and clean up the received signal. This approach enables more accurate decision-making regarding the current symbol. Validating DFE in PCIe 6.0 involves testing the equalization process to ensure it effectively compensates for ISI and supports the high data rates of the new standard. This method requires accurately modeling this dynamic behavior to ensure that DFE mitigates ISI without introducing additional noise or distortions.

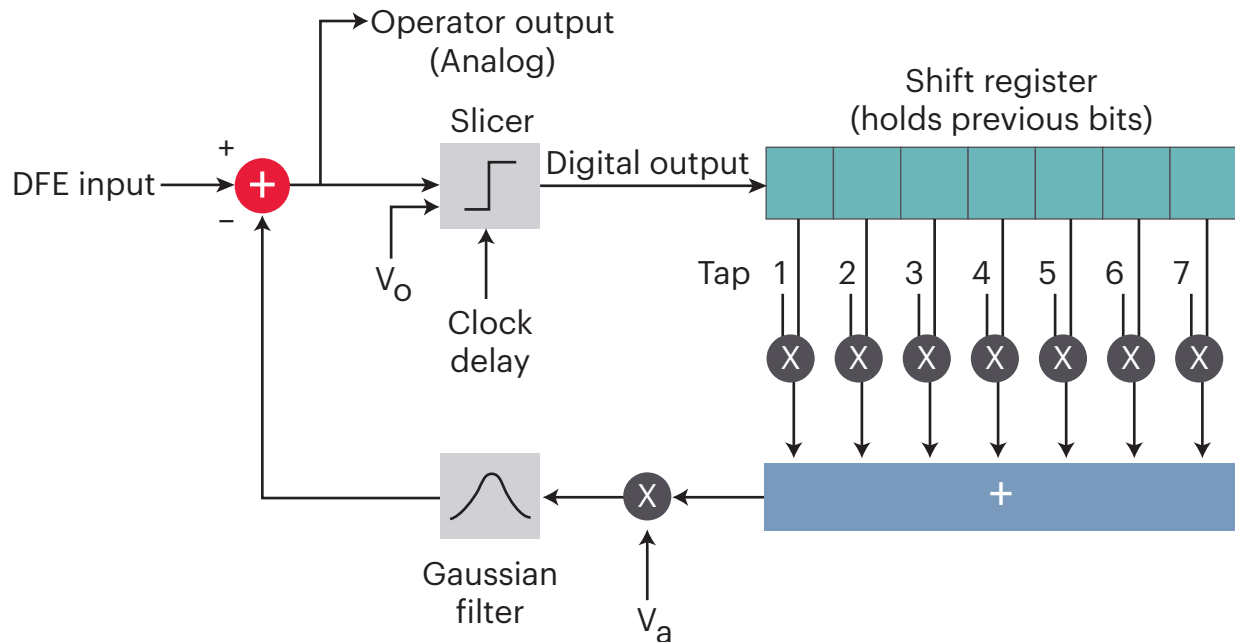


Figure 3. DFE block diagram

Overall, the adoption of PCIe 6.0 brings about a significant leap in performance but also requires careful consideration and validation of these new features to ensure robust and reliable operation in high-speed data transfer applications.

Accelerating Compliance: Simulation and Automation

The principal challenge in designing high-speed digital electronics is that designers are often venturing into uncharted territory, leading to important questions, such as:

- How do you characterize brand-new silicon without the actual hardware for lab measurements?
- How do you characterize connectors, packaging, and printed circuit boards (PCBs)?
- How do you validate your signal and power performance assumptions without spinning multiple versions of a physical prototype?

These questions underscore why designers and hardware engineers use electronic design automation (EDA) tools equipped with accurate modeling and simulation capabilities.

Electronic design automation tools are software applications that automate and facilitate the design and verification of electronic systems. These tools provide various capabilities and features, such as schematic capture, layout generation, circuit simulation, signal integrity analysis, power integrity analysis, timing analysis, design rule checking, functional verification, compliance testing, and debugging. By modeling and simulating the behavior and performance of the PCIe 6.0 system earlier in the design process, electronic design automation tools can facilitate higher-quality prototypes that pass on the first attempt.

Simulation is common in modern EDA tools as a method of using mathematical models and algorithms to emulate the behavior and performance of a real system. Simulation can help evaluate and optimize the designs under various scenarios and conditions. Depending on the design's objectives and requirements, you can use this approach at various levels of abstraction and accuracy, including behavioral, functional, logical, physical, and mixed-signal. However, for a simulation to be effective, accurate models of signal sources, receivers, and signal paths are necessary.

Traditionally, the input / output buffer information specification (IBIS) models the inputs and outputs of the system's chips. The IBIS Open Forum is the industry consortium responsible for creating and advancing the IBIS and related specifications.

Semiconductor manufacturers provide IBIS-AMI model files to their customers designing the system. However, the IBIS-AMI model is often unavailable when designing new components.

IBIS-AMI

The input / output buffer information specification (IBIS) defines a file format which is universally applicable in most simulation and signal integrity tools currently available. The IBIS file may be as simple as modeling the I/O buffer voltage versus current (VI) curves, but usually includes key details such as power supply clamping, slew rate, drive strength, chip-package-ball channel models, and more.

With complex high-speed systems, it became necessary to model more information about the signal itself. To enable this advanced modeling, the IBIS Open Forum introduced IBIS-AMI (AMI represents an algorithmic modeling interface) to provide a self-contained I/O buffer and dynamic algorithm-based behaviors to model other factors like equalization and error-correction schemes.

The following are options to mitigate the lack of IBIS-AMI models:

Generic models

Use a generic IBIS model from a library provided with the EDA tool of your choice. While this is less accurate, it is often adequate if the library provided comes from a tool vendor that is deeply involved in creating new interconnect standards, as is the case with Keysight, a member of the Peripheral Component Interconnect Special Interest Group (PCI-SIG).

Creating the model from scratch can be challenging, especially without access to silicon. Ideally, you would want to be able to measure it to validate the model. However, it is possible with the right input data and knowledge of the signaling interface, albeit time-consuming and difficult.

PCIe modeling interface

Use the Keysight PCIe algorithmic modeling interface (AMI) model builder software available in Keysight ADS to build AMI models quickly and easily. Figure 4 illustrates a wizard tool that guides you through the process of selecting transmitter / receiver, linear equalization, gain control, compensation, decision-feedback equalization, and loop filter parameters by outputting the model files.

The PCIe AMI model builder provides accurate models with the right standards-based configuration inputs, which are typically available before silicon vendor models. These models are highly accurate because the algorithms generated have decades of experience building high-speed test and measurement tools. Models serve as the foundation for signal sources in simulation.

As Figure 4 illustrates, you can source these models from the silicon vendor or library. Furthermore, you can generate models using tools like the PCIe AMI model builder. If the models are standard-compliant, you can import them into your library and use them in your designs.

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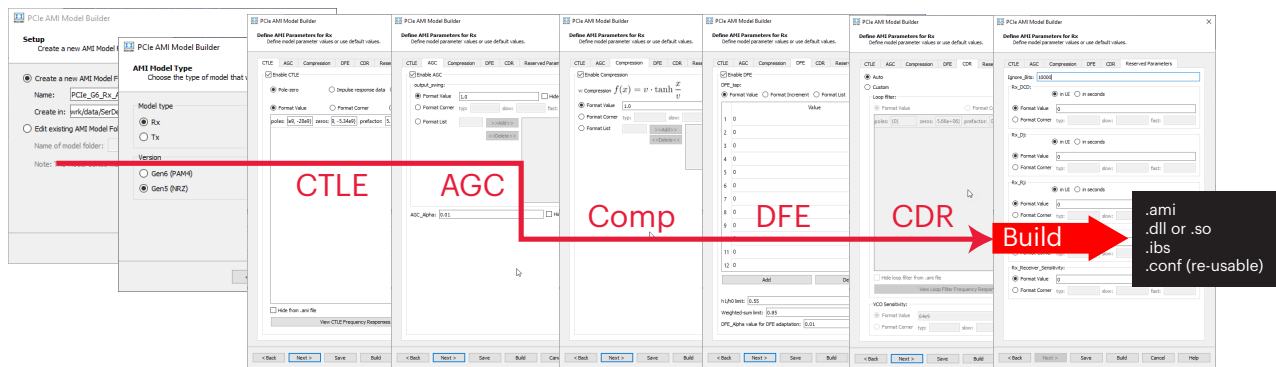


Figure 4. PCIe AMI model builder and ADS solution working together

Measurement Correlation: The Link Between Simulation and Reality

Simulation and measurement correlation bridges the gap between theoretical models and real-world behavior, leading to better designs and more reliable electronic systems. The following aspects are examples of the benefits of consistent correlation across the design process:

Model validation and verification

Correlating simulation results with actual measurements validate and verifies the accuracy of the models. This process ensures that the simulated behavior aligns with the observed behavior in practice.

De-embedding and equalization

For accurate measurements, high-speed electronic systems often need to post-process data during the de-embedding and equalization stages. De-embedding involves removing the effects of measurement circuits, such as test fixtures and probes, from the acquired data. This step enables engineers to isolate the intrinsic behavior of the device under test. Equalization compensates for signal distortions caused by transmission lines, connectors, and other components. By applying equalization, engineers can open closed eyes in the received waveform. Correlating simulation and measurement results ensures that the de-embedded and equalized data match, providing confidence in the accuracy of the measurements.

Streamlined workflow with end-to-end EDA tools

Implementing a new PCIe design when you have varying numbers of multilink, multilane, and multilevel (PAM4) systems, including the AMI model generation for transmitters, repeaters, and receivers, can be daunting. The System Designer for PCIe® automates the setup and simulation of PCIe systems using a smart design environment integrated with a simulation-driven compliance test solution that minimizes design iterations and shortens time to market.

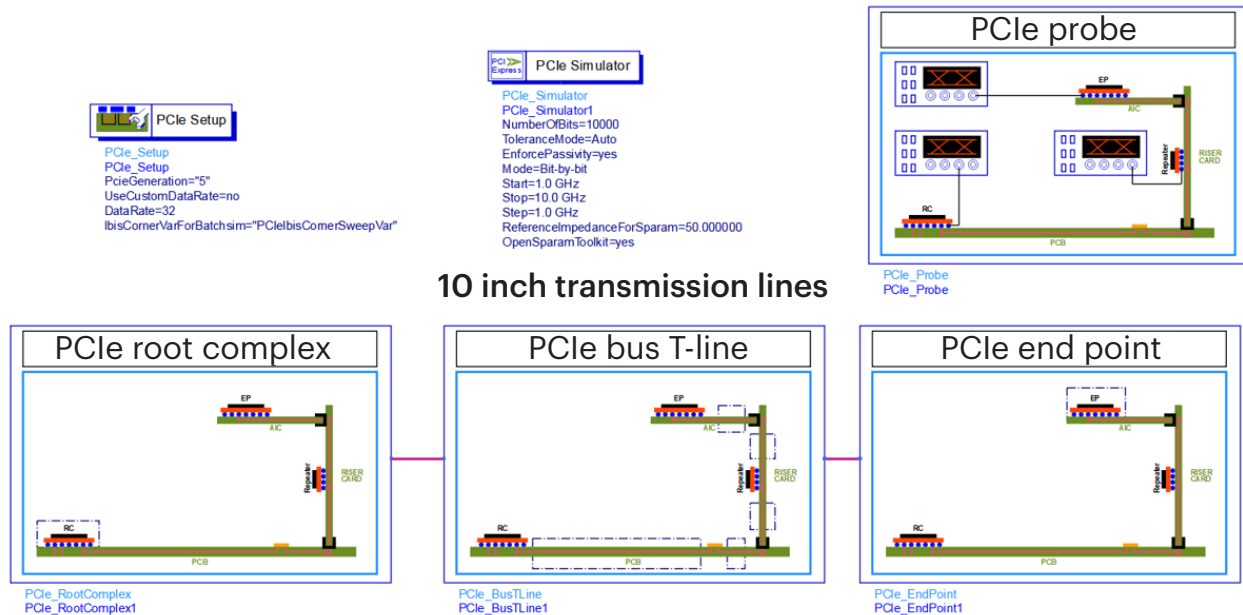


Figure 5. Example of an ADS schematic of a PCIe 6.0 design ready for simulation

S-parameter modeling

Designers use scattered parameters (S-parameters) to model multiport signal networks mathematically. This modeling process enables designers to stimulate a chosen port, record the transmission through other ports, and reflect the information to the source port. This process gives the designer a clear understanding of the design's behavior in frequency domains. The S-parameters analyze the system's behavior during simulation. S-parameters are physically measurable using advanced instruments such as a **Keysight vector signal analyzer** (VNA), shown in Figure 6. Correlating S-parameter-based simulations with actual measurements provides insights into system performance and helps to identify discrepancies. Simulation and measurement correlation leads to better designs and more reliable electronic systems.

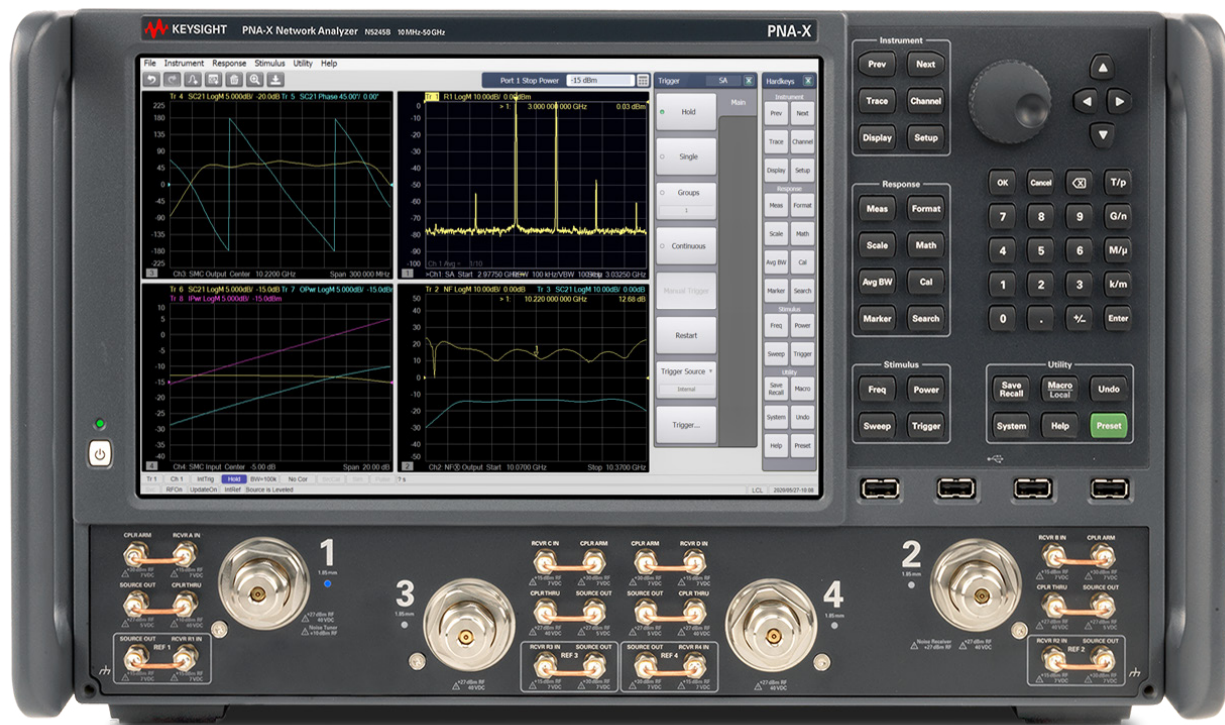


Figure 6. Keysight PNA-X vector network analyzer

Optimizing Designs: Retimers and Equalization

PCIe 6.0 retains the same basic channel hardware as PCIe 5.0. However, it uses a new signaling method. Specifically, PCIe 5.0 uses NRZ with a nominal channel loss budget of 36 dB. Contrastingly, PCIe 6.0 employs PAM4, which requires a tighter channel loss budget of 32 dB to reflect the increased sensitivity to signal degradation and the need for better-quality channels to support the higher data rates. As a result, PCIe 6.0 requires novel approaches for equalization and long-distance synchronization.

Transmitter equalization

You can add transmitter (Tx) equalization (EQ) for pre-emphasis to overcome the channel's natural low-pass filter nature. While this is a function of silicon, you can preconfigure PCIe devices with a set of filter coefficients. When chosen correctly, the filter coefficients speed up the channel link process between the root complex and the end-point device.

Receiver continuous time linear equalization

While Tx equalization adds pre-emphasis to overcome the channel's low-pass filter response, it is prone to amplify noise and crosstalk transients. As a result, it is necessary to add additional equalization at the receiver. PCIe 6.0 uses a three-zero, six-pole infinite impulse response (IIR) filter for Rx continuous time linear equalization (CTLE), compared to a two-zero, four-pole for PCIe 5.0. The additional pole and zero offer steeper roll-off in the stopband with more passband ripple options.

Decision feedback equalization — 16-tap

The inherent limitation of transmitter equalization and Rx CTLE is that they operate on the entire signal, thereby incorporating all sources of noise, including crosstalk, noise, jitter, and intersymbol interference. Intersymbol interference is important as it can interact with the channel and introduce distortion. PCIe 6.0 uses 16-tap DFE at the receiver compared to PCIe 5.0 three-tap DFE. As the data rates increase with each generation of PCIe, the channel's frequency-dependent loss becomes more significant. The increase from three taps in PCIe 5.0 to 16 taps in PCIe 6.0 allows for more precise correction of the signal, which is necessary due to the higher speeds and associated challenges such as increased insertion loss and crosstalk.

You can use the 16 adjustable coefficients or taps to cancel out ISI. The 16-tap DFE design is more complex but provides finer control over the signal, enabling better optimization of high-speed data transmission. Comparatively, a three-tap DFE is simpler in design and less capable of compensating for complex channel conditions. Figure 7 illustrates that with the advancement of PCIe technology to PCIe 6.0, which incorporates higher data rates and PAM4 signaling, more sophisticated DFE designs, like the 16-tap DFE, are necessary to maintain signal integrity over the transmission channel.

Redrivers and retimers

Redrives and retimers can amplify, reshape, and retransmit the PCIe signals to maintain the required maximum channel loss and keep the timing within skew tolerance across the entire system.

Figure 8 illustrates the typical placement of retimers in the PCIe signal path. Retimers are transceivers with built-in equalization (CTLE and DFE), deskew, and retransmit capabilities. They typically contain their own microprocessor for smart configuration, link training, and diagnostics. In contrast, redrivers will amplify and reshape the signal without further processing. The ADS solution with the System Designer for PCIe® bundle enables users to model and perform parametric sweeps and experimentation with redriver or retimer placement within the overall signal path.

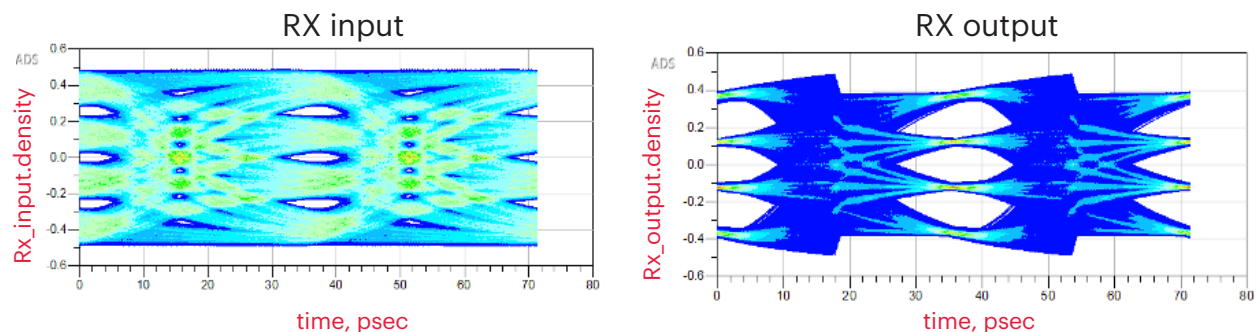


Figure 7. The left illustration shows the PCIe 6.0 eye pattern without DFE, which does not pass the PCI-SIG specification. The right illustration shows the same design after applying 16-tap DFE, now passing PCI-SIG specification.

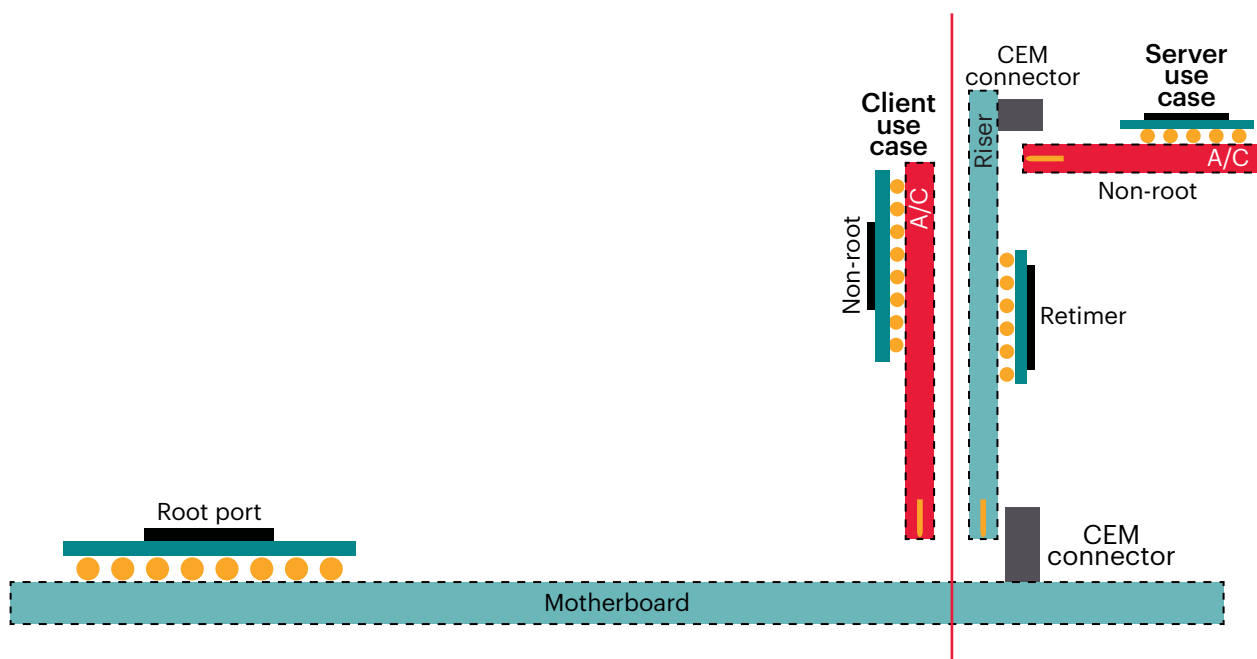


Figure 8. Examples of a typical PCIe channel signal path for a client use case for a short channel and a server use case for a longer channel

Furthermore, with prior PCIe generations, the specification focused on signals measured at the device pin or package balls. This approach enabled physical measurement using differential probes and interposers. In the context of PCIe 6.0, Tx EQ, Rx CTLE, and DFE have become significantly more involved. However, directly evaluating the equivalent received bit patterns is impossible, as designers cannot probe into the silicon. Consequently, simulation becomes even more critical, enabling the designer to probe inside the transmitter and receiver devices.

Shortening Test Time: Software-Driven Compliance

Each generational change of a standard introduces new compliance test challenges for digital designs. Software-driven compliance is a technique that uses software tools to perform automated compliance testing and analysis for electronic designs. Software-driven compliance plays a pivotal role in ensuring that designs adhere to industry standards, regulations, and performance benchmarks before they reach the manufacturing stage.

Designers integrate compliance checks into the design process to avoid costly rework and delays that could arise at later stages in the workflow. Figure 9 illustrates a software-driven compliance workflow that facilitates a more streamlined process. Automated tools can quickly identify and rectify compliance-related issues, thereby accelerating the design cycle and reducing time to market.

Simulation driven virtual compliance test

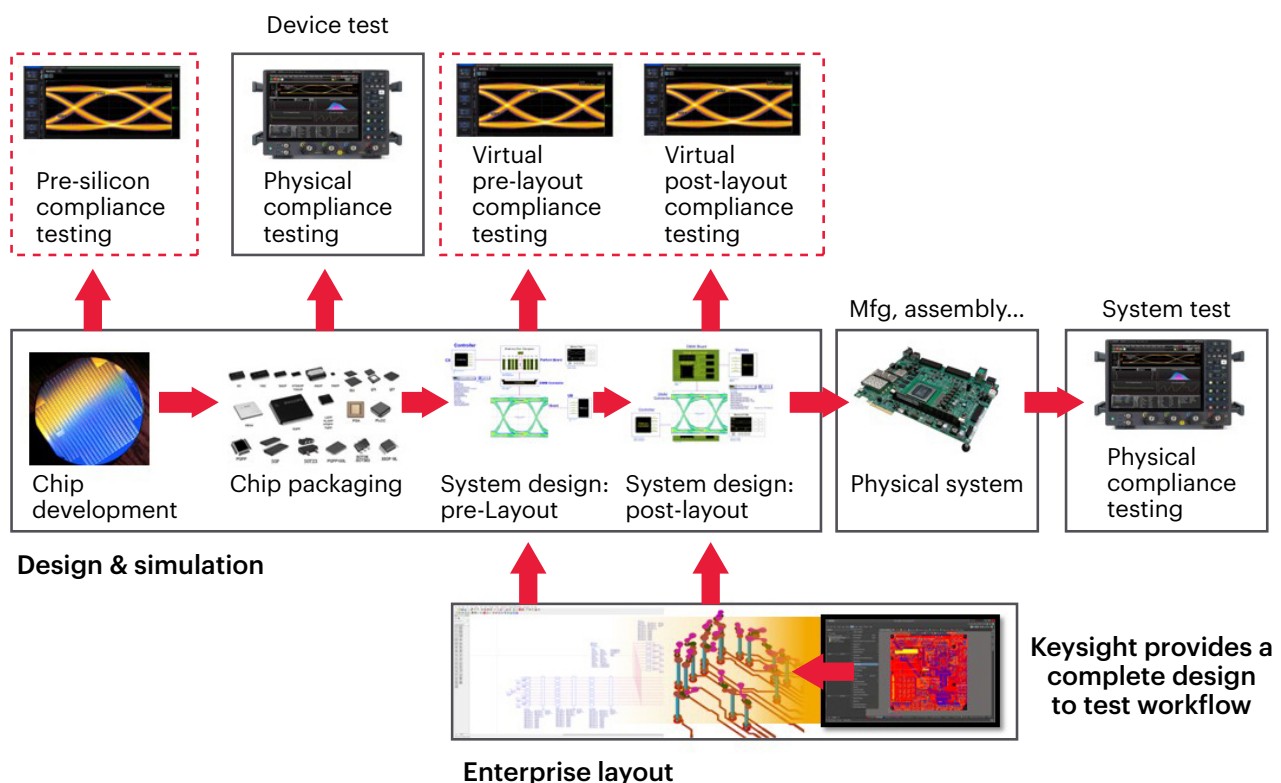


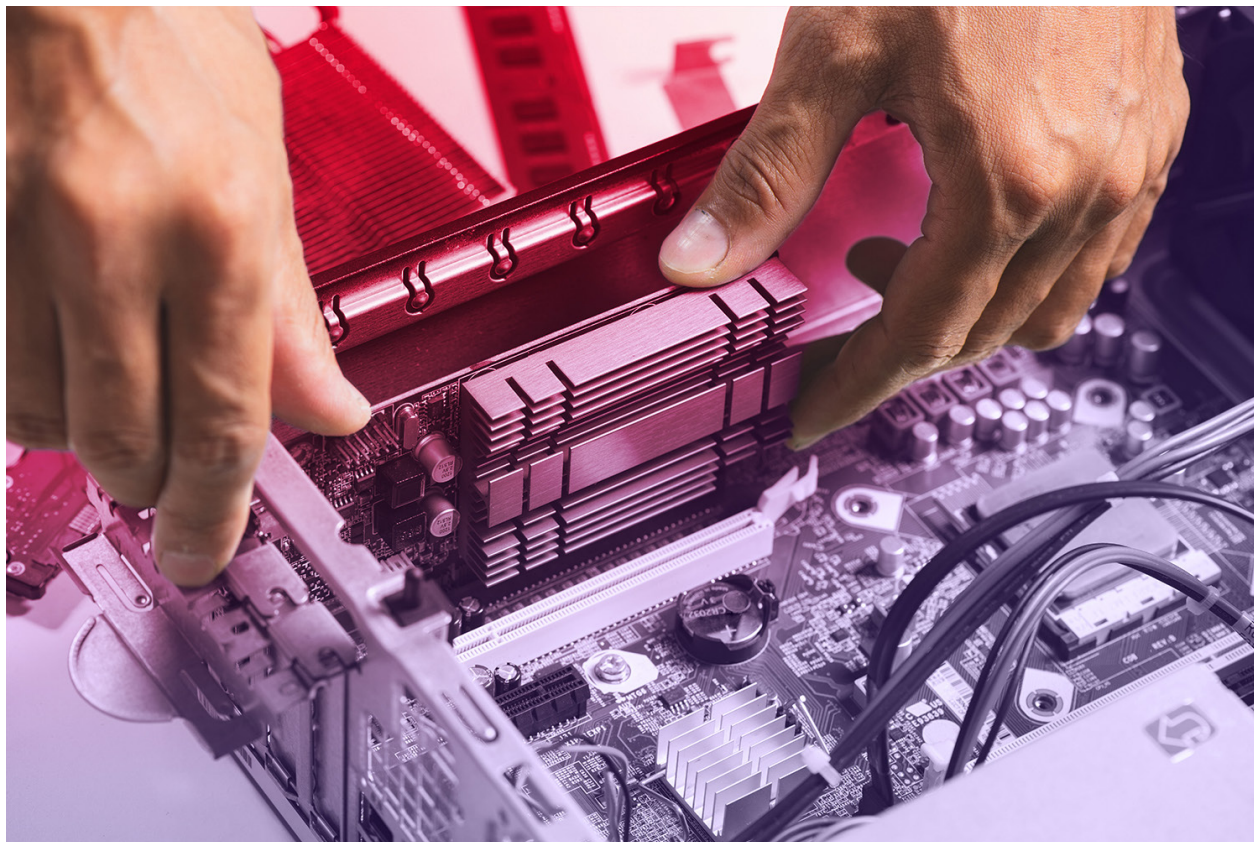
Figure 9. Simulation-driven virtual compliance workflow

Software-driven compliance is an essential part of the PCIe 6.0 design workflow, as it helps designers overcome the challenges and complexity of the PCIe 6.0 standard and deliver high-quality electronics faster and more efficiently.

Conclusion

PCIe 6.0 is the latest and fastest PCIe standard, offering unprecedented data rates and bandwidth for high-speed digital systems. However, PCIe 6.0 also introduces significant challenges and complexity to designing and verifying the PCIe physical layer, the electrical and mechanical interface, and the protocol layer.

As a result, to ensure the compliance and interoperability of their PCIe 6.0 devices and systems, designers must adopt effective strategies and tools that can address these challenges. Electronic design automation tools, coupled with simulation, provide designers with robust and versatile simulation capabilities to model the performance of PCIe 6.0 systems. Designers can address design issues earlier in the workflow and reduce the need for physical prototypes.



The **Keysight ADS** solution with the **System Designer for PCIe®** bundle enables accurate crosstalk and skew (lane-to-lane), equalization, and channel parameter sweeping to converge on the optimal design. The solution automates the setup for multilink, multilane, and multilevel (PAM4) PCIe systems using a smart design environment. The PCIe algorithm modeling interface (AMI) modeler, which supports NRZ and PAM4 modulations, facilitates the quick implementation of PCIe systems. The integrated simulation-driven compliance test solution can reduce design costs by minimizing design iterations and shortening the time to market.

Learn more

- Discover the methods of implementation, read the **PCIe Automated Test Application reference guide**.
- Achieve high-speed digital design success using a holistic design approach, read the eBook **Four Considerations for High-Speed Digital Design Success**.
- Discover industry insights, hear interviews with industry experts in the podcast **From Frustration to Elation — Surviving the Tech Tsunami**.
- Read **Power Integrity: The Foundation for Reliable Electronics Performance** – eBook to build a solid foundation for reliable electronics performance.

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