SOLUTION BRIEF

DisplayPort (DP) Version 2.1 Passive Cable Test MOI

Method of Implementation (MOI) for DisplayPort (DP) Version 2.1 DP80/DP54/DP8K and DP Alt Mode passive cable compliance test using Keysight vector network analyzer with Enhanced TDR app

KEYSIGHT

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Revision History

Revision	Comments	Date
1.0	First draft for E5080B series	15-November-2022
1.1	Updated test fixture information	10-February-2023
1.2	Updated impedance test diagram	25-June-2023
1.3	Updated tests based on DP v2.1a spec to replace DP40 with DP54 to enable up to 4-lane UHBR13.5 support over a 2-m passive cable.	11-June-2024

Reference documents

1. VESA DisplayPort v2.1a PHY Layer Compliance Test Specification (PHY CTS), Section 4.1; Revision 8; June 2024.
2. VESA DisplayPort (DP) Standard; Version 2.0; June 2019.
3. VESA® DisplayPort® Interoperability Compliance Test Specification; Version 1.0; Jan-2012.
4. VESA DisplayPort Alt Mode on USB Type-C Standard (DisplayPort Alt Mode), Version 2.0, 12 March, 2020.
5. VESA DisplayPort Alt Mode on USB Type-C 2.1 Compliance Test Specification (DP Alt Mode on USB Type-C 2.1 CTS), Revision 1.0, November 2022

Configuration Requirements

Description	Test equipment	Qty
Network analyzer	Keysight Vector Network Analyzer: - The minimum test frequency for DP v2.1 CTS required **20 GHz**. **4-Port, 20GHz VNA:** • E5080B-4K0: 4-port test set, 9 kHz to 20 GHz or • E5081A: 4-port test set, 10MHz to 20 GHz or • P5024A/P5024B-400 Streamline USB/TBT Series VNA or • M9804A-400 PXI Multiport VNA or • N522xB PNA Note: Ensure that VNA firmware revision is at least version A.15.60.xx or above (Windows 10).	1 ea.
VNA software	S9x011A/B Enhanced time-domain analysis with TDR * Selection is based on the VNA platforms. x=6 for ENA, x=7 for Streamline USB, x=5 for PXI, x=3 for PNA family	1 ea.
DP80/DP54 compliance tool	Download Get_iPar tool from USB-IF: https://compliance.usb.org/files/Ger_iPar_v0p91a_release.zip (Released on 7-Dec-2020) Download the latest Get_iPar config file from VESA (https://groups.vesa.org/wg/PHY/document/folder/1890) DP80 configuration file: GetIPAR DP80 Configuration File.zip DP54 configuration file: DP54 Configuration File.zip	1 ea.

DP8K compliance tool	Compliance Tool provided by VESA: IntePar_DP Test tool (Rev.0, Released on Dec-2018) https://groups.vesa.org/wg/PHY/document/11171	
Matlab Software	Matlab runtime library R2016a (9.0.1) and R2014b (8.4). Software pre-requisite to run USB-IF compliance tool. Free download from: https://ch.mathworks.com/products/compiler/matlab-runtime.html	2 ea.
Microsoft Excel	Software pre-requisite to run Get_iPar compliance tool.	1 ea.
Test Fixture	DP v2.1 official test fixture. • Enh mDP receptable test fixture (DP80/DP54) • Enh DP receptable test fixture (DP54) • DP receptacle test fixture (DP8K or lower) • Mini DP receptacle test fixture (DP8K or lower) • USB4 Type-C receptacle test fixture (DP Alt Mode) Note 1: Cable test fixtures (PCB Type) for testing DP2.1 Enhanced-DisplayPort, Enhanced-mDP are available for purchase through LUXSHARE-ICT. Note 2: Fixtures for testing USB4 Type-C are available for purchase through LUXSHARE-ICT.	1 set for each based on cable type
ECal Module	Min. 2-Port / 4-Port Electronic Calibration (ECal) Module EG: N4433D-010/0DC 4-Ports	1 ea.
RF cable	3.5 mm or SMA cables of 4 GHz bandwidth or more * Y1740A-100 (3.5-mm m-m, 36 inch) cable is recommended for USB and PXI VNA	2 ea.
Adapter (For E5080B only)	Coaxial straight Female-SMA Female-SMA 50-Ohm adapters (Keysight 1250-1666).	4 ea.
Terminator	50-ohm terminations to terminate unused channels (EG: Keysight 909D-301)	2 ea.

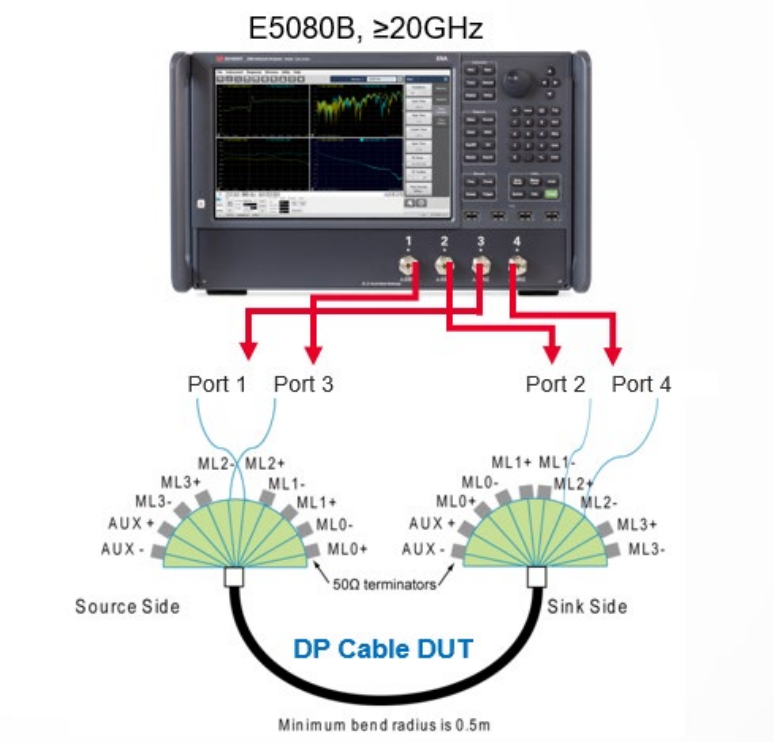
Test Procedure

Test flow chart

Steps	Procedure
Step 1	The VNA should be powered on and allowed to warm up – the recommendation is for 24 hours before measurement.
Step 2	Set measurement conditions by recalling a state file or manual setup.
Step 3	Setup test equipment and test fixture connections based on connection diagrams in next page.
Step 4	Perform 4-Port Electronic Calibration (ECal) for frequency-domain and time-domain.
Step 5	Perform 4-Port test fixture de-embedding for frequency-domain and time-domain.
Step 6	Perform time-domain measurements. **Passive DP80/DP54/DP8K cable** • Differential impedance profile (normative) • Intra-pair skew (normative) • Inter-pair skew (informative)
Step 7	Perform frequency domain measurements. **Passive DP80/DP54 cable** Save S-parameter touchstone file (s4p) and run the Get_iPar.exe compliance tool for DP80/DP54 Channel Metrics • Insertion Loss Fit at Nyquist Frequencies, ILfitatNq (normative) • Integrated Return Loss, IRL (normative) • Integrated Crosstalk, IXT_DP (normative) • Differential-to-Common Mode Conversion (normative) • Integrated Multi-Reflection, IMR (informative) • Integrated Crosstalk between DP Lanes, IFEXT (informative) **Passive DP8K cable** Save S-parameter touchstone file (s4p) and run the IntePar_DP.exe compliance tool for DP8K Channel Metrics. • Insertion Loss Fit at Nyquist Frequencies, ILfitatNq (normative) • Integrated Return Loss, IRL (normative) • Differential-to-Common Mode Conversion (normative) • Integrated Multi-Reflection, IMR (informative) • Integrated Crosstalk between DP Lanes, INEXT/IFEXT (informative) For lower bit rate HBR2, HBR and RBR only: Measurement by VNA trace • Insertion Loss (normative) • Return Loss (normative) • Near End Noise (NEN) (normative) • Far End Noise (FEN) (normative)

Test setup connection

The cable under test will be tested in the following manner.



Normative and **Informative** Parameters

Channel 1- Time Domain	Channel 2- Frequency Domain
1. **Differential Impedance Profile** 2. **Intra-Pair Skew** 3. **Inter-Pair Skew**	4. **DP80/DP54 Channel Metrics** • ILfitatNq (Normative) • Integrated Return Loss, IRL (Normative) • Integrated Crosstalk, IXT_DP (Normative) • Differential-to-Common Mode Conversion (Normative) • Integrated Multi-Reflection, IMR (Informative) • Integrated Crosstalk btw DP Lanes, IFEXT (Informative) 5. **DP8K Channel Metrics** • ILfitatNq (Normative) • Integrated Return Loss, IRL (Normative) • Differential-to-Common Mode Conversion (Normative) • Integrated Multi-Reflection, IMR (Informative) • Integrated Crosstalk btw DP Lanes, INEXT/IFEXT (Informative) **For lower bit rates HBR2, HBR and RBR only** 6. Insertion Loss (Normative) 7. Return Loss (Normative) 8. Near End Noise (NEN) (Normative) 9. Far End Noise (FEN) (Normative)

Note:

1. *Hard Keys are displayed in **Blue** color and **Bold**. (Example: **Avg, Analysis**)*
2. *Soft keys (Keys on the screen) are displayed in **Bold**. (Example: **S11, Real, Transform**)*
3. *Buttons (in the TDR) are displayed in **Green** color and **Bold**. (Example: **Trace, Rise Time**)*
4. *Tabs (in the TDR) are displayed in **Brown** color and **Bold**. (Example: **Setup, Trace Control**)*

Measurement Setups

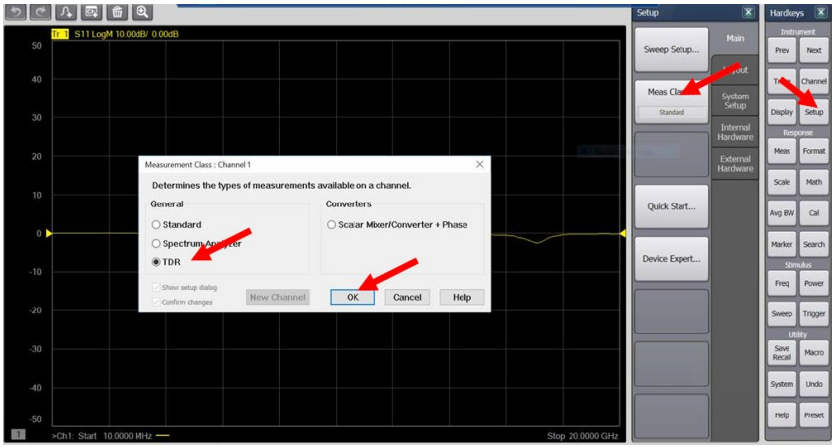
Recalling a state file

This section describes how to recall a state file for Time Domain and Frequency Domain settings. A state file can be downloaded from Keysight.com at the following URL.
www.keysight.com/find/ena-tdr_compliance

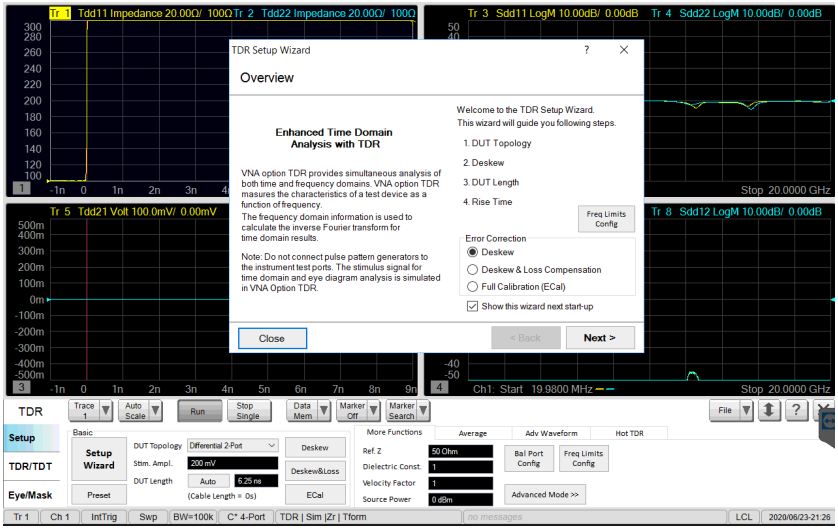
If you use your local PC to download, save the state file to a USB mass storage device in order to move it to the VNA unit. Connect the USB mass storage device into the front USB port of the VNA unit.

For manual measurement settings, refer to Appendix for the manual setup procedure.

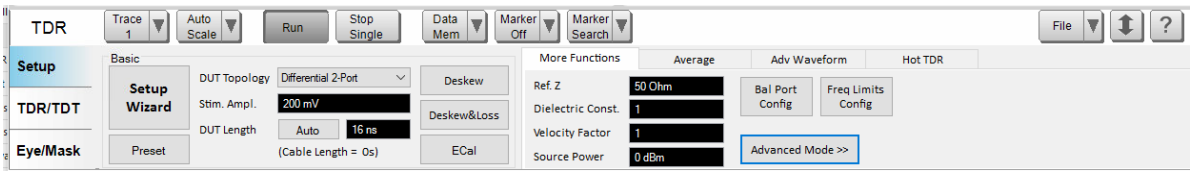
1. Click **Setup > Main > Meas Class**… to launch the measurement class setup dialog box
2. Select **TDR** and click OK.



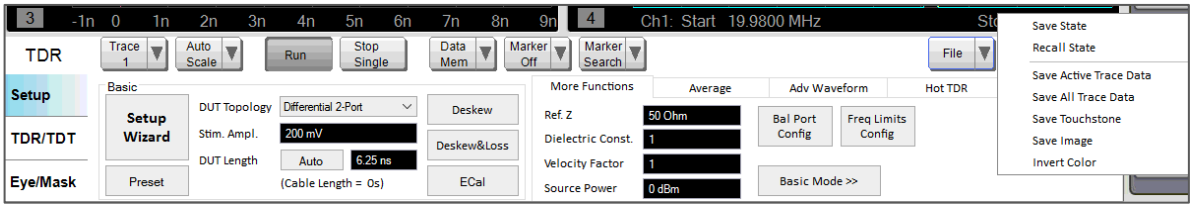
3. Select Close and confirm with Yes to close the setup wizard.



4. Select Click **Advanced Mode** of TDR software and Click Yes to enter the advanced mode.



5. Click **File > Recall State**. Select the state file (*.tdr) and click Open to recall.



6. Windows will launch pre-define state file configuration for compliance testing.
7. All the measurement settings including calibration information can be saved.
   Select **File > Save State As…** > State and Cal Set Date (*.csa) to save the settings.

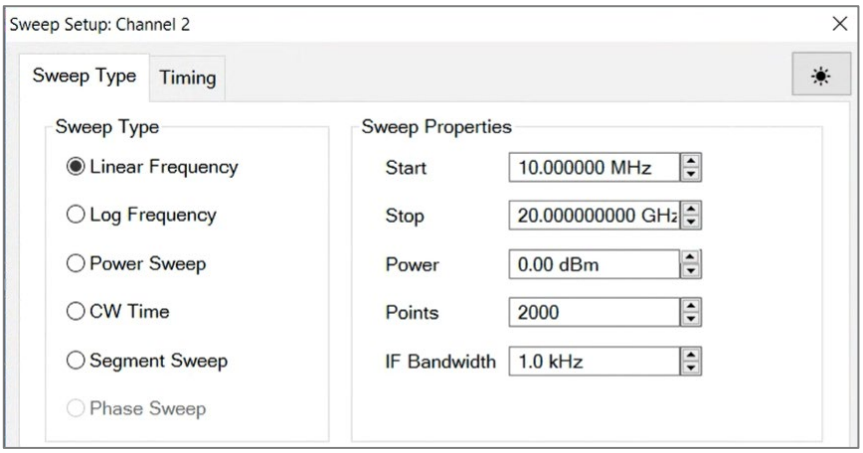
Common parameters setup for frequency domain measurements

1. Press **Channel Next** to select Channel 2.
2. Select **Sweep** > Sweep Setup and key-in sweep properties as below:

   - Set **Start** value to “10 MHz”.
   - Set **Stop** value to “20 GHz”.
   - Set **Power** value to “0 dBm”.
   - Set **Points** value to “2000”.
   - Set **IF Bandwidth** to “1 kHz”.

   Note: Stop frequency for DP2.1 = 20GHz; DP1.4 = 15GHz.

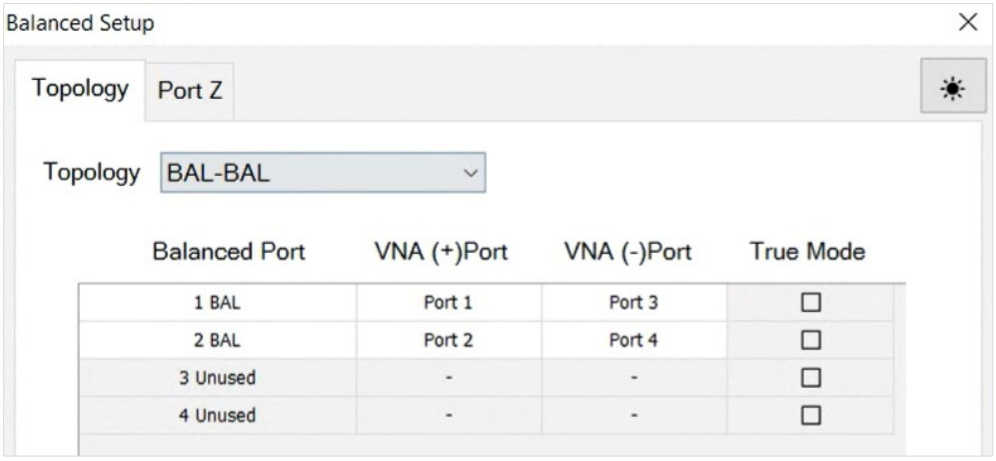
   Note: All frequency domain tests must follow the mandatory sweep setting defined by VESA.



3. Select **Cal > Fixtures > Fixture Setup > Port Z**… Select and check "**Enable Port Z Conversion (all ports)**" to turn ON Port Z conversion for 100-Ohm differential system impedance.
4. Select **Meas > Balanced > Topology… > BAL-BAL**
5. Select **Balanced Port > 1 BAL > Port 1- Port 3**

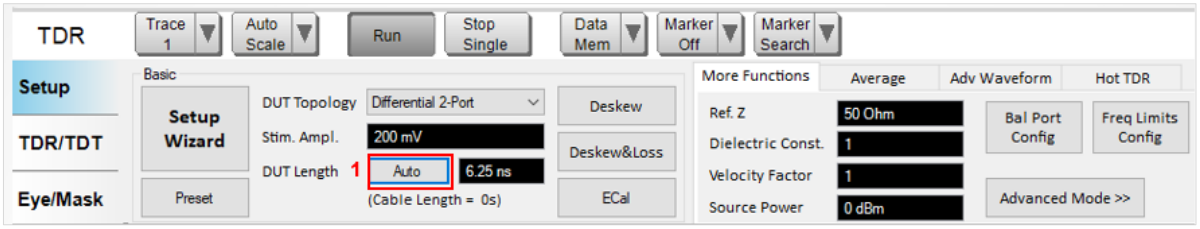
   Select **Balanced Port > 2 BAL > Port 2- Port 4**

   Note 1: DUT Topology setting is to match port mapping use in compliance test tool.



DUT length setup

1. Click Auto (item1) to measure the DUT length.

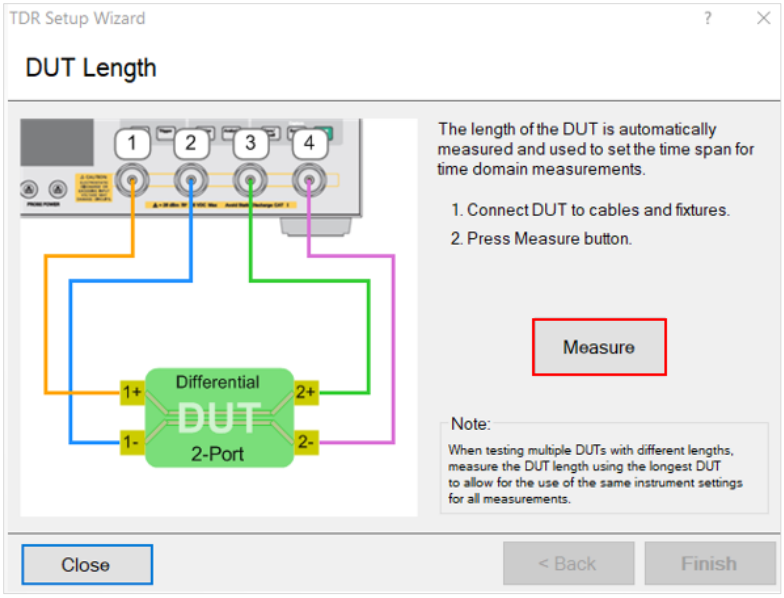


2. Connect the test fixture and DUT as follows.

VNA Port	Port 1	Port 2	Port 3	Port 4
TF pin number	A ML0+	B ML0+	A ML0-	B ML0-

Note: A: Source Side (Left); B: Sink side (Right)

3. Click **Measure** then click Finish to close the setup.



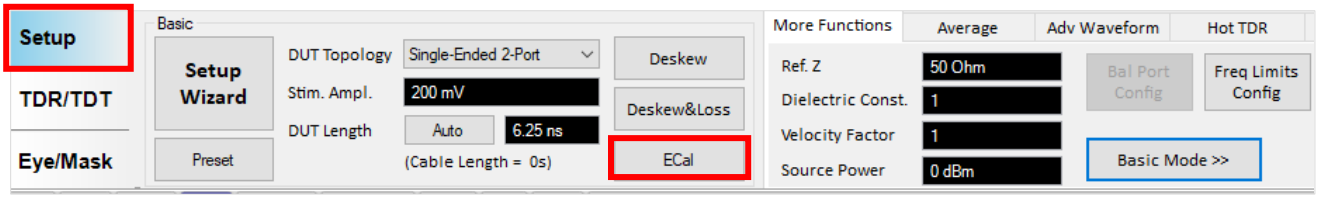
Calibration setup

The purpose of this step is to calibrate the RF effects such as delay, loss or mismatch of RF cables and test fixture traces before measurements. To remove the fixture trace effect, two calibration methods (ECal calibration and de-embedding) are available with the VNA firmware.

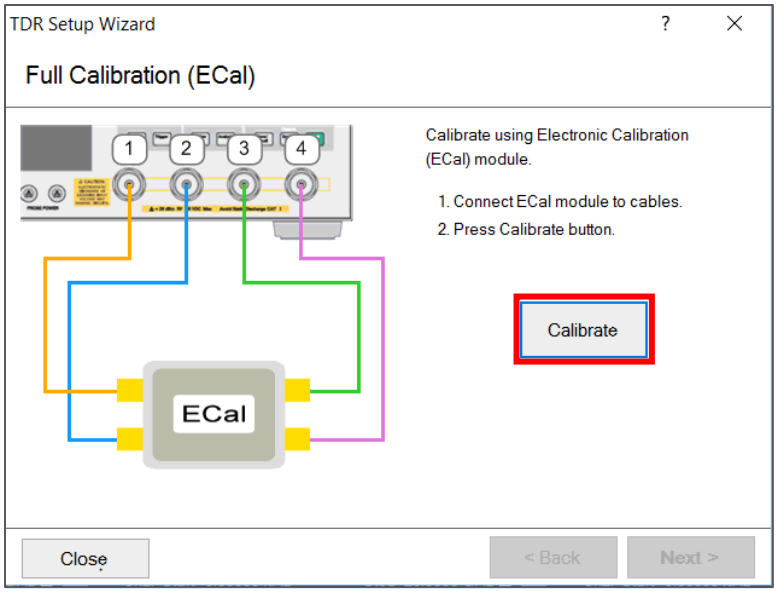
ECal calibration on time domain

ECal calibration for time-domain measurements will be performed by the TDR software.

1. Press **Channel Next** to select Channel 1.
2. Click **Setup** tab.
3. Click **ECal** to launch the TDR Setup Wizard.



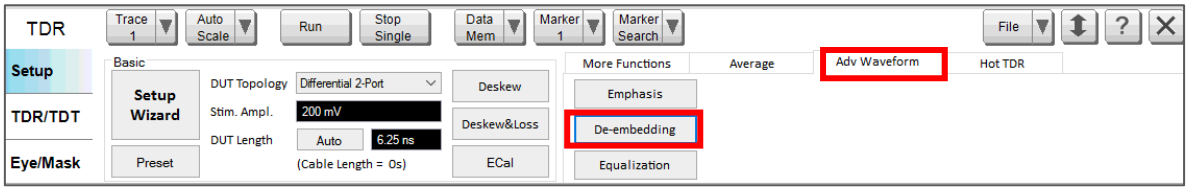
4. Connect the VNA ports (Port 1 - Port 4) to the ECal module with RF cables. Terminate unused ports with 50-Ohm terminators.
5. Click **Calibrate** button to perform 4-Port ECal Calibration.



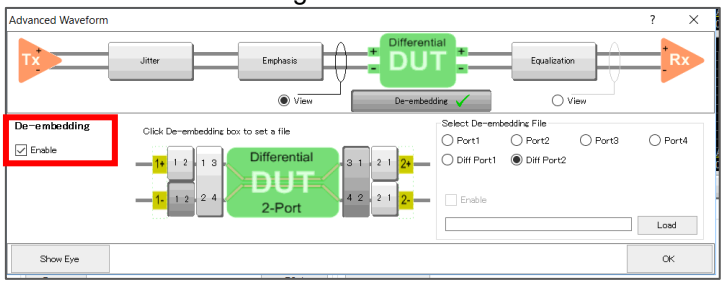
6. Click **Next >** to proceed. Completed calibration will show Green √ sign

De-embedding on time domain

1. Click **Adv Waveform** tab > **De-embedding** to launch Advanced Waveform wizard.



2. Click De-embedding box to set the Touchstone file. 2 port files (*.s2p) for single ended lines or 4 port files (*.s4p) for differential lines can be selected for the de embedding function.
3. Load the DP test fixture Touchstone file as below (files will be provided by Test fixture vendor):
   - Select Port1 > Load “eDP Test Fixture1” file.
   - Select Port2 > Load “eDP Test Fixture 2” file.
   - Select Port3 > Load “eDP Test Fixture 3” file.
   - Select Port4 > Load “eDP Test Fixture 4” file.
4. Enable the de-embedding function and Click OK.

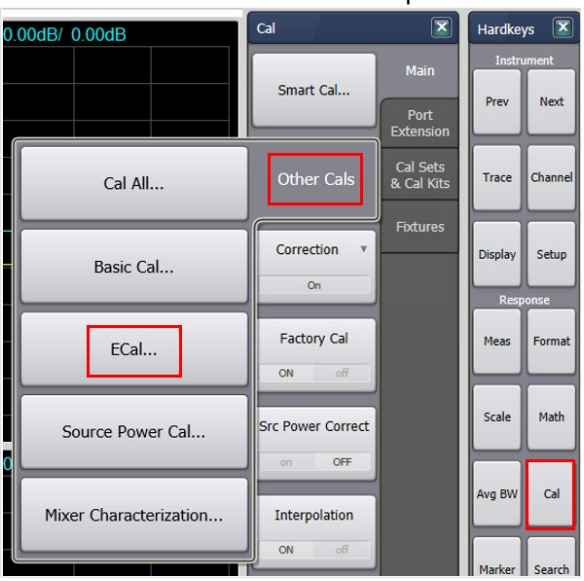


ECal calibration on frequency domain

ECal calibration for frequency-domain measurements will be performed by the VNA firmware.

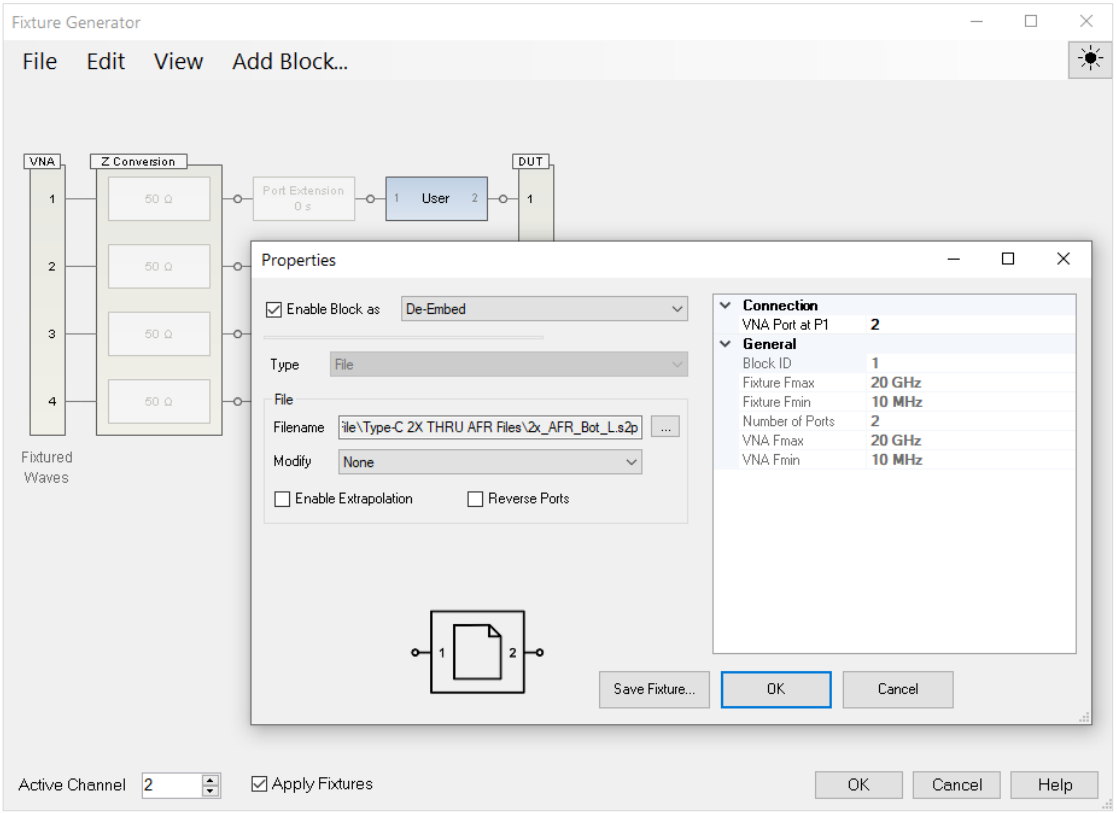
IMPORTANT: Please load the test state file or set up the test frequency sweep setting before performing the calibration to ensure the full test frequency range are calibrated. The current state file is based on maximum operating data rates (UHBR20) at 20 GHz.

1. Press **Channel Next** to select Channel 2.
2. Connect the VNA ports (Port 1 - Port 4) to the ECal module with RF cables.
3. Press **Cal** > **Main** > **Other ECal** > **Ecal…** > select **4-Port ECal** and click **Next** to proceed.
4. Click **Finish** when the ECal is completed.



De-embedding on frequency domain

1. Press **Cal** > Fixtures > Fixture Setup > "User" block > *Right click* to "**Edit…"**
2. Select User S2P File and specify a 2-port de-embedding file (*.s2p). Check on "**Enable Block as**" **De-Embed** (all ports) to de-embed fixture trace.
   Note: files will be provided by Test fixture vendor.
   - Select Port-1 > User Defined (S2P File) > Load "*eDP Test Fixture 1*" file.
   - Select Port-2 > User Defined (S2P File) > Load "*eDP Test Fixture 2*" file.
   - Select Port-3 > User Defined (S2P File) > Load "*eDP Test Fixture 3*" file.
   - Select Port-4 > User Defined (S2P File) > Load "*eDP Test Fixture 4*" file.
3. Close and proceed.



Note 1: Other method like Automatic Fixture Removal (AFR) is also applicable. Refer more to VNA help: https://helpfiles.keysight.com/csg/e5080b/S3_Cals/Auto_Fixture_Removal.htm

Note 2: For more details about the de-embedding function, refer to the VNA help below. https://helpfiles.keysight.com/csg/e5080b/S3_Cals/Fixture_Simulator.htm

Measurement and Data Analysis

The connections for DisplayPort (DP) cable assemblies are assumed as follows (Note: TF stands for Test Fixture). For cable assembly frequency domain measurements, the VESA/USB-IF standard compliance tool is used for the pass/fail judgment.

Note: USB Type-C-to-USB Type-C cables shall meet all the specification requirements as described in USB-IF-published cable and connector specifications and CTS documents. DP Alt Mode in this MOI document and DP Alt Mode CTS shall not describe how to test USB Type-C-to-USB Type-C passive or active cables. All USB Type-C-to-USB Type-C cables shall be certified according to the requirements specified by the USB-IF certification program.

Below table shows the supported connector type and bit rate for DP cable assemblies.

DP2.1 passive cable assemblies

Cable type	Supported bit rate	Supported connector
DP80 (20 Gbps/lane)	UHBR20, UHBR13.5, UHBR10, HBR3 and lower	Enh mDP-to-Enh mDP Enh DP-to-Enh DP Enh mDP-to-Type-C (DP Alt Mode)
DP54 (13.5 Gbps/lane)	UHBR13.5, UHBR10, HBR3 and lower	Enh mDP-to-Enh mDP Enh DP-to-Enh DP Enh mDP/Enh DP-to-Type-C (DP Alt Mode)
DP8K (8.1Gbps/lane)	HBR3 and lower (Lower spec tolerances)	DP-to-DP mDP-to-mDP DP/mDP-to-Type-C (DP Alt Mode)
HBR (8.1, 5.4, 2.7, Gbps/lane, and RBR 1.62Gbps/lane)	HBR2, HRB and RBR	DP-to-DP mDP-to-DP mDP-to-mDP

1. Connect DisplayPort DP80/DP54 Enh mDP/Enh DP test fixtures to the test port cables according to tables below. Unused terminals should be terminated with 50-ohm terminators.
2. Press **Channel Next** key on the instrument front panel to select Channel 1/Channel 2.
3. Channel 1 for time domain measurements
4. Channel 2 for frequency domain measurements
5. Click **Stop Single** for Time Domain measurements.
6. Press **Trigger** > **Single** for Frequency Domain measurements.

Differential impedance profile

Using limit line files, the VNA will automatically perform pass/fail test. Since pass/fail criteria vary depending on the bit rate, cable category or connector type, appropriate limit line files should be loaded prior to making measurements.

1. Connect the VNA ports (port 1 to port 4) to the test fixture ports with RF cables.

	TF source (left)		TF sink (right)	
Measurement parameters	**Port 1**	**Port 3**	**Port 2**	**Port 4**
DP2.1 cable	A ML0+	A ML0-	B ML0+	B ML0-
	A ML1+	A ML1-	B ML1+	B ML1-
	A ML2+	A ML2-	B ML2+	B ML2-
	A ML3+	A ML3-	B ML3+	B ML3-
DP Alt Mode (Type-C to Enh mDP/Enh DP)	TX1+	TX1-	ML2+	ML2-
	RX1+	RX1-	ML3+	ML3-
	TX2+	TX2-	ML1+	ML1-
	RX2+	RX2-	ML0+	ML0-
DP Alt Mode (Enh mDP/Enh DP to Type-C)	ML1+	ML1-	TX1+	TX1-
	ML0+	ML0-	RX1+	RX1-
	ML2+	ML2-	TX2+	TX2-
	ML3+	ML3-	RX2+	RX2-

2. Select a trace on which a limit line should be set.
3. Press **Math** > **Analysis** > Limit…> Limit Table > Load Table > select from CSV File. Click Recall.
4. Select **Trace 1 (Tdd11)** for differential impedance.
5. Click **Stop Single** button on TDR time-domain panel.
6. Confirm the measured impedance is within the limit. Otherwise, it will show Fail.
7. Select **Trace 2 (Tdd22)** and repeat Step 5-6 for the far end of the DUT.
8. The measurement should be evaluated using the required rise time and test limit based on connector type.

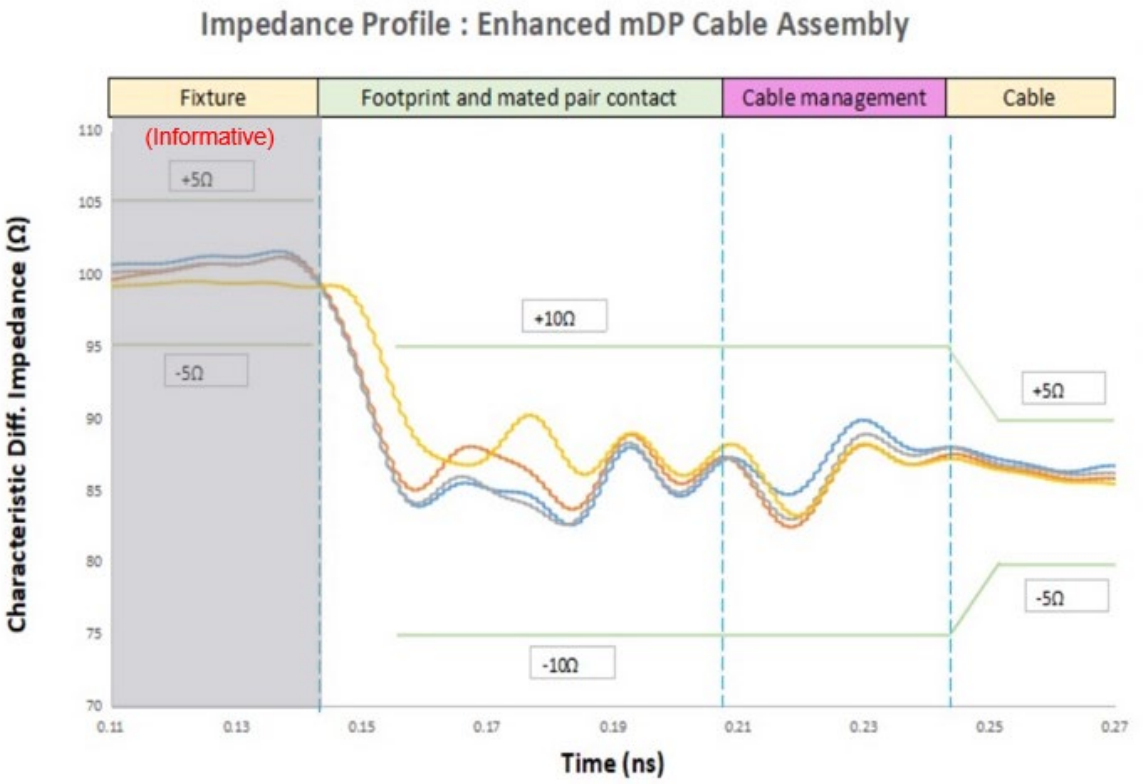
DP2.1 differential impedance profile - Normative

DUT bit rate	Connector type	Limit settings
DP80/DP54	Enh mDP-to-Enh mDP Enh DP-to-Enh DP	DP2.1_EnhmDP_Impedance_Limit.CSV *Using 25ps (20%-80%) rise time*
DP8K and below	DP-to-DP	DP2.1_FSDP_Impedance_Limit.CSV *Using 50ps (20%-80%) rise time*
	mDP-to-mDP	DP2.1_mDP_Impedance_Limit.CSV *Using 50ps (20%-80%) rise time*

9. For DP Alt Mode cable assemblies, the test limit should follow below based on each DUT segment. Note: rise time setting follow DP connector requirements.

DP2.1 Alt Mode differential impedance profile - Normative

DUT segment	Maximum tolerance	Limit settings
USB Type-C connector	85Ω ±9 Ω, per USB Type-C Specification.	Max: 94Ω; Min: 76Ω *Using 25ps (20%-80%) rise time*
USB Type-C bulk cable	90Ω ±5 Ω, per USB Type-C Specification.	Max: 95Ω; Min: 85Ω *Using 25ps (20%-80%) rise time*
Standards DP connector	FSDP 100 Ω ±10%	Max: 110Ω; Min: 90Ω *Using 50ps (20%-80%) rise time*
	mDP 100 Ω ±15%	Max: 115Ω; Min: 85Ω *Using 50ps (20%-80%) rise time*



Segment	Differential impedance value	Maximum tolerance	Comment
Fixture (Informative)	100Ω	±5Ω	Fixture must be de-embedded during measurements
Connector	85Ω	±10Ω	Measurements to be made from 20% to 80% with a rise time of 25 ps
Paddle Card and Wire Management	85Ω	±10Ω	
Cable	85Ω	±5Ω	

Intra-pair skew

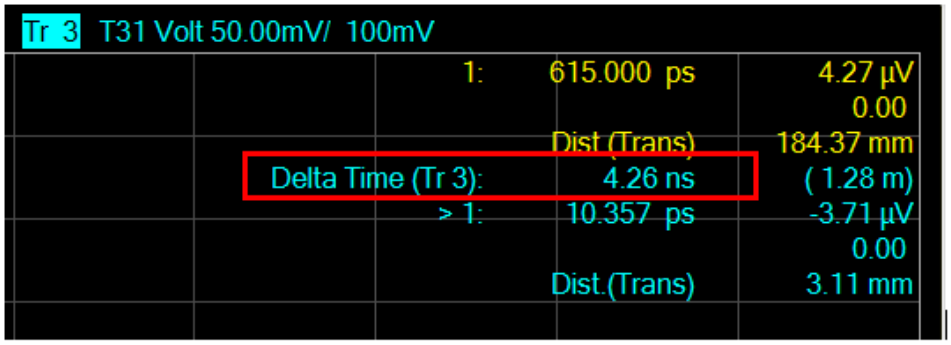
Intra-pair skew defines the difference between the minimum and maximum delay times for transmitted signals along lines within a channel.

1. Connect the VNA ports (port 1 to port 4) to the test fixture ports with RF cables.

	TF source (left)		TF sink (right)	
Measurement parameters	**Port 1**	**Port 3**	**Port 2**	**Port 4**
DP2.1 cable	A ML0+	A ML0-	B ML0+	B ML0-
	A ML1+	A ML1-	B ML1+	B ML1-
	A ML2+	A ML2-	B ML2+	B ML2-
	A ML3+	A ML3-	B ML3+	B ML3-
DP Alt Mode	TX1+	TX1-	ML2+	ML2-

(Type-C to Enh mDP/Enh DP)	RX1+	RX1-	ML3+	ML3-
	TX2+	TX2-	ML1+	ML1-
	RX2+	RX2-	ML0+	ML0-
DP Alt Mode (Enh mDP/Enh DP to Type-C)	ML1+	ML1-	TX1+	TX1-
	ML0+	ML0-	RX1+	RX1-
	ML2+	ML2-	TX2+	TX2-
	ML3+	ML3-	RX2+	RX2-

2. Press **Channel Next** to select Channel 1.
3. Select **Trace 3 (T31)**.
4. Click **Stop Single**
5. Read the Delta Time and confirm the measured value is within the limit shown below.
6. The measurement should be evaluated using required rise time and test limit based on cable type.



DP2.1 intra-pair skew - Normative

DUT bit rate	Connector type	Test limit
DP80	All type	Pass if Delta Time ≤ 10 ps, else: Fail. Using 25ps (20%-80%) rise time
DP54	All type	Pass if Delta Time ≤ 20 ps, else: Fail. Using 25ps (20%-80%) rise time
DP8K and below	All type	Pass if Delta Time ≤ 30 ps, else: Fail. Using 50ps (20%-80%) rise time

DP2.1 Alt mode intra-pair skew - Normative

DUT bit rate	Connector type	Test limit
DP80/DP54/DP8K Alt mode	All type	Pass if Delta Time < 30 psc, else: Fail. Using 50ps (20%-80%) rise time

Inter-pair skew

Inter-pair skew defines the difference between the minimum and maximum delay times for transmitted signals along the group of channels that comprise the system.

1. Connect the VNA ports (port 1 to port 4) to the test fixture ports with RF cables.

	TF source (left)		TF sink (right)	
Measurement parameters	**Port 1**	**Port 3**	**Port 2**	**Port 4**
DP2.1 cable	A ML0+	A ML0-	B ML0+	B ML0-
	A ML1+	A ML1-	B ML1+	B ML1-
	A ML2+	A ML2-	B ML2+	B ML2-
	A ML3+	A ML3-	B ML3+	B ML3-
DP Alt Mode (Type-C to Enh mDP/Enh DP)	TX1+	TX1-	ML2+	ML2-
	RX1+	RX1-	ML3+	ML3-
	TX2+	TX2-	ML1+	ML1-
	RX2+	RX2-	ML0+	ML0-
DP Alt Mode (Enh mDP/Enh DP to Type-C)	ML1+	ML1-	TX1+	TX1-
	ML0+	ML0-	RX1+	RX1-
	ML2+	ML2-	TX2+	TX2-
	ML3+	ML3-	RX2+	RX2-

2. Press **Channel Next** to select Channel 1.
3. Select **Trace 5 (Tdd21)**.
4. Click **Stop Single**
5. Read and record the propagation delay value.
6. Repeat Step 1-5 for every port combination.
7. Find the maximum and minimum values among the measured propagation delay. Then,

Inter pair Skew = Absolute (maximum value - minimum value)

Note: UI (Unit Interval) is the reciprocal of the bit rate. Example: DP54 at 13.5Gbps, then 1 UI equals 1s/13.5e9 = 74ps, 2UI equals 148ps.

8. Calculate the Delta Time and confirm the measured value is within the limit shown below. Otherwise, Fail.
9. The measurement should be evaluated using the required rise time and test limit based on cable type.

DP2.1 Inter-pair skew - informative

DUT bit rate	Connector type	Test limit
DP80/DP54	All type	Pass if Delta Time < 2UI, else: Fail. Using 25ps (20%-80%) rise time DP80: 100 ps, DP54: 148 ps.
DP8K and below	All type	Pass if Delta Time < 2UI, else: Fail. Using 50ps (20%-80%) rise time HBR3 (8.1Gbps): 246.91 ps, HBR2/HBR (5.4Gbps): 370.37 ps, RBR (1.62Gbps): 1234.57 ps.

DP2.1 Alt Mode inter-pair skew - informative

DUT bit rate	Connector type	Test limit
DP80/DP54/DP8K alt mode	All type	Pass if Delta Time < 2UI, else: Fail. Using 50ps (20%-80%) rise time

DP80/DP54 channel metrics

The DP80/DP54 channel metrics or integrated S-parameters cover below test parameters:

- Insertion Loss Fit at Nyquist Frequencies, ILfitatNq (Normative)
- Integrated Return Loss, IRL (Normative)
- Integrated Crosstalk, IXT_DP (Normative)
- Differential-to-Common Mode Conversion (Normative)
- Integrated Multi-Reflection, IMR (Informative)
- Integrated Crosstalk between DP Lanes, INEXT/IFEXT (Informative)

The DP80/DP54 channel metrics will perform by a standard tool (Get_iPar.exe) provided by USB-IF. The compliance tool can be downloaded from the following link:
https://compliance.usb.org/files/Ger_iPar_v0p91a_release.zip

Note: The default configuration file for "Get_iPar.exe" is "input_data.mat" under **…> Get_iPar tool…> data>** folder. To test DP80/DP54, each of these config files should renamed to **"input_data.mat"** and placed in the same directory. Then launch the Get_iPar application and run as usual.

DP80/DP54 Get_iPar config file can be downloaded from VESA:
(https://groups.vesa.org/wg/PHY/document/folder/1890)

DP80 configuration file: GetIPAR DP80 Configuration File.zip

DP54 configuration file: DP54 Configuration File.zip

DP2.1 channel metrics

DUT bit rate	Connector type	Get_iPar tool config file (Please rename to "input_data.mat")
DP80	Enh mDP-to-Enh mDP Enh DP-to-Enh DP	DP80_DP2DP_20G_input_data_R3.mat
DP80 Alt Mode	Type-C-to-Enh mDP Type-C-to-Enh DP	DP80_DP2TC_20G_input_data_R3.mat
DP54	Enh mDP-to-Enh mDP Enh DP-to-Enh DP	DP54_DP2DP_13p5G_input_data_R6.mat
DP54 Alt Mode	Type-C-to-Enh mDP Type-C-to-Enh DP	DP54_DP2TC_13p5G_input_data_R6.mat

Note: **Trace 7** is allocated for the measurements.

Note: Turn off the Port Z conversion to perform the measurements based on 85-ohm port impedance setting which is required by the standard compliance tool.

DisplayPort Alt Mode

USB Type-C-to-Enh mDP passive cables shall support both Scenario 2a (USB-C DP Source device-to-Enh mDP Sink device) and Scenario 2b (Enh mDP Source device-to-USB-C DP Sink device). Table below defines the use and configuration of the USB-C connector pins when the pins are reconfigured to support DisplayPort in normal and flipped plug orientations.

Note: Only normal plug orientation is required for the DP Alt mode cable test.

Scenario 2a – USB-C DP source device-to-Enh mDP sink device



Source device		Sink device		Source device		Sink device	
USB-C pin		Enh mDP (normal plug)	Enh mDP (flipped plug)	USB-C Pin		Enh mDP (normal plug)	Enh mDP (flipped plug)
A1	GND	GND	GND	B12	GND	GND	GND
A2	TX1+	ML2+	ML1+	B11	RX1+	ML3+	ML0+
A3	TX1-	ML2-	ML1-	B10	RX1-	ML3-	ML0-
A4	VBUS	-	-	B9	VBUS	-	-
A5	CC1	-	-	B8	SBU2	AUX-	AUX+
A6	D+	-	-	B7	D-	-	-
A7	D-	-	-	B6	D+	-	-
A8	SBU1	AUX+	AUX-	B5	CC2	-	-
A9	VBUS	-	-	B4	VBUS	-	-
A10	RX2-	ML0-	ML3-	B3	TX2-	ML1-	ML2-
A11	RX2+	ML0+	ML3+	B2	TX2+	ML1+	ML2+
A12	GND	GND	GND	B1	GND	GND	GND

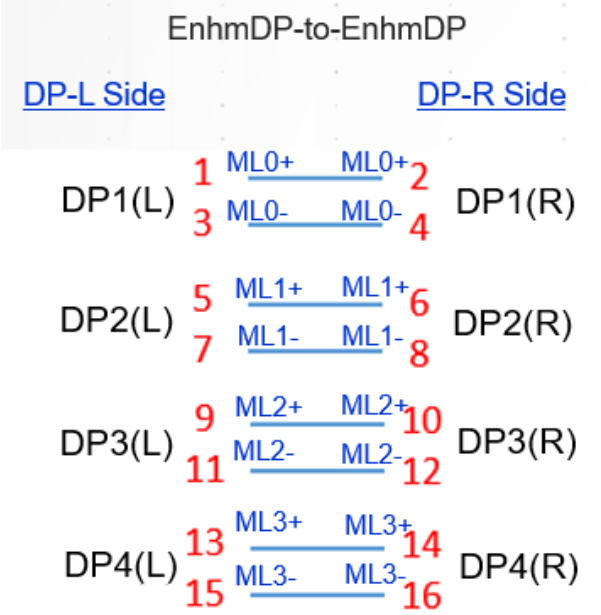
Scenario 2b – EnhmDP source device-to-USB-C DP sink device



Source device		Sink device		Source device		Sink device	
Enh mDP (normal plug)	Enh mDP (flipped plug)	USB-C Pin		Enh mDP (normal plug)	Enh mDP (flipped plug)	USB-C Pin	
GND	GND	A1	GND	GND	GND	B12	GND
ML1-	ML1-	A2	TX1+	ML0-	ML0-	B11	RX1+
ML1+	ML1+	A3	TX1-	ML0+	ML0+	B10	RX1-
-	-	A4	VBUS	-	-	B9	VBUS
-	-	A5	CC1	AUX-	AUX+	B8	SBU2
-	-	A6	D+	-	-	B7	D-
-	-	A7	D-	-	-	B6	D+
AUX+	AUX-	A8	SBU1	-	-	B5	CC2
-	-	A9	VBUS	-	-	B4	VBUS
ML3+	ML3+	A10	RX2-	ML2+	ML2+	B3	TX2-
ML3-	ML3-	A11	RX2+	ML2-	ML2-	B2	TX2+
GND	GND	A12	GND	GND	GND	B1	GND

1. Connect the VNA ports (Port 1 to Port 4) to the test fixture ports with RF cables based on DUT connector type (Enh mDP-to-Enh mDP or DP Alt Mode with USB Type-C).

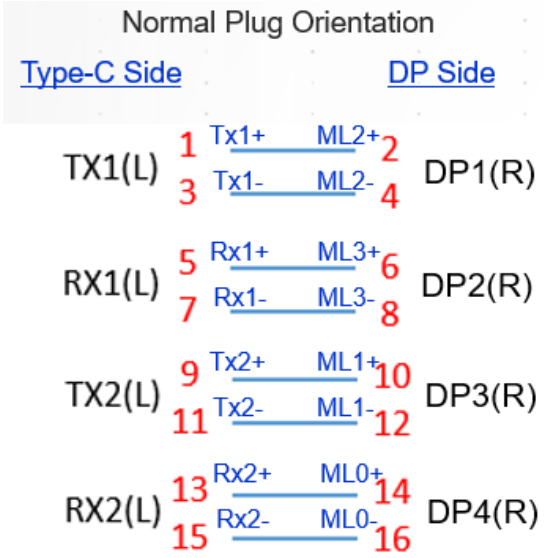
DP80/DP54 (Enh mDP to Enh mDP/ Enh DP to Enh DP)



DP80/DP54 (Enh mDP to Enh mDP/ Enh DP to Enh DP)

Test path name	Test	Port 1	Port 2	Port 3	Port 4
DP1(L), DP1(R) [1,2,3,4]	IL	L Side ML0+	R Side ML0+	L Side ML0-	R Side ML0-
DP1(L), DP2(R) [1,6,3,8]	FEXT	L Side ML0+	R Side ML1+	L Side ML0-	R Side ML1-
DP1(L), DP3(R) [1,10,3,12]	FEXT	L Side ML0+	R Side ML2+	L Side ML0-	R Side ML2-
DP1(L), DP4(R) [1,14,3,16]	FEXT	L Side ML0+	R Side ML3+	L Side ML0-	R Side ML3-
DP1(L), DP2(L) [1,5,3,7]	NEXT	L Side ML0+	L Side ML1+	L Side ML0-	L Side ML1-
DP1(L), DP3(L) [1,9,3,11]	NEXT	L Side ML0+	L Side ML2+	L Side ML0-	L Side ML2-
DP1(L), DP4(L) [1,13,3,15]	NEXT	L Side ML0+	L Side ML3+	L Side ML0-	R Side ML3-
DP1(R), DP2(L) [2,5,4,7]	FEXT	R Side ML0+	L Side ML1+	R Side ML0-	L Side ML1-
DP1(R), DP3(L) [2,9,4,11]	FEXT	R Side ML0+	L Side ML2+	R Side ML0-	L Side ML2-
DP1(R), DP4(L) [2,13,4,15]	FEXT	R Side ML0+	L Side ML3+	R Side ML0-	L Side ML3-
DP1(R), DP2(R) [2,6,4,8]	NEXT	R Side ML0+	R Side ML1+	R Side ML0-	R Side ML1-
DP1(R), DP3(R) [2,10,4,12]	NEXT	R Side ML0+	R Side ML2+	R Side ML0-	R Side ML2-
DP1(R), DP4(R) [2,14,4,16]	NEXT	R Side ML0+	R Side ML3+	R Side ML0-	R Side ML3-
DP2(L), DP2(R) [5,6,7,8]	IL	L Side ML1+	R Side ML1+	L Side ML1-	R Side ML1-
DP2(L), DP3(R) [5,10,7,12]	FEXT	L Side ML1+	R Side ML2+	L Side ML1-	R Side ML2-
DP2(L), DP4(R) [5,14,7,16]	FEXT	L Side ML1+	R Side ML3+	L Side ML1-	R Side ML3-
DP2(L), DP3(L) [5,9,7,11]	NEXT	L Side ML1+	L Side ML2+	L Side ML1-	L Side ML2-
DP2(L), DP4(L) [5,13,7,15]	NEXT	L Side ML1+	L Side ML3+	L Side ML1-	L Side ML3-
DP2(R), DP3(L) [6,9,8,11]	FEXT	R Side ML1+	L Side ML2+	R Side ML1-	L Side ML2-
DP2(R), DP4(L) [6,13,8,15]	FEXT	R Side ML1+	L Side ML3+	R Side ML1-	L Side ML3-
DP2(R), DP3(R) [6,10,8,12]	NEXT	R Side ML1+	R Side ML2+	R Side ML1-	R Side ML2-
DP2(R), DP4(R) [6,14,8,16]	NEXT	R Side ML1+	R Side ML3+	R Side ML1-	R Side ML3-
DP3(L), DP3(R) [9,10,11,12]	IL	L Side ML2+	R Side ML2+	L Side ML2-	R Side ML2-
DP3(L), DP4(R) [9,14,11,16]	FEXT	L Side ML2+	R Side ML3+	L Side ML2-	R Side ML3-
DP3(L), DP4(L) [9,13,11,15]	NEXT	L Side ML2+	L Side ML3+	L Side ML2-	L Side ML3-
DP3(R), DP4(L) [10,13,12,15]	FEXT	R Side ML2+	L Side ML3+	R Side ML2-	L Side ML3-
DP3(R), DP4(R) [10,14,12,16]	NEXT	R Side ML2+	R Side ML3+	R Side ML2-	R Side ML3-
DP4(L), DP4(R) [13,14,15,16]	IL	L Side ML3+	R Side ML3+	L Side ML3-	R Side ML3-

DP Alt Mode (Type-C to Enh mDP)

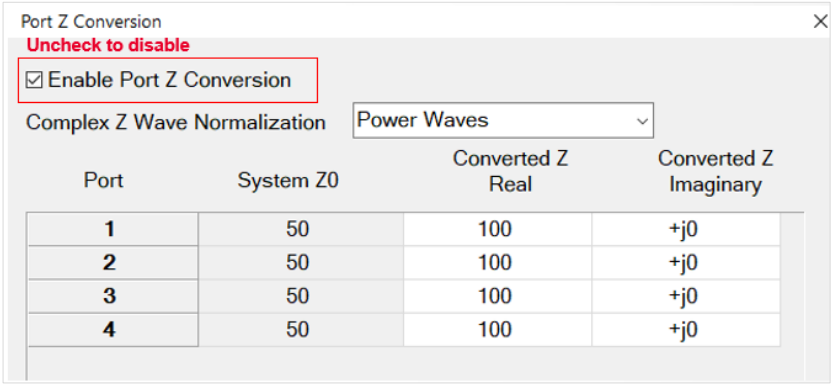


DP Alt Mode (Type-C to Enh mDP/Enh DP) - Scenario 2a (Normal plug orientation)

Test path name	Test	Port 1	Port 2	Port 3	Port 4
TX1(L), DP1(R) [1,2,3,4]	IL	L Side Tx1+	R Side ML2+	L Side Tx1-	R Side ML2-
TX1(L), DP2(R) [1,6,3,8]	FEXT	L Side Tx1+	R Side ML3+	L Side Tx1-	R Side ML3-
TX1(L), DP3(R) [1,10,3,12]	FEXT	L Side Tx1+	R Side ML1+	L Side Tx1-	R Side ML1-
TX1(L), DP4(R) [1,14,3,16]	FEXT	L Side Tx1+	R Side ML0+	L Side Tx1-	R Side ML0-
TX1(L), RX1(L) [1,5,3,7]	NEXT	L Side Tx1+	L Side Rx1+	L Side Tx1-	L Side Rx1-
TX1(L), TX2(L) [1,9,3,11]	NEXT	L Side Tx1+	L Side Tx2+	L Side Tx1-	L Side Tx2-
TX1(L), RX2(L) [1,13,3,15]	NEXT	L Side Tx1+	L Side Rx2+	L Side Tx1-	R Side ML3-
DP1(R), RX1(L) [2,5,4,7]	FEXT	R Side ML2+	L Side Rx1+	R Side ML2-	L Side Rx1-
DP1(R), TX2(L) [2,9,4,11]	FEXT	R Side ML2+	L Side Tx2+	R Side ML2-	L Side Tx2-
DP1(R), RX2(L) [2,13,4,15]	FEXT	R Side ML2+	L Side Rx2+	R Side ML2-	L Side Rx2-
DP1(R), DP2(R) [2,6,4,8]	NEXT	R Side ML2+	R Side ML3+	R Side ML2-	R Side ML3-
DP1(R), DP3(R) [2,10,4,12]	NEXT	R Side ML2+	R Side ML1+	R Side ML2-	R Side ML1-
DP1(R), DP4(R) [2,14,4,16]	NEXT	R Side ML2+	R Side ML0+	R Side ML2-	R Side ML0-
RX1(L), DP2(R) [5,6,7,8]	IL	L Side Rx1+	R Side ML3+	L Side Rx1-	R Side ML3-
RX1(L), DP3(R) [5,10,7,12]	FEXT	L Side Rx1+	R Side ML1+	L Side Rx1-	R Side ML1-
RX1(L), DP4(R) [5,14,7,16]	FEXT	L Side Rx1+	R Side ML0+	L Side Rx1-	R Side ML0-
RX1(L), TX2(L) [5,9,7,11]	NEXT	L Side Rx1+	L Side Tx2+	L Side Rx1-	L Side Tx2-
RX1(L), RX2(L) [5,13,7,15]	NEXT	L Side Rx1+	L Side Rx2+	L Side Rx1-	L Side Rx2-
DP2(R), TX2(L) [6,9,8,11]	FEXT	R Side ML3+	L Side Tx2+	R Side ML3-	L Side Tx2-
DP2(R), RX2(L) [6,13,8,15]	FEXT	R Side ML3+	L Side Rx2+	R Side ML3-	L Side Rx2-

DP2(R), DP3(R) [6,10,8,12]	NEXT	R Side ML3+	R Side ML1+	R Side ML3-	R Side ML1-
DP2(R), DP4(R) [6,14,8,16]	NEXT	R Side ML3+	R Side ML0+	R Side ML3-	R Side ML0-
TX2(L), DP3(R) [9,10,11,12]	IL	L Side Tx2+	R Side ML1+	L Side Tx2-	R Side ML1-
TX2(L), DP4(R) [9,14,11,16]	FEXT	L Side Tx2+	R Side ML0+	L Side Tx2-	R Side ML0-
TX2(L), RX2(L) [9,13,11,15]	NEXT	L Side Tx2+	L Side Rx2+	L Side Tx2-	L Side Rx2-
DP3(R), RX2(L) [10,13,12,15]	FEXT	R Side ML1+	L Side Rx2+	R Side ML1-	L Side Rx2-
DP3(R), DP4(R) [10,14,12,16]	NEXT	R Side ML1+	R Side ML0+	R Side ML1-	R Side ML0-
RX2(L), DP4(R) [13,14,15,16]	IL	L Side Rx2+	R Side ML0+	L Side Rx2-	R Side ML0-

2. Select **Cal** > Fixtures > Fixture Setup > Z Conversion… right click and uncheck “Enable Port Z Conversion (all ports)” to turn OFF Port Z conversion.



3. Press **Channel Next** to select Channel 2.
4. Select **Trace 7**. Double-click on the instrument front panel to enlarge the trace.
5. Press **Trigger** > Single.
6. Press **Save Recall** > ***Save Other*** > **Save Data...> Filename.s4p** to save all the 28-sets measured Touchstone file (*.s4p). Select format “Real/Imaginary” and “Normal” mode > then OK.
7. After completing the measurement, Press **Cal** > **Fixtures** > **Fixture Setup** > **Port Z…** check “**Enable Port Z Conversion (all ports)**” to turn ON Port Z conversion as the default setting.
8. Open the Excel spreadsheet “**s4p_example_0p91a.xlsx”** and update “file location path” (sp_file_1 until sp_file_28) with 28-sets 4-port Touchstone files (*.s4p) you have measured.
9. Modify the excel spreadsheet “**USB4_Gen3_CableCom_Config_Example1.xlsx**” settings as below:
   “**comp_check_type”** = 2 to check iPar (Integrated S-parameters)
   “**Cable_Type**” = 0 for passive cable.
   “**case_number**” = [1] for 4-ports measurements and

USB4 Gen3 Cable Complaince Check Configuration File Example	
comp_check_type	2
result_folder	.\Templates\USB4 Active Cable\Results
cable_type	0
eta_0	5.67E-08
save_assembled_cable_sp	0
plot_cable_sp	1
case_number	[1]
case_1	.\Templates\[Touchstone file folder]\s4p_example_1.xlsx
case_2	.\Templates\s8p_example_0p91a.xlsx
case_3	.\Templates\s16p_example_0p91a.xlsx
case_4	.\Templates\s20p_example_0p91a.xlsx

10. Goto Get_iPar compliance tool folder:
    …\Ger_iPar_v0p91a_release\data
11. Copy the Matlab config file according to your cable type to the folder and rename it to the default file name **"input_data.mat"**.
12. Launch the USB-IF compliance test tool (***Get_iPar.exe***) to load the excel spreadsheet "**USB4_Gen3_CableCom_Config_Example1.xlsx**" in order to execute the tool and check compliance for pass/fail judgment. The result will show in "***cable_iPar_report_case_1.xlsx**" for iPar Channel metrics result in the tool's results folder.

Passive cable	TX1(L)	TX1(R)	RX1(L)	RX1(R)	TX2(L)	TX2(R)	RX2(L)	RX2(R)	Limit	Pass/Fail
ILfit@0.1GHz, dB	-0.51	-0.51	-0.5	-0.5	-0.5	-0.5	-0.53	-0.53	-1	Pass
ILfit@2.5GHz, dB	-2.84	-2.84	-2.81	-2.81	-2.83	-2.83	-2.88	-2.88	-4.2	Pass
ILfit@5GHz, dB	-3.96	-3.96	-3.99	-3.99	-3.98	-3.98	-4.09	-4.09	-6	Pass
ILfit@10GHz, dB	-5.94	-5.94	-6.11	-6.11	-5.88	-5.88	-6.09	-6.09	-7.5	Pass
ILfit@12.5GHz, dB	-7.15	-7.15	-7.34	-7.34	-6.96	-6.96	-7.24	-7.24	-9.3	Pass
ILfit@15GHz, dB	-8.62	-8.62	-8.76	-8.76	-8.23	-8.23	-8.58	-8.58	-11	Pass
IMR, dB	-43.59	-43.59	-41.93	-41.93	-40.99	-40.99	-41.76	-41.76	-32.38	Pass
IRL, dB	-20.03	-20.03	-19.97	-19.97	-19.15	-19.15	-19.39	-19.39	-14.88	Pass
C2D, dB	-33.3	-33.25	-24.56	-24	-28.88	-27.9	-22.97	-21.9	-17	Pass
D2C, dB	-32.82	-33.24	-23.05	-24.32	-28.99	-28.09	-22.85	-22.08	-17	Pass
IXT_DP, dB	-49.39	-49.03	-49.25	-49.29	-49.6	-49.85	-49.62	-49.73	-40.11	Pass
IXT_USB, dB	-50.7	-48.85	-49.74	-48.93	-49.77	-49.27	-50.76	-49.2	-40.21	Pass

13. Repeat the test to cover both source-to-sink and sink-to-source directions in Normal plug orientation.

DP8K channel metrics

The DP8K channel metrics or integrated S-parameters will cover below test parameters:

- Insertion Loss Fit at Nyquist Frequencies, ILfitatNq (Normative)
- Integrated Return Loss, IRL (Normative)
- Differential-to-Common Mode Conversion (Normative)
- Integrated Multi-Reflection, IMR (Informative)
- Integrated Crosstalk between DP Lanes, INEXT/IFEXT (Informative)

The DP8K channel metrics will check by a standard tool (**IntePar_DP.exe**) provided by VESA. The compliance tool can be downloaded from the following link:
https://groups.vesa.org/wg/PHY/document/11171
Note: The default configuration file for "IntePar_DP_R0p9.exe" is "C2DP_inputData.mat". To use each of these config files it should be renamed to the default config file name, "C2DP_inputData.mat." and placed in the same directory as the application file of "IntePar_DP_R0p9.exe". Then launch the application and run it as normal.

DP8K channel metrics - normative

DUT bit rate	Connector type	IntePar_DP tool config file
DP8K	DP-to-DP mDP-to-mDP	DP2DP_input_rev0p9_RZ90_1p35-2p7-4p05GHz.mat
DP8K Alt Mode	Type-C-to-DP/mDP	C2DP_input_rev0p9_RZ90_1p35-2p7-4p05GHz.mat

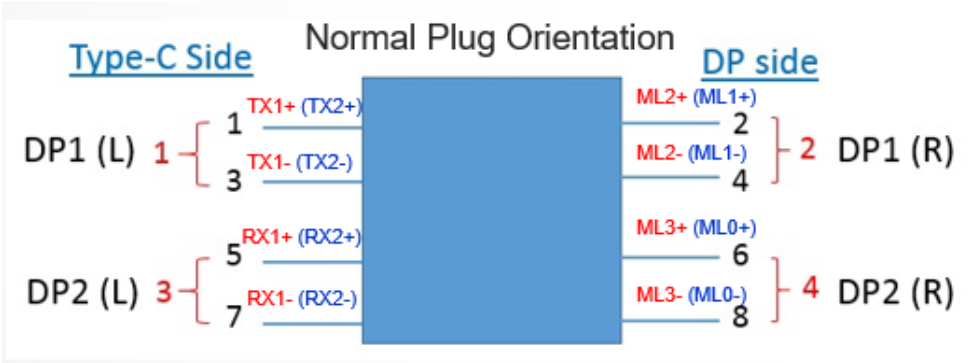
1. Connect the VNA ports (port 1 to 4) to the test fixture ports with RF cables based on DUT connector type (DP2DP or DP Alt Mode).

DP/mDP to DP/mDP mode - first set for ML0/ML1 signals

Test Path Name	Port 1	Port 2	Port 3	Port 4
DP1(L) DP1(R) [1,2,3,4]	A ML0+	B ML0+	A ML0-	B ML0-
DP2(L) DP2(R) [5,6,7,8]	A ML1+	B ML1+	A ML1-	B ML1-
DP1(L) DP2(L) [1,3,5,7]	A ML0+	A ML1+	A ML0-	A ML1-
DP1(R) DP2(R) [2,4,6,8]	B ML0+	B ML1+	B ML0-	B ML1-
DP1(L) DP2(R) [1,3,6,8]	A ML0+	B ML1+	A ML0-	B ML1-
DP1(R) DP2(L) [2,4,5,7]	B ML0+	A ML1+	B ML0-	A ML1-

DP/mDP to DP/mDP mode - second set for ML2/ML3 signals

Test path name	Port 1	Port 2	Port 3	Port 4
DP1(L) DP1(R) [1,2,3,4]	A ML2+	B ML2+	A ML2-	B ML2-
DP2(L) DP2(R) [5,6,7,8]	A ML3+	B ML3+	A ML3-	B ML3-
DP1(L) DP2(L) [1,3,5,7]	A ML2+	A ML3+	A ML2-	A ML3-
DP1(R) DP2(R) [2,4,6,8]	B ML2+	B ML3+	B ML2-	B ML3-
DP1(L) DP2(R) [1,3,6,8]	A ML2+	B ML3+	A ML2-	B ML3-
DP1(R) DP2(L) [2,4,5,7]	B ML2+	A ML3+	B ML2-	A ML3-



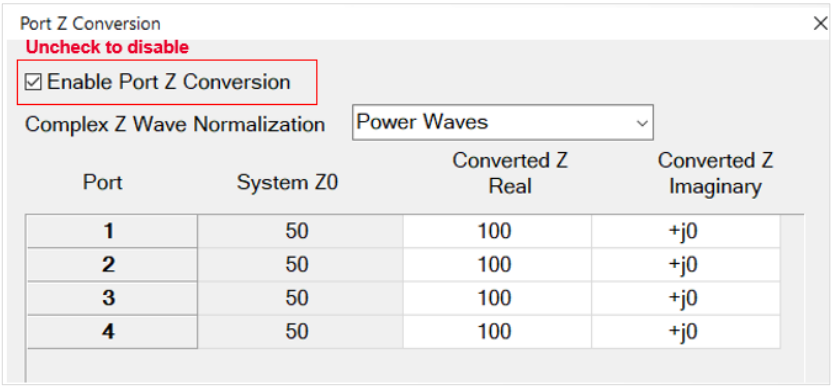
DP Alt Mode (Type-C to DP/mDP) - first set for TX1/RX1 signals (normal plug orientation)

Test path name	Port 1	Port 3	Port 2	Port 4
DP1(L) DP1(R) [1,2,3,4]	TX1+	ML2+	TX1-	ML2-
DP2(L) DP2(R) [5,6,7,8]	RX1+	ML3+	RX1-	ML3-
DP1(L) DP2(L) [1,3,5,7]	TX1+	RX1+	TX1-	RX1-
DP1(R) DP2(R) [2,4,6,8]	ML2+	ML3+	ML2-	ML3-
DP1(L) DP2(R) [1,3,6,8]	TX1+	ML3+	TX1-	ML3-
DP1(R) DP2(L) [2,4,5,7]	ML2+	RX1+	ML2-	RX1-

DP Alt Mode (Type-C to DP/mDP) - second set for TX2/RX2 signals (normal plug orientation)

Test path name	Port 1	Port 3	Port 2	Port 4
DP1(L) DP1(R) [1,2,3,4]	TX2+	ML1+	TX2-	ML1-
DP2(L) DP2(R) [5,6,7,8]	RX2+	ML0+	RX2-	ML0-
DP1(L) DP2(L) [1,3,5,7]	TX2+	RX2+	TX2-	RX2-
DP1(R) DP2(R) [2,4,6,8]	ML1+	ML0+	ML1-	ML0-
DP1(L) DP2(R) [1,3,6,8]	TX2+	ML0+	TX2-	ML0-
DP1(R) DP2(L) [2,4,5,7]	ML1+	RX2+	ML1-	RX2-

2. Select **Cal** > Fixtures > Fixture Setup > Z Conversion… right click and uncheck “Enable Port Z Conversion (all ports)” to turn OFF Port Z conversion.

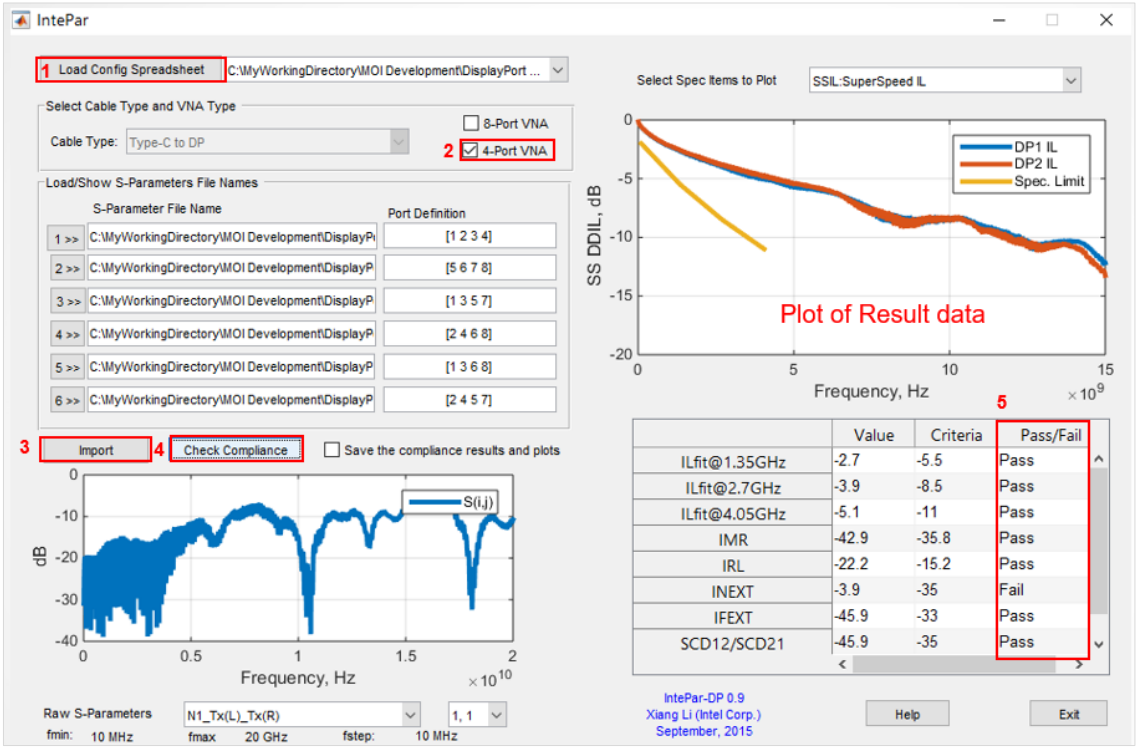


3. Press **Channel Next** to select Channel 2.
4. Select **Trace 7**. Double-click on the instrument front panel to enlarge the trace.
5. Press **Trigger** > Single.
6. Press **Save Recall** > ***Save Other*** > **Save Data...**> Filename.s4p to save the measured Touchstone file (*.s4p). Select format “Real/Imaginary” and “Normal” mode > then OK.
7. Open the Excel spreadsheet “Config_4ports.xlsx” and update “S4P file location path” with 6-sets 4-port Touchstone files (*.s4p) you have measured.
8. Goto IntePar_DP compliance tool folder in your directory: …\IntePar_DP Tool\
9. Copy the Matlab config file according to your cable type to the folder and rename it to default file name "C2DP_inputData.mat":

DP8K channel metrics - normative

DUT bit rate	Connector type	IntePar_DP tool config file
DP8K	DP-to-DP mDP-to-mDP	Rename “DP2DP_input_rev0p9_RZ90_1p35-2p7-4p05GHz.mat” to "C2DP_inputData.mat"
DP8K Alt mode	Type-C-to-DP/mDP	Rename “C2DP_input_rev0p9_RZ90_1p35-2p7-4p05GHz.mat” to "C2DP_inputData.mat"

10. Launch the **IntePar_DP.exe** compliance test tool and load the Excel spreadsheet "Config_4ports.xlsx" by clicking "Load Config Spreadsheet". Click Import to import six 4-port Touchstone files (*.s4p), then click Check Compliance for pass/fail judgment.
11. Repeat Steps 4-7 for the second set of signal pairs.



12. Repeat the test to cover both source-to-sink and sink-to-source directions in Normal plug orientation.

For Lower Bit Rate HBR2, HBR and RBR Only Insertion loss (Normative)

The VNA will automatically perform a pass/fail test using limit line files depending on the bit rate, cable category or connector type. Please download the appropriate limit line files from K.com prior making the measurements.

1. Connect the VNA ports (port 1 to 4) to the test fixture ports with RF cables.

Measurement parameters	TF A side		TF B side	
	Port 1	Port 3	Port 2	Port 4
Insertion loss	A ML0+	A ML0-	B ML0+	B ML0-
	A ML1+	A ML1-	B ML1+	B ML1-
	A ML2+	A ML2-	B ML2+	B ML2-
	A ML3+	A ML3-	B ML3+	B ML3-
	A AUX+	A AUX-	B AUX+	B AUX-

2. Press Channel Next to select Channel 2.
3. Select **Trace 7-Trace 10 (Sdd21).**

4. Press **Trigger** > Single
5. Run and confirm the measured value is within the limit shown below. Otherwise, it will show Fail.

DUT bit rate	Cable category	Connector type	Connector type
HBR2/HBR	Cable (Tr-7)	All	DP1.4_HBR_IL_Cable_Limit.CSV
	Resizing adapter (Tr-8)	All	DP1.4_HBR_IL_Adapter_Limit.CSV
	Extension cable (Tr-9)	All	DP1.4_HBR_IL_ExtCable_Limit.CSV
RBR	All (Tr-10)	All	DP1.4_RBR_IL_Limit.CSV

Insertion Loss – Lower Limit for High Bit Rate Cable Assembly Types C1, C2, and C3.

Where f is given in GHz, f0 = 1.35 GHz

$$IL_{\min.}[dB] = \begin{cases} -8.7 \times \sqrt{\frac{f}{f_0}} - 0.072; & 0.1 < f \le \frac{f_0}{3} \\ 5.68\sqrt{f} - 5.3 * f - 6.52; & \frac{f_0}{3} < f \le 8.1 \end{cases}$$

Insertion Loss – Lower Limit for High Bit Rate Resizing Adapters.

Where f is given in GHz, f0 = 1.35GHz

$$IL_{\min.}[dB] = \begin{cases} -1.6 \times \sqrt{\frac{f}{f_0}}; & 0.1 < f \le \frac{f_0}{3} \\ 1.75\sqrt{f} - 1.65 * f - 1.31; & \frac{f_0}{3} < f \le 8.1 \end{cases}$$

Insertion Loss – Lower Limit for Extension Cables.

Where f is given in GHz, f0 = 1.35 GHz

$$IL_{\min.}[dB] = \begin{cases} -5.22 \times \sqrt{\frac{f}{f_0}} - 0.043; & 0.1 < f \le \frac{f_0}{3} \\ 3.41\sqrt{f} - 3.18 * f - 3.91; & \frac{f_0}{3} < f \le 8.1 \end{cases}$$

Insertion Loss – Lower Limit for Reduced Bit Rate Cable Assembly.

Where f is given in GHz, f0 = 0.825 GHz

$$IL_{\min.}[dB] = \begin{cases} -1 - 13.5 \times \sqrt{\frac{f}{f_0}} & ; \quad 0.01 < f \le \frac{f_0}{3} \\ -2.1 - [12(f - \frac{f_0}{3}) + 6.8] & ; \quad \frac{f_0}{3} < f \le 4 \end{cases}$$

Return loss (normative)

1. Connect the VNA ports (port 1 to 4) to the test fixture ports with RF cables.

Measurement parameters	TF A side		TF B side	
	Port 1	Port 3	Port 2	Port 4
Insertion loss	A ML0+	A ML0-	B ML0+	B ML0-
	A ML1+	A ML1-	B ML1+	B ML1-
	A ML2+	A ML2-	B ML2+	B ML2-
	A ML3+	A ML3-	B ML3+	B ML3-
	A AUX+	A AUX-	B AUX+	B AUX-

2. Press Channel Next to select Channel 2.
3. Select **Trace 11/Trace 12 (Sdd11).**
4. Press **Trigger** > Single
5. Run and confirm the measured value is within the limit shown below. Otherwise, it will show Fail.

DUT bit rate	Cable category	Connector type	Connector type
HBR2/HBR	All (Tr-11)	All	DP1.4_HBR_RL_Limit.CSV
RBR	All (Tr-12)	All	DP1.4_RBR_RL_Limit.CSV

Return Loss – Upper Limit for HBR Cable Assembly/Adapter (Full-sized DP Connector),

Where f is given in GHz, f0 = 1.35 GHz

$$RL_{\max.}[dB] = \begin{cases} -15; & 0.1 < f \le \dfrac{f_0}{2} \\ -15 + 12.3\, Log_{10}\left(\dfrac{2f}{f_0}\right); & \dfrac{f_0}{2} < f \le 8.1 \end{cases}$$

Return Loss – Upper Limit for Reduced Bit Rate Cable Assembly,

Where f is given in GHz, f0 = 0.8 GHz

$$RL_{\max.}[dB] = \begin{cases} -15 & ; \quad 0.1 < f \le \dfrac{f_0}{2} \\ -15 + 12\, Log_{10}\left(2x\dfrac{f}{f_0}\right) & ; \quad \dfrac{f_0}{2} < f \le 4 \end{cases}$$

Near End Noise (NEN) (normative)

1. Connect the VNA ports (port 1 to 4) to the test fixture ports with RF cables.

Measurement parameters	TF A side		TF B side	
	Port 1	Port 3	Port 2	Port 4
Near End Noise (NEN)	A ML0+	A ML0-	B ML0+	B ML0-
	A ML1+	A ML1-	B ML1+	B ML1-
	A ML2+	A ML2-	B ML2+	B ML2-

	A ML3+	A ML3-	B ML3+	B ML3-
	B AUX+	B AUX-	B ML0+	B ML0-
	B AUX+	B AUX-	B ML1+	B ML1-
	B AUX+	B AUX-	B ML2+	B ML2-
	B AUX+	B AUX-	B ML3+	B ML3-

2. Press Channel Next to select Channel 2.
3. Select **Trace 13/Trace 14 (Sdd11).**
4. Press **Trigger** > Single
5. Run and confirm the measured value is within the limit shown below. Otherwise, it will show Fail.

DUT bit rate	Cable category	Connector type	Connector type
HBR2/HBR	All (Tr-13)	All	DP1.4_HBR_NEN_Limit.CSV
RBR	All (Tr-14)	All	DP1.4_RBR_NEN_Limit.CSV

Near-End Noise – Upper Limit for High Bit Rate Cable Assembly,
Where f is given in GHz, f0 = 1.35GHz

$$Isolation_{max.}[dB] = \begin{cases} -26 & ; \quad 0.1 < f \le f_0 \\ -26 + 15\,Log_{10}\left(\frac{f}{f_0}\right) & ; \quad f_0 < f \le 8.1 \end{cases}$$

Near-End Noise – Upper Limit for Reduced Bit Rate Cable Assembly,
Where f is given in GHz, f0 = 0.8GHz

$$Isolation_{max.}[dB] = \begin{cases} -26 & ; \quad 0.1 < f \le f_0 \\ -26 + 15\,Log_{10}\left(\frac{f}{f_0}\right) & ; \quad f_0 < f \le 4 \end{cases}$$

Far End Noise (FEN) (normative)

The Power Sum Equal Level Far-End Noise (PSELFEN) represents the difference between cable insertion loss and the total power sum far end noise from aggressor cable lanes. Prior to measuring the far end noise between the victim and aggressor channels, the insertion loss of the victim channel must be measured on **Trace 7** and saved to the trace memory.

$$PSFEN(f) = 10 \times \log \sum_{1}^{n} 10^{\left(\frac{FENn(f)}{10}\right)}$$

$$PSELFEN(f) = PSFEN(f) - IL(f)$$

where:

• FENn(f) is the far-end noise in dB
• IL(f) is the victim lane insertion loss in dB

Since the number of aggressor channels depends on the victim channel, use an appropriate trace for each test according to the Table below. For test number 2, 3 and 4 (dual aggressor test), the crosstalk measurements need to be performed separately on each combination of victim aggressor and combine the results to calculate Far End Noise. For instance, to obtain Far End Noise for test 3, measure Sdd21 between Main Link (0) and Main Link (1) crosstalk, then measure Sdd21 between Main Link (2) and Main Link (1).

Note: For Single Aggressor FEN, read Pass/Fail signs on Trace 15. For Dual Aggressor 1 & 2, read Pass/Fail signs on **Trace 16**.

Test #	Aggressor channel (source side)	Victim channel (sink side)	Trace #
1	Main Link-2	Main Link-3	Tr-15
2	Main Link-1 + Main Link-3	Main Link-2	Tr-16
3	Main Link-0 + Main Link-2	Main Link-1	Tr-16
4	Main Link-1 + AUX Ch.	Main Link-0	Tr-16
5	Main Link-0	AUX Ch.	Tr-15

1. Connect the VNA ports (Port 1 to 4) to the test fixture ports with RF cables for victim channel insertion loss.
2. Press Channel Next to select Channel 2.
3. Select **Trace 7 (Sdd21).**
4. Press **Trigger** > Single
5. Press **Math** > Memory > Data → Memory

VNA port	Test #	Port 1	Port 3	Port 2	Port 4
Insertion loss connection for victim channel (Tr-7)	1	A ML3+	A ML3-	B ML3+	B ML3-
	2	A ML2+	A ML2-	B ML2+	B ML2-
	3	A ML1+	A ML1-	B ML1+	B ML1-
	4	A ML0+	A ML0-	B ML0+	B ML0-
	5	A AUX+	A AUX-	B AUX+	B AUX-

6. Connect the VNA ports (port 1 to 4) to the test fixture ports with RF cables for Single aggressor Far End Noise.

VNA port	Test #	Port 1	Port 3	Port 2	Port 4
Far end noise connection for single aggressor	1	A ML2+	A ML2-	B ML3+	B ML3-
	5	A ML0+	A ML0-	B AUX+	B AUX-

7. Select **Trace 15 (Sdd21).**
8. Press **Trigger** > Single.
9. Press **Math** > Analysis > Equation Editor…and turn it ON.

10. Connect the VNA ports (Port 1 to 4) to the test fixture ports with RF cables for Dual aggressor 1 Far End Noise.

VNA port	Test #	Port 1	Port 3	Port 2	Port 4
Far end noise connection for dual aggressor 1	2	A ML1+	A ML1-	B ML2+	B ML2-
	3	A ML0+	A ML0-	B ML1+	B ML1-
	4	A ML1+	A ML1-	B ML0+	B ML0-

11. Select **Trace 16 (Sdd21)**.
12. Press **Math** > Analysis > Equation Editor…and turn it OFF.
13. Press **Trigger** > Single.
14. Press **Math** > Memory > Data → Memory
15. Connect the VNA ports (Port 1 to 4) to the test fixture ports with RF cables for Dual aggressor 2 Far End Noise.

VNA port	Test #	Port 1	Port 3	Port 2	Port 4
Far end noise connection for dual aggressor 2	2	A ML3+	A ML3-	B ML2+	B ML2-
	3	A ML2+	A ML2-	B ML1+	B ML1-
	4	A AUX+	A AUX-	B ML0+	B ML0-

16. Press **Trigger** > Single.
17. Press **Math** > Analysis > Equation Editor…and turn it ON.
18. Once you finish the measurement, switch the Display Port cable end and repeat the same measurement for the opposite direction.
19. Load and confirm the measured value is within the limit shown below. Otherwise, it will show Fail.

DUT bit rate	Cable category	Connector type	Connector type
HBR2/HBR	All	All	DP1.4_HBR_FEN_Limit.CSV
RBR	All	All	DP1.4_RBR_FEN_Limit.CSV

Power Sum Equal Level Far-End Noise – Upper Limit for High Bit Rate Cable Assembly

Where f is given in GHz, f0 = 2.70GHz

$$PSELFEN_{\max.}[dB] = \begin{cases} -22 + 6Log_{10}\left(\frac{f}{f_0}\right); & 0.1 < f \le f_0 \\ -22 + 40Log_{10}\left(\frac{f}{f_0}\right); & f_0 < f \le 8.1 \end{cases}$$

Power Sum Equal Level Far-End Noise – Upper Limit for Reduced Bit Rate Cable Assembly

-26 dB; 0.1 < f ≤ 10 GHz.

Manual Setup

The procedures of manual setup for time domain and frequency domain measurements are introduced in this section for reference. All the required testing parameters have been properly set and saved in the respective standards testing state file (*.tdr).

Channel and trace setup

If TDR setup wizard is shown when launching the TDR software, click **Close** button in the TDR setup wizard main window.

1. Open **Setup** tab in the TDR software.
2. Click **Preset** to preset the instrument Click OK in a dialog box to continue.
3. Set **DUT Topology** to "***Differential 2-Port***" Click OK in a dialog box.
4. Click **Advanced Mode>>** and click Yes to enter to Advanced mode.
5. Set DUT Length to "Auto".

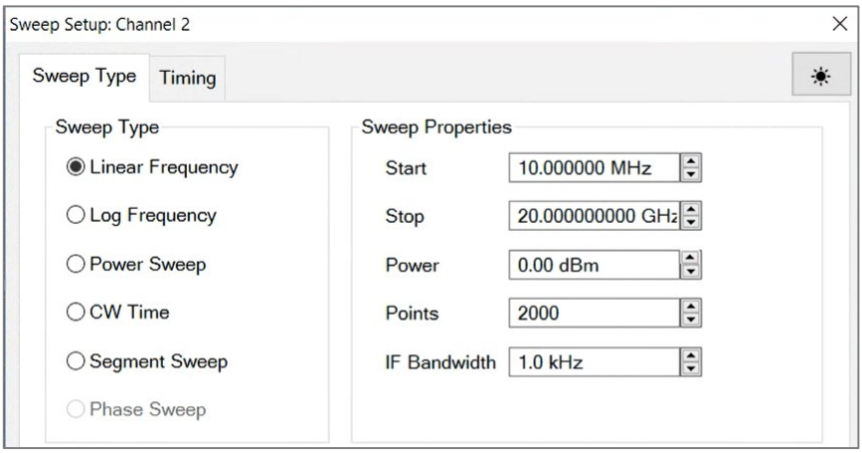


Frequency range setup

1. Based on DP2.1 CTS, setup the required testing requirements.
2. Select Sweep > Sweep Setup and key-in sweep properties as below:

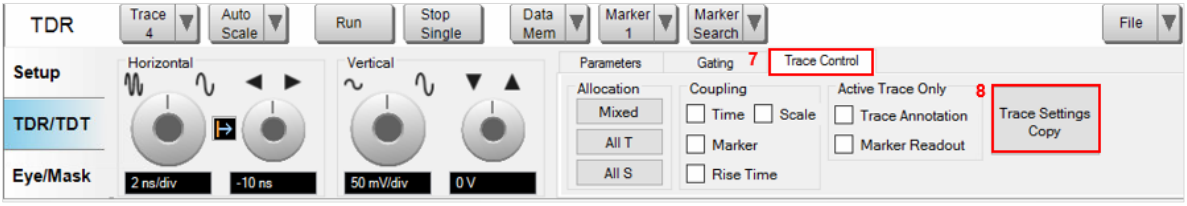
- Set **Start** value to "10 MHz".
- Set **Stop** value to "20 GHz".
- Set **Power** value to "0 dBm".
- Set **Points** and set to "2000".
- Set **IF Bandwidth** to "1 kHz".

Note: All frequency domain tests must follow the mandatory sweep setting defined by VESA.



Differential impedance profile

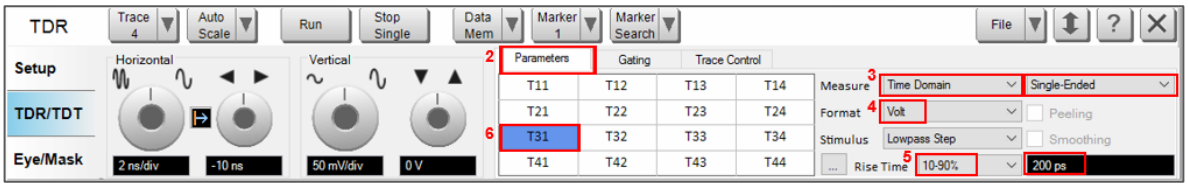
1. Select **Trace 1**.
2. Open **Parameters** tab.
3. Select "***Time Domain***" and "***Differential***" for Measure.
4. Select Formant to "***Impedance***".
5. Select **Rise Time** to "***20-80%"*** and input value "***25ps (DP80/DP54) or 50ps (DP8K or lower)***".
6. Click **Tdd11**.
   Input Horizontal scale (1 ns/div) and horizontal position (-1 ns).
   Input vertical scale (5 Ohm/div) and vertical position (25 Ohm).
7. Open **Trace Control** tab.
8. Click **Trace Settings Copy** to launch trace copy dialog box.



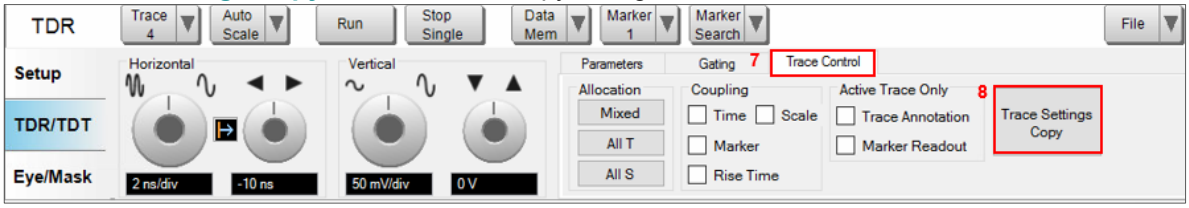
9. Select **Trace 1** the From list.
10. Select **Trace 2** in the To list.
11. Click **Copy**.
12. Click **Close**.
13. Select **Trace 2**.
14. Open **Parameter** tab.
15. Click **Tdd22**.

Intra-pair skew

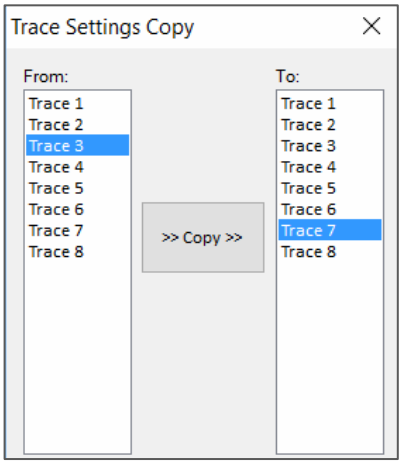
1. Select **Trace 3**.
2. Open **Parameters** tab.
3. Select "***Time Domain***" and "***Single-Ended***" for Measure.
4. Select Formant to "***Volt***".
5. Select **Rise Time** to "***20-80%"*** and input value to ***25ps (DP80/DP54) or 50ps (DP8K or lower)***.
6. Click **T31**.



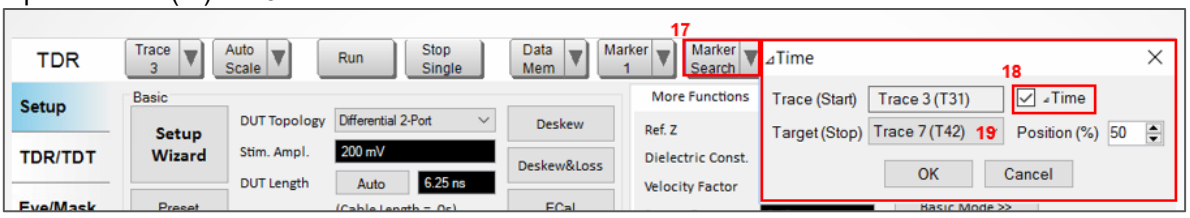
7. Open **Trace Control** tab.
8. Click **Trace Settings Copy** to launch trace copy dialog box.



9. Select **Trace 3** in the From list.
10. Select **Trace 4** in the To list.
11. Click **Copy**.
12. Click **Close**.



13. Select **Trace 4**.
14. Open **Parameters** tab.
15. Click **T42**
16. Select **Trace 3 (T31)**
17. Click Marker Search and select Δ Time
18. Check Δ Time
19. Select Target (Stop) to **Trace 4 (T42)** and click OK
20. Input Position (%) to 15.



Inter-pair skew

1. Select **Trace 5**.
2. Open **Parameters** tab.
3. Select "***Time Domain***" and "***Differential***" for Measure.
4. Select Formant to "***Volt***".
5. Select **Rise Time** to "***20-80%"*** and input value "***25ps (DP80/DP54) or 50ps (DP8K or lower)***".
6. Click **Tdd21**.
7. Input Horizontal scale (5 ns/div) and horizontal position (0 s).
8. Input vertical scale (100 mV/div) and vertical position (200 mV).
9. Press **Search**> **Target**> **Target Value** and enter 60 mV.
10. Press **Search**> **Target**> **Tracking**> **Target** to turn on **Tracking**.

Far End Noise (FEN)

1. Select **Channel Next** to select Channel 2 (Frequency Domain Measurement).
2. Select **Trace 15 (Sdd21)**.
3. Press **Math** > Analysis > Equation Editor…and enter the equation below:
4. “SingleAggressor= 20*log10(mag(data))-20*log10(mag(mem(7)))”
5. Select **Trace 16 (Sdd21)**.
6. Press **Math** > Analysis > Equation Editor…and enter the equation below:
7. “DualAggressor=10*log10(mag(data^2+mag(mem^2)-20*log10(mag(mem(7)))”

Defining limit line tables

1. Press **Trace Next** to select trace to set the limit line table.
2. Press **Math**> Analysis > Limit Table > Limit > to edit the limit table.

	Type	Begin Stimulus	End Stimulus	Begin Response	End Response
1	Max	50.0000 MHz	2.50000 GHz	-3.00000 dB	-3.00000 dB
2	Max	2.50000 GHz	12.0000 GHz	-1.00000 dB	-1.00000 dB
3	Off	0.000000 Hz	0.000000 Hz	0.000000 dB	0.000000 dB

3. Press **Math**> Analysis > Limit… > to launch Limit Test Setup window.
4. Select to turn on “Limit Test ON” and “Limit Line ON”, optional to turn on “Sound ON Fail”.

Appendix: DP80/DP54/DP8K Channel Limits

DP80 cable assemblies

	High speed test parameter	Tool	Requirement	Compliance test requirements
1	Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	Get_iPar & S4P	Normative	For DP80 DP to DP pairs: ≥ −1.0 dB at 0.1GHz, ≥ −4.0 dB at 2.7 GHz, ≥ −5.5 dB at 5 GHz, ≥ −6.5 dB at 6.75 GHz, ≥ −8.5 dB at 10 GHz, and ≥ −13 dB at 15 GHz. For DP80 DP to USB-C pairs: ≥ −1.0 dB at 0.1GHz, ≥ −3.8 dB at 2.7 GHz, ≥ −5.3 dB at 5 GHz, ≥ −6.2 dB at 6.75 GHz, ≥ −8.1 dB at 10 GHz, and ≥ −12.25 dB at 15 GHz.
2	Integrated Return Loss (IRL)	Get_iPar & S4P	Normative	For DP80 HS Pairs: IRL PWL limit ≤ -18.5dB @ ILfit -8.5 dB IRL PWL limit ≤ -15 dB @ ILfit -5 dB IRL PWL limit ≤ -15 dB @ ILfit -4 dB For DP80 DP to USB-C Pairs: IRL PWL limit ≤ -19.5dB @ ILfit -8.5 dB IRL PWL limit ≤ -15.5 dB @ ILfit -5 dB IRL PWL limit ≤ -15.5 dB @ ILfit -4 dB
3	Integrated Total Crosstalk (IXT_DP)	Get_iPar & S4P	Normative	For DP80 HS Pairs: IXT_DP PWL limit ≤ -36dB @ ILfit -8.5 dB IXT_DP PWL limit ≤ -34dB @ ILfit -5 dB IXT_DP PWL limit ≤ -34dB @ ILfit -4 dB For DP80 DP to USB-C Pairs: IXT_DP PWL limit ≤ -36.5dB@ILfit -8.5 dB IXT_DP PWL limit ≤ -34.5dB @ ILfit -5 dB IXT_DP PWL limit ≤ -34.5dB @ ILfit -4 dB
4	Differential to common mode conversion (SCD12/SCD21)	Get_iPar & S4P	Normative	For all DP80 HS Pairs: ≤ -17 dB from 100 MHz to 20 GHz
5	Integrated Multi-reflection (IMR)	Get_iPar & S4P	Informative	For DP80 HS Pairs: IMR PWL limit ≤ -34 dB @ ILfit -8.5 dB IMR PWL limit ≤ -28 dB @ ILfit -5 dB IMR PWL limit ≤ -28 dB @ ILfit -4 dB For DP80 DP to USB-C Pairs: IMR PWL limit ≤ -35 dB @ ILfit -8.5 dB IMR PWL limit ≤ -29 dB @ ILfit -5 dB IMR PWL limit ≤ -29 dB @ ILfit -4 dB
6	Integrated Crosstalk on DP Lanes (IFEXT)	Get_iPar & S4P	Informative	Integrated far-end crosstalk within a port: IFEXT ≤ -43 dB. (Up to 10 GHz)

DP54 cable assemblies

	High speed test parameter	Tool	Requirement	Compliance test requirements
1	Insertion Loss Fit Frequencies (ILFit)	Get_iPar & S4P	Normative	For DP54 DP to DP pairs: > −1.1 dB at 0.1GHz, > −6.5 dB at 2.7 GHz, > −8.0 dB at 4.05 GHz, > −9.0 dB at 5.0 GHz, > −10.5 dB at 6.75 GHz, > −16.7 dB at 13.5 GHz. For DP54 DP to USB-C pairs: > −1.05 dB at 0.1GHz, > −6.2 dB at 2.7 GHz, > −7.7 dB at 4.05 GHz, > −8.7 dB at 5.0 GHz, > −10.1 dB at 6.75 GHz, > −16.2 dB at 13.5 GHz.
2	Integrated Return Loss (IRL)	Get_iPar & S4P	Normative	For DP54 HS Pairs: IRL PWL limit is -23 dB @ ILfitAtNq of -10.5 dB, IRL PWL limit is -18.5 dB @ ILfitAtNq of ≥ -6 dB. For DP54 DP to USB-C Pairs: IRL PWL limit is -23 dB @ ILfitAtNq of -10.1 dB, IRL PWL limit is -18.5 dB @ ILFitAtNq of ≥ -6 dB.
3	Integrated Total Crosstalk (IXT_DP)	Get_iPar & S4P	Normative	For DP54 HS Pairs: IXT_DP PWL limit is -42 dB@ ILfitAtNq of -10.5 dB, IXT_DP PWL limit ≤ -31 dB @ ILfitAtNq of -4.3 dB, IXT_DP PWL limit ≤ -31 dB @ ILfitAtNq of 0 dB. For DP54 DP to USB-C Pairs: IXT_DP PWL limit is -46.5 dB@ ILfitAtNq of -10.1 dB, IXT_DP PWL limit ≤ -35.5 dB @ ILfitAtNq of -4.3 dB, IXT_DP PWL limit ≤ -35.5 dB @ ILfitAtNq of 0 dB.
4	Differential to common mode conversion	Get_iPar & S4P	Normative	For all DP54 HS Pairs: ≤ -17 dB from 100 MHz to 20 GHz
5	Integrated Multi-reflection (IMR)	Get_iPar & S4P	Informative	For DP54 HS Pairs: IMR PWL limit = -45 dB @ ILfit -11.3 dB IMR PWL limit ≤ -38 dB @ ILfit -4.3 dB IMR PWL limit ≤ -38 dB @ ILfit -3.0 dB For DP54 DP to USB-C Pairs: IMR PWL limit = -48 dB @ ILfit -11.3 dB IMR PWL limit ≤ -41 dB @ ILfit -4.3 dB IMR PWL limit ≤ -41 dB @ ILfit -3.0 dB
6	Integrated Crosstalk on DP Lanes (IFEXT)	Get_iPar & S4P	Informative	Integrated far-end crosstalk within a port: IFEXT ≤ -43 dB. (Up to 20 GHz)

DP8K cable assemblies

	High speed test parameter	Tool	Requirement	Compliance test requirements
1	Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	IntePar_DP & S4P	Normative	For DP8K DP to DP pairs: ≥ −5.5 dB at 1.35GHz, ≥ −8.5 dB at 2.7 GHz, ≥ −11.0 dB at 4.05 GHz, ≥ −13.3 dB at 5.0 GHz.
2	Integrated Return Loss (IRL)	IntePar_DP & S4P	Normative	For DP8K HS Pairs: IRL < 0.0336 × ILFitAtNq2 + 1.28 × ILFitAtNq – 8.87
3	Differential to Common Mode Conversion	IntePar_DP & S4P	Normative	For all DP8K HS Pairs: ≤ -17 dB from 100 MHz to 8.1 GHz
4	Integrated Multi-reflection (IMR)	IntePar_DP & S4P	Informative	IMR < 0.0579 × ILFitAtNq2 + 1.64 × ILFitAtNq – 23.23
5	Integrated Crosstalk on DP Lanes (INEXT/IFEXT)	IntePar_DP & S4P	Informative	Integrated far-end crosstalk within a port: IFEXT < -35dB (up to 12GHz) INEXT < -23dB (up to 12GHz)

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