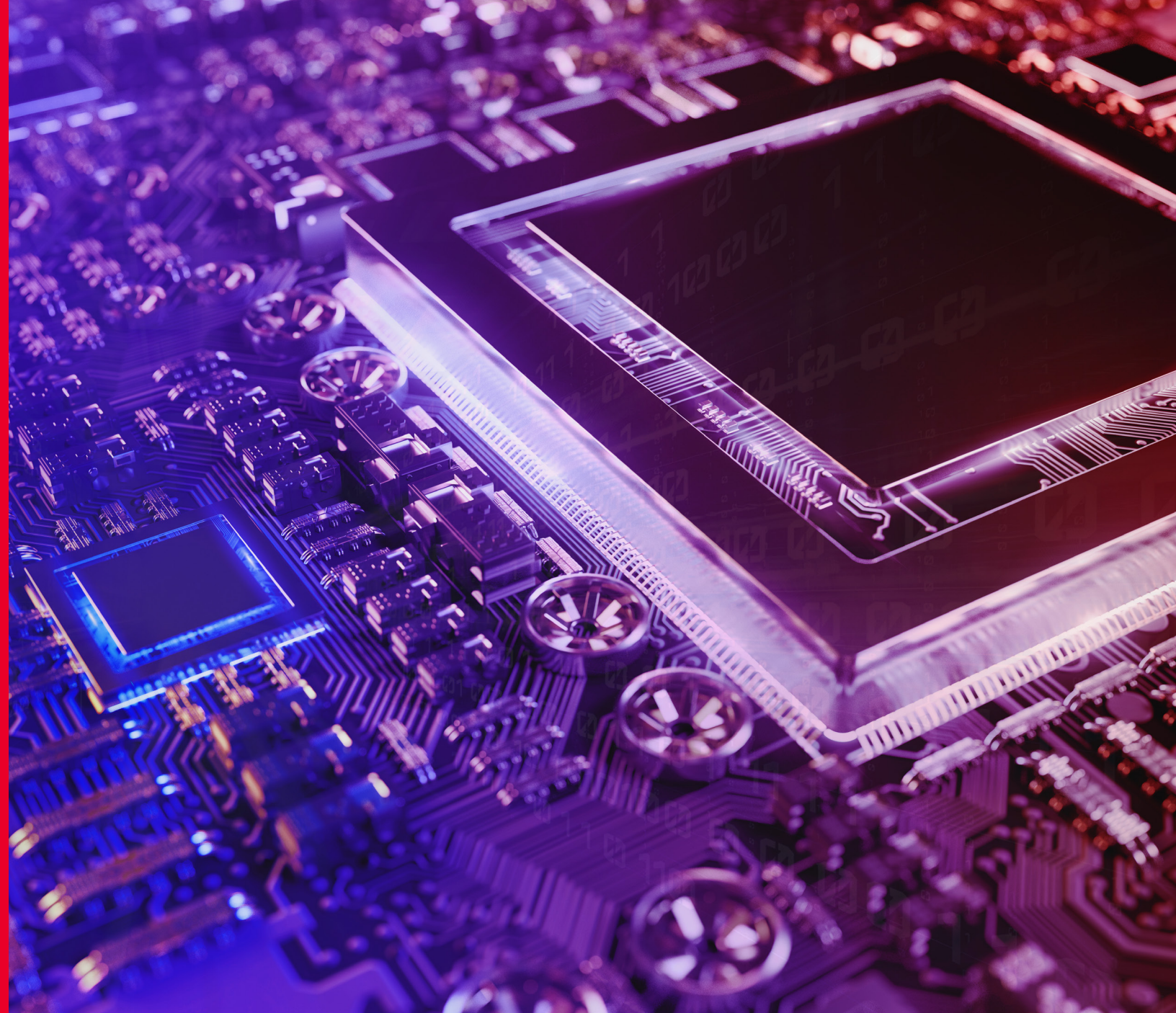




Power Integrity: The Foundation for Reliable Electronics Performance

eBook

 KEYSIGHT

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1. Introduction

Electronics have become an integral part of our daily lives in today's rapidly advancing technological landscape. From smartphones to smart homes and medical devices to autonomous vehicles, electronic systems play a pivotal role in shaping how we live and work.

However, the performance and reliability of these electronic devices and systems depend heavily on an often overlooked aspect: power integrity. Power integrity refers to the consistent and reliable delivery of electrical power to electronic components, which is paramount in ensuring the proper functioning of electronic systems. Electronics do not run without power, so power integrity is the foundation that drives signal integrity performance.

A great example of how power integrity drives the performance of signal integrity is autonomous vehicles. Autonomous vehicles produce

four terabytes of data from the sensors collecting data and then processing all that data.

With four terabytes of data, it becomes difficult to send all of that up to the cloud to be processed. As a result, there's a lot of local CPUs, FPGAs, and different technology to process that information locally and make decisions. If you start looking at the density of electronics on some of these autonomous vehicles, it's mind-boggling in the sense of how many different power rails are involved in delivering the correct power, the different power levels to all of the different electronics.

2. Technology and Simulation Test Trends in Electronics Design

Several technology drivers and test trends are influencing the power integrity field. These test trends help engineers and designers address the challenges of delivering clean and stable power to increasingly complex electronic

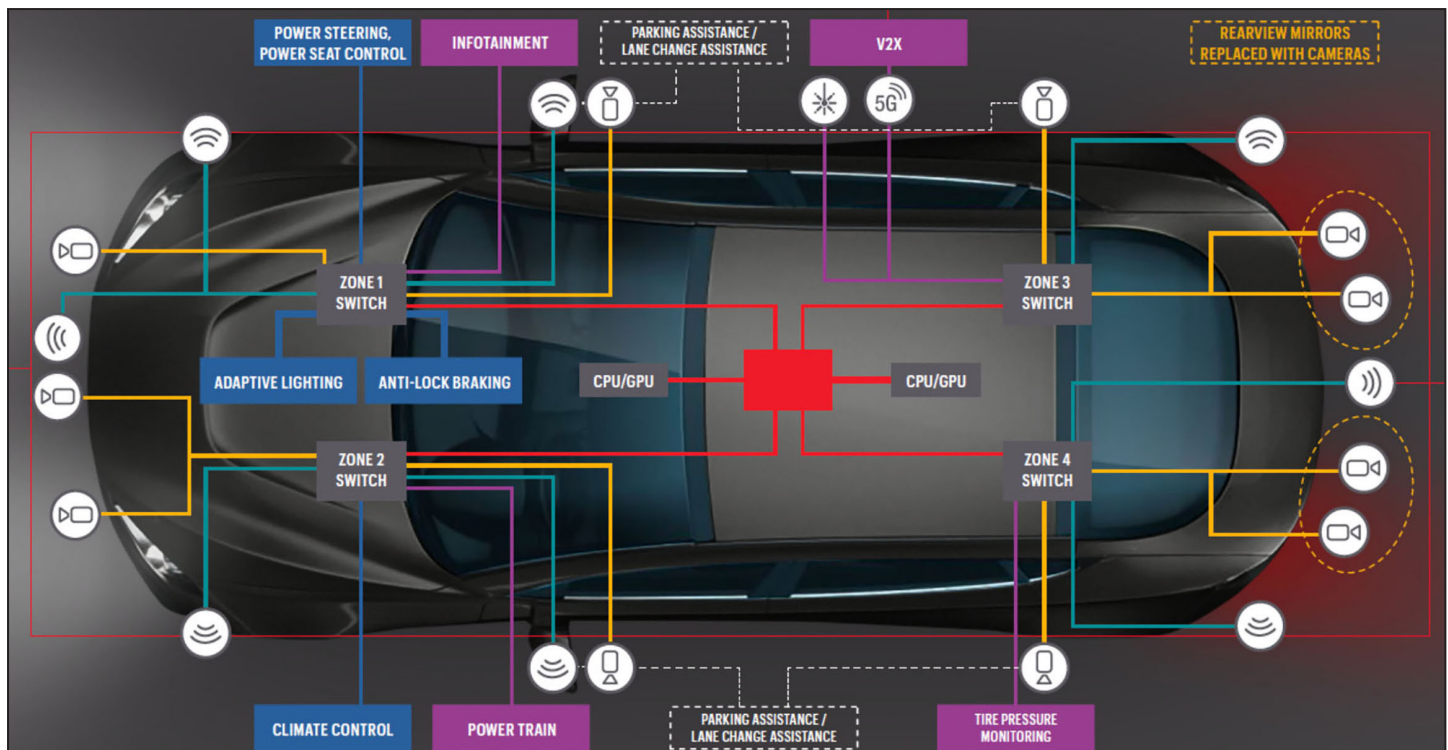


Figure 1: Autonomous vehicles require advanced electronics in dense packages to digest data from hundreds of sensors.

components. Here are some of the key drivers and test trends in power integrity:

2.1 Increasing Integration and Miniaturization

Driver: The trend toward smaller and more integrated electronic devices, such as mobile phones and IoT devices, requires highly compact printed circuit boards (PCBs) with densely packed components.

Trend: Testing and ensuring power integrity in compact PCB designs can be challenging. Techniques like 3D electromagnetic field solvers and simulation tools analyze power distribution in tight spaces where measurements cannot reach.

2.2 High-Speed and High-Performance Components

Driver: Modern electronic components, like microprocessors and FPGAs running at gigabit data processing speeds, demand fast and stable power delivery to operate at their maximum potential. The power delivery system must provide power from DC to the GHz frequency range of the final switching transistors at the load.

Trend: Advanced simulation tools leveraging measure-based component models are used to analyze transient voltage drop, noise, and power plane resonance at high frequencies to ensure that components receive the needed power. Simulation enables the exploration of worst-case noise by exciting worst-case resonance combinations often overlooked when using simple measurement step-load tests.

2.3 Low Power and Energy Efficiency

Driver: Energy-efficient electronics are essential for prolonging battery life in portable devices and reducing power consumption in data centers. Fast-switching eGaN technology for DC/DC converter design, along with point-of-load regulators moving closer and closer to the load, helps reduce

costly capacitors and IR drop losses. Power Management ICs, PMICs, can help manage low power modes and power on sequencing.

Trend: Engineers focus on optimizing power distribution networks by simulating cascaded and parallel power conversion topologies and optimizing decoupling capacitors. Low ESR capacitors can help reduce losses, but designing for a controlled decoupling capacitor ESR to achieve flat impedance helps to avoid noise ripple from resonances. End-to-end power integrity measurements can measure fabricated hardware efficiency and validate low-power states.

2.4 DDR and High-Speed Memory Interfaces

Driver: DDR (Double Data Rate) single-ended memory interfaces and other high-speed memory technologies require careful power integrity design to minimize signal integrity issues. Single-ended data transmission requires fewer I/O device pins but produces more significant noise-producing di/dt transients on the power rail.

Trend: The DDR industry supports power-aware simulation models enabling end-to-end simulations of the power rail that include the dynamic behavior of the single-ended burst DDR data. This mission mode dynamic load on the power rail results in voltage noise ripples on the power rail that then directly influence the DDR signal levels in the power-aware model. High-density DDR routing is also efficiently simulated for power rail crosstalk into other systems.

2.5 Decoupling and Capacitor Technologies

Driver: Proper decoupling is essential to provide low noise minimum voltage ripple power delivery across the full bandwidth of the dynamic current demands of the high-speed digital load.

Trend: Engineers are exploring advanced capacitor technologies to maximize capacitance with

the lowest possible ESL and ESR, and decoupling solutions to optimize power integrity.

2.6 Electromagnetic Compatibility (EMC) and Signal Integrity

Driver: Ensuring that power distribution does not interfere with electromagnetic compatibility and signal integrity is crucial to power integrity.

Trend: Co-simulation of EMC, signal integrity, and power integrity is becoming more common. This approach allows engineers to analyze the interactions between these aspects and optimize designs for all three.

2.7 Advanced Materials and Manufacturing Techniques

Driver: Advanced PCB materials and manufacturing methods are being developed to address the challenges posed by high-speed electronics.

Trend: Material testing and modeling help ensure that the PCB stack-up and materials provide adequate power integrity. Manufacturing techniques such as thin high dielectric materials, controlled impedance routing, and tight tolerance components are employed to meet design requirements.

2.8 Power Delivery Network Resilience

Driver: The need for reliable operation in safety-critical systems, such as automotive and aerospace applications.

Trend: Testing for resilience against extreme conditions, such as temperature variations, electromagnetic interference, and power supply stability, is becoming a critical part of power integrity verification.

These drivers and trends highlight the evolving nature of power integrity in electronics and PCB design. Engineers and designers must adapt to these changes to ensure that electronic systems

continue functioning with high reliability and performance while addressing the unique challenges of modern technology.

3. Miniaturization and Chiplets Adoption

Printed Circuit Boards (PCBs) are the backbone of modern electronics, serving as the foundation upon which electronic components are interconnected to form functional devices. Over the decades, the electronics industry has witnessed an unceasing quest for innovation and advancement, leading to the evolution of PCBs.

A significant driver behind this evolution is the demand for miniaturization and the adoption of chiplets technology. Miniaturization refers to the process of reducing the size of electronic components and devices. In contrast, chiplets refer to small integrated circuits (IC) with specific functionality (memory, logic, accelerator, transceiver, etc.) that is intended to be combined and connected with other chiplets in a shared package. The combined impact of these trends has led to the rising complexity of packaging technology, fundamentally transforming the way electronics are designed, manufactured, and used.

Advancements in miniaturization have led to IC packages with a higher level of integration which requires careful attention to details such as component layout routing, heat dissipation, package capacitors for power integrity, signal integrity, and reliability.

3.1 Heterogeneous Integration of Chip Scale Packaging

The high scalability achieved by integrating multiple heterogeneous chiplets in a single design has led to increasingly complex packaging technology. This complexity manifests in several ways:

High component density: Multi-layer laminate packaging often features a high component density. This requires careful placement

of components and routing of traces to ensure signal integrity and prevent crosstalk, ground bounce, EMI, and thermal issues.

Signal integrity challenges: Standardized serial and parallel data interfaces for chiplets help to simplify integration, allowing diverse chips to “plug” together. However, standard interfaces also have fixed routing topologies and layout design constraints. Floor planning placement of multiple chiplets is critical for controlling impedance and mitigating crosstalk.

Thermal management: Heterogeneous multi-chip packages are prone to heat buildup due to the proximity of components. Effective thermal management is crucial to prevent overheating and ensure long-term reliability.

Power distribution: Efficient power distribution is essential in miniaturized PCBs. Ensuring power is supplied to all components without voltage drop or interference is complex.

Compatibility and interoperability: Integrating chiplets from different manufacturers introduce compatibility and interoperability challenges. Ensuring that chiplets communicate effectively and reliably with the rest of the PCB requires additional attention.

Manufacturing challenges: The manufacturing of miniaturized PCBs demands precision and often

relies on advanced manufacturing techniques, such as microfabrication and multilayer PCBs, which can be more costly and time-consuming.

Testing and validation: Miniaturized PCBs are more challenging to test and validate due to the compact design and complexity of the components. Specialized testing equipment and methodologies may be required.

3.2 The Rise of Chiplets

In recent years, chiplets have emerged as a revolutionary semiconductor design and packaging technology. A chiplet is a modular IC with dedicated functionality intended to be combined and connected with other chiplets in a shared package.

It helps with design reuse by breaking functionality into smaller blocks (memory, transceiver, accelerator, etc.) that make integration easier and not be tied to the same process node (logic = 3 nm, DRAM = 7 nm, and so on). Chiplets communicate with one another with die-to-die interconnects that use an open specification, the Universal Chiplet Interconnect Express (UCIe).

Adopting chiplets has redefined how PCBs are designed, validated, and assembled. While offering significant advantages, it introduces new complexities related to interconnectivity, thermal management, and compatibility between chiplets and traditional PCBs. As chiplets

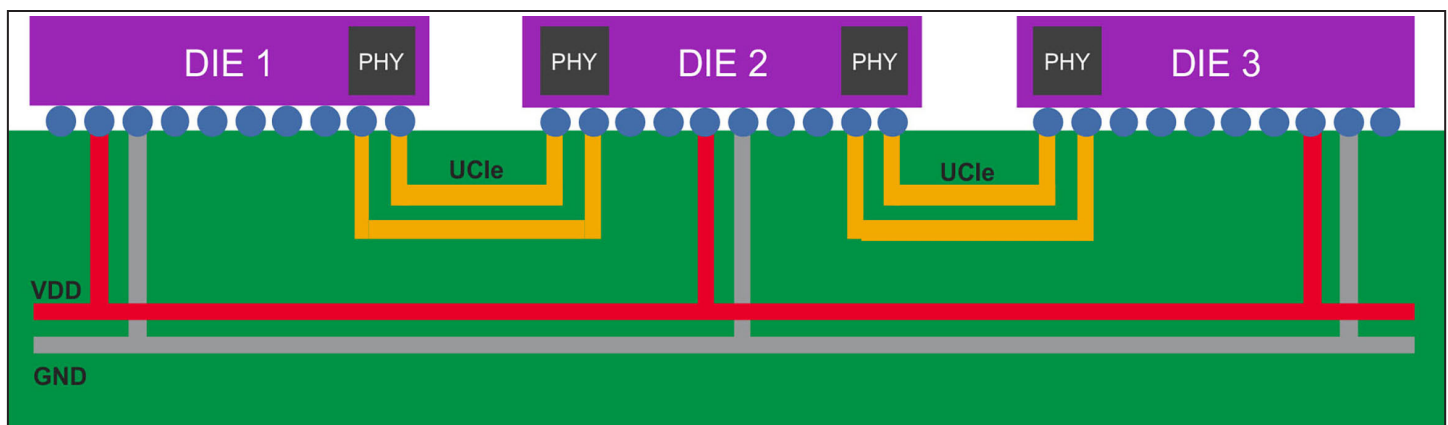


Figure 2: Typical multi-chiplet physical architecture

become mainstream, electronic design automation (EDA) software must continue evolving to meet the demands of the next generation of electronic devices.

4. Overview of Electronic Design Automation

Electronic Design Automation (EDA) is a field that emerged in response to the growing complexity of electronic systems in the mid-20th century. As electronic devices became more sophisticated, the manual design processes used earlier became impractical. Engineers needed automated tools to handle the intricacies of designing integrated circuits (ICs), laying the foundation for EDA.

The early 1960s marked the birth of EDA, with the advent of computer-aided design (CAD) tools that could assist engineers in schematic capture and manual routing. These early tools were rudimentary compared to today's EDA

suites but were instrumental in reducing design time and errors.

In the 1970s, the introduction of SPICE (Simulation Program with Integrated Circuit Emphasis) revolutionized electronic circuit design. SPICE allowed engineers to simulate electronic circuits accurately, enabling iterative design improvements and increasing the reliability of electronic systems.

In the 1990's EM simulators started to evolve rapidly to address the growing need for high frequency circuit simulation. At first EM simulators were driven by the RF/uW community, but rapidly expanded to high-speed digital electronics to address both SI and PI challenges.

As electronic technology advances, driven by the relentless pursuit of smaller, faster, and more efficient electronic devices, designing robust and reliable power delivery networks (PDN) becomes increasingly important. As a result, EDA tools must

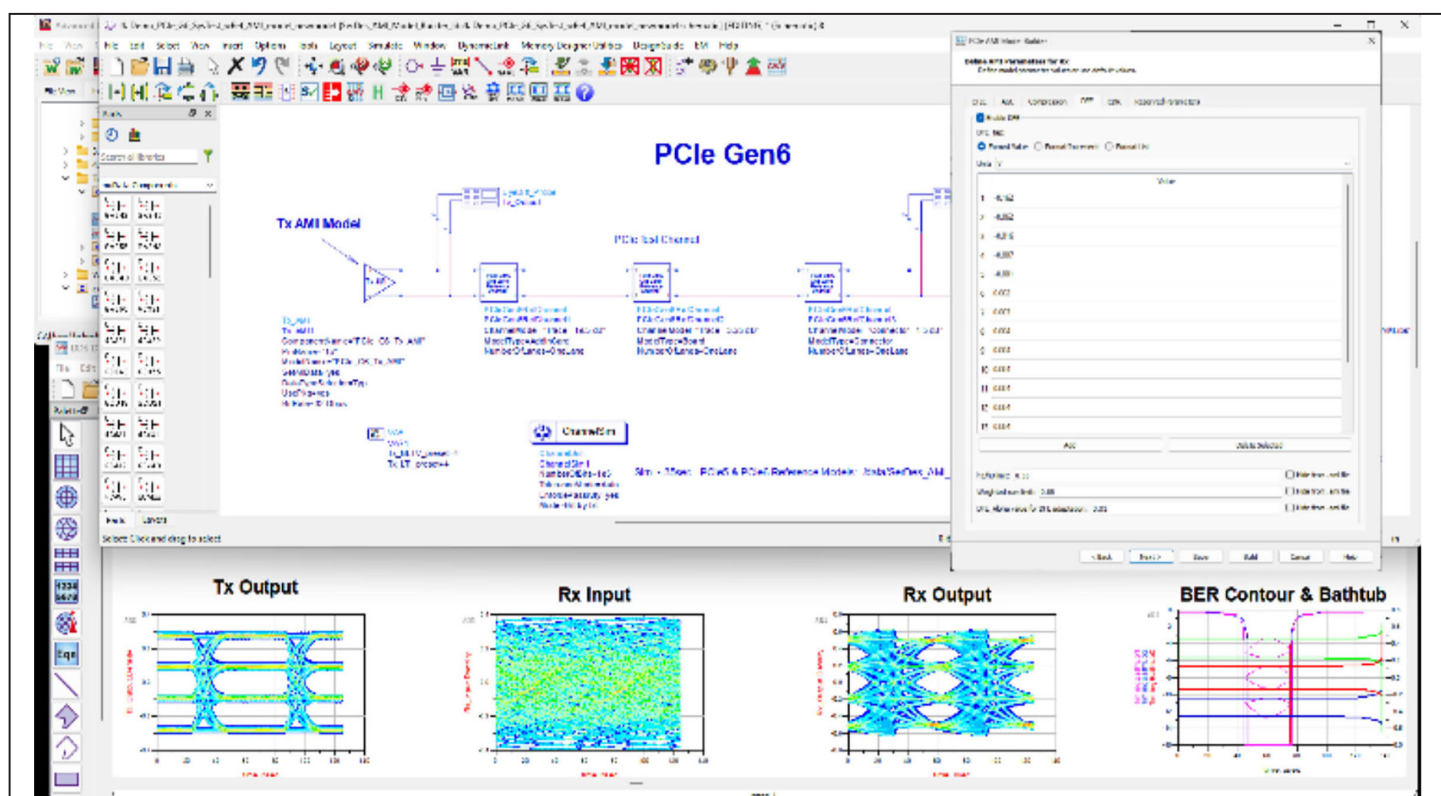


Figure 3: Keysight EDA software aid engineers to explore design trade-offs in the latest high-speed digital technologies.

continue to evolve to offer essential capabilities for PDN simulation, analysis, and optimization.

4.1 Key Concepts in EDA

To understand the role of EDA in PDN design, it is crucial to grasp some fundamental concepts in EDA:

Electronic Design Automation Tools: EDA tools encompass a wide range of software and hardware applications used for electronic design. These tools include schematic capture, simulation, layout design, verification, and testing tools, among others. EDA tools have evolved to handle not only digital but also analog and mixed-signal designs.

Design Abstraction Levels: EDA tools operate at multiple levels of design abstraction. These levels include behavioral, RTL (Register Transfer Level), gate-level, and physical-level abstractions. The choice of abstraction level depends on the specific design task and the desired trade-offs between design accuracy and efficiency.

Design Methodologies: EDA promotes structured design methodologies, such as VLSI (Very Large-Scale Integration) and ULSI (Ultra-Large-Scale Integration), to manage the complexity of modern electronic systems. These methodologies involve hierarchical design, reuse of IP (Intellectual Property) blocks, and design for manufacturability (DFM) principles.

Verification and Validation: EDA tools provide extensive verification and validation capabilities. These include logic simulation, formal verification, static timing analysis, and physical verification to ensure that the designed circuits meet performance, functionality, and manufacturability criteria.

Power Integrity Analysis: EDA tools are equipped with EM simulators for power integrity analysis, allowing engineers to simulate and analyze the

DC and AC behavior of the PDN under different operational scenarios. This analysis helps in identifying and mitigating voltage drops and resonant noise sources that can affect circuit performance.

Co-Design of Digital and Analog Blocks: In modern ICs, digital and analog blocks often coexist on the same chip. EDA tools enable the co-design of these blocks and facilitate their integration into a harmonious PDN, ensuring that digital switching noise does not interfere with sensitive analog circuitry.

Thermal Simulation: Thermal management is a critical aspect of PDN design, as excessive heat can degrade performance and reliability. EDA tools provide thermal simulation capabilities to predict and address thermal issues, ensuring that the PDN can dissipate heat effectively.

Package and PCB Design: Beyond IC design, EDA tools are also used in package and PCB (Printed Circuit Board) design. These tools help optimize the PCB's layout of components, traces, and power delivery networks, ensuring efficient power distribution and signal integrity.

4.2 Key Concepts in Power Integrity

Several power integrity concepts must be understood to a successful new design completion:

Decoupling Capacitors: Decoupling capacitors are a critical part of the power delivery in an electronic design to ensure power integrity at the higher frequencies that are required by a digital load. They are strategically placed on a circuit board to absorb transient voltage spikes and supply fast current delivery to avoid dips, thus providing a stable voltage supply to integrated circuits. These capacitors act as a stable high frequency source of power, preventing abrupt changes in voltage that could affect device performance.

Controlled Impedance Routing: Proper controlled impedance routing can help minimize voltage drops and electromagnetic interference (EMI). Additionally, the length, width, and impedance of traces must be optimized to minimize resistive losses and inductance. Dynamic current from the load multiplied by any resistance or inductance in the PDN path leads to voltage noise ripple.

Voltage Regulation: Voltage regulators are vital in maintaining stable power supplies. They are responsible for converting an input voltage to a precise and constant output voltage with a wide range of load currents. For instance, voltage regulators are commonly used to ensure that the voltage supplied to microcontrollers remains within the specified operating range. In power fluctuations, voltage regulators adjust the output to maintain a steady supply, preventing damage to sensitive components.

Signal and Power Integrity Interdependency: By examining signal propagation and signal quality in high-speed digital designs, engineers can identify potential problems that may impact power integrity. Tools like simulation software and network analyzers can help pinpoint issues such as reflections, crosstalk, and overshoot, leading to signal degradation and lost data.

Power Distribution Networks (PDN): Modern electronic systems have complex power distribution networks, often with multiple voltage domains and power rails. Engineers must carefully design these networks to provide the right amount of power to each component while also managing power fluctuations and noise. Effective power distribution includes designing low-impedance power planes, incorporating power on sequencing techniques to reduce power surges, and establishing proper power budgets for different functional blocks within a system.

5. Factors to Consider Designing a Reliable and Robust PDN

5.1 Flat Impedance Design

Designing for flat impedance across various frequencies is crucial for electronic and radio frequency (RF) systems. In high-speed digital designs, it takes only one rogue voltage wave to kill a PDN. Flat impedance optimization before layout lowers the risk of rogue voltage waves in your design. To achieve this, you need to consider the following aspects:

Frequency Range Definition: Start by specifying the frequency range you want to maintain a flat impedance. Consider the minimum and maximum frequencies of interest.

Target Impedance Selection: Determine the desired impedance value for the frequency range you are working with. The specific value will depend on your application. 50 ohms is commonly used in electronic PCB design because it balances low attenuation and power handling well.

Detecting and Addressing Sources of Resonance: Use circuit analysis and simulation tools to identify any resonant frequencies in your system. Resonance can lead to impedance variations. Address resonance issues by adding damping components such as decoupling capacitors, distributed inductors, and resistors to spread the resonance.

Power Supply Bandwidth Extension: Ensure your power supply systems have sufficient bandwidth to support the desired frequency range. Use appropriate bypass capacitors and low-impedance power distribution networks to minimize power supply impedance.

Determining Loads and Noise Sources: Analyze the loads connected to the system and their impedance characteristics. Ensure that they match

the desired impedance. Identify noise sources in your system and take measures to reduce their impact on impedance stability.

Balanced vs. Unbalanced Impedance: Determine whether you need a balanced or unbalanced impedance design. Unbalanced impedance is typical in single-ended systems, while balanced impedance is used in differential systems.

Component Selection and Placement: Carefully select and place components in your design to minimize parasitic effects, such as parasitic capacitance and inductance. These can introduce impedance variations.

Impedance Transitioning: Use impedance matching techniques, such as L-section or T-section matching networks, to transition between impedance values if necessary.

5.2 Impedance Optimization in the Frequency Domain

A common challenge for PI engineers is designing power delivery systems that meet their circuits' time domain voltage ripple specifications. However, analyzing the power rails only in the time domain may not reveal the complete picture of their performance. A better approach is to use the frequency domain to ensure that the

impedance of the power delivery system is flat and resistive across a wide bandwidth.

This technique lets us quickly identify if the power rails behave like capacitors, inductors, or resistors at different frequencies. Capacitors and inductors have phase shifts between voltage and current, which can cause noise and resonance problems. Resistors have no phase shift, providing a stable and quiet power delivery. Understanding and applying this concept can help PI engineers design more robust and reliable power delivery systems.

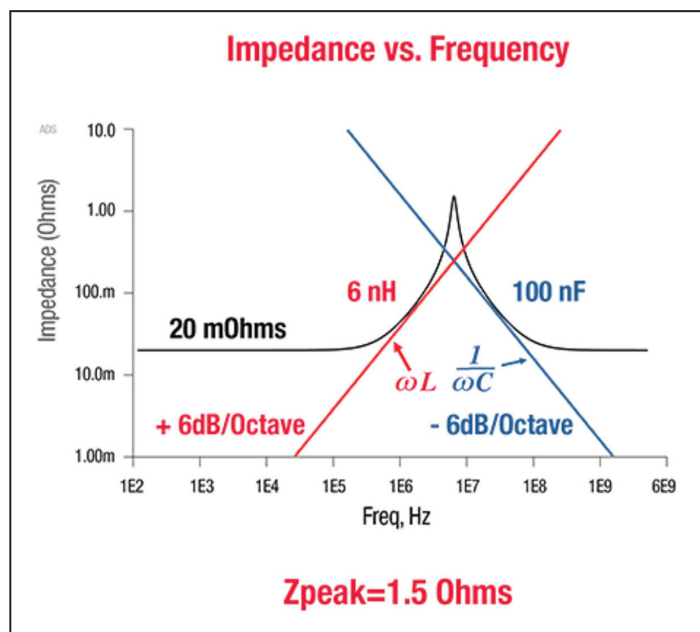


Figure 4: Impedance behavior in the frequency domain indicates if voltage and current are out of phase.

"One of the themes that goes through all of power delivery and supply is that they are not running on direct current (DC); they use alternating current (AC). When power is AC and not DC (a steady state non-changing supply), impedance becomes critical. The idea is to match source and load impedance and optimize it in the frequency domain, so you don't get reflections."

Heidi Barnes,
Senior Applications Engineer, Keysight

5.3 Capacitor Selection Optimization and Placement

Optimizing capacitor selection and placement is crucial for ensuring power integrity in electronic systems. Proper selection and placement of capacitors help reduce voltage noise, maintain a stable power supply, and prevent signal integrity issues.

Figure 5 depicts the key factors that go into capacitor selection and placement:

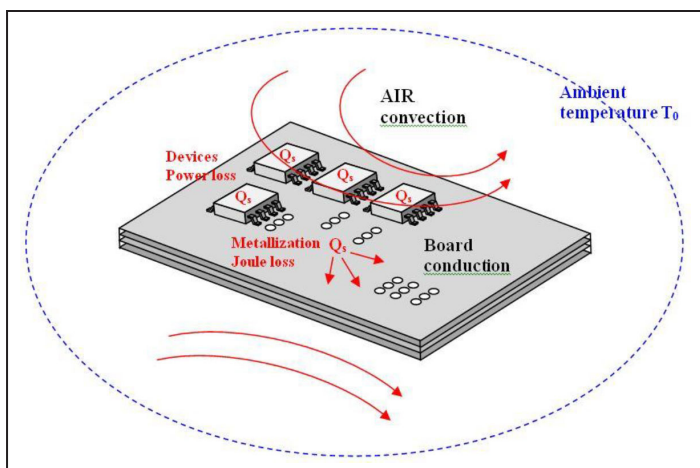


Figure 5: Key factors that influence capacitor selection and placement.

"The sophistication of the computer tools is so advanced now that they are designed to help us figure out what capacitors to put where on the board in order to achieve the end performance. A lot of that is automated now in Keysight software and so that takes a lot of pressure off the engineers."

Steve Sandler,
Founder and CEO of Pictotest.

By carefully selecting and placing capacitors, you can improve power integrity, reduce voltage noise, and maintain stable power supplies in your electronic systems. Additionally, it is essential to perform thorough testing and measurement to validate the effectiveness of your capacitor selection and placement in real-world conditions, which will be covered in the next section.

5.4 Simulation and Measurement Reconciliation

Reconciling measurement and simulation in power integrity design is crucial to ensuring that electronic systems function in the real-world as intended with respect to their power supply.

Simulation is the first step when designing new PCBs. It is a cost-effective way to explore design trade-offs without spinning new versions of a

PCB. However, simulations are only as accurate as their models. Poorly created models, that are done without subsequent measurement reconciliation, can result in wasted time and money.

"The simulation is a valuable tool that reflects the careful choices and expertise of the person who created it. However, it may not capture all the nuances and complexities of reality. The measurement is a reliable source of data that shows the actual outcomes and effects of the phenomenon."

Heidi Barnes,
Keysight

Measurement reconciliation is the process of comparing real-world measurements with simulation results and using this information to fine-tune PDN component models. Designers gain real-world insights that improve their overall model accuracy by systematically performing simulation and measurement reconciliation. Over time, it allows them to build comprehensive and high-accuracy model libraries that can be reused in future designs.

Next, for precise and accurate measurements, it is essential to understand the physical characteristics of the signal you are trying to measure and use high-performance instrumentation that does not interfere with it. Real-time oscilloscopes and high-impedance probes are often used to improve

"If I got a simulation and a measurement that agree with each other, that's great because it is two independent approaches that give you the same answer. Only then you can believe that there's a really good probability that your design will behave as expected."

Steve Sandler,
Founder & CEO, Picotest

measurement performance. For example, using a 50 ohms probe to connect to the milliohm impedance of a power rail will result in a considerable reflection that will misrepresent the actual signal you are trying to measure.

5.5 Voltage Regulator Module Selection and Stability Analysis

VRM

Selecting the appropriate voltage regulator module (VRM) is crucial in power delivery network design. The VRM is responsible for regulating the power supply's voltage level to the required load level. The VRM selection is not arbitrary, and it is essential to consider the following factors:

- **VRM voltage mode vs. current mode control:** The VRM can operate in either voltage mode or current mode control. The voltage mode control is more sensitive to tolerances, while the current mode control is less sensitive.
- **VRM shunt feedback vs. series feedback for transconductance amplifiers:** The VRM can use either shunt feedback or series feedback for transconductance amplifiers. The series feedback is better suited for transconductance amplifiers.
- **Flat impedance:** Flat impedance is the PDN design goal. The VRM should have a flat impedance to reduce the package anti-resonance at higher frequencies.
- **Tolerance impact:** Tolerances can impact voltage mode, feed-forward mode, and current mode VRMs. It is essential to consider the tolerance distribution when selecting the VRM.
- **Power Supply Rejection Ratio (PSRR):** PSRR is the ratio of the input voltage ripple to the output voltage ripple. The VRM should have a high PSRR to minimize the power supply noise.

Stability Analysis

Ensuring the VRM's stability is crucial because an unstable VRM can lead to voltage fluctuations and, in the worst case, cause system malfunction or damage to components. Stability analysis focuses on understanding the behavior of the VRM and its interaction with the load and the power distribution network. The following analysis are commonly used in stability evaluation:

- **Transfer Function Analysis:** involves creating a transfer function that describes the relationship between the input and output voltage variations of the VRM. This transfer function is crucial for predicting the VRM's performance under different load conditions.
- **Bode Plot:** Used to analyze the VRM's transfer function. These plots show the magnitude and phase of the transfer function over a range of frequencies. The stability of the VRM can be determined by examining the phase margin and gain margin. A stable VRM should have sufficient phase and gain margins to prevent oscillations and voltage spikes.
- **Control Loop Analysis:** For switching VRMs, control loop analysis is crucial. This involves studying the control loop's dynamics, which includes factors like the loop gain, bandwidth, and stability criteria such as the Nyquist criterion.

6. Power Integrity Measurement Tips

Tip 1. Choose the Lowest Noise Oscilloscope Measurement Path

If you are about to measure the noise riding on your DC supply, you want the noise of your oscilloscope measurement system to be as small as possible.

For many oscilloscopes, the 50 ohm (Ω) input is a lower-noise path than the 1 M Ω path. The image below shows the baseline noise of the

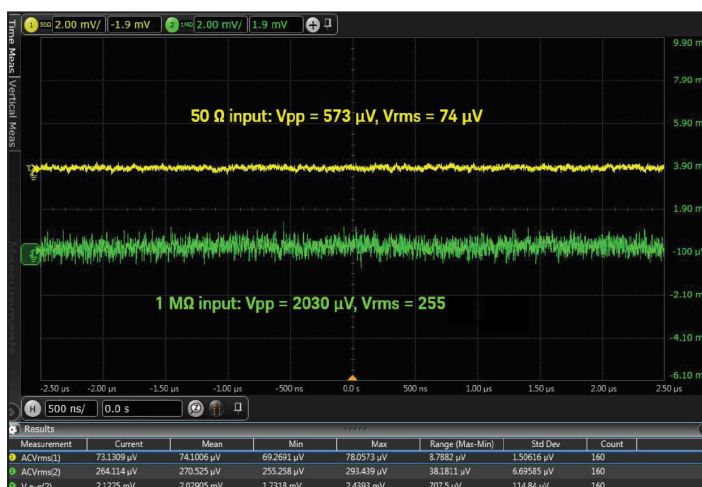


Figure 6: Baseline noise comparison of 50 Ω and 1 M Ω scope input of a Keysight Infiniium MXR104A.

50 Ω input and 1 M Ω input of a Keysight DSO-S054A high-definition oscilloscope (500 MHz, four channels).

This type of measurement, commonly called a null measurement, tracks the baseline noise of your oscilloscope measurement system. It is a sanity check similar to shorting the leads together on a digital multimeter (DMM) before making a continuity or resistance measurement. It is a good practice to perform a null measurement on your complete oscilloscope measurement system — including probe — to be confident that your scope and probe are appropriate for the power supply noise measurements you are about to make.

To make a null measurement, configure your oscilloscope and probes as you intend to use them when making your supply noise measurement. Then short the input to ground (or short the inputs together on a differential probe) and measure the noise.

Tip 2. Limit Bandwidth to Reduce Measurement System Noise

More bandwidth is not always better. The noise voltage of an oscilloscope and probe is a function of frequency. Limiting the bandwidth to just the amount necessary for the given measurement

reduces the amount of oscilloscope and probe noise in the measurement.

Consider the measurements shown in the figure 7 below. For these measurements, a null measurement described above was performed using a Keysight MXR-Series oscilloscope (6 GHz, 10-bit ADC, 16 GSa/s) with an N7020A power rail probe (2 GHz, 1:1 attenuation).

Tip 3. Use 1:1 Attenuation to Reduce Measurement System Noise

Oscilloscope probes come in a variety of attenuation ratios. One of the most common passive probes is the 10:1. One benefit of using a 10:1 probe is that it allows you to measure signals that otherwise would exceed that maximum input to the scope. The downside of attenuation is that the size of the scope noise relative to the size of the signal you are measuring increases proportionally to the attenuation ratio.

Consider the measurement result shown in Figure 8 below. Both a 10:1 probe and a 1:1 probe are measuring the same signal simultaneously — a 20 MHz 50 mVpp sine wave. The only difference between the two measurements is the attenuation ratio. The 1:1 measurement is 52 mVpp, while the 10:1 measurement is 65 mVpp. The higher attenuation ratio overstates the measurement by at least 25% because of the reduced signal-to-noise ratio resulting from the higher attenuation ratio. From this, we can see that when measuring small signals where oscilloscope and probe noise can be problematic, it is best to use as small an attenuation ratio as possible or available.

Tip 4. Use Probe Offset to Increase Dynamic Range

Probe offset is a feature of active probes that enables the user to remove DC content from signals under measurement. This feature is especially useful when a small AC signal is riding on a DC



Figure 7: Baseline noise at various bandwidth limits with the Keysight N7020A power rail probe and MXR-Series oscilloscope.

signal, as is the case when measuring power rail noise. In the Figure 9 below shows the noise measurement results on a 1.5 V supply with and without the use of probe offset. The attenuation applied by the oscilloscope at the larger V / division settings causes the difference.

Tip 5. Understand the Limitations of DC Blocks

A DC block is a specialized large-value capacitor that you can place in series with the signal before the input to the oscilloscope. The benefit of a DC block is that it removes the large DC component so you can place

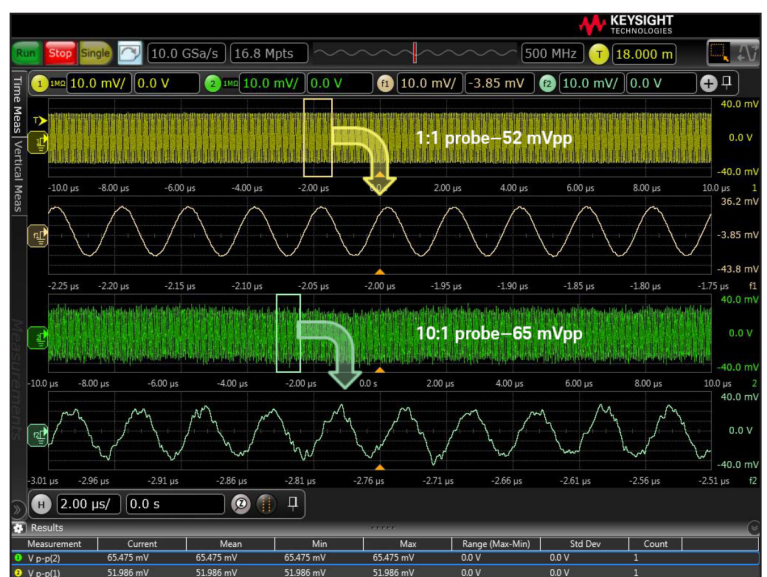


Figure 8: Noise comparison of a 1:1 and 10:1 probe measuring a 50 mVpp sine wave.

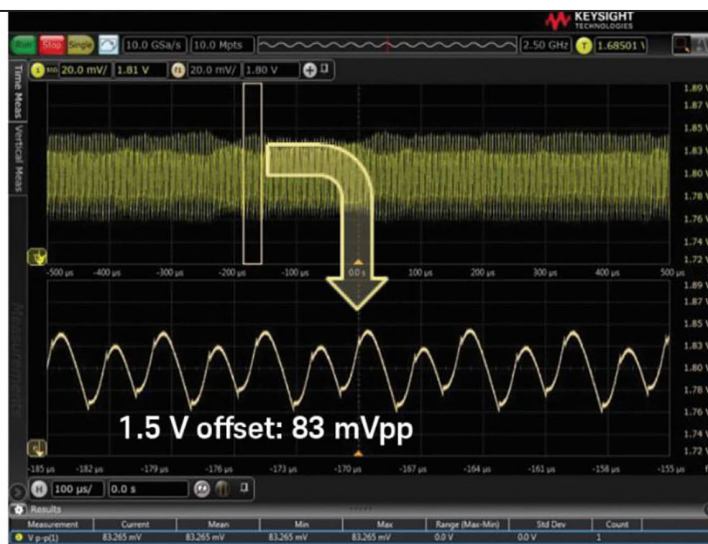


Figure 9: Measuring the noise on a 1.5 V DC supply with no offset and with the use of probe offset.

the scope in a more sensitive range — the same measurement principle mentioned previously regarding using a probe offset. The limitation of a DC block is that it blocks low-frequency AC content, such as drift or supply compression, in addition to the DC content.

Tip 6. Minimize Oscilloscope and Probe Loading of the Supply

Any time an oscilloscope probes a system, it becomes part of that system because of the electrical contact it makes. This process changes the behavior of the system under measurement. This is known as loading, and the goal is to minimize it as much as possible.

Tip 7. Use the Frequency Domain for Analysis

Using an oscilloscope's fast Fourier transform (FFT) capabilities to view signals in the frequency domain can help identify sources contributing to a supply's noise.

Tip 8. Use Triggering to View and Measure Signal Components in the Supply Noise

Triggering can help you visualize and measure components of supply noise that are coupling into the supply from, and are phase coherent to, other elements in the system.

Tip 9. Have Enough Bandwidth

In Tip 2, we discussed the value of limiting the bandwidth of the measurement to only that

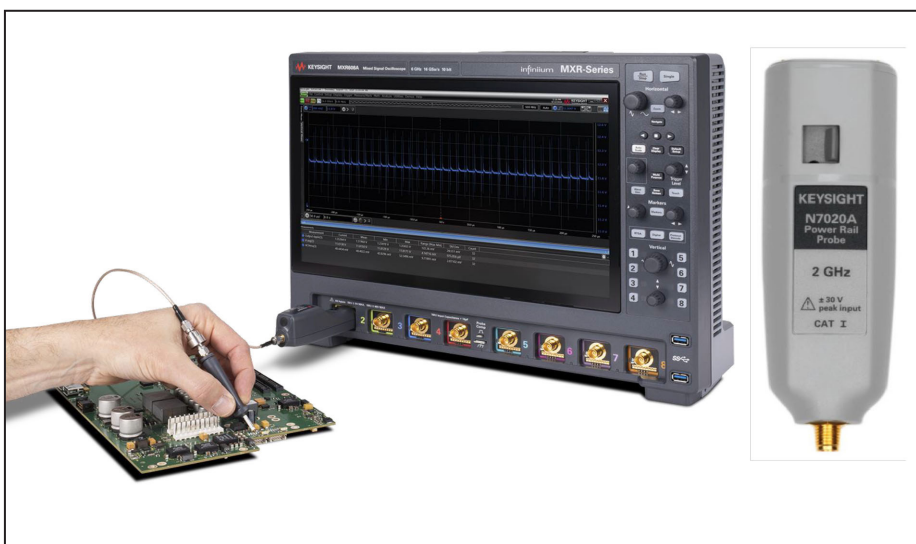


Figure 10: N7020A power rail probe (right) was designed specifically for measuring power supply noise and works with a variety of Keysight oscilloscopes, including the Infiniium MXR-Series high-definition oscilloscopes (left).

needed to minimize noise for the task at hand. An opposite pitfall can await users who do not have enough bandwidth for the task — they may miss high-frequency noise and transients that can adversely affect clocks and data in their systems.

Tip 10. The N7020A Power Rail Probe

The previous tips will help minimize oscilloscope measurement system noise when measuring power supply noise and identify noise sources in the power supply. These techniques work even better with specialized tools designed to measure power supply noise.

For example, the N7020A power rail probe, shown in figure 10 above (and used in some previous examples), is the first probe to measure noise on DC power supplies. This probe has a 1.1:1 attenuation ratio (Tip 3) and ± 24 V of offset (Tip 4), and it connects to the 50 Ω scope input (Tip 1). It has 2 GHz bandwidth to capture the high-frequency noise and transients that can cause clock and data jitter (Tip 7). When used with an oscilloscope like the Keysight Infiniium MXR-Series, it can be bandwidth-limited (Tip 2) to reduce noise when you do not need the full 2 GHz bandwidth.

7. Meet the Experts



Heidi Barnes is a Senior Application Engineer and Power Integrity Product Owner at Keysight, specializing in High-Speed Digital applications. With 26+ years of experience in electronic design automation, her recent activities include the application of electromagnetic, transient, and channel simulators to solve signal and power integrity challenges. She contributed to the IEEE-370 Standard on fixture removal for high-frequency interconnects and is Co-Chair for the IEEE EPS EDMS Packaging Benchmark Sub-Committee. Heidi holds five patents and was awarded the DesignCon Engineer of the Year in 2017.



Steve Sandler has been involved with power system engineering for over 40 years. He is the Founder and CEO of Picotest, a company specializing in instruments and accessories for high-performance power system and distributed system testing. He is also the Founder of AEi Systems, a company specializing in modeling, simulation, and analysis of large spacecraft. He frequently lectures at IEEE conferences and has authored numerous articles and books on power electronics and power integrity-related topics.