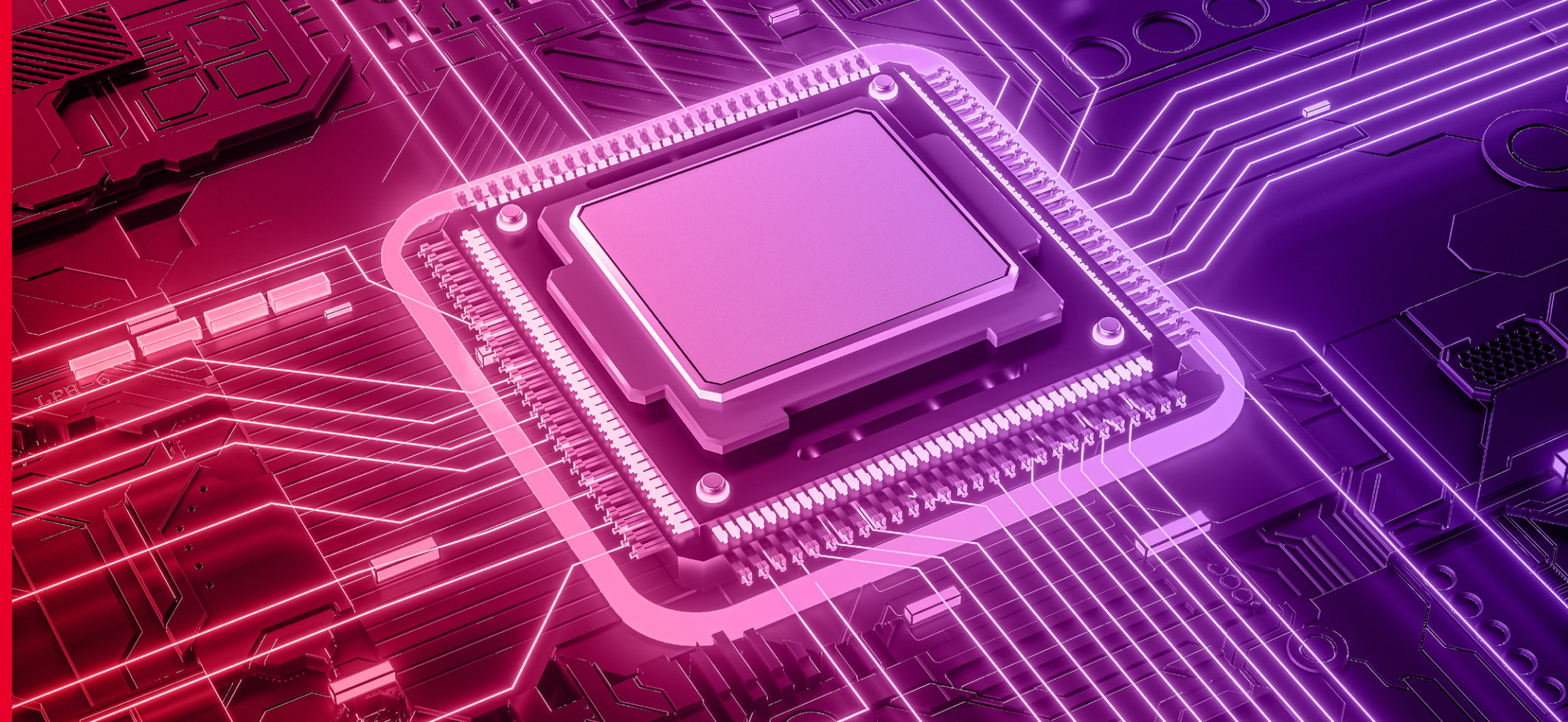




Four Real-World Applications for Electromagnetic Simulation

PATHWAVE

eBook

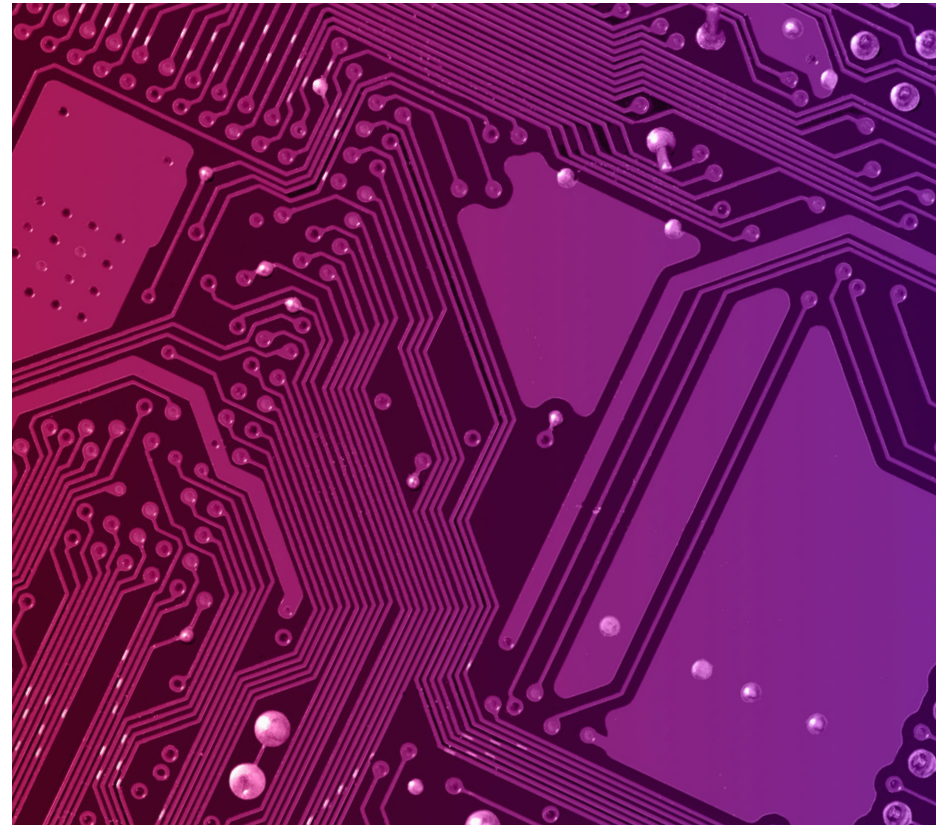
 KEYSIGHT

Expand the Possibilities for Electromagnetic Circuit Analysis

With the complexity of integrated circuit (IC) components increasing, electromagnetic (EM) circuit simulation is now critical for accurate and efficient design. The EM effects on a circuit can drastically alter voltage levels and damage semiconductor devices. With EM simulation, designers can account for EM effects on their circuit to avoid costly problems before they happen.

EM simulation enables designers to accurately model both large portions of the system or the entire system. Additionally, integrating 3D EM modeling with traditional circuit simulation is one method to simplify your design flow radically. Many designers perform circuit simulation separately from EM simulation. However, with the right tools, you can accomplish these tasks together.

EM analysis is fast becoming the component designers' tool of choice. This eBook details four applications of how you can use EM simulation to accelerate and simplify your design workflow to create better designs.



Contents



APPLICATION 1

Quad Flat No-Leads Package

[GO TO APPLICATION 1 >](#)



APPLICATION 2

Solder Bumps in Chip-Scale Packaging

[GO TO APPLICATION 2 >](#)



APPLICATION 3

Low-Temperature Co-Fired Ceramic Modules

[GO TO APPLICATION 3 >](#)



APPLICATION 4

Multi-Chip Modules

[GO TO APPLICATION 4 >](#)



SUMMARY

Summary

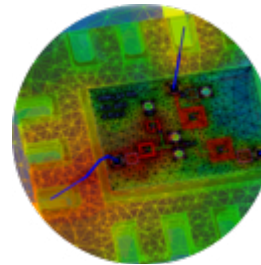
[GO TO SUMMARY >](#)

EM Simulation Basics

Electromagnetic forces exist in various frequency ranges across multiple application areas. Performing EM simulation on your circuit is beneficial, whether you are designing for wireless, digital, or power applications. Several different technical approaches to EM simulation exist, and each one aligns to one or more application areas. Knowing the technical advantages of each approach and how to apply them to various designs is critical for a successful design and simulation process. Knowing which EM simulator to use will help when you begin your next high-frequency circuit design.

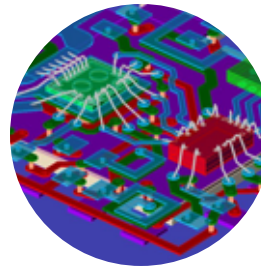
The most commonly used EM simulators are Method of Moments (MoM), Finite Element Method (FEM), and Finite Difference Time Domain (FDTD).

3 Main EM Simulation Technologies



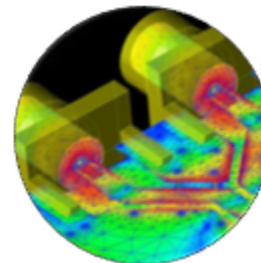
Method of Moments (MoM)

- 3D-planar EM simulator
- Use for passive circuit analysis
- Efficient for planar and multilayer applications; such as electronics and antennas



Finite Element Method (FEM)

- 3D full-wave EM simulator
- Measures frequency domain
- Use for arbitrary 3D structures such as connectors, wire-bonds, and packaging



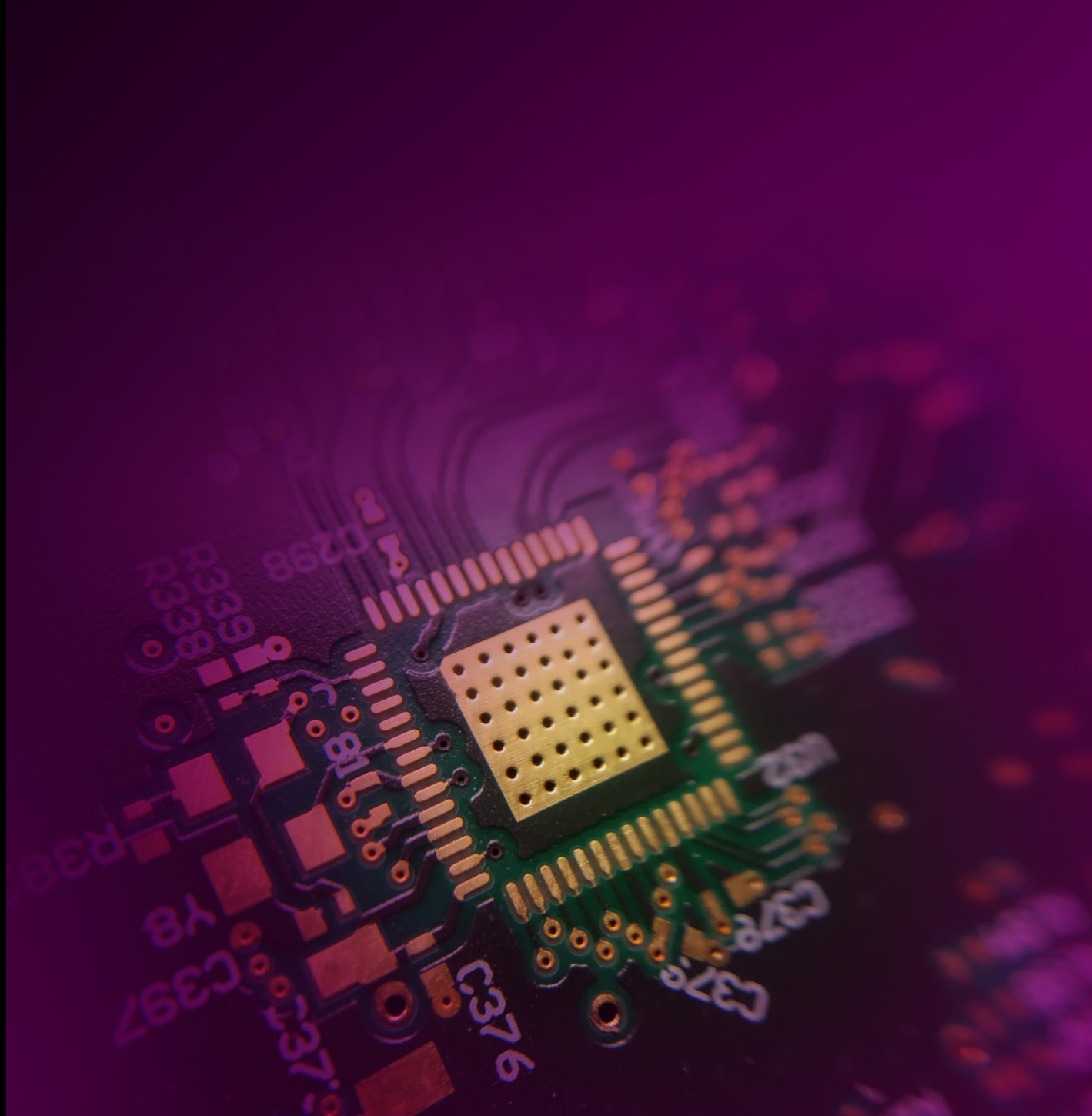
Finite Difference Time Domain (FDTD)

- 3D EM simulator
- Measures time domain
- Use for structures larger than the wavelength of interest; such as antenna systems



APPLICATION 1

Quad Flat No-Leads Package

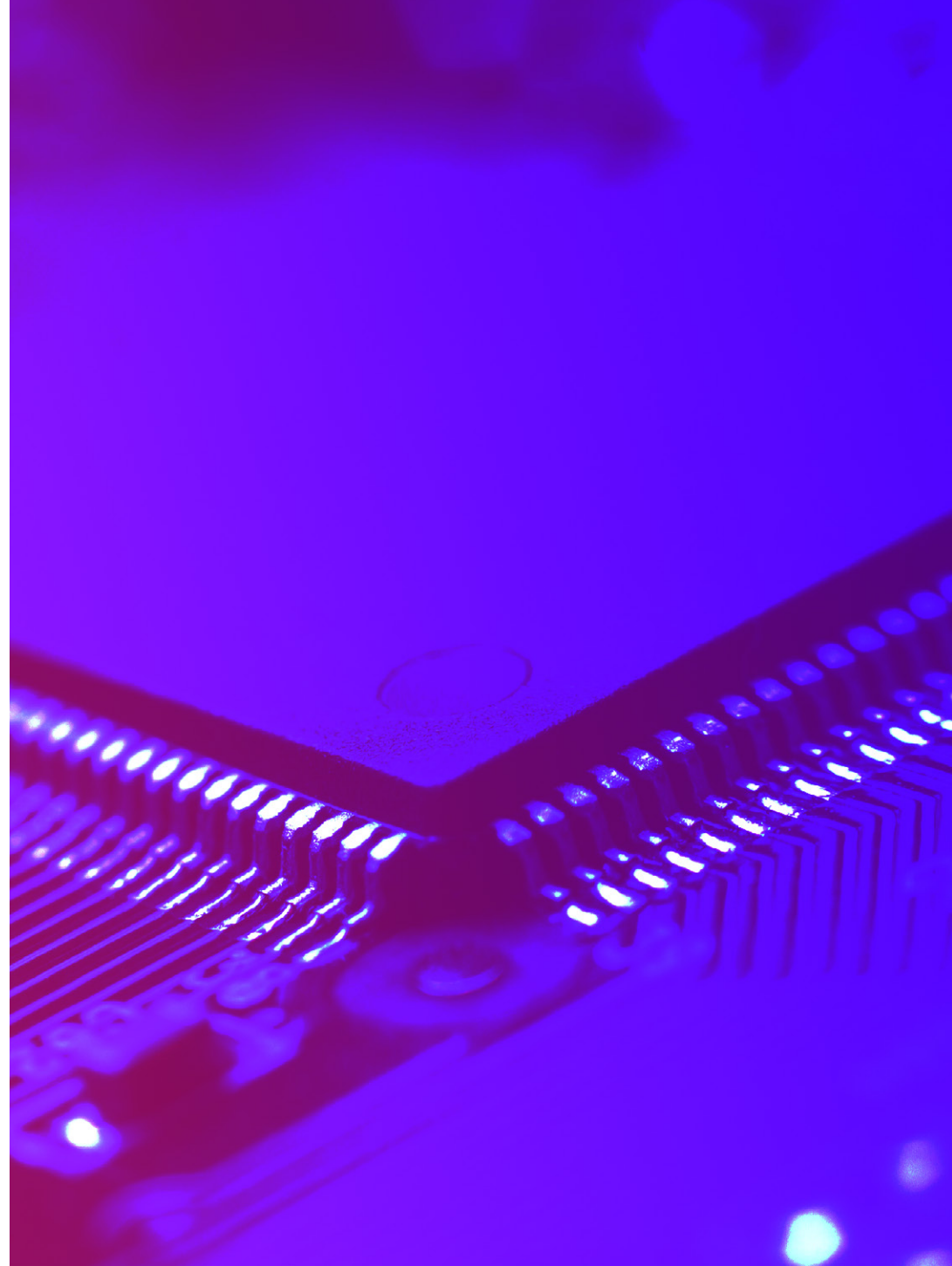


APPLICATION 1

Quad Flat No-Leads Package

Once packaged, an IC design is considered finished. The protective packaging enables easy handling and assembly of the IC. It also protects the IC from damage. While the packaging takes place as the last step in the workflow, IC designers must understand the package's electrical performance early in the design process. What is the upper frequency limit at which the package can operate? Can using a lower-cost package type decrease the final product cost? What about the performance of package isolation?

Quad flat no-leads (QFN) is one of the most advanced IC packaging technologies in electronics. As a near chip-scale package (CSP), it boasts a thin profile, moderate thermal dissipation, and excellent electrical performance. The QFN package provides good thermal and electrical performance — making it a very popular low-cost option for RFIC, MMIC, and RF SiP applications.

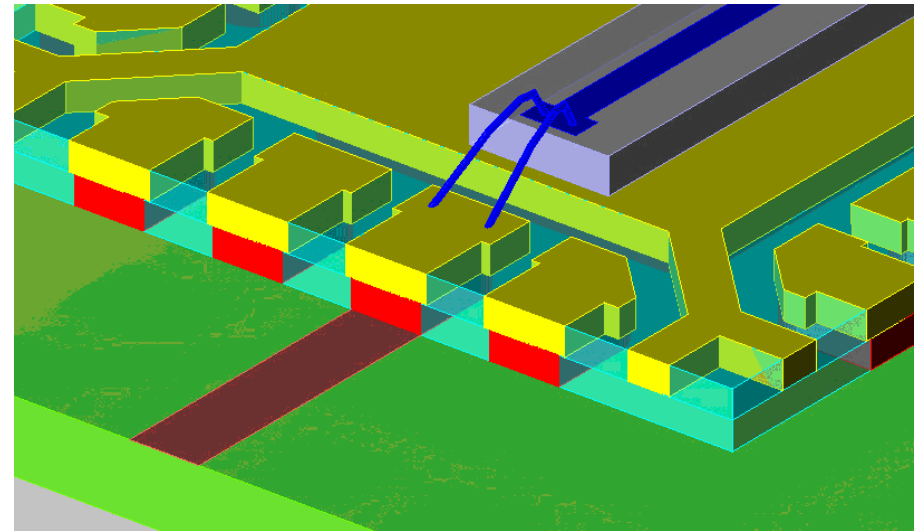


Design challenges

A 3 x 3 mm, 16-pin QFN package performs reasonably well up to 15 GHz. However, new designs require a much higher operating frequency within the same package. To enhance the transition design on the circuit board, the designer must optimize the impedance of the input-output feed line and transitional structure. Knowing the package performance limitations before final assembly is an efficient way to reduce last-minute design respins.

Solution

To improve QFN package performance, you can optimize your design to maintain a good impedance profile throughout transitions. Augmenting the transition design is possible with a 3D EM design tool integrated into your design software. By increasing the width of the input and output lines and using two lead frames, you can optimize the performance of your QFN package.

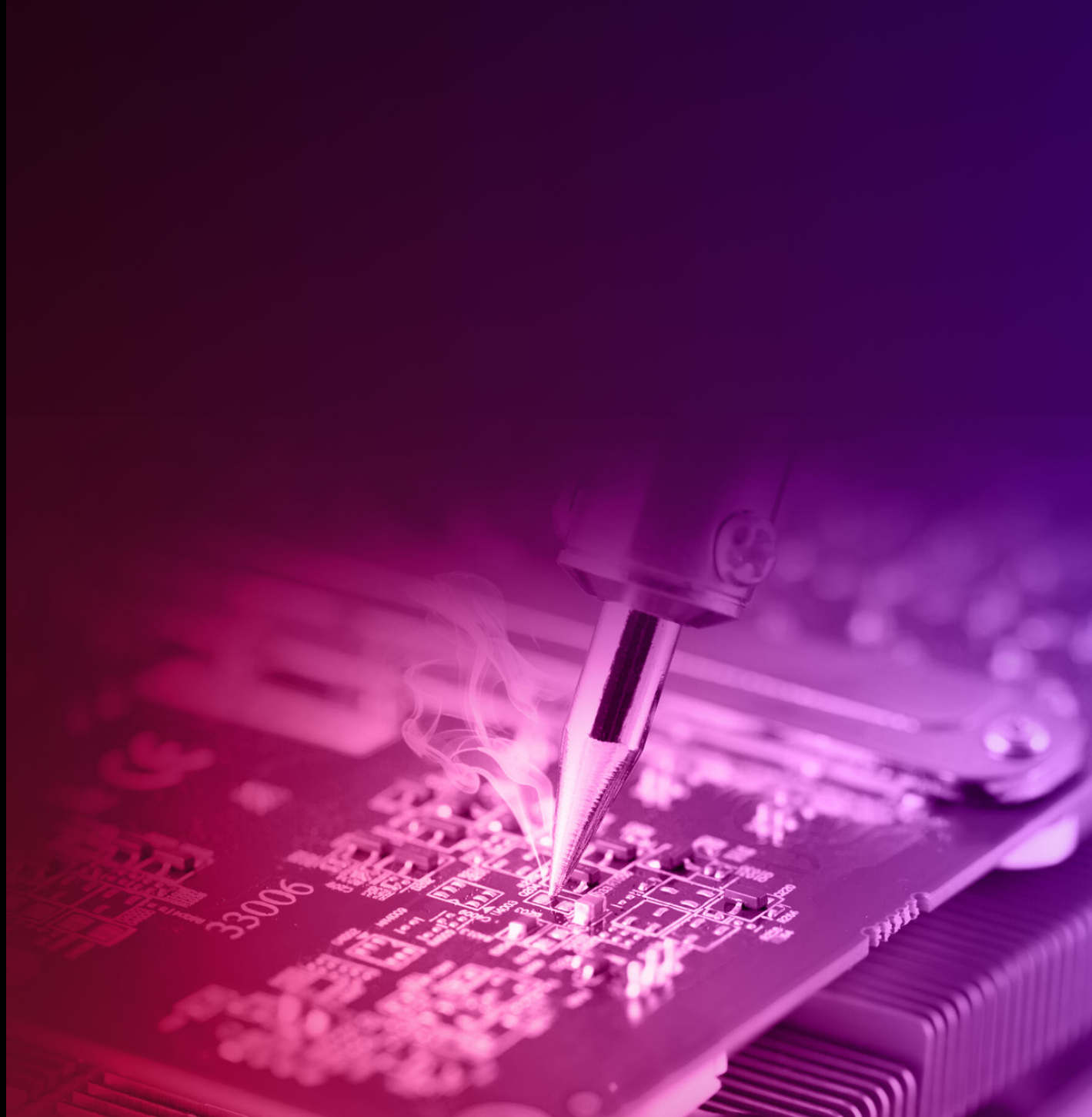


QFN package with a wider transition line and two lead frames instead of one, enabling a 50 Ω impedance



APPLICATION 2

Solder Bumps in Chip-Scale Packaging



APPLICATION 2

Solder Bumps in Chip-Scale Packaging

Multiple methods exist for packaging IC chips onto substrates and circuit boards. Chip-scale packaging (CSP), is a process that continues to gain popularity among cell phones and other small electronics manufacturers. The process occurs after dicing the IC chips from the semiconductor wafer.

CSP allows packaging small IC chips individually by interconnecting semiconductor devices to external circuitry using solder bumps. This method saves space and results in a package that is lighter weight. The package also has a thinner profile because of the elimination of wire bonds and leads.

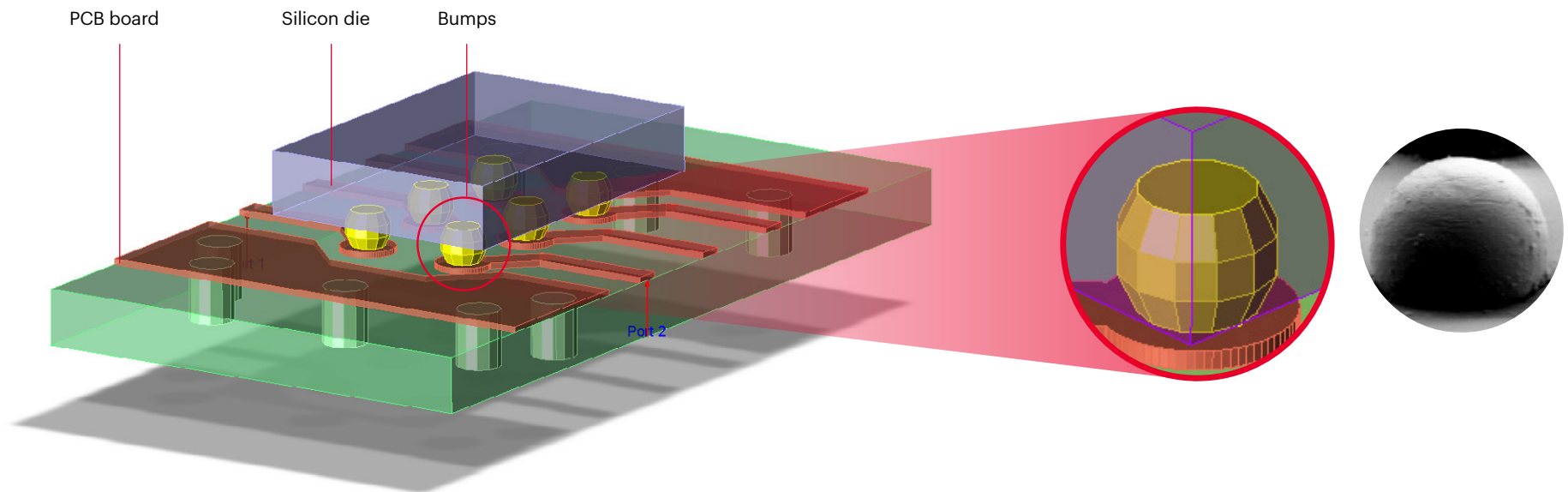
When designing and simulating an IC, engineers must take into account the EM effects of the entire package. This includes the EM effects of the solder bumps, as well as the rest of the chip.



Design challenges

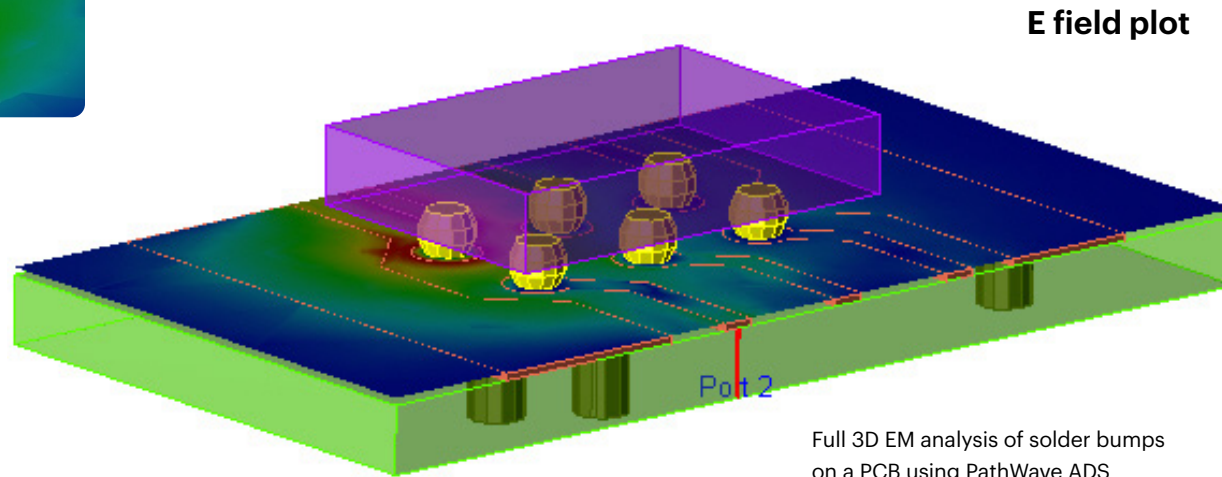
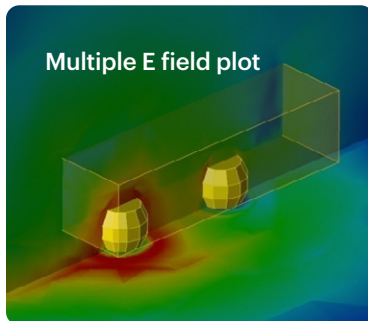
The popularity of CSP brings a new set of design challenges requiring 3D full-wave EM simulation tools. Solder bumps are large 3D objects that impact overall IC performance. With modern technological advances comes the expectation of some level of coupling or crosstalk between bumps, chips, and boards. Increasing operating frequency introduces even more complex design challenges, such as cross-coupling, which are prominent in today's wireless and high-speed digital applications. Minimizing these challenges and ensuring first-pass design success requires careful analysis from IC and package designers.

Solder bumps on a PCB board



Solution

Optimize your design fully using co-design and co-simulation. Use a parameterized 3D component design kit to quickly draw 3D components, such as solder bumps. You can co-design the 3D components with other schematic components. Rearranging and optimizing the bumps in the layout with the co-design of the schematic circuit provides a full 3D EM analysis of your entire system. Finite Element Method (FEM) solvers can handle arbitrarily shaped structures such as solder bumps, where Z-dimensional changes appear in the structure.

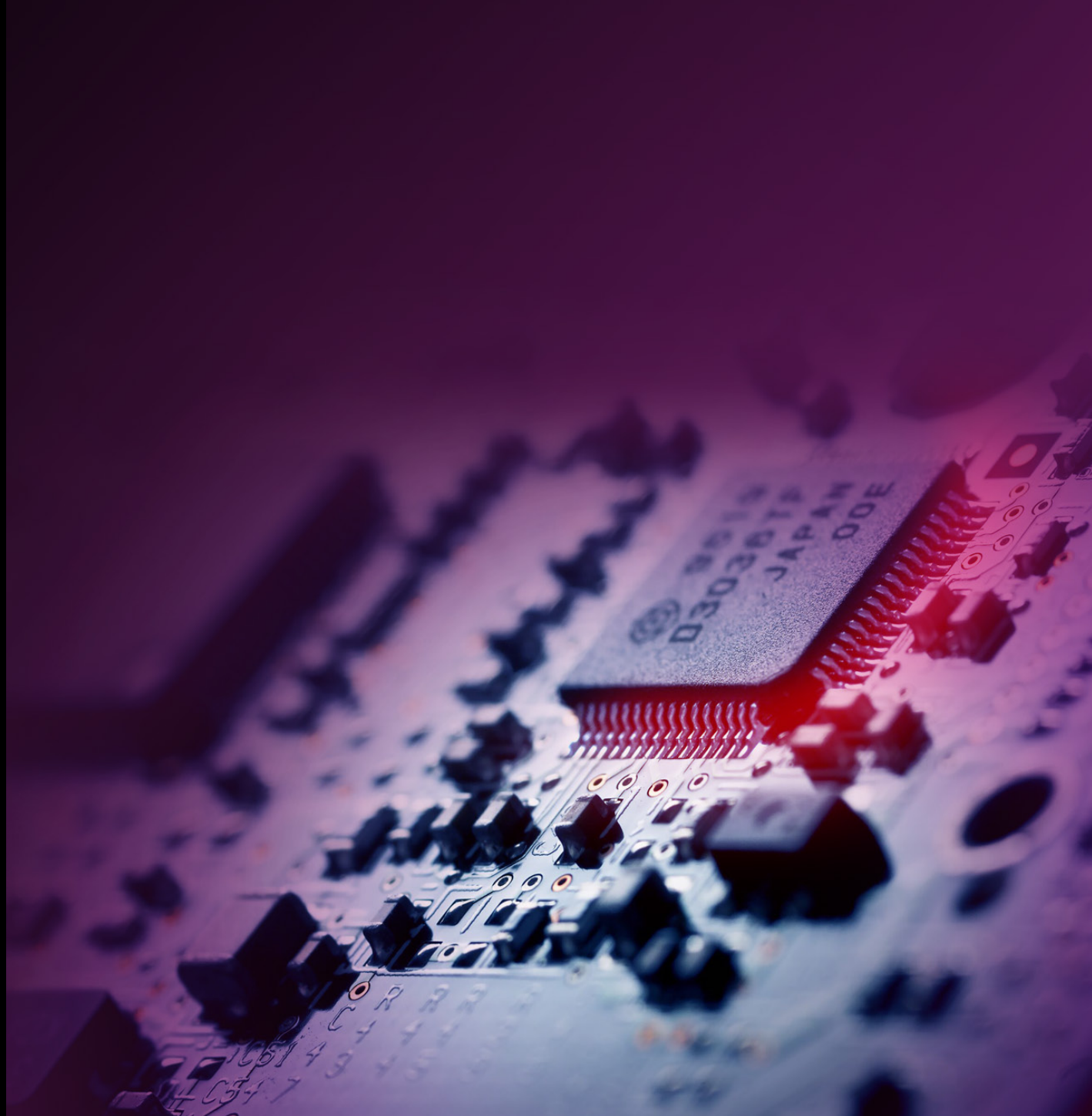


Full 3D EM analysis of solder bumps
on a PCB using PathWave ADS



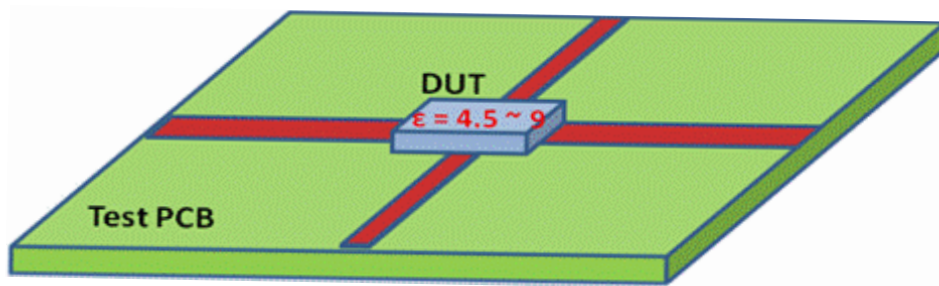
APPLICATION 3

Low-Temperature Co-Fired Ceramic Modules



Low-Temperature Co-Fired Ceramic Modules

A well-established solution for wireless and automotive applications is low-temperature co-fired ceramic (LTCC) modules. LTCC modules provide advantages in terms of size, cost, and time to market. Because they can incorporate capacitors, resistors, and inductors in a small area, RFICs easily fit on the modules. With conductor paths typically made of gold or silver, they offer excellent physical and electrical properties, as well as reduced production costs. Additionally, LTCC products are small, typically less than 5 x 5 mm in size, with a relatively high dielectric constant.

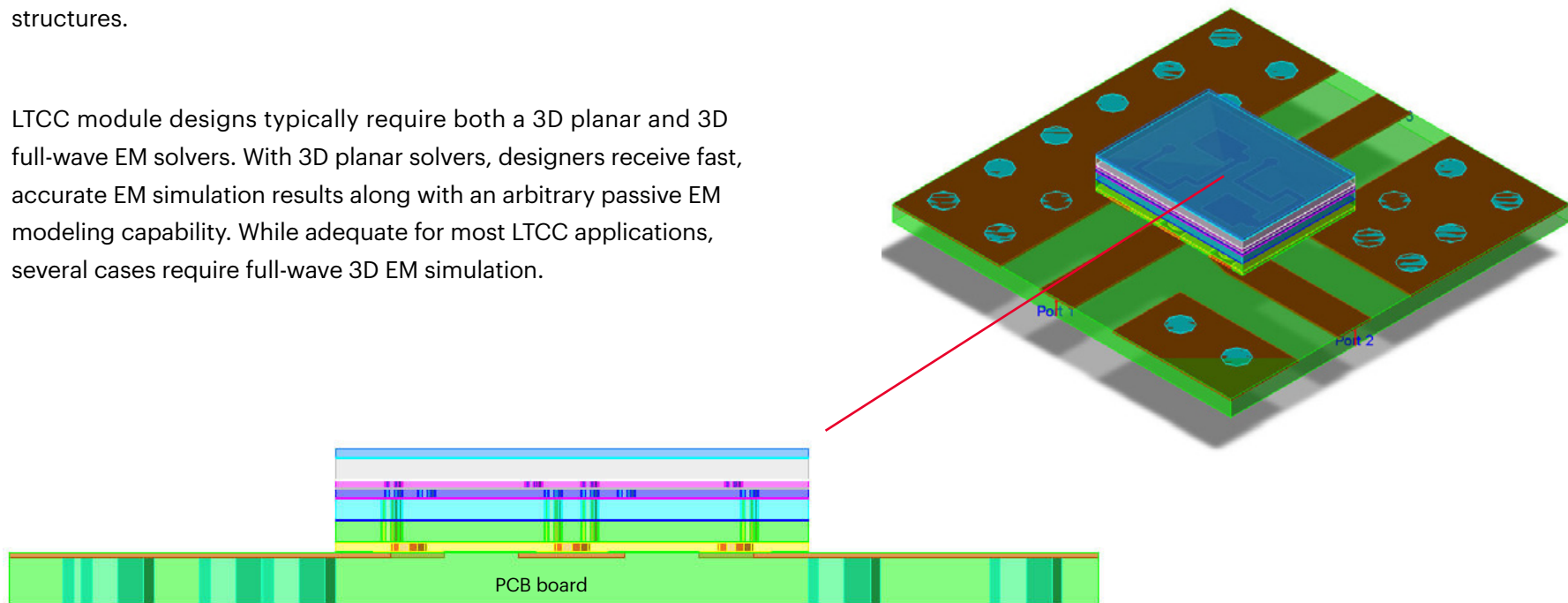


LTCC products are generally assembled and measured on PCBs

Design challenges

Despite their advantages, LTCC modules present some design challenges for wireless device designers. Parasitic coupling can result from multiple large structures. Their complex geometry and many dense layers require an advanced design solution: a flexible and customizable layout editor with a combination of simulation technologies capable of modeling geometrically complex 3D structures.

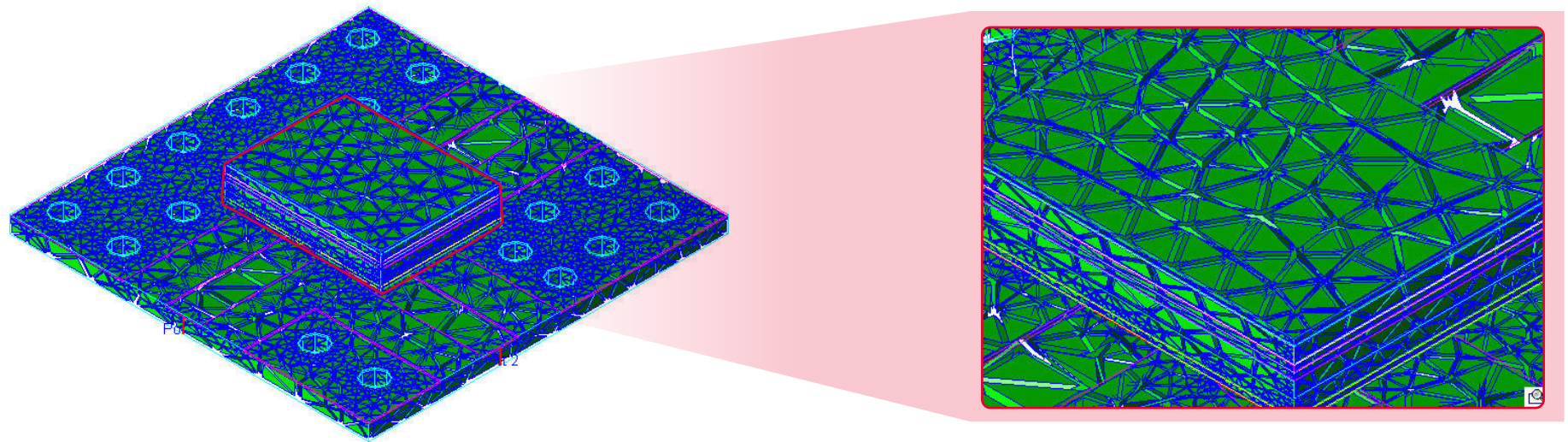
LTCC module designs typically require both a 3D planar and 3D full-wave EM solvers. With 3D planar solvers, designers receive fast, accurate EM simulation results along with an arbitrary passive EM modeling capability. While adequate for most LTCC applications, several cases require full-wave 3D EM simulation.



Substrate stack-up definition and 3D view for 3D EM simulations on PathWave ADS

Solution

Use 3D EM simulation software to simulate LTCC modules accurately. A method of moments (MoM) solver provides an ideal solution for these complex designs because only the metal surface, where currents flow, factor into the meshing. For optimal accuracy, use 3D full-wave FDTD EM simulation.

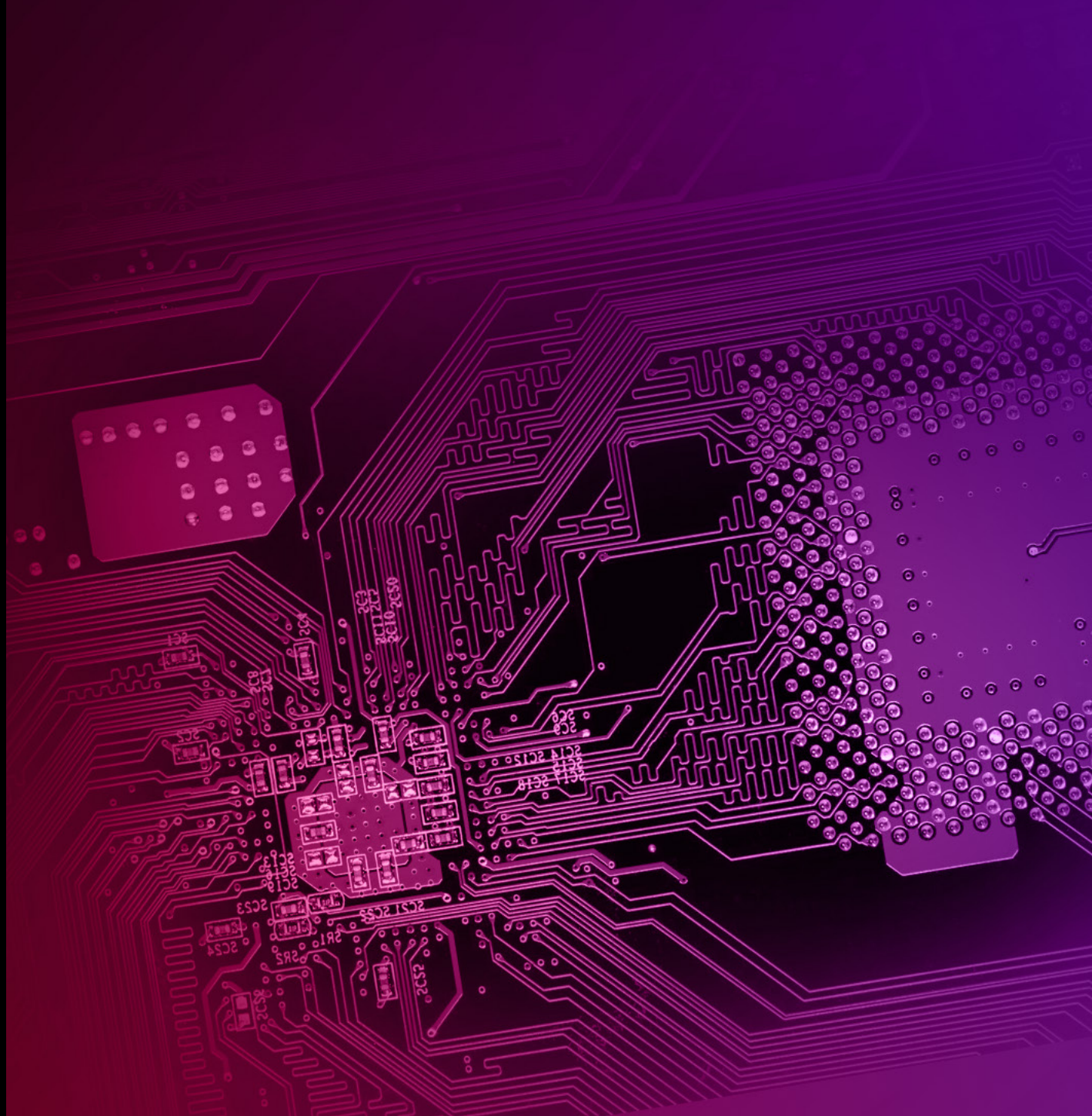


MoM discretization of a 3D planar structure



APPLICATION 4

Multi-Chip Modules

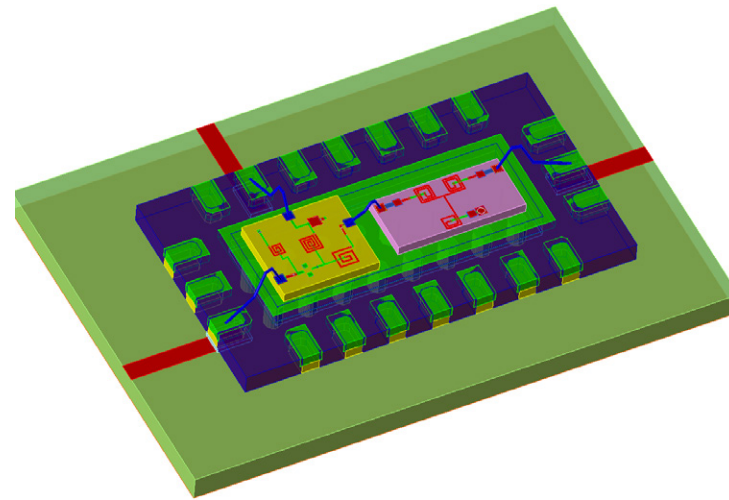


Multi-Chip Modules

Multi-chip module packaging is an essential aspect of modern electronic and microelectronic systems. Commercial wireless and aerospace and defense industries are rapidly moving from single packaged monolithic microwave integrated circuits (MMICs) to larger, more complex ICs in multi-chip modules. Demand for further size reduction of wireless devices drives the need for compact packaging without causing performance degradation. With multi-chip module design, multiple ICs can reside within a single package offering advantages in terms of device size and performance.

Design challenges

Multi-chip circuit simulation requires co-simulation across the entire package. The design for multiple die and substrates need to be performed together. Likewise, the IC, laminate, packaging, and PCB design and simulation must occur together. The EM interactions between technologies require accurate modeling. The different manufacturing technologies used makes EM analysis challenging.



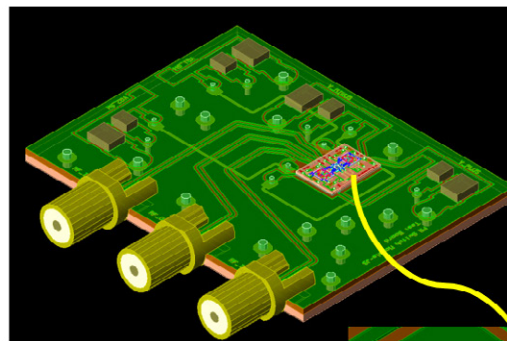
Multi-chip RF module designed using PathWave ADS

The solution

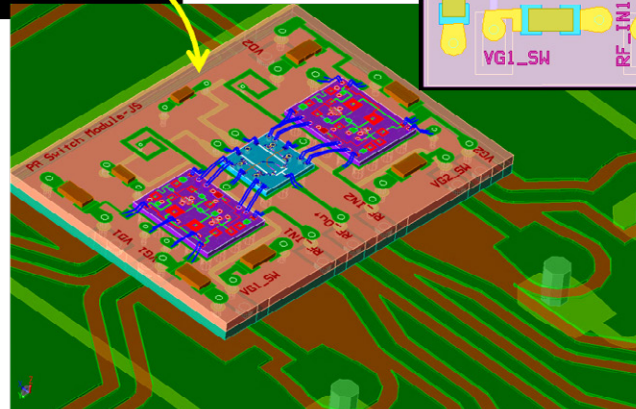
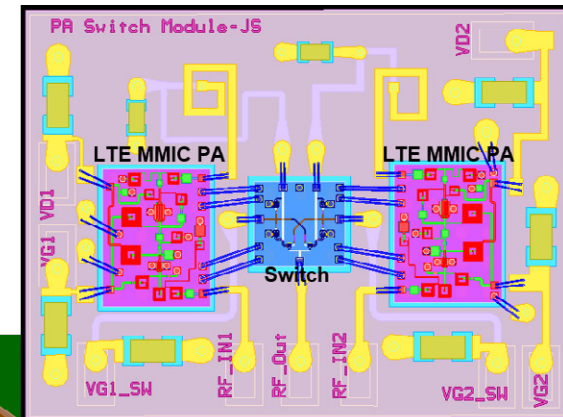
Employ integrated EDA software with multi-technology design and co-simulation capabilities. Simulate EM interactions between technologies in one integrated workflow, allowing you to optimize design elements quickly and effectively for final packaging. Use a co-simulation tool to perform both FEM and MoM analysis on a single package. Co-simulation provides for a more cohesive simulation throughout the product development lifecycle, enabling you to detect and solve issues before manufacturing. Plus, simulate any portion of your design to give you an accurate answer without having to configure your layout.

The complete PA/switch multichip module

- PA/switch ICs
- Bond wires
- Laminate board
- Solder bumps
- PCB test board
- Connectors



Multi-chip power amplifier/switch module designed in PathWave ADS



Laminate board with PA/switch ICs

SUMMARY

Traditional circuit simulation no longer provides an adequate solution to designing RF modules, RFICs, and MMICs. Today's high operating frequencies, complex waveforms, and technology integration require consideration of all EM effects throughout the design process. Modern EM analysis offers the ideal solution.

A dynamic, simple, integrated 3D EM design flow saves cycle time and increases first-pass design success. **PathWave ADS** offers a parameterized 3D component design kit that allows designers to quickly draw, co-design, and optimize 3D components with other schematic components. For today's designers, it provides a powerful method to realize an accurate and efficient design.

For more information on how Keysight solutions can help you address your EM simulation challenges, visit the following links:

PathWave ADS RFPPro, a next-generation EM simulation platform for RF/MW circuit designs

PathWave EM Design (EMPro), simulation software for analyzing the 3D EM effects of components

For a free trial of PathWave Design software, visit www.keysight.com/us/en/products/design-software.html



Keysight enables innovators to push the boundaries of engineering by quickly solving design, emulation, and test challenges to create the best product experiences. Start your innovation journey at www.keysight.com.

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