APPLICATION NOTE

In-Circuit Test (ICT) Fixture Testing

Detect wiring and probe issues before production with the i3070 ICT Fixture Verification Tool (FVT)

KEYSIGHT

What is an ICT Test Fixture?

An ICT (In-Circuit Test) fixture is a specialized mechanical interface used to connect a Printed Circuit Board Assembly (PCBA) to an in-circuit tester. It contains a bed of spring-loaded test probes (also known as pogo pins) arranged to make electrical contact with test points, component leads, or vias on the PCBA. The fixture holds the board in place and ensures consistent and reliable electrical connections during testing. It enables automated testing of individual components and circuit paths for faults such as open circuits, shorts, missing components, or incorrect values.

Challenges in Fixture Troubleshooting

A third-party fixture house fabricates these fixtures based on a set of mechanical files. However, due to the intricate arrangement of closely spaced probes and wiring, it is prone to manufacturing defects or human errors, which can lead to shorts and opens.

Fixture houses rely primarily on shorts and pin tests to detect potential errors. However, this method does not provide full coverage, as not all the wiring is used in these tests. Suppose these defects go undetected before delivery and cause testing issues. Troubleshooting test fixtures during the program debugging and production stages will become significantly more challenging. In that case, the manufacturer must call in the fixture house resources to troubleshoot and make corrections, which is costly, less productive, and may delay or disrupt the production plan.



Figure 1. i3070 Series 6 In-Circuit Tester with fixture

i3070’s Fixture Verification Tool

In order to address these challenges, Keysight has developed a Fixture Verification Tool integrated within the i3070 software revision 11.20p, which enables fixture houses to validate their fixtures prior to shipment. This tool facilitates early detection of wiring issues and mitigates the costs associated with troubleshooting during subsequent test phases.

What is the fixture verification tool?

The i3070 software revision 11.20p introduces FVT (Fixture Verification Tool), a new feature that enables independent testing of all the connections within the fixture. This can be done on an i3070 test system, either in the fixture house or the manufacturing site, with a dust cover and shorting plate, with or without the golden DUT (Device Under Test).

This tool is automatically generated when the user runs the ICT Program Generator (IPG), and no additional license is required. It leverages the existing shorts and pin test capabilities with extended coverage. It verifies that all test probes and P-pins are correctly wired and that no unintended electrical shorts exist between them.

This tool is not designed for production, so versioning is not supported, and the test coverage is also limited to testhead resources (BRCs) that can be connected to a ground bus on the pin card.

Key Features of Fixture Verification Test

Test program generation

The fixture verification test source files and test object file are automatically generated at the "Generate Test Object Files" stage while running the IPG. This process requires a “wirelist.o” file, which defines module pin assignments, and a “fixture.o” file, which contains preliminary information about the board.

The test generation assumes all wires to the ground node are shorted together due to using a grounding plate in the fixture, which interconnects all ground wires. Once the tests are generated, test resources will be updated in the “testorder” and “wirelist” files.

All the other related files are saved in a newly created subfolder called “fixture verification” under the board directory, and these files are:

Table 1. Fixture verification test files name table.

File name	Description	Plate needed	Fixture position
testplan	A program to test your fixture. The testplan is an output of the Testplan Generator.	NA	NA
brc_to_brc	Wire-to-wire connection test under each probe when all control card GP relays are opened.	Dust cover	All probe positions
gp_to_gp	Wire-to-wire connection test under each probe when all control card GP relays are closed.	Dust cover	All probe positions
indgp#	Wire-to-wire connection test under each probe when the individual control card GP relays are closed.	Dust cover	All probe positions
fix_val_pins	Wire to probe connection and probe presence test for short and long probes.	Shorting plate	All probe positions
fix_val_shorts	Probe-to-probe connection test for short and long probes.	Dust cover	All probe positions
fix_val_pins_long	Test to ensure long probes are correctly positioned in the fixture.	Shorting plate	Long probe position
fix_val_shorts_long	Test to ensure short probes are correctly positioned in the fixture.	Shorting plate	Long probe position

And after running the tool, it saves all the relevant test reports in the same subfolder:

Table 2. Fixture verification test report file table.

Report file	Description
brcreport	Failure report for brc_to_brc test
gpreport	Failure report for gp_to_gp test
indgp#report	Failure report for indgp# test
pinsreport	Failure report for fix_val_pins test
pinslongreport	Failure report for fix_val_pins_long test
shortsreport	Failure report for fix_val_shorts test
shortslongreport	Failure report for fix_val_shorts_long test

Command for fixture verification test generation

If the whole test program was generated before software revision 11.20p, the fixture verification tests can be generated manually by running a few commands on the existing test program.

The 'generate fixture verification test' command in BT-Basic software allows users to create fixture verification tests, with the option to specify which items to include.

```
generate fixture verification test

generate fixture verification test; <options list>

<options list> can be:   <item>

                         <item>,<item>

                         <item>,<item>, . . . <item>

<item> can be: testplan, brc, gp, probes
```

```
generate fixture verification test ! generate
testplan, br"c_to_brc,gp_to_gp and probe test
source files

generate fixture verification test; testplan !
generate only testplan

generate fixture verification test; brc ! generate
only brc_to_brc test source file

generate fixture verification test; gp ! generate
gp_to_gp and indgp# test source file

generate fixture verification test; probes ! generate
only probe tests source files

generate fixture verification test; testplan, brc !
generate testplan and brc_to_brc test source file
```

Figure 2. Syntax to generate fixture verification test.

Table 3. Generate fixture verification test option list.

Syntax	Description
<option list>	A list of optional parameters that determine how the function works. The options are: ***testplan*** - Generate only fixture verification testplan. ***brc*** – Generate only brc_to_brc test source file **gp** - Generate gp_to_gp and indgp# test source file ***probes*** – Generate only probe tests source files

What are the Tests Performed by This Tool?

BRC_to_BRC test

The BRC_to_BRC test verifies wire-to-wire connections under each probe when the General Purpose (GP) relays are open. The assigned nodes are not connected, allowing for independent testing of the wiring between probes and P-pins (BRCs) for the same node.

To ensure accuracy, the test engineer must place a dust cover over all probe positions and apply a vacuum for offline testers or pressure for inline testers during the test. This simulates the actual test conditions in production.

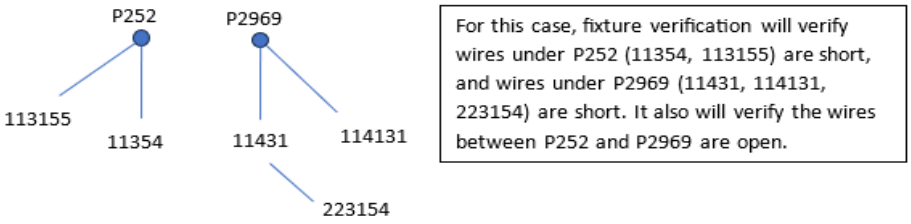


Figure 3. Brc_to_Brc test overview.

```
Threshold 5
Settling delay 1m
Short 113155 to 11354
Short 11431 to 114131
Short 11431 to 223154
Threshold 1000
Nodes 113155
Nodes 11355
Nodes 11431
Nodes 114131
Nodes 223154
```

Figure 4. Examples of BRC_to_BRC test.

GP_to_GP test

The GP-to-GP test is similar to the BRC-to-BRC test, except that all the GP relays are closed. This test provides an additional wiring test for the GP relays BRCs.

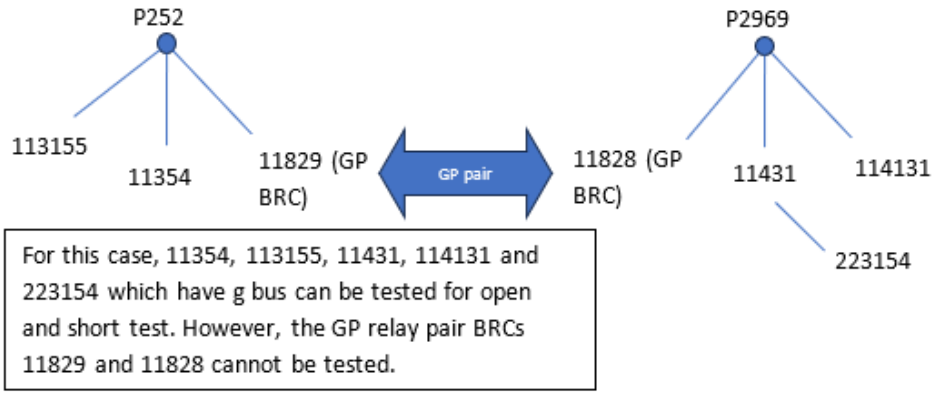


Figure 5. GP_to_GP test overview.

```
relay
   wire "A2B-BUS-PWR-EN" to  11829 general
   wire "P3V3-BKUP" to  11828 general
end relay
```

```
NODE "P3V3-BKUP"
  PINS
    223154;
    11828;
    11431;
    114131;
  PROBES
    P2969    102984,    47671 tp17005.1 LWT;
  ALTERNATES
      81754,    33085 TOP;
      80090,    34955;
  WIRES
    223154 TO 11431 Blue     28    20.00;
    11828 TO P2969 Blue      28     7.00;
    11431 TO P2969 Blue      28     5.00;
    114131 TO P2969 Blue     28     5.00;
```

```
NODE "A2B-BUS-PWR-EN"
  PINS
    11829;
    11354;
    113155;
  PROBES
    P252      108929,    48222 LWT 75MIL;
  WIRES
    11829 TO P252 Blue     28     6.50;
    11354 TO P252 Blue     28     1.00;
    113155 TO P252 Blue     28     1.00;
```

Figure 6. Example of a wire related to the GP replay pair in “wirelist” and “fixture” files.

```
Threshold 5
Settling delay 1m
Short 11354 to 11431
Short 11354 to 113155
Short 11354 to 114131
Short 11354 to 223154
Threshold 1000
Nodes 113155
Nodes 11355
Nodes 11431
Nodes 114131
Nodes 223154
```

Figure 7. Examples of Short Statement in GP_to_GP, which links GP relay when they are closed.

Indgp# test

The indgp# test is a more detailed variation of the GP_to_GP test. During this test, only one pair of the GP relays is closed at a time, and the connection of each GP relay is verified individually.

Fix_val_pins test

The Fix_val_pins test is a probe validation test that examines wire-to-probe connections and verifies the presence of short/long probes in a test fixture.

The test engineer must place a shorting plate on top to create a common electronic connection for all the probes. The test ensures that probes are properly positioned and make contact with the plate. If a probe is missing or broken, an open circuit will be detected at that position.

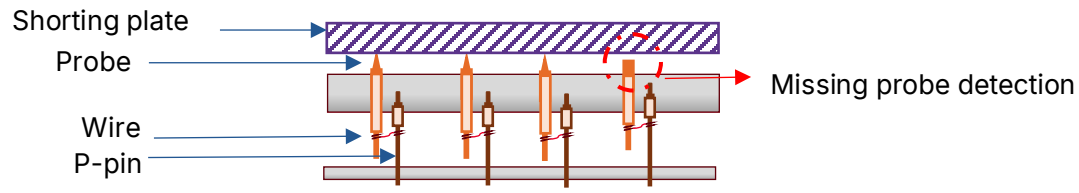


Figure 8. Fix_val_pins test checking for missing probes.

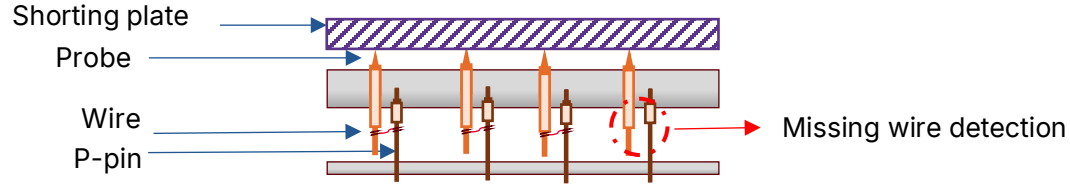


Figure 9. Fix_val_pins test checking for missing wires.

Fix_val_shorts test

The fix_val_shorts test checks for probe-to-probe connections for short/long probes, ensuring no unintended electrical shorts exist between groups of probes. This test ensures that probes are correctly positioned and electrically separated. This test requires a dust cover.

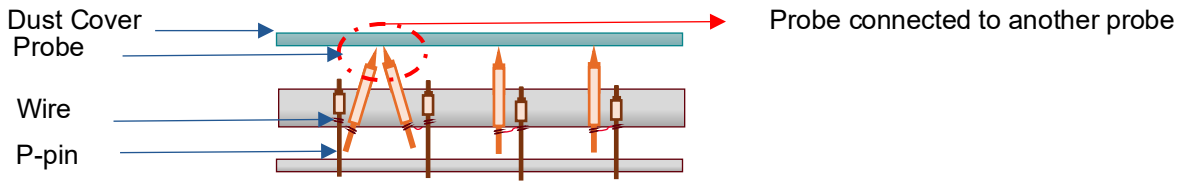


Figure 10. Fix_val_shorts test diagram.

Fix_val_pins_long test

The fix_val_pins_long test is generated only when long probes are present in the “fixture.o” file. Its purpose is to ensure that long probes are correctly placed within the fixture. This is achieved using a shorting plate at the designated long probe positions. If a long probe is correctly positioned, it will make physical contact with the shorting plate, confirming its placement. This test prevents misalignment and ensures that long probes function as intended during subsequent measurements.

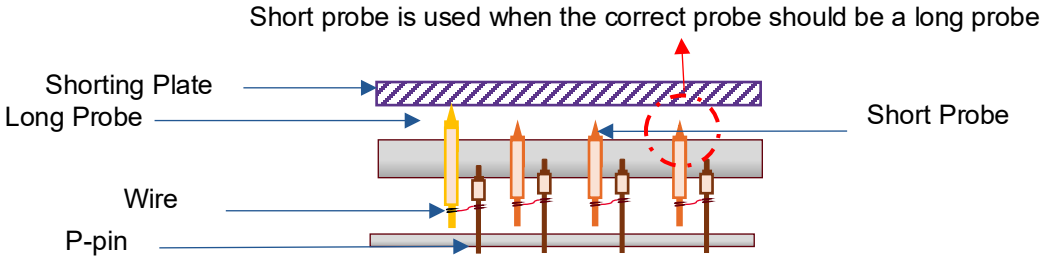


Figure 11. Fix_val_pins_long test diagram.

Run Fixture Verification Tool via “Fixture Macros”

With ease of use in mind, all the functionality has been grouped into “Fixture Macros” under Push Button Debug, as shown below. These macros help ensure consistency and reduce manual intervention. There are 3 Macros available for fixture verification.

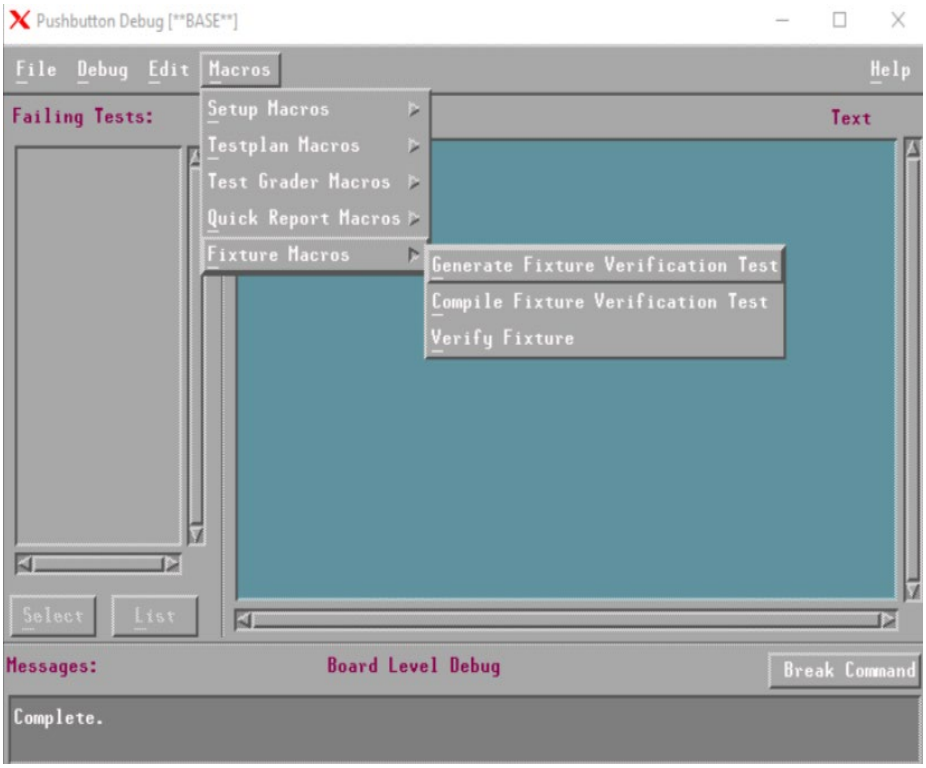


Figure 13. Fixture Macros in Push Button Debug Graphic User Interface (GUI).

Generate fixture verification test

It creates a fixture verification test source file and testplan. It automatically compiles all fixture verification test source files into test object files, ensuring that all necessary test configurations, sequences, and macros are appropriately integrated and formatted for execution.

Compile fixture verification test

Compile Fixture Verification Test compiles all fixture verification test source files, ensuring no errors or misconfigurations before execution.

Verify fixture

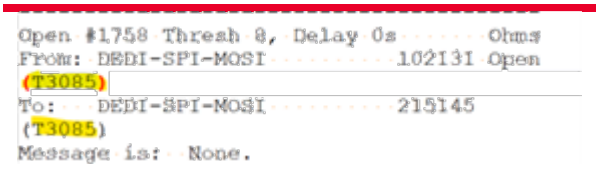
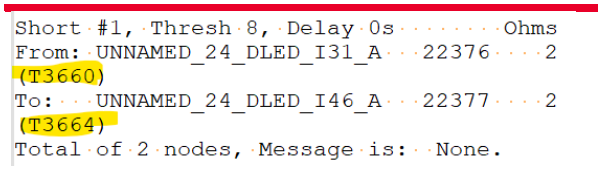
All the tests listed in Table x will be executed automatically, with occasional prompts for the user to place a dust cover or shorting plate. This ensures all components are in place before the test, preventing errors caused by incorrect setup.

Table 4. Fixture verification test success or failure.

Successful test: Inline system	Failed test: Offline system
	

When the tests are complete, it generates relevant reports and saves them to the same folder. When open or short test failures are detected, the report will provide detailed probe information to assist in troubleshooting and making corrections. Example as shown below:

Table 5. Fixture verification test open and short failure.

Open failure	Short failure
	

Conclusion

The i3070's fixture verification tool in the i3070 software revision 11.20p is a very powerful quality control tool that ensures fixtures meet the design specifications using the i3070 ICT system. This test leverages the system's built-in shorts and pins test capabilities to identify potential connectivity issues. Incorporating the wire and probe tests, it can detect wiring or probe faults, such as missing, broken, open, or shorted wires or probes.

By utilizing the test resources and macros within the i3070 ICT system, users can independently verify and troubleshoot their fixtures in the early stage of product development, significantly improving productivity and reducing the time to market.

Keysight enables innovators to push the boundaries of engineering by quickly solving design, emulation, and test challenges to create the best product experiences. Start your innovation journey at www.keysight.com.

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