Keysight Technologies

Serial ATA Design and Test – A Better Way

Thorough characterization and validation of Serial ATA designs

Application Note

KEYSIGHT TECHNOLOGIES

New Challenges

The Serial ATA International Organizations (SATA-IO) has released the SATA Revision 3.0 specification, providing support for 6 Gb/s data transfer between hosts, devices and port multipliers. At higher data rates, power consumption and emissions become more of a concern on system budgets. Link designers seek to find optimum voltages, emphasis levels and edge rates to manage these challenging design limits while ensuring functional protocol operation at the receiver. The SATA-IO has designed a comprehensive interoperability test program to assess the electromechanical physical layer design limits, protocol state machine branching and command execution as well as system-level functional operation. The goal of the program is to improve interoperability between SATA products in the market, and to provide an equitable test vehicle through which all vendors' products can be fairly compared to the provisions of the specification. Several new features and test requirements exist within the SATA Revision 3.0 specification, which require new tools and new validation methods to assess accurately.

Key tasks

SATA physical layer validation and compliance can be segmented into three areas: transmitter (PHY/TSG/OOB), receiver (RSG), and impedance/return loss (RX/TX). The specification aims to balance the design budgets among the transmitter, receiver, and interconnect channel to ensure zero-sum accounting for key attributes such as jitter and minimum differential amplitude, which directly influence interoperability between products. If all products adhere to the SATA specifications, then by definition, all SATA products should work together in any system configuration. Keysight Technologies,Inc. offers complete and certified physical layer to protocol layer test solutions for 1.5 Gb/s, 3 Gb/s, and 6 Gb/s data rates and provides official SATA-IO GOLD suite testing for all three physical layer areas at the biannual SATA-IO Interoperability Workshops. Several key certified test labs also utilize Keysight equipment to provide Interoperability test support for SATA-IO throughout the year. Utilizing the same equipment configurations and test suites in your lab allows you to have greater confidence in your design margins relative to the specification requirements well ahead of official certification, helping speed your time-to-market and time-to-profit.

Table 1. SATA design and test solutions.

Transmitter characterization (PHY/TSG/OOB)	**Receiver characterization (RSG)**	**Impedance/return loss (RX/TX)**
DSA91204A oscilloscope	J-BERT N4903B high-performance serial BERT	DCA 86100C wideband sampling oscilloscope
with	with	with
N5411B SATA compliance software	N5990A automated compliance and device characterization test	54754A TDR/TDT module
and	and	
N5436A-002 protocol viewer software*	N4915A-005 6.5 GBit/s serial bus switch	86108A precision waveform analyzer* (for active waveform characterization)
	and	
N5465A InfiniiSim waveform transformation toolset for de-embedding*	N4915-60001 SATA ISI channel	W2212 Advanced Design System (ADS) core, transient, convolution, layout, momentum G2, FEM, ptolemy bundled* (for signal integrity analysis)
		N5230C 4-port 26.5 GHz vector network analyzer with N1930B PLTS software

These test solutions are optional for characterization – all others are required for compliance testing.

SATA – Keysight Total Solution

Transmitter characterization (PHY/TSG/OOB)

DSA91204A oscilloscope

N5411B SATA compliance N5436A-002 protocol

viewer software*

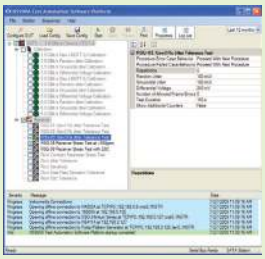
N5465A InfiniiSim waveform transformation toolset for de-embedding*

Industry's lowest scope noise floor/sensitivity and trigger jitter

Receiver characterization (RSG)

J-BERT N4903B high-performance serial BERT

N5990A automated compliance and device characterization test



BusXpert SAS/SATA test solution

Automated compliance software accurate, efficient, and consistent

Impedance/ return loss (RX/TX)

DCA 86100C wideband sampling oscilloscope

54754A TDR/TDT module

86108A precision waveform analyzer*

N5230C 4-port 26.5 GHz vector network analyzer with N1930B

DCA ultra low jitter

SATA fixture De-embed

Protocol testing and validation

BusXpert SAS/SATA test solution

U3051A micro analyzer

U3052A pro analyzer

Hardware with native PHY and fast data re-lock

Software with pre-indexing, view any size trace in under 5 seconds

Keysight solutions for digital applications are driven and supported by Keysight experts that are involved in the various international standard committees. We call it the Keysight Digital Test Standards Program. Our experts are active in the Joint Electronic Device Engineering Council (JEDEC), PCI Special Interest Group (PCI-SIG®), Video Electronics Standards Association (VESA), Serial ATA International Organization (SATA-IO), Serial Attached SCSI (T10), USB-Implementers Forum (USB-IF), Mobile Industry Processor Interface (MIPI) Alliance, Ethernet standards (IEEE 802.3), Optical Internetworking Forum (OIF), and many others. Our involvement in these standards groups and their related workshops, plugfests, and seminars enables Keysight to bring the right solutions to the market when you need them.

Applying expertise

When it comes to quality digital measurements and signal integrity, Keysight has decades of experience in RF, microwave and protocol engineering. We understand the reflections, skin effect, insertion and return loss, impedance profiles as well as jitter budget and tolerance, timing margins, compliance and other issues that digital designers and developers have to face in high data rate standards. As an active member of SATA-IO, with consistent participation in workshops and specification issues and definition, Keysight has a solid background in the physical layer, protocol layer and functional test of Serial ATA devices.

Thanks to its premier position as a test company, Keysight also has a long history of collaborative innovation with industry leaders. The expertise of Keysight's Application Engineering team reflects these important experiences. They also put Keysight in a position to develop tools that meet the physical challenges, are customized to the needs of the standard, and are relevant to the way designers and developers need to use them.

Complete, reliable test coverage

What makes Keysight's design and test solutions so compelling is that they are the best tools, in every category, to meet the challenges presented by Serial ATA. Keysight's participation in SATA-IO, developing thorough SATA-IO approved Method of Implementations (MOIs), and keeping Keysight solutions SATA-IO verified, gives you the solution that you need to guarantee your design for interoperability and system quality. Go to a workshop knowing that your device will pass and know that quality and margin is designed into your device.

The quality of Keysight solutions is the key to easier, faster and more confident testing of your Serial ATA designs. That takes strain out of engineering and lowers development costs. Accurate results reduce the number of design cycles to help you get to market faster, and they ensure robust products that uphold your hard-won lead in the market.

Transmitter Compliance Testing (PHY/TSG/OOB)

Validating Serial ATA performance involves characterizing transmitter signal speed, stability, output levels and amplitude imbalance, rise/fall times and imbalance, common mode voltages, and jitter. Manually making these measurements is time consuming and prone to error. An automated method to trigger properly and measure as defined by SATA-IO will allow you to analyze the complex traffic on the Serial ATA bus efficiently and accurately.

Measure with confidence

Whether you are troubleshooting, assessing design margin, or validating compliance, an oscilloscope with the lowest vertical noise will provide the best measurement quality with the least measurement error. This is crucial to maximizing the accuracy of critical interoperability measurements such as transmitter jitter and minimum eye amplitude. Keysight's Infiniium 90000 Series oscilloscopes provide the lowest noise floor in the industry, enabling more accurate characterization of your design.

Automate complex tasks

The SATA Compliance Test software complements the accuracy of the 90000 Series oscilloscopes by simplifying set up and performing compliance tests (see Figure 1). The software comes with 1.5 Gb/s (Gen1) and 3 Gb/s (Gen2) with an upgrade option to add 6 Gb/s (Gen3) and runs on the oscilloscope itself, using a test framework that is fully automated and has proven value to busy engineers who want quick, accurate answers. This solution's Method of Implementation (MOI) is approved by SATA-IO to certify Serial ATA devices and is used in SATA-IO approved test houses.

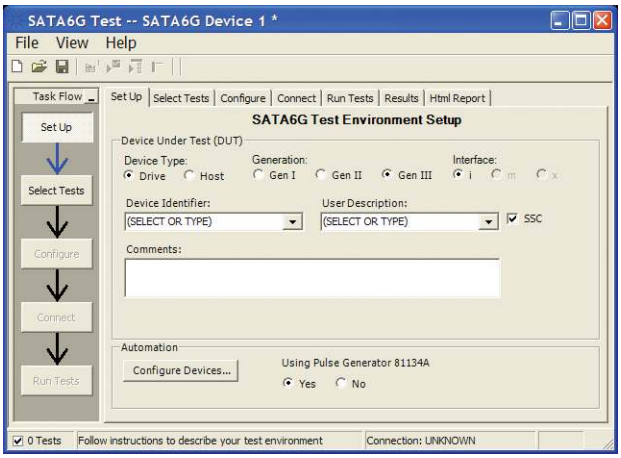


Figure 1. N5411B SATA electrical test software saves you time by selecting tests, configuring tests, setting up the connection, running the tests, and viewing the results

Key feature:

Keysight's Infiniium 90000 Series oscilloscopes provide the lowest noise floor, jitter noise floor, and trigger jitter in the industry

The software brings together Keysight's intimate knowledge of the oscilloscope and knowledgeable understanding of the specifications to ensure the best results, high repeatability with minimal effort. The software produces an HTML report, complete with screenshots, which makes it easy to share your results, and margin analysis to determine how close you are to the specification (see Figure 2).

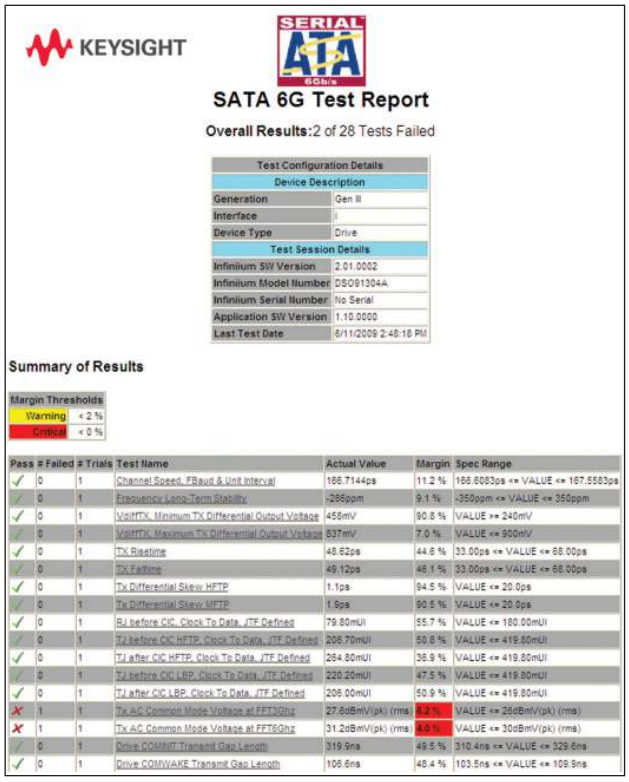
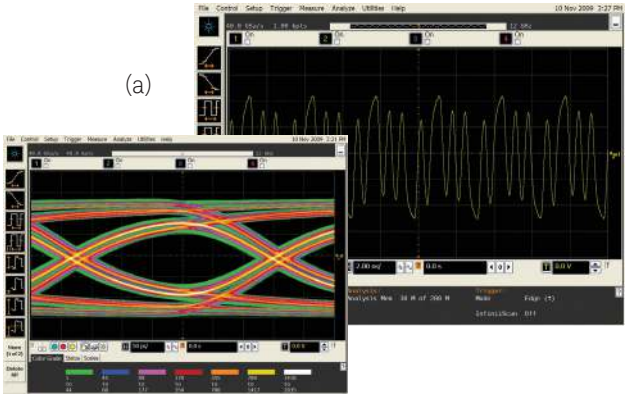


Figure 2. N5411B SATA electrical test software generates a summary report for your device quickly, including waveforms and the margin of the result to provide further insight

Receiver Compliance Testing (RSG)

The receiver test is a bit more complicated than the transmitter test, due to the DUT's task within a digital transmission system: the extraction of the digital content from its input signal with a specified, very low bit error rate (BER); the difficulty of this task is, that the signal is heavily deteriorated after it left the (non-ideal) transmitter and propagated through a lossy channel (see Figure 3); the difficulty of the test is, that it is necessary to stimulate the receiver under test with a deliberately deteriorated signal and check the quality of the conversion, utilizing the implemented loop back, which in the case of SATA only allows to use frame error rate (FER) instead of BER as a figure of merit.

(a)



(b)

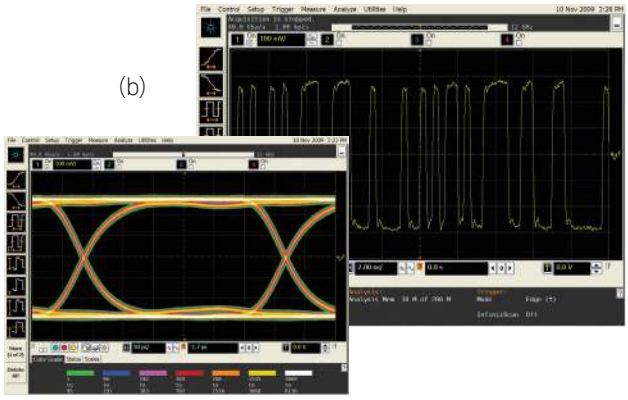


Figure 3. (a) receiver input with degraded performance due to lossy cables or test fixtures and (b) receiver input with improved signal performance through de-embedding capability to remove effect of lossy cables or test fixtures

Automated real jitter performance

To characterize jitter tolerance, you need a source that provides calibrated jitter injection. The Keysight J-BERT N4903B offers complete jitter tolerance testing with integrated injection of SJ and RJ built-in clock data recovery (CDR) with tunable loop bandwidth, and spread spectrum clocking (SSC). The built-in and calibrated jitter source allows accurate jitter tolerance testing of receivers.

Jitter tolerance curves are key to understanding the real jitter performance of a receiver. The N5990A test automation platform offers not only automated RSG compliance testing, but also automated receiver characterization including jitter tolerance (see Figure 4). Realistic conditions are emulated and certain properties of the signal deliberately stress specific building blocks of the DUT. Unlike other time consuming stimulus solutions that create the files in software to load waveforms for each individual jitter test point, the J-BERT N4903B allows real-time sweeping of signal parameters using its built in HW resources for the generation of calibrated jitter; thus, reducing measurement time to a minimum.

Key feature:

The J-BERT N4903A greatly reduces measurement time by using its built-in hardware resources for real-time sweeping of signal parameters

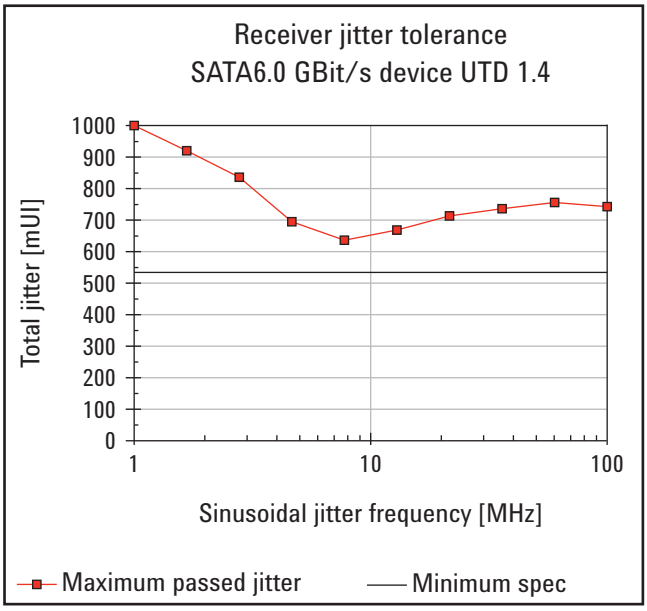


Figure 4. Receiver jitter tolerance test

Receiver Compliance Testing (RSG)

Improved operation with N4915A-005 high-speed serial data switches

In SATA receiver compliance testing, different tools are needed for turning on the test mode and for performing the actual test. Without a serial bus switch this requires a change of cables as part of the test procedure. Changing cables is certainly undesired. Especially in automated test setups. It consumes additional time and labor. Also in order to avoid connectivity errors and preserving mechanically sensitive test fixtures, changing cable should be avoided. Besides that, the SATA setup also benefits from the fast switching time. Products under test that do not support disconnect during the test mode won't detect a signal loss while being switched between test tools.

Calibrated channels

The N4915-60001 is a precision ISI channel that follows the definitions of the standard for the 6 Gb/s Compliance Interconnect Channel (CIC) and the requirements for compliance testing specified in the Unified Test Document (UTD). It allows for an accurately calibrated setup. It leaves no doubt in the compliance of the stress signal and gives the maximum margin to the device under test. The N4915-60001 integrates perfectly into the Keysight sink test setups as described in detail in the method of implementation (MOI) documents for the Keysight J-BERT.

Frame error rate counting with U3051A or U3052A BusXpert SAS/SATA analyzer

To verify proper RSG compliance, as approved by SATA-IO in Keysight's RSG MOI, a frame error rate counter is needed to verify the correct data frames are looped back during BIST Far-end Retimed Loopback mode. Automated to work with the N4309B and N5990A, the U3051A and U3052A can not only display a live counter but simultaneously capture the bus data for in-depth protocol analysis at 1.5/3.0/6.0 speeds.

Impedance/Return Loss (RX/TX)

As data rates increase, designers need to pay special attention to their board design to minimize signal integrity problems. Long trace lengths cause signal attenuation, rise-time degradation, and jitter. Impedance transitions between a trace and via can cause reflections and crosstalk. Designers need to utilize tools that are more commonly used by high-frequency engineers – a time-domain reflectometer (TDR), a vector network analyzer (VNA), and high-frequency simulation software.

Accurate impedance measurements

For quick impedance measurements, a TDR is commonly used. By injecting a fast pulse into your design, the TDR measures the reflected signal to determine impedance versus time, which is easily converted to the distance domain. Likewise, measuring the signal at the far end of the circuit defines the insertion loss profile. TDR displays are intuitive, the measurement setup is easy, and the calibration approach is simple.

The Keysight 86100C Infiniium DCA-J with the 54754A differential TDR/TDT module makes quick work of interconnect analysis. To improve accuracy, it utilizes a unique calibration process that removes the effects of cabling, allowing you to isolate your device from the test system. By switching to frequency mode, you can also examine the S-parameters for transmission and impedance performance of channels, cables, and connectors (see Figure 5). Digital engineers, already familiar with oscilloscopes, can quickly see the relationships between frequency and time effects without having to purchase and learn new equipment.

Key feature:

To improve accuracy, the 86100C TDR utilizes a unique calibration process that removes the effects of cabling, allowing you to isolate your device from the test system

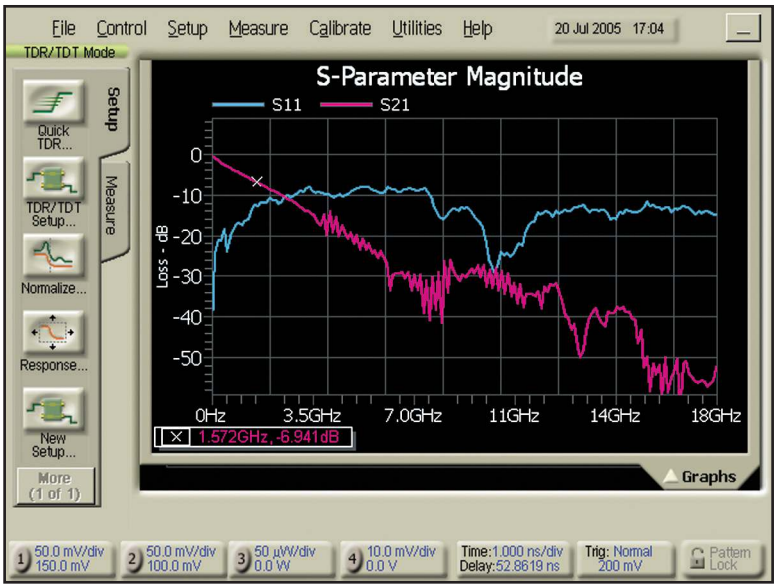


Figure 5. S-parameters can be automatically generated from the 86100C Infiniium DCA-J TDR measurement

Impedance/Return Loss (RX/TX)

A single test system can provide the total view

As the combination of both time-domain and frequency domain analysis becomes more important, the need for multiple test systems becomes difficult to manage. A single test system that can fully characterize differential high-speed digital devices such as SATA cables, while leaving domain and format of the analysis up to the designer, is a very powerful tool. Keysight's Physical Layer Test System (PLTS) is designed specifically for this purpose.

PLTS has been designed specifically for signal integrity analysis using a vector network analyzer (VNA) or time domain reflectometer (TDR). PLTS software guides the user through VNA and/or TDR hardware setup and calibration and controls the data acquisition. As an added benefit, the VNA calibration can be made simple by using the popular N4433A electronic calibration (Ecal) module that contains the short-open-load-thru (SOLT) standards. After data acquisition, the PLTS software then automatically applies patented transformation algorithms to accurately present the data in both frequency and time domains, in both forward and reverse transmission and reflection terms, and in all possible modes of operation (single-ended, differential, and mode-conversion). A powerful virtual bit pattern generator feature allows a user defined binary sequence to be applied to the measured data to convolve eye pattern diagrams. Next, highly accurate RLCG 1 models can be extracted and used to enhance the accuracy of your SATA models and simulations. A direct link to Keysight ADS software is built into the software.

SATA signal integrity engineers get the right answers fast with ADS

SATA signal integrity engineers who are hurdling the multi-gigabit/s barrier look to Advanced Design System (ADS) for the correct treatment of high-speed effects like distortion, mismatch, and crosstalk. Uniquely, ADS integrates accurate system, circuit, and electromagnetic (EM) simulators (see Figure 6), so you can not only get the right answers but also get them faster by avoiding error-prone and time-consuming data transfer between a collection of point tools. ADS Transient Convolution includes Channel Simulator that gives ultra low bit error rate (BER) contours in seconds not days. ADS Momentum is the fastest most accurate EM solver for trace-and-via geometries. Keysight's Finite Element Method (FEM) Element provides an integration solution for non-trace-and-via geometries such as bond wires and connectors that require a FEM solver. The FEM Element can be used not only for parameterized components under the ADS platform but also as one of the solvers for full 3D structures captured in our EMPro platform. The EMPro platform can utilize both our FEM and finite difference time-domain (FDTD) solvers.

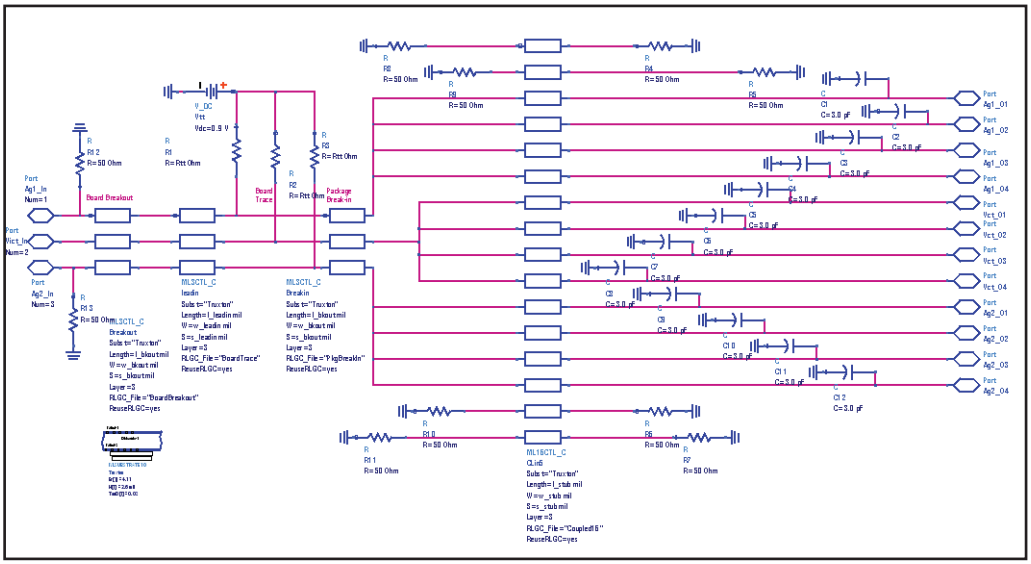


Figure 6. ADS is used to simulate the impact of crosstalk and line lengths of three active lines. After optimizing several trace parameters, you see the optimized eye measurement.

Link/Transaction Level Protocol Layer Debug

When needing to examine SATA traffic at the link layer and above, having a protocol analyzer is essential for development and debugging purposes. Protocol analyzers are able to detect protocol errors and display the traffic related to the error. When protocol errors are detected, you need to analyze why, and then correct the issue. To do this, you need to access the signals, trigger on specific events, capture the traffic reliably, and view the results for quick interpretation.

Quickly find and solve protocol issues

Debugging Serial ATA protocol involves capturing traffic at line-speed and during link power management transitions. A protocol analyzer will need to lock onto traffic quickly, capture a large window of traffic, then trigger on a unique protocol sequence. Debugging lower level problems such as power management and speed negotiation requires exceptionally fast lock times. Once you capture the traffic, you'll want to view the data at different levels of abstraction to assess what is happening. The Keysight U3051A and U3052A Series Serial Attached SCSI and Serial ATA BusXpert protocol analyzers are powerful tools for debug and development. The analyzer supports 1.5/3.0/6.0 Gb/s speeds and has the industry's largest recording buffers of 18 GB and 36 GB respectively. Its reliable data capture has the industry's fastest lock time (average 75 ns non-SSC, 150 ns SSC) for speed negotiation and power management debugging. Use the protocol or spreadsheet views to observe data to find issues associated with entering and exiting out of link power management or during the various speed negotiation phases. For higher layer problems, such as data integrity, the transaction viewer lets you observe all the data from multiple completions together in one location for easy analysis.

Spreadsheet View

Time	Delta time (...	Channel	Type - Initiator	Type - Target	Decode	Command
0.002.344.706	5,642	I4	OPEN		ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.349.632	4,926	T4		DMA Setup (FIS 41)	STP DMA SETUP (FIS 41); D:0; I:0; A:0; Offset:0h; 512 bytes	
0.002.373.930	24,298	T4		OPEN	ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.377.598	3,668	T4		DMA Activate (FIS 39)	STP DMA ACTIVATE (FIS 39)	
0.002.387.166	9,568	I4	Data (FIS 46)		STP DATA (FIS 46); 512 bytes	
0.002.397.592	10,426	I4	OPEN		ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.401.798	4,206	I4	Register Host->Dev (FIS 27)		STP REGISTER HOST->DEV (FIS 27); WRITE FPDMA QUEUED	61: WRITE FPDMA QUEUED
0.002.450.036	48,238	T4		OPEN	ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.453.810	3,774	T4		Register Dev->Host (FIS 34)	STP REGISTER DEV->HOST (FIS 34); I:0; Status:40h; Error:00h	
0.002.459.050	5,240	T4		OPEN	ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.459.320	270	I4	OPEN		ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.462.130	2,810	T4		Set Device Bits (FIS A1)	STP SET DEVICE BITS (FIS A1); Tags: 1 9 10; I:1; N:0; Status...	
0.002.468.922	6,792	I4	Register Host->Dev (FIS 27)		STP REGISTER HOST->DEV (FIS 27); READ FPDMA QUEUED	60: READ FPDMA QUEUED
0.002.491.528	22,606	T4		OPEN	ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.495.222	3,694	T4		Register Dev->Host (FIS 34)	STP REGISTER DEV->HOST (FIS 34); I:0; Status:40h; Error:00h	
0.002.500.802	5,580	I4	OPEN		ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.504.950	4,148	I4	Register Host->Dev (FIS 27)		STP REGISTER HOST->DEV (FIS 27); READ FPDMA QUEUED	60: READ FPDMA QUEUED
0.002.538.514	33,564	T4		OPEN	ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.542.234	3,720	T4		Register Dev->Host (FIS 34)	STP REGISTER DEV->HOST (FIS 34); I:0; Status:40h; Error:00h	
0.002.547.758	5,524	I4	OPEN		ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.551.970	4,212	I4	Register Host->Dev (FIS 27)		STP REGISTER HOST->DEV (FIS 27); READ FPDMA QUEUED	60: READ FPDMA QUEUED
0.002.555.016	3,046	I2	OPEN		ADDRESS OPEN; PROTOCOL:1(SSP); Rate:A(6 Gbps)	
0.002.556.274	1,258	I2	COMMAND		SSP COMMAND; WRITE (10)	2a: WRITE (10)
0.002.569.980	13,706	T4		OPEN	ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.573.648	3,668	T4		Register Dev->Host (FIS 34)	STP REGISTER DEV->HOST (FIS 34); I:0; Status:40h; Error:00h	
0.002.578.758	5,110	T3		OPEN	ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.579.310	552	I4	OPEN		ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.582.420	3,110	T4		DMA Setup (FIS 41)	STP DMA SETUP (FIS 41); D:1; I:0; A:0; Offset:0h; 512 bytes	
0.002.601.740	19,320	T4		OPEN	ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.605.486	3,746	T4		Data (FIS 46)	STP DATA (FIS 46); 512 bytes	
0.002.616.094	10,608	I4	Register Host->Dev (FIS 27)		STP REGISTER HOST->DEV (FIS 27); WRITE FPDMA QUEUED	61: WRITE FPDMA QUEUED
0.002.728.964	112,870	T4		OPEN	ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.732.658	3,694	T4		Register Dev->Host (FIS 34)	STP REGISTER DEV->HOST (FIS 34); I:0; Status:40h; Error:00h	
0.002.738.228	5,570	I4	OPEN		ADDRESS OPEN; PROTOCOL:2(STP); Rate:8(1,5 Gbps)	
0.002.742.374	4,146	I4	Register Host->Dev (FIS 27)		STP REGISTER HOST->DEV (FIS 27); WRITE FPDMA QUEUED	61: WRITE FPDMA QUEUED

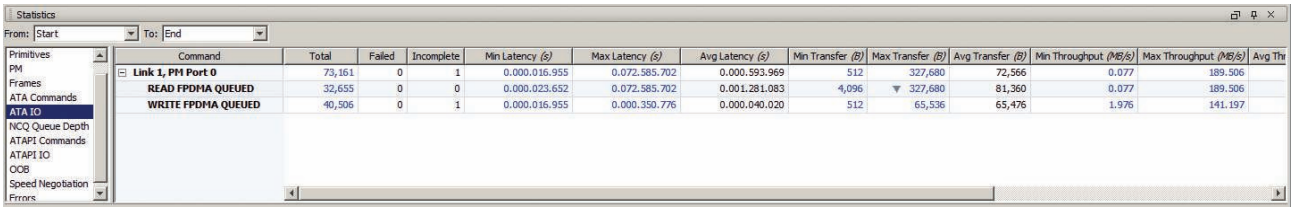
Transaction View

Time	Channel	Command	Status	Source	Destination	Tag	LBA/Sector	Transfer Size	Duration
0.002.556.274	[I2, T2, T4]	WRITE (10)	GOOD	102030405060708	5000CCA008019B61	c036	000000009B4	512	0.039.272.675
0.002.556.274	I2	COMMAND; WRITE (10)							
0.038.133.392	T2	XFER_RDY; 512 bytes							
0.038.139.358	I2	DATA; Offset:0h; 512 bytes							
0.041.828.848	T4	RESPONSE; STATUS:00(GOOD)							
0.002.616.094	[I3, T3, I4...	WRITE FP...	Error:00h; Status:40h	102030405060708	500E004AAAAAAA...	0008	000000002527	512	0.002.311.655
0.002.616.094	I4	Register Host->Dev (FIS 27); WRITE FPDMA QUEUED							
0.002.732.658	T4	Register Dev->Host (FIS 34); I:0; Status:40h; Error:00h							
0.004.238.794	T4	DMA Setup (FIS 41); D:0; I:0; A:0; Offset:0h; 512 bytes							
0.004.250.510	T3	DMA Activate (FIS 39)							
0.004.259.666	I3	Data (FIS 46); 512 bytes							
0.004.927.636	T4	Set Device Bits (FIS A1); Tags: 1 8 9 14 15; I:1; N:0; StatusLo:0h; StatusHi:4h; Error:00h							
0.002.742.374	[I2, T2, I4...	WRITE FP...	Error:00h; Status:40h	102030405060708	500E004AAAAAAA...	000e	000000002528	512	0.002.185.375
0.002.742.374	I4	Register Host->Dev (FIS 27); WRITE FPDMA QUEUED							

Figure 7. Spreadsheet and transaction traffic views

Performance and statistics-based analysis Link/Transaction Level Protocol Layer Debug

The Keysight U3051A and U3052A BusXpert software is also able to display live performance statistics during capture and provide in-depth analysis on the captured data. Command throughput, frame turn-around time, queue depth and other analytical information are calculated and hyperlinked to navigate easily within the trace data. The statistical reports can also be exported to XML, XLS, and HTML for exterior reporting. These metrics allow customers to look for potential areas of interest and benchmark products under test.

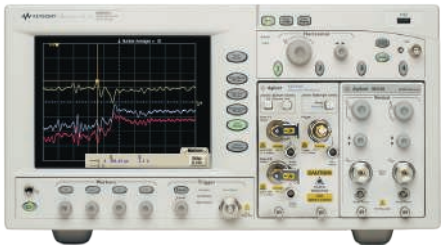


Command	Total	Failed	Incomplete	Min Latency (s)	Max Latency (s)	Avg Latency (s)	Min Transfer (B)	Max Transfer (B)	Avg Transfer (B)	Min Throughput (MB/s)	Max Throughput (MB/s)	Avg Thr
Link 1, PM Port 0	73,161	0	1	0.000.016.955	0.072.585.702	0.000.593.969	512	327,680	72,566	0.077	189.506	
READ FPDMA QUEUED	32,655	0	0	0.000.023.652	0.072.585.702	0.001.281.083	4,096	327,680	81,360	0.077	189.506	
WRITE FPDMA QUEUED	40,506	0	1	0.000.016.955	0.000.350.776	0.000.040.020	512	65,536	65,476	1.976	141.197	

Figure 8. Read and write performance statistics screenshot

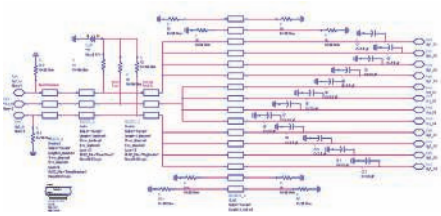
Keysight SATA Solutions

86100C Infiniium DCA-J wide-bandwidth oscilloscope with TDR



The Keysight 86100C Infiniium DCA-J can view electrical waveforms with bandwidths up to 93 GHz. The DCA-J is an ideal tool for making signal integrity and jitter measurements for high speed signaling standards. Complete jitter analysis is simplified via a one-button approach to review the random and deterministic jitter components. With the Keysight 54754A Differential TDR/TDT module, you can characterize impedance and crosstalk in channels and view the results in either time-domain or as S-parameters in the frequency domain.

Advanced Design System (ADS)



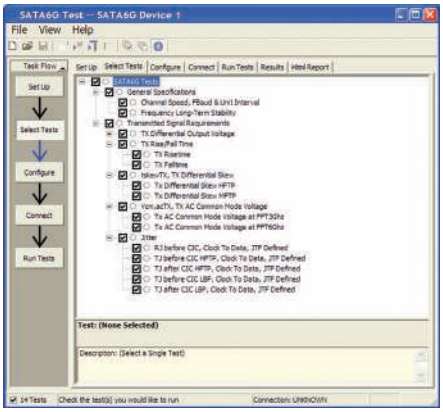
SATA signal integrity engineers who are hurdling the multi-gigabit/s barrier look to ADS for the correct treatment of high-speed effects like distortion, mismatch, and crosstalk. Uniquely, ADS integrates accurate system, circuit, and EM simulators so you can not only get the right answers but also get them faster by avoiding error-prone and time-consuming data transfer between a collection of point tools.

90000 Series Infiniium 12 GHz bandwidth oscilloscope

The Keysight 90000 Series Infiniium oscilloscopes deliver the highest performance real-time measurement system available. The Infiniium 90000 Series offers the industry's lowest noise floor, jitter noise floor, and trigger jitter, making it the ideal tool for signal integrity and jitter measurements. Models are available from 2.5 GHz to 13 GHz, and can be upgraded in bandwidth for future needs.

Keysight SATA Solutions

N5411B SATA compliance test software

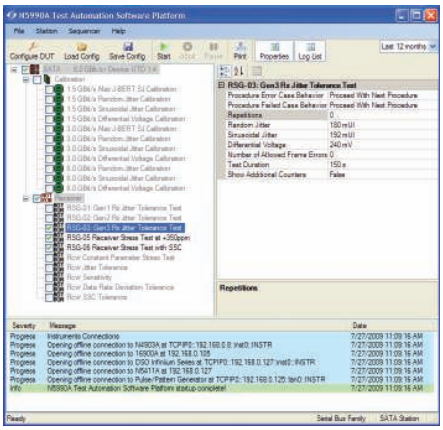


The N5411B SATA compliance test software for Infiniium oscilloscopes provides you with a fast and easy way to validate and debug your SATA 1.5 Gb/s (Gen1), 3 Gb/s (Gen2) and 6 Gb/s (Gen3) silicon, host bus adapter, port multiplier, high-density disk drive, solid-state disk drive or optical disk drive. The N5411B software provides automated compliance test support for the i (internal), m (eSATA) and x (SAS attachment) interfaces points, and displays the results in a flexible report format. In addition to the measurement data, the report provides a margin analysis that shows how closely your device passed or failed each test.

J-BERT N4903B high-performance serial BERT

The J-BERT N4903B is the ideal solution for the design and test of digital components; devices and subsystems up to 12.5 Gb/s. It provides complete, calibrated jitter sources for stressed eye testing of receivers. Automated jitter tolerance testing allows quick and accurate compliance and characterization testing. For transmitter analysis, a wide range of jitter analysis tools are built-in and provide insight into the underlying causes behind bit errors.

N5990A test automation software platform



The Keysight N5990A test automation software platform is the most powerful tool for serial and multi-lane gigabit testing. It is the unique universal platform for testing a wide range of digital buses such as SATA, PCI Express®, USB or HDMI. The N5990A can be tailored to individual test needs with the flexible test sequencer and controls all instruments needed for your tests. The configurable database interface of the N5990A test automation platform enables the convenient storage of all test results. The N5990A software takes test automation to the next level of performance and convenience. It addresses specific bus standards by individual software modules with the same user interface. N5990A controls e.g. the oscilloscope, J-BERT and protocol analyzer and thus creates an integrated, automated test system.

Keysight SATA Solutions

U3051A and U3052A SerialTek Micro and Pro SAS/SATA protocol analyzers

SerialTek´s BusXpert SAS/SATA test solutions represent the industry´s most advanced protocol analyzer. Hardware and software innovations such as a PCI Express to host connection, trace indexing, and microprocessor-assisted InstaSearch improve the user experience when developing and debugging with a protocol analyzer. These technologies, along with the industry´s largest buffer size of 36 GB, and a simple, robust GUI allow the BusXpert to efficiently display, manipulate, trigger and save traces at speeds not seen in any other competitive offering. The BusXpert is available in several configurations varying on protocol line rate, port count, buffer size and platform. Both the Pro and Micro platforms are lightweight, highly portable and easily upgraded.

For digging deep into the SATA protocol for debugging and development, the BusXpert features in-depth triggering including errors such as CRC and 10b encoding, meaningful display of captured data, and native PHYs for accurate recording of clock sensitive events such as power management, speed negotiation, and SSC traffic. Users can view traffic at the application layer and drill down through the various layers to determine potential issues.

N5230C 4-port 26.5 GHz vector network analyzer with N1930B physical layer test system software

As the combination of both time-domain and frequency domain analysis becomes more important, the need for multiple test systems becomes difficult to manage. A single test system that can fully characterize differential high-speed digital devices such as SATA cables, while leaving domain and format of the analysis up to the designer, is a very powerful tool. Keysight's Physical Layer Test System (PLTS) is designed specifically for this purpose. More information is available at **www.keysight.com/find/plts**

Keysight SATA Design And Test Solutions

To quickly identify the Keysight solutions you need, the following table indicates what SATA technologies each tool supports.

Table 2. Keysight SATA solutions by SATA technology

			Technology supported		
	Product	**Description**	**1.5 Gbps**	**3.0 Gbps**	**6.0 Gbps**
Transmitter compliance	DSA90804A	8 GHz Infiniium oscilloscope*	X		
	DSA91204A	12 GHz Infiniium oscilloscope	X	X	X
	DSA91304A	13 GHz Infiniium oscilloscope	X	X	X
	N5411B	SATA compliance software	X	X	X
	N9398C	DC blocking cap (0.045 to 26.5 GHz) - Qty 2	X	X	X
	81134A	Pulse Pattern Generator	X	X	X
	15442A	SMA phase match cable (4 pc)	X	X	X
		ULINK DriveMaster 2008, SATA Explorer AND PC w/Intel ICH 7/8 chipset	X	X	X
		SATA Near End Fixture (Crescent Heart software)	X	X	X
		SATA Far End Fixture (Crescent Heart software)	X	X	X
Receiver compliance	N4903B	J-BERT high-performance serial BERT	X	X	X
	N5990A	Automated compliance and device characterization test software	X	X	X
	N4915A-005	6.5 GBit/s serial bus switch	X	X	X
	N4915-60001	SATA ISI channel	X	X	X
	U3051A	SerialTek Micro SAS/SATA protocol analyzer	X	X	X
	U3052A	SerialTek Pro SAS/SATA protocol analyzer	X	X	X
Impedence/return loss	86100C	DCA-J Infiniium oscilloscope	X	X	X
	54754A	TDR module	X	X	X
	86108A*	Precision waveform analyzer	X	X	X
	W2212B*	ADS Design Software bundle (ADS Core, Transient Convolution, Layout, Momentum G2, FEM, Ptolemy)	X	X	X

Optional for debug – not required for compliance

Related Keysight Literature

Publication title	Pub number
Keysight Technologies Infiniium 90000 Series Oscilloscopes Data Sheet	5989-7819EN
Keysight Technologies N5411B SATA 6Gb/s Compliance Test Software Data Sheet	5990-3594EN
86100C Infiniium DCA-J Wide Bandwidth Oscilloscope with TDR Brochure	5989-5235EN
Keysight J-BERT N4903B High-Performance Serial BERT Data Sheet	5990-3217EN
Keysight Technologies N5990A Test Automation Software Platform Data Sheet	5989-5483EN
Designing for Signal Integrity with Advanced Design System Data Sheet	5989-8392EN

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Further information on Keysight's SATA solutions can be found online at www.keysight.com/find/SATA

Have questions about SATA design and test? Consult the Keysight discussion forum online at www.keysight.com/find/forums

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at:
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