Keysight D9030TBTC Thunderbolt 3 Test Application

KEYSIGHT TECHNOLOGIES

Programmer's Reference

Notices

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In This Book

This book is your guide to programming the Keysight Technologies D9030TBTC Thunderbolt 3 Test Application.

- Chapter 1, “Introduction to Programming,” starting on page 7, describes compliance application programming basics.
- Chapter 2, “Configuration Variables and Values,” starting on page 9, Chapter 3, “Test Names and IDs,” starting on page 47, Chapter 4, “Instruments,” starting on page 103, and Chapter 5, “Message IDs,” starting on page 105 provide information specific to programming the D9030TBTC Thunderbolt 3 Test Application.

How to Use This Book

Programmers who are new to compliance application programming should read all of the chapters in order. Programmers who are already familiar with this may review chapters 2, 3, 4, and 5 for changes.

Contents

1 Introduction to Programming

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This chapter introduces the basics for remote programming a compliance application. The programming commands provide the means of remote control. Basic operations that you can do remotely with a computer and a compliance app running on an oscilloscope include:

- Launching and closing the application.
- Configuring the options.
- Running tests.
- Getting results.
- Controlling when and were dialogs get displayed
- Saving and loading projects.

You can accomplish other tasks by combining these functions.

Remote Programming Toolkit

The majority of remote interface features are common across all the Keysight Technologies, Inc. family of compliance applications. Information on those features is provided in the N5452A Compliance Application Remote Programming Toolkit available for download from Keysight here: www.keysight.com/find/rpi. The D9030TBTC Thunderbolt 3 Test Application uses Remote Interface Revision 6.3. The help files provided with the toolkit indicate which features are supported in this version.

In the toolkit, various documents refer to "application-specific configuration variables, test information, and instrument information". These are provided in Chapters 2, 3, and 4 of this document, and are also available directly from the application's user interface when the remote interface is enabled (View>Preferences::Remote tab::Show remote interface hints). See the toolkit for more information.

2 Configuration Variables and Values

The following table contains a description of each of the D9030TBTC Thunderbolt 3 Test Application options that you may query or set remotely using the appropriate remote interface method. The columns contain this information:

- GUI Location – Describes which graphical user interface tab contains the control used to change the value.
- Label – Describes which graphical user interface control is used to change the value.
- Variable – The name to use with the SetConfig method.
- Values – The values to use with the SetConfig method.
- Description – The purpose or function of the variable.

For example, if the graphical user interface contains this control on the **Set Up** tab:

- Enable Advanced Features

then you would expect to see something like this in the table below:

Table 1 Example Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Set Up	Enable Advanced Features	EnableAdvanced	True, False	Enables a set of optional features.

and you would set the variable remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SetConfig 'EnableAdvanced' 'True'"

C# syntax
```

```
---------
remoteAte.SetConfig("EnableAdvanced", "True");
```

Here are the actual configuration variables and values used by this application:

NOTE Some of the values presented in the table below may not be available in certain configurations. Always perform a "test run" of your remote script using the application's graphical user interface to ensure the combinations of values in your program are valid.

NOTE The file, "ConfigInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 2 Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Configure	ACCM Acquisition Number	ACCMAcqNum	(Accepts user-defined text), 1, 5, 10, 15	Select the number of signal acquisitions for live signal analysis (Signal Acquisition Method = [Live]) of AC Common Mode tests.
Configure	Acquisition Bandwidth	RiseFallTimeAcqBW	AUTO, AcquisitionSetup	Select the acquisition bandwidth for the rise/fall time measurement. For [Auto], the acquisition bandwidth will be set to maximum (Automatic). For [Acquisition Setup], the acquisition bandwidth will be set to the value based on the settings in Tools->Acquisition Setup.
Configure	Automation Auto Retry Count	AutomationAutoRetryCount	(Accepts user-defined text), 0, 1, 3, 5	Select the number of auto retry for automation if the signal pattern check fail. Select [0] if user want the automation error shown without any auto retry.
Configure	Automation Timeout	AutomationTimeout	(Accepts user-defined text), 200	Select the controller automation timeout. Unit: Second.
Configure	CTLE Calibration Acquisition Number	CTLECalibrationAcqNum	(Accepts user-defined text), 1, 5, 10, 15	Select the number of signal acquisition for live signal analysis (Signal Acquisition Method = [Live]) of CTLE Calibration.
Configure	Configure Preset Number	ConfigurePresetNumber	1.0, 0.0	Select whether to enable or disable the configure preset number message prompt.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Eye Mask Acquisition Number	MaskAcqNum	(Accepts user-defined text), 1, 5, 10, 15	Select the number of signal acquisition for live signal analysis (Signal Acquisition Method = [Live]) of mask test.
Configure	ISI Filter Lagging Bit	ISILagBit	0.0, 1.0, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0, 10.0, 11.0, 12.0, 13.0, 14.0, 15.0	Select a value for the lagging/trailing bit, which is used to calculate the ISI filter. This config is only applicable when the Jitter Pattern Length value is set to [Arbitrary]. The lagging/trailing bit is greater than or equal to 0.
Configure	ISI Filter Leading Bit	ISILeadBit	0.0, -1.0, -2.0, -3.0, -4.0, -5.0, -6.0, -7.0, -8.0, -9.0, -10.0	Select a value for the leading bit, which is used to calculate the ISI filter. This config is only applicable when the Jitter Pattern Length value is set to [Arbitrary]. The leading bit is less than or equal to 0.
Configure	Interpolation Point	InterpolationPoint	OFF, ON, INT1, INT2, INT4, INT8, INT16	Select the Sin(x)/x interpolation point for acquiring the waveform for all Thunderbolt 3 tests.
Configure	Jitter Pattern Length	JitterPLength	Default, ARBitrary, AUTO	Select the type of pattern length used for the RjDj measurement. For [Default] Jitter Pattern Length, Periodic algorithm will be used for patten length less than 4096; Arbitrary algorithm will be used for others.
Configure	Lane 0 Connection	L0Connection	5, 7	Select the input channel for the Lane 0.
Configure	Lane 1 Connection	L1Connection	6, 7	Select the input channel for the Lane 1.
Configure	Lane to Lane Skew Pattern	LaneToLaneSkewSearchPattern	(Accepts user-defined text), 0111111111111110	Set the triggering pattern and the search pattern used for inter lane skew measurement in Lane to Lane Skew tests.
Configure	Lane to Lane Skew Pattern Match Bit Number	LaneToLaneSkewPatternMatchBitNum	(Accepts user-defined text), 1, 10, 100, 200	Set the number of bit for pattern matching in Lane to Lane Skew tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Lane to Lane Skew Search Method	LaneToLaneSkewSearchMethod	1, 2	Select the method for the pattern search in Lane to Lane Skew tests. For [Method 1], TEdge measurement is used to search for serial data pattern. For [Method 2], InfiniiScan Generic Serial Trigger and TEdge measurement are used to search for serial data pattern.
Configure	Low Frequency Jitter LPF Bandwidth (10.3125 Gb/s or 10Gb/s)	LFJitter_LPF_Bandwidth_10G	(Accepts user-defined text), 1.0E+6, 2.0E+6, 3.0E+6, 4.0E+6, 5.0E+6, 6.0E+6, 7.0E+6, 8.0E+6	Set the bandwidth for the 2nd order Low-Pass Filter (LPF) used to filter on the 10.3125 GB/s and 10 Gb/s signal jitter for low frequency jitter measurement. Unit: Hz.
Configure	Low Frequency Jitter LPF Bandwidth (20.625 Gb/s or 20Gb/s)	LFJitter_LPF_Bandwidth_20G	(Accepts user-defined text), 1.0E+6, 2.0E+6, 3.0E+6, 4.0E+6, 5.0E+6, 6.0E+6, 7.0E+6, 8.0E+6	Set the bandwidth for the 2nd order Low-Pass Filter (LPF) used to filter on the 20.625 GB/s and 20 Gb/s signal jitter for low frequency jitter measurement. Unit: Hz.
Configure	Pattern Check	EnableSignalCheck	1.0, 0.0	When pattern check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run.
Configure	Preset Calibration Acquisition Number	PresetCalibrationAcqNum	(Accepts user-defined text), 1, 5, 10, 15	Select the number of signal acquisition for live signal analysis (Signal Acquisition Method = [Live]) of Preset Calibration.
Configure	RJ Bandwidth	RJBandwidth	NARRow, WIDE	Select the type of filter bandwidth used to separate the DDJ from the RJ and PJ.
Configure	RJ Method	RJMethod	BOTH, SPECtral	Select the type of method used to separate the RJ component.
Configure	SSC Filter Window Size (10.3125 Gb/s or 10Gb/s)	SSC_LPF_WindowSize_10G	(Accepts user-defined text), 0, 900, 1000, 2000, 3000, 4000, 5000, 6000, 8000, 10000	Set the Moving Average Filter's window size used to separate the SSC profile for 10.3125 GB/s and 10 Gb/s Unit Interval and SSC measurement.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	SSC Filter Window Size (20.625 Gb/s or 20Gb/s)	SSC_LPF_WindowSize_20G	(Accepts user-defined text), 0, 900, 1000, 2000, 3000, 4000, 5000, 6000, 8000, 10000	Set the Moving Average Filter's window size used to separate the SSC profile for 20.625 GB/s and 20 Gb/s Unit Interval and SSC measurement.
Configure	SSC Phase Acquisition Number	SSCPhaseAcqNum	(Accepts user-defined text), 1, 5, 10, 15	Select the number of signal acquisition for live signal analysis (Signal Acquisition Method = [Live]) of SSC Phase tests.
Configure	SSC Phase LPF Bandwidth (10.3125 Gb/s or 10Gb/s)	SSCPhaseLPF_Bandwidth_10G	(Accepts user-defined text), 1.0E+6, 2.0E+6, 3.0E+6, 4.0E+6, 5.0E+6, 6.0E+6, 7.0E+6, 8.0E+6	Set the bandwidth for the 2nd order Low-Pass Filter (LPF) used to filter on the 10.3125 GB/s and 10 Gb/s signal phase jitter. Unit: Hz.
Configure	SSC Phase LPF Bandwidth (20.625 Gb/s or 20Gb/s)	SSCPhaseLPF_Bandwidth_20G	(Accepts user-defined text), 1.0E+6, 2.0E+6, 3.0E+6, 4.0E+6, 5.0E+6, 6.0E+6, 7.0E+6, 8.0E+6	Set the bandwidth for the 2nd order Low-Pass Filter (LPF) used to filter on the 20.625 GB/s and 20 Gb/s signal phase jitter. Unit: Hz.
Configure	SSC Phase LPF Damping Factor (10.3125 Gb/s or 10Gb/s)	SSCPhaseLPF_DampFactor_10G	(Accepts user-defined text), 0.570, 0.580, 0.707, 0.940, 1.250, 1.750	Set the damping factor for the 2nd order Low-Pass Filter (LPF) used to filter on the 10.3125 GB/s and 10 Gb/s signal phase jitter.
Configure	SSC Phase LPF Damping Factor (20.625 Gb/s or 20Gb/s)	SSCPhaseLPF_DampFactor_20G	(Accepts user-defined text), 0.570, 0.580, 0.707, 0.940, 1.250, 1.750	Set the damping factor for the 2nd order Low-Pass Filter (LPF) used to filter on the 20.625 GB/s and 20 Gb/s signal phase jitter.
Configure	SSC Slew Rate Filter Window Size	SSCSlewRateLPF_WindowSize	(Accepts user-defined text), 0, 900, 1000, 2000, 3000, 4000, 5000	Set the Moving Average Filter's window size used to separate the SSC profile for signal phase jitter measurement for SSC Slew Rate measurement.
Configure	SSC Slew Rate Interval	SSCSlewRate_Interval	(Accepts user-defined text), 0.5E-6	Set the measurement intervals used for SSC Slew Rate measurement.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Sample Size - All Pattern (Live)	SampSize_MemPts_TBT3_Live	(Accepts user-defined text), 20.0, 26.0, 27.0, 40.0, 32.0, 41.6, 43.2, 64.0	Select the memory points used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]), except Preset Calibration, CTLE Calibration, Rise/Fall Time, Eye Diagram, Unit Interval, SSC, Lane to Lane Skew and Equalization tests. Unit: Mpts.
Configure	Sample Size - Equalization (Live)	SampSize_MemPts_Equalization_Live	(Accepts user-defined text), 0.10, 0.50, 1.0, 0.16, 0.80, 1.6	Select the memory points used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]) of Equalization tests. Unit: Mpts.
Configure	Sample Size - Eye Diagram (Live)	SampSize_NumberOfUI_EyeDiagram_Live	(Accepts user-defined text), 0.5, 1.0, 2.0, 5.0	Select the number of UI points used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]) of Preset Calibration, CTLE Calibration, Eye Diagram tests. Unit: MUI.
Configure	Sample Size - Lane to Lane Skew (Live)	SampSize_MemPts_LaneToLaneSkew_Live	(Accepts user-defined text), 10.0, 20.0, 26.0, 27.0, 16.0, 32.0, 41.6, 43.2	Select the memory points used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]) of Lane to Lane Skew tests. Unit: Mpts.
Configure	Sample Size - Rise/Fall Time (Live)	SampSize_MemPts_RiseFall_Live	(Accepts user-defined text), 4.0, 20.0, 26.0, 27.0, 6.4, 32.0, 41.6, 43.2	Select the memory points used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]) of Rise/Fall Time tests. Unit: Mpts.
Configure	Sample Size - SSC Phase (Live)	SampSize_MemPts_SSCPhase_Live	(Accepts user-defined text), 20.0, 26.0, 27.0, 40.0, 32.0, 41.6, 43.2, 64.0	Select the memory points used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]) of SSC Phase tests. Unit: Mpts.
Configure	Sample Size - Unit Interval and SSC Modulation (Live)	SampSize_MemPts_UI_SSC_Live	(Accepts user-defined text), 20.0, 26.0, 27.0, 40.0, 32.0, 41.6, 43.2, 64.0	Select the memory points used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]) of Unit Interval and SSC Modulation tests. Unit: Mpts.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Sampling Rate	SampRate	80.0E9, 40.0E9, 128.0E9, 64.0E9, 32.0E9	Select the sampling rate that must be used to acquire the waveform(s) for all Thunderbolt 3 tests. Unit: Sa/s.
Configure	Screenshot Image Size	ScreenShotImageSize	GRAT, SCR	Select the screenshot image size for the report items.
Configure	Signal Trigger Level	TriggerThreshold	(Accepts user-defined text), 0.0, 50.0E-03, 100.0E-03, 150.0E-03, 200.0E-03, 250.0E-03, 300.0E-03, 350.0E-03, 400.0E-03, 450.0E-03, 500.0E-03, 550.0E-03, 600.0E-03	Choose the trigger level for all the signal in Thunderbolt 3 tests. Unit: Volt.
Configure	Transmitter Equalization Waveform Acquire	EqualizationNumberOfWfm	2, 5, 10, 20, 50, 100, 150	Select the number of signal acquisition for live signal analysis (Signal Acquisition Method = [Live]) of equalization test.
Configure	Tx CDR Bandwidth (10.3125 Gb/s or 10Gb/s)	TxCDR_Bandwidth_10G	(Accepts user-defined text), 1.0E+6, 2.0E+6, 3.0E+6, 4.0E+6, 5.0E+6, 6.0E+6, 7.0E+6, 8.0E+6	Set the bandwidth for the Thunderbolt 3 CDR (2nd order PLL) used in clock-to-data-recovery for 10.3125 GB/s and 10 Gb/s transmitter test. Unit: Hz.
Configure	Tx CDR Bandwidth (20.625 Gb/s or 20Gb/s)	TxCDR_Bandwidth_20G	(Accepts user-defined text), 1.0E+6, 2.0E+6, 3.0E+6, 4.0E+6, 5.0E+6, 6.0E+6, 7.0E+6, 8.0E+6	Set the bandwidth for the Thunderbolt 3 CDR (2nd order PLL) used in clock-to-data-recovery for 20.625 GB/s and 20 Gb/s transmitter test. Unit: Hz.
Configure	Tx CDR Damping Factor (10.3125 Gb/s or 10Gb/s)	TxCDR_DampFactor_10G	(Accepts user-defined text), 0.570, 0.580, 0.707, 0.940, 1.750	Set the damping factor for the Thunderbolt 3 CDR (2nd order PLL) used in clock-to-data-recovery for 10.3125 GB/s and 10 Gb/s transmitter test.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Tx CDR Damping Factor (20.625 Gb/s or 20Gb/s)	TxCDR_DampFactor_20G	(Accepts user-defined text), 0.570, 0.580, 0.707, 0.940, 1.750	Set the damping factor for the Thunderbolt 3 CDR (2nd order PLL) used in clock-to-data-recovery for 20.625 GB/s and 20 Gb/s transmitter test.
Configure	Tx CTLE AC Gain (10.3125 Gb/s or 10Gb/s)	TxCTLE_ACGain_10G	(Accepts user-defined text), 1.41	Set the AC Gain of the CTLE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests.
Configure	Tx CTLE AC Gain (20.625 Gb/s or 20Gb/s)	TxCTLE_ACGain_20G	(Accepts user-defined text), 1.41	Set the AC Gain of the CTLE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests.
Configure	Tx CTLE Pole 1 (10.3125 Gb/s or 10Gb/s)	TxCTLE_Pole1_10G	(Accepts user-defined text), 1.0E+9, 1.5E+9, 2.0E+9, 2.5E+9, 3.0E+9, 5.0E+9, 10.0E+9, 15.0E+9	Set the Pole 1 of the CTLE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests. Unit: rad/sec.
Configure	Tx CTLE Pole 1 (20.625 Gb/s or 20Gb/s)	TxCTLE_Pole1_20G	(Accepts user-defined text), 1.0E+9, 1.5E+9, 2.0E+9, 2.5E+9, 3.0E+9, 5.0E+9, 10.0E+9, 15.0E+9	Set the Pole 1 of the CTLE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests. Unit: rad/sec.
Configure	Tx CTLE Pole 2 (10.3125 Gb/s or 10Gb/s)	TxCTLE_Pole2_10G	(Accepts user-defined text), 1.0E+9, 1.5E+9, 2.0E+9, 2.5E+9, 3.0E+9, 5.0E+9, 10.0E+9, 15.0E+9	Set the Pole 2 of the CTLE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests. Unit: rad/sec.
Configure	Tx CTLE Pole 2 (20.625 Gb/s or 20Gb/s)	TxCTLE_Pole2_20G	(Accepts user-defined text), 1.0E+9, 1.5E+9, 2.0E+9, 2.5E+9, 3.0E+9, 5.0E+9, 10.0E+9, 15.0E+9	Set the Pole 2 of the CTLE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests. Unit: rad/sec.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Tx Cable Model - TP3EQ Test (10.3125 Gb/s or 10Gb/s)	TxCable_Model_10G	(Accepts user-defined text), DoNothing.tf4, TBT_2_0m.tf4, 1mCable_TBT_2_0m.tf4, N7015A_IncludingPlug_TBT_2_0m.tf4, N7015A_NotIncludingPlug_TBT_2_0m.tf4, N7015A_IncludingPlug_1mCable_TBT_2_0m.tf4, N7015A_NotIncludingPlug_1mCable_TBT_2_0m.tf4	Select the cable model transfer function used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests. If different transfer function need to be used for Lane 0 and Lane 1, separate two transfer function file with comma. TBT_2_0m: Embed 2m reference cable. 1mCable_TBT_2_0m: De-embed 1m SMA cable and embed 2m reference cable. N7015A_IncludingPlug_TBT_2_0m: De-embed N7015A which include plug and embed 2m reference cable. N7015A_NotIncludingPlug_TBT_2_0m: De-embed N7015A which don't include plug and embed 2m reference cable. N7015A_IncludingPlug_1mCable_TBT_2_0m: De-embed N7015A which include plug and 1m SMA cable and embed 2m reference cable. N7015A_NotIncludingPlug_1mCable_TBT_2_0m: De-embed N7015A which don't include plug and 1m SMA cable and embed 2m reference cable. The default transfer files are available in following directory: C:\ProgramData\Keysight\Infiniium\Apps\TBT3Test\app\Transfer Function\ To use custom transfer function file, please copy the transfer function file (*.tf4) into the directory above and type the transfer function file name (include the file extension) in the textbox above to apply the transfer function file in TP3EQ transmitter tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Tx Cable Model - TP3EQ Test (20.625 Gb/s or 20Gb/s)	TxCable_Model_20G	(Accepts user-defined text), DoNothing.tf4, TBT_0_8m.tf4, 1mCable_TBT_0_8m.tf4, N7015A_IncludingPlug_TBT_0_8m.tf4, N7015A_NotIncludingPlug_TBT_0_8m.tf4, N7015A_IncludingPlug_1mCable_TBT_0_8m.tf4, N7015A_NotIncludingPlug_1mCable_TBT_0_8m.tf4	Select the cable model transfer function used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests. If different transfer function need to be used for Lane 0 and Lane 1, separate two transfer function file with comma. TBT_0_8m: Embed 0.8m reference cable. 1mCable_TBT_0_8m: De-embed 1m SMA cable and embed 0.8m reference cable. N7015A_IncludingPlug_TBT_0_8m: De-embed N7015A which include plug and embed 0.8m reference cable. N7015A_NotIncludingPlug_TBT_0_8m: De-embed N7015A which don't include plug and embed 0.8m reference cable. N7015A_IncludingPlug_1mCable_TBT_0_8m: De-embed N7015A which include plug and 1m SMA cable and embed 0.8m reference cable. N7015A_NotIncludingPlug_1mCable_TBT_0_8m: De-embed N7015A which don't include plug and 1m SMA cable and embed 0.8m reference cable. The default transfer files are available in following directory: C:\ProgramData\Keysight\Infiniium\Apps\TBT3Test\app\Transfer Function\ To use custom transfer function file, please copy the transfer function file (*.tf4) into the directory above and type the transfer function file name (include the file extension) in the textbox above to apply the transfer function file in TP3EQ transmitter tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Tx DFE Delay (10.3125 Gb/s or 10Gb/s)	TxDFE_Delay_10G	(Accepts user-defined text), Auto, InfiniiumAuto, 0	Set the delay to be used to amplify the eye back to the original size of the DFE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests. Unit: ps. For [Auto], the Thunderbolt 3 application will set the delay to center the eye based on the histogram. For [Infiniium Auto], the Infiniium application will set the delay to center the eye.
Configure	Tx DFE Delay (20.625 Gb/s or 20Gb/s)	TxDFE_Delay_20G	(Accepts user-defined text), Auto, InfiniiumAuto, 0	Set the delay to be used to amplify the eye back to the original size of the DFE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests. Unit: ps. For [Auto], the Thunderbolt 3 application will set the delay to center the eye based on the histogram. For [Infiniium Auto], the Infiniium application will set the delay to center the eye.
Configure	Tx DFE Eye Width (10.3125 Gb/s or 10Gb/s)	TxDFE_EyeWidth_10G	(Accepts user-defined text), 0	Set the eye width to be used for the optimization of the DFE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests. Unit: UI. This configuration only applicable when the [Tx DFE Setup] configuration variable is set to [Auto].
Configure	Tx DFE Eye Width (20.625 Gb/s or 20Gb/s)	TxDFE_EyeWidth_20G	(Accepts user-defined text), 0	Set the eye width to be used for the optimization of the DFE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests. Unit: UI. This configuration only applicable when the [Tx DFE Setup] configuration variable is set to [Auto].

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Tx DFE Feedback Coefficient Maximum (10.3125 Gb/s or 10Gb/s)	TxDFE_FeedbackCoefficient Max_10G	(Accepts user-defined text), 0.050	Set the maximum feedback coefficient of the DFE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests. Unit: V. This configuration only applicable when the [Tx DFE State] configuration variable is set to [Enable].
Configure	Tx DFE Feedback Coefficient Maximum (20.625 Gb/s or 20Gb/s)	TxDFE_FeedbackCoefficient Max_20G	(Accepts user-defined text), 0.050	Set the maximum feedback coefficient of the DFE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests. Unit: V. This configuration only applicable when the [Tx DFE State] configuration variable is set to [Enable].
Configure	Tx DFE Gain (10.3125 Gb/s or 10Gb/s)	TxDFE_Gain_10G	(Accepts user-defined text), 1	Set the gain to be used to amplify the eye back to the original size of the DFE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests. This configuration only applicable when the [Tx DFE Setup] configuration variable is set to [Partial Auto] or [Manual].
Configure	Tx DFE Gain (20.625 Gb/s or 20Gb/s)	TxDFE_Gain_20G	(Accepts user-defined text), 1	Set the gain to be used to amplify the eye back to the original size of the DFE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests. This configuration only applicable when the [Tx DFE Setup] configuration variable is set to [Partial Auto] or [Manual].
Configure	Tx DFE Lower Target (10.3125 Gb/s or 10Gb/s)	TxDFE_LowerTarget_10G	(Accepts user-defined text), -1.00	Set the lower target value of the DFE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests. Unit: V. This configuration only applicable when the [Tx DFE Setup] configuration variable is set to [Manual].

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Tx DFE Lower Target (20.625 Gb/s or 20Gb/s)	TxDFE_LowerTarget_20G	(Accepts user-defined text), -1.00	Set the lower target value of the DFE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests. Unit: V. This configuration only applicable when the [Tx DFE Setup] configuration variable is set to [Manual].
Configure	Tx DFE Max Tap Value (10.3125 Gb/s or 10Gb/s)	TxDFE_MaxTapValue_10G	(Accepts user-defined text), 1.000	Set the maximum tap value to be used for the optimization of the DFE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests. This configuration only applicable when the [Tx DFE Setup] configuration variable is set to [Auto].
Configure	Tx DFE Max Tap Value (20.625 Gb/s or 20Gb/s)	TxDFE_MaxTapValue_20G	(Accepts user-defined text), 1.000	Set the maximum tap value to be used for the optimization of the DFE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests. This configuration only applicable when the [Tx DFE Setup] configuration variable is set to [Auto].
Configure	Tx DFE Min Tap Value (10.3125 Gb/s or 10Gb/s)	TxDFE_MinTapValue_10G	(Accepts user-defined text), 0	Set the minimum tap value to be used for the optimization of the DFE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests. This configuration only applicable when the [Tx DFE Setup] configuration variable is set to [Auto].
Configure	Tx DFE Min Tap Value (20.625 Gb/s or 20Gb/s)	TxDFE_MinTapValue_20G	(Accepts user-defined text), 0	Set the minimum tap value to be used for the optimization of the DFE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests. This configuration only applicable when the [Tx DFE Setup] configuration variable is set to [Auto].

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Tx DFE Number of Taps (10.3125 Gb/s or 10Gb/s)	TxDFE_TapNumber_10G	1	Set the number of taps of the DFE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests. This configuration only applicable when the [Tx DFE State] configuration variable is set to [Enable].
Configure	Tx DFE Number of Taps (20.625 Gb/s or 20Gb/s)	TxDFE_TapNumber_20G	1	Set the number of taps of the DFE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests. This configuration only applicable when the [Tx DFE State] configuration variable is set to [Enable].
Configure	Tx DFE Setup (10.3125 Gb/s or 10Gb/s)	TxDFE_Setup_10G	Auto, PartialAuto, Manual	Select whether to automatically setup or manually setup of the DFE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests. For [Auto], the Infiniium will perform optimization based on the eye width, minimum and maximum tap value. For [Partial Auto], the Infiniium will perform optimization based on the eye width, minimum and maximum tap value. Then, override the gain and delay. For [Manual], the user need to specify the tap value, upper target voltage, lower target voltage, gain and delay.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Tx DFE Setup (20.625 Gb/s or 20Gb/s)	TxDFE_Setup_20G	Auto, PartialAuto, Manual	Select whether to automatically setup or manually setup of the DFE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests. For [Auto], the Infiniium will perform optimization based on the eye width, minimum and maximum tap value. For [Partial Auto], the Infiniium will perform optimization based on the eye width, minimum and maximum tap value. Then, override the gain and delay. For [Manual], the user need to specify the tap value, upper target voltage, lower target voltage, gain and delay.
Configure	Tx DFE State (10.3125 Gb/s or 10Gb/s)	TxDFE_State_10G	true, false	Select whether to enable or disable the DFE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests.
Configure	Tx DFE State (20.625 Gb/s or 20Gb/s)	TxDFE_State_20G	true, false	Select whether to enable or disable the DFE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests.
Configure	Tx DFE State (CTLE Calibration)	TxDFE_State_CTLE_Calibration	true, false	Select whether to enable or disable the DFE used for the CTLE Calibration.
Configure	Tx DFE State (Eye Diagram)	TxDFE_State_EyeDiagram	true, false	Select whether to enable or disable the DFE used for the eye diagram measurement of TP3EQ transmitter tests.
Configure	Tx DFE State (Jitter)	TxDFE_State_Jitter	true, false	Select whether to enable or disable the DFE used for the RjDj measurement of TP3EQ transmitter tests.
Configure	Tx DFE Tap 1 Value (10.3125 Gb/s or 10Gb/s)	TxDFE_Tap1Value_10G	(Accepts user-defined text), 0.005	Set the tap 1 value of the DFE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests. This configuration only applicable when the [Tx DFE Setup] configuration variable is set to [Manual].

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Tx DFE Tap 1 Value (20.625 Gb/s or 20Gb/s)	TxDFE_Tap1Value_20G	(Accepts user-defined text), 0.005	Set the tap 1 value of the DFE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests. This configuration only applicable when the [Tx DFE Setup] configuration variable is set to [Manual].
Configure	Tx DFE Upper Target (10.3125 Gb/s or 10Gb/s)	TxDFE_UpperTarget_10G	(Accepts user-defined text), 1.00	Set the upper target value of the DFE used for the 10.3125 Gb/s and 10 Gb/s TP3EQ transmitter tests. Unit: V. This configuration only applicable when the [Tx DFE Setup] configuration variable is set to [Manual].
Configure	Tx DFE Upper Target (20.625 Gb/s or 20Gb/s)	TxDFE_UpperTarget_20G	(Accepts user-defined text), 1.00	Set the upper target value of the DFE used for the 20.625 Gb/s and 20 Gb/s TP3EQ transmitter tests. Unit: V. This configuration only applicable when the [Tx DFE Setup] configuration variable is set to [Manual].
Configure	Tx Equalization Preset	TxEqualization_Preset	ALL, P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select ALL for all Preset numbers or select specific Preset number to test.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Tx Transfer Function - TP1 Test (10.3125 Gb/s or 10Gb/s)	TxTransferFunction_10G	(Accepts user-defined text), DoNothing.tf4, 1mCable.tf4, N7015A_IncludingPlug.tf4, N7015A_NotIncludingPlug.tf4, N7015A_IncludingPlug_1mCable.tf4, N7015A_NotIncludingPlug_1mCable.tf4	Select the transfer function used for the 10.3125 Gb/s and 10 Gb/s TP1 transmitter tests except Tx AC Common Mode Voltage tests. If different transfer function need to be used for Lane 0 and Lane 1, separate two transfer function file with comma. 1mCable: De-embed 1m SMA cable. N7015A_IncludingPlug: De-embed N7015A which include plug. N7015A_NotIncludingPlug: De-embed N7015A which don't include plug. N7015A_IncludingPlug_1mCable : De-embed N7015A which include plug and 1m SMA cable. N7015A_NotIncludingPlug_1mCable: De-embed N7015A which don't include plug and 1m SMA cable. The default transfer files are available in following directory: C:\ProgramData\Keysight\Infiniium\Apps\TBT3Test\app\Transfer Function\ To use custom transfer function file, please copy the transfer function file (*.tf4) into the directory above and type the transfer function file name (include the file extension) in the textbox above to apply the transfer function file in TP1 transmitter tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Tx Transfer Function - TP1 Test (20.625 Gb/s or 20Gb/s)	TxTransferFunction_20G	(Accepts user-defined text), DoNothing.tf4, 1mCable.tf4, N7015A_IncludingPlug.tf4, N7015A_NotIncludingPlug.tf4, N7015A_IncludingPlug_1mCable.tf4, N7015A_NotIncludingPlug_1mCable.tf4	Select the transfer function used for the 20.625 Gb/s and 20 Gb/s TP1 transmitter tests except Tx AC Common Mode Voltage tests. If different transfer function need to be used for Lane 0 and Lane 1, separate two transfer function file with comma. 1mCable: De-embed 1m SMA cable. N7015A_IncludingPlug: De-embed N7015A which include plug. N7015A_NotIncludingPlug: De-embed N7015A which don't include plug. N7015A_IncludingPlug_1mCable: De-embed N7015A which include plug and 1m SMA cable. N7015A_NotIncludingPlug_1mCable: De-embed N7015A which don't include plug and 1m SMA cable. The default transfer files are available in following directory: C:\ProgramData\Keysight\Infiniium\Apps\TBT3Test\app\Transfer Function\ To use custom transfer function file, please copy the transfer function file (*.tf4) into the directory above and type the transfer function file name (include the file extension) in the textbox above to apply the transfer function file in TP1 transmitter tests.
Configure	Unit Interval Mean Filter Window Size (10.3125 Gb/s or 10Gb/s)	UI_LPF_WindowSize_10G	(Accepts user-defined text), 0, 900, 1000, 2000, 3000, 4000, 5000, 6000, 8000, 10000	Set the Moving Average Filter's window size used for 10.3125 GB/s and 10 Gb/s Unit Interval mean measurement.
Configure	Unit Interval Mean Filter Window Size (20.625 Gb/s or 20Gb/s)	UI_LPF_WindowSize_20G	(Accepts user-defined text), 0, 900, 1000, 2000, 3000, 4000, 5000, 6000, 8000, 10000	Set the Moving Average Filter's window size used for 20.625 GB/s and 20 Gb/s Unit Interval mean measurement.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Unit Interval Mean Window Count	UI_WindowCount	Max, 10, 20, 50, 100	Select the number of windows used for Unit Interval mean measurement.
Configure	Unit Interval and SSC Test Method	UI_SSC_TestMethod	EXE, UDF	Select the type of method used to perform the Unit Interval and SSC measurement. For [Executable File (EXE)], the Thunderbolt 3 application will use the executable file to perform the Unit Interval and SSC measurement. For [User Defined Function (UDF)], the Thunderbolt 3 application will use the Infiniium's User Defined Function to perform the Unit Interval and SSC measurement.
Run Tests	Event	RunEvent	(None), Fail, Margin < N, Pass	Names of events that can be used with the StoreMode=Event or RunUntil RunEventAction options
Run Tests	RunEvent=Margin < N: Minimum required margin %	RunEvent_Margin < N_MinPercent	Any integer in range: 0 <= value <= 99	Specify N using the 'Minimum required margin %' control.
Set Up	10 Gb/s	10 Gb/s	0.0, 1.0	Select whether the DUT support 10 Gb/s bit rate. Select whether the DUT support 10 Gb/s bit rate.
Set Up	10.3125 Gb/s	10.3125 Gb/s	0.0, 1.0	Select whether the DUT support 10.3125 Gb/s bit rate. Select whether the DUT support 10.3125 Gb/s bit rate.
Set Up	20 Gb/s	20 Gb/s	0.0, 1.0	Select whether the DUT support 20 Gb/s bit rate. Select whether the DUT support 20 Gb/s bit rate.
Set Up	20.625 Gb/s	20.625 Gb/s	0.0, 1.0	Select whether the DUT support 20.625 Gb/s bit rate. Select whether the DUT support 20.625 Gb/s bit rate.
Set Up	Automation Controller	AutomationController	TBT-TPA-UHG2, TCPIP	Select the type of Thunderbolt Automation Controller. Select the type of Thunderbolt Automation Controller.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	CTLE DC Gain 0dB	DC0dB	0.0, 1.0	Enable or disable 0dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 0dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 1dB	DC1dB	0.0, 1.0	Enable or disable 1dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 1dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 2dB	DC2dB	0.0, 1.0	Enable or disable 2dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 2dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 3dB	DC3dB	0.0, 1.0	Enable or disable 3dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 3dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 4dB	DC4dB	0.0, 1.0	Enable or disable 4dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 4dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 5dB	DC5dB	0.0, 1.0	Enable or disable 5dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 5dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 6dB	DC6dB	0.0, 1.0	Enable or disable 6dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 6dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 7dB	DC7dB	0.0, 1.0	Enable or disable 7dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 7dB CTLE DC Gain for the CTLE Calibration Run.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	CTLE DC Gain 8dB	DC8dB	0.0, 1.0	Enable or disable 8dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 8dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	CTLE DC Gain 9dB	DC9dB	0.0, 1.0	Enable or disable 9dB CTLE DC Gain for the CTLE Calibration Run. Enable or disable 9dB CTLE DC Gain for the CTLE Calibration Run.
Set Up	Consumer Power Profile 1	ConsumerPowerProfile1	0.0, 1.0	Enable or disable Consumer Power Profile 1 support. Enable or disable Consumer Power Profile 1 support.
Set Up	Consumer Power Profile 2	ConsumerPowerProfile2	0.0, 1.0	Enable or disable Consumer Power Profile 2 support. Enable or disable Consumer Power Profile 2 support.
Set Up	Consumer Power Profile 3	ConsumerPowerProfile3	0.0, 1.0	Enable or disable Consumer Power Profile 3 support. Enable or disable Consumer Power Profile 3 support.
Set Up	DUT Orientation (USB Type-C)	DUTOrientation	Normal, Inverted	Select the orientation type, either 'Normal' or 'Inverted' for USB Type-C DUT. Select the orientation type, either 'Normal' or 'Inverted' for USB Type-C DUT.
Set Up	DUT Type	DUTType	Device, Host	Select the device type of the DUT, either 'Device' or 'Host'. Select the device type of the DUT, either 'Device' or 'Host'.
Set Up	Device Identifier	DeviceIdentifier	(Accepts user-defined text)	Identifier for the DUT in testing. Identifier for the DUT in testing.
Set Up	Enable Automation Controller	AutomationEnable	0.0, 1.0	Enable or disable the use of Thunderbolt Automation Controller. Enable or disable the use of Thunderbolt Automation Controller.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Enable CTLE Calibration	cfgCTLECal	0.0, 1.0	Enable or disable CTLE calibration to find the optimum CTLE DC Gain. Enable or disable CTLE calibration to find the optimum CTLE DC Gain.
Set Up	Enable Predefined CTLE DC Gain	cfgPredefinedDCgain	0.0, 1.0	Enable or disable to predefined optimum CTLE DC Gain. Enable or disable to predefined optimum CTLE DC Gain.
Set Up	Enable Predefined Preset Number	cfgPredefinedPresetNum	0.0, 1.0	Enable or disable predefined optimum Preset Number. Enable or disable predefined optimum Preset Number.
Set Up	Enable Preset Calibration	cfgPresetCal	0.0, 1.0	Enable or disable preset calibration run to find the optimum Preset Number. Enable or disable preset calibration run to find the optimum Preset Number.
Set Up	Enable Saved Waveform	EnableSavedWaveform	0.0, 1.0	Enable or disable the use of saved waveform in the tests. Enable or disable the use of saved waveform in the tests.
Set Up	Enable Type-C Controller Automation	TCTCEnabled	0.0, 1.0	Enable or disable USB Type-C Test Controller automation. Enable or disable USB Type-C Test Controller automation.
Set Up	PRBS11_NegSignal Directory	PRBS11_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS11 negative signal waveform. This variable use to store the directory of PRBS11 negative signal waveform.
Set Up	PRBS11_PosSignal Directory	PRBS11_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS11 positive signal waveform. This variable use to store the directory of PRBS11 positive signal waveform.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	PRBS31_NegSignal Directory	PRBS31_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS31 negative signal waveform. This variable use to store the directory of PRBS31 negative signal waveform.
Set Up	PRBS31_PosSignal Directory	PRBS31_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS31 positive signal waveform. This variable use to store the directory of PRBS31 positive signal waveform.
Set Up	PRBS9_NegSignalD irectory	PRBS9_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS9 negative signal waveform. This variable use to store the directory of PRBS9 negative signal waveform.
Set Up	PRBS9_PosSignalD irectory	PRBS9_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS9 positive signal waveform. This variable use to store the directory of PRBS9 positive signal waveform.
Set Up	Port Number	PortNumber	1 Port, 2 Ports	Select the number of ports supported by the DUT. Select the number of ports supported by the DUT.
Set Up	Port1 Name	Port1Name	(Accepts user-defined text), Port 1, (SELECT OR TYPE)	Set the port name for the first port. This field will be show in report. Set the port name for the first port. This field will be show in report.
Set Up	Port2 Name	Port2Name	(Accepts user-defined text), Port 2, (SELECT OR TYPE)	Set the port name for the second port. This field will be show in report. Set the port name for the second port. This field will be show in report.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined CTLE DC Gain (10 Gb/s) (Port 1, Lane 0)	PredefinedCTLEDCGain10GbpsPort1Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3EQ tests of Port 1, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3EQ tests of Port 1, Lane 0.
Set Up	Predefined CTLE DC Gain (10 Gb/s) (Port 1, Lane 1)	PredefinedCTLEDCGain10GbpsPort1Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3EQ tests of Port 1, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3EQ tests of Port 1, Lane 1.
Set Up	Predefined CTLE DC Gain (10 Gb/s) (Port 2, Lane 0)	PredefinedCTLEDCGain10GbpsPort2Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3EQ tests of Port 2, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3EQ tests of Port 2, Lane 0.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined CTLE DC Gain (10 Gb/s) (Port 2, Lane 1)	PredefinedCTLEDCGain10GbpsPort2Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3EQ tests of Port 2, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 10 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10 Gb/s TP3EQ tests of Port 2, Lane 1.
Set Up	Predefined CTLE DC Gain (10.3125 Gb/s) (Port 1, Lane 0)	PredefinedCTLEDCGain10_3125GbpsPort1Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3EQ tests of Port 1, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3EQ tests of Port 1, Lane 0.
Set Up	Predefined CTLE DC Gain (10.3125 Gb/s) (Port 1, Lane 1)	PredefinedCTLEDCGain10_3125GbpsPort1Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3EQ tests of Port 1, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3EQ tests of Port 1, Lane 1.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined CTLE DC Gain (10.3125 Gb/s) (Port 2, Lane 0)	PredefinedCTLEDCGain10_3125GbpsPort2Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3EQ tests of Port 2, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3EQ tests of Port 2, Lane 0.
Set Up	Predefined CTLE DC Gain (10.3125 Gb/s) (Port 2, Lane 1)	PredefinedCTLEDCGain10_3125GbpsPort2Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3EQ tests of Port 2, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 10.3125 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 10.3125 Gb/s TP3EQ tests of Port 2, Lane 1.
Set Up	Predefined CTLE DC Gain (20 Gb/s) (Port 1, Lane 0)	PredefinedCTLEDCGain20GbpsPort1Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3EQ tests of Port 1, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3EQ tests of Port 1, Lane 0.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined CTLE DC Gain (20 Gb/s) (Port 1, Lane 1)	PredefinedCTLEDCGain20GbpsPort1Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3EQ tests of Port 1, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3EQ tests of Port 1, Lane 1.
Set Up	Predefined CTLE DC Gain (20 Gb/s) (Port 2, Lane 0)	PredefinedCTLEDCGain20GbpsPort2Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3EQ tests of Port 2, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3EQ tests of Port 2, Lane 0.
Set Up	Predefined CTLE DC Gain (20 Gb/s) (Port 2, Lane 1)	PredefinedCTLEDCGain20GbpsPort2Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3EQ tests of Port 2, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 20 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20 Gb/s TP3EQ tests of Port 2, Lane 1.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined CTLE DC Gain (20.625 Gb/s) (Port 1, Lane 0)	PredefinedCTLEDCGain20_625GbpsPort1Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3EQ tests of Port 1, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 1, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3EQ tests of Port 1, Lane 0.
Set Up	Predefined CTLE DC Gain (20.625 Gb/s) (Port 1, Lane 1)	PredefinedCTLEDCGain20_625GbpsPort1Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3EQ tests of Port 1, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 1, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3EQ tests of Port 1, Lane 1.
Set Up	Predefined CTLE DC Gain (20.625 Gb/s) (Port 2, Lane 0)	PredefinedCTLEDCGain20_625GbpsPort2Lane0	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3EQ tests of Port 2, Lane 0. Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 2, Lane 0. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3EQ tests of Port 2, Lane 0.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined CTLE DC Gain (20.625 Gb/s) (Port 2, Lane 1)	PredefinedCTLEDCGain20_625GbpsPort2Lane1	0dB, 1dB, 2dB, 3dB, 4dB, 5dB, 6dB, 7dB, 8dB, 9dB	Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3EQ tests of Port 2, Lane 1. Select the predefined optimum CTLE DC Gain for bit rate 20.625 Gb/s tests of Port 2, Lane 1. The optimum CTLE DC Gain will be used to run the bit rate 20.625 Gb/s TP3EQ tests of Port 2, Lane 1.
Set Up	Predefined Preset Number (10 Gb/s) (Port 1, Lane 0)	PredefinedPresetNumber10GbpsPort1Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 1, Lane 0. Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 1, Lane 0.
Set Up	Predefined Preset Number (10 Gb/s) (Port 1, Lane 1)	PredefinedPresetNumber10GbpsPort1Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 1, Lane 1. Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 1, Lane 1.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined Preset Number (10 Gb/s) (Port 2, Lane 0)	PredefinedPresetNumber10GbpsPort2Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 2, Lane 0. Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 2, Lane 0.
Set Up	Predefined Preset Number (10 Gb/s) (Port 2, Lane 1)	PredefinedPresetNumber10GbpsPort2Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 2, Lane 1. Select the predefined optimum Preset Number for bit rate 10 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 10 Gb/s tests of Port 2, Lane 1.
Set Up	Predefined Preset Number (10.3125 Gb/s) (Port 1, Lane 0)	PredefinedPresetNumber10_3125GbpsPort1Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 1, Lane 0. Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 1, Lane 0.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined Preset Number (10.3125 Gb/s) (Port 1, Lane 1)	PredefinedPresetNumber10_3125GbpsPort1Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 1, Lane 1. Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 1, Lane 1.
Set Up	Predefined Preset Number (10.3125 Gb/s) (Port 2, Lane 0)	PredefinedPresetNumber10_3125GbpsPort2Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 2, Lane 0. Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 2, Lane 0.
Set Up	Predefined Preset Number (10.3125 Gb/s) (Port 2, Lane 1)	PredefinedPresetNumber10_3125GbpsPort2Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 2, Lane 1. Select the predefined optimum Preset Number for bit rate 10.3125 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 10.3125 Gb/s tests of Port 2, Lane 1.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined Preset Number (20 Gb/s) (Port 1, Lane 0)	PredefinedPresetNumber20GbpsPort1Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 1, Lane 0. Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 1, Lane 0.
Set Up	Predefined Preset Number (20 Gb/s) (Port 1, Lane 1)	PredefinedPresetNumber20GbpsPort1Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 1, Lane 1. Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 1, Lane 1.
Set Up	Predefined Preset Number (20 Gb/s) (Port 2, Lane 0)	PredefinedPresetNumber20GbpsPort2Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 2, Lane 0. Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 2, Lane 0.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined Preset Number (20 Gb/s) (Port 2, Lane 1)	PredefinedPresetNumber20GbpsPort2Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 2, Lane 1. Select the predefined optimum Preset Number for bit rate 20 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 20 Gb/s tests of Port 2, Lane 1.
Set Up	Predefined Preset Number (20.625 Gb/s) (Port 1, Lane 0)	PredefinedPresetNumber20_625GbpsPort1Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 1, Lane 0. Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 1, Lane 0. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 1, Lane 0.
Set Up	Predefined Preset Number (20.625 Gb/s) (Port 1, Lane 1)	PredefinedPresetNumber20_625GbpsPort1Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 1, Lane 1. Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 1, Lane 1. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 1, Lane 1.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Predefined Preset Number (20.625 Gb/s) (Port 2, Lane 0)	PredefinedPresetNumber20_625GbpsPort2Lane0	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 2, Lane 0. Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 2, Lane 0. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 2, Lane 0.
Set Up	Predefined Preset Number (20.625 Gb/s) (Port 2, Lane 1)	PredefinedPresetNumber20_625GbpsPort2Lane1	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 2, Lane 1. Select the predefined optimum Preset Number for bit rate 20.625 Gb/s tests of Port 2, Lane 1. The optimum Preset Number will be used to run the bit rate 20.625 Gb/s tests of Port 2, Lane 1.
Set Up	Preset Number 0	P0	0.0, 1.0	Enable or disable Preset Number 0 for the Preset Calibration Run. Enable or disable Preset Number 0 for the Preset Calibration Run.
Set Up	Preset Number 1	P1	0.0, 1.0	Enable or disable Preset Number 1 for the Preset Calibration Run. Enable or disable Preset Number 1 for the Preset Calibration Run.
Set Up	Preset Number 10	P10	0.0, 1.0	Enable or disable Preset Number 10 for the Preset Calibration Run. Enable or disable Preset Number 10 for the Preset Calibration Run.
Set Up	Preset Number 11	P11	0.0, 1.0	Enable or disable Preset Number 11 for the Preset Calibration Run. Enable or disable Preset Number 11 for the Preset Calibration Run.
Set Up	Preset Number 12	P12	0.0, 1.0	Enable or disable Preset Number 12 for the Preset Calibration Run. Enable or disable Preset Number 12 for the Preset Calibration Run.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Preset Number 13	P13	0.0, 1.0	Enable or disable Preset Number 13 for the Preset Calibration Run. Enable or disable Preset Number 13 for the Preset Calibration Run.
Set Up	Preset Number 14	P14	0.0, 1.0	Enable or disable Preset Number 14 for the Preset Calibration Run. Enable or disable Preset Number 14 for the Preset Calibration Run.
Set Up	Preset Number 15	P15	0.0, 1.0	Enable or disable Preset Number 15 for the Preset Calibration Run. Enable or disable Preset Number 15 for the Preset Calibration Run.
Set Up	Preset Number 2	P2	0.0, 1.0	Enable or disable Preset Number 2 for the Preset Calibration Run. Enable or disable Preset Number 2 for the Preset Calibration Run.
Set Up	Preset Number 3	P3	0.0, 1.0	Enable or disable Preset Number 3 for the Preset Calibration Run. Enable or disable Preset Number 3 for the Preset Calibration Run.
Set Up	Preset Number 4	P4	0.0, 1.0	Enable or disable Preset Number 4 for the Preset Calibration Run. Enable or disable Preset Number 4 for the Preset Calibration Run.
Set Up	Preset Number 5	P5	0.0, 1.0	Enable or disable Preset Number 5 for the Preset Calibration Run. Enable or disable Preset Number 5 for the Preset Calibration Run.
Set Up	Preset Number 6	P6	0.0, 1.0	Enable or disable Preset Number 6 for the Preset Calibration Run. Enable or disable Preset Number 6 for the Preset Calibration Run.
Set Up	Preset Number 7	P7	0.0, 1.0	Enable or disable Preset Number 7 for the Preset Calibration Run. Enable or disable Preset Number 7 for the Preset Calibration Run.
Set Up	Preset Number 8	P8	0.0, 1.0	Enable or disable Preset Number 8 for the Preset Calibration Run. Enable or disable Preset Number 8 for the Preset Calibration Run.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Preset Number 9	P9	0.0, 1.0	Enable or disable Preset Number 9 for the Preset Calibration Run. Enable or disable Preset Number 9 for the Preset Calibration Run.
Set Up	Provider Power Profile 1	ProviderPowerProfile1	0.0, 1.0	Enable or disable Provider Power Profile 1 support. Enable or disable Provider Power Profile 1 support.
Set Up	Provider Power Profile 2	ProviderPowerProfile2	0.0, 1.0	Enable or disable Provider Power Profile 2 support. Enable or disable Provider Power Profile 2 support.
Set Up	Provider Power Profile 3	ProviderPowerProfile3	0.0, 1.0	Enable or disable Provider Power Profile 3 support. Enable or disable Provider Power Profile 3 support.
Set Up	SQ2_NegSignalDirectory	SQ2_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of SQ2 negative signal waveform. This variable use to store the directory of SQ2 negative signal waveform.
Set Up	SQ2_PosSignalDirectory	SQ2_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of SQ2 positive signal waveform. This variable use to store the directory of SQ2 positive signal waveform.
Set Up	SQ_NegSignalDirectory	SQ_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of SQ16/SQ32 negative signal waveform. This variable use to store the directory of SQ16/SQ32 negative signal waveform.
Set Up	SQ_PosSignalDirectory	SQ_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of SQ16/SQ32 positive signal waveform. This variable use to store the directory of SQ16/SQ32 positive signal waveform.
Set Up	Specification Version	SpecVersion	Thunderbolt Specification Rev 3.0	Select the test specification for testing. Select the test specification for testing.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Test Lane Port 1	TestLanePort1	Both lanes, Lane 0 only, Lane 1 only	Select the test lane of Port 1 for testing. Select the test lane of Port 1 for testing.
Set Up	Test Lane Port 2	TestLanePort2	Both lanes, Lane 0 only, Lane 1 only	Select the test lane of Port 2 for testing. Select the test lane of Port 2 for testing.
Set Up	Test Setup Complete	TestSetupComplete	0.0, 1.0	Determine whether the test setup is completed. Determine whether the test setup is completed.
Set Up	User Comment	UserComments	(Accepts user-defined text)	Additional comments for the DUT in testing. Additional comments for the DUT in testing.
Set Up	User Description	UserDescription	(Accepts user-defined text)	Short description for the DUT in testing. Short description for the DUT in testing.

3 Test Names and IDs

The following table shows the mapping between each test's numeric ID and name. The numeric ID is required by various remote interface methods.

- Name – The name of the test as it appears on the user interface **Select Tests** tab.
- Test ID – The number to use with the RunTests method.
- Description – The description of the test as it appears on the user interface **Select Tests** tab.

For example, if the graphical user interface displays this tree in the **Select Tests** tab:

- All Tests
  - Rise Time
  - Fall Time

then you would expect to see something like this in the table below:

Table 3 Example Test Names and IDs

Name	Test ID	Description
Fall Time	110	Measures clock fall time.
Rise Time	100	Measures clock rise time.

and you would run these tests remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SelectedTests '100,110'"
arsl -a ipaddress -c "Run"

C# syntax
---------
remoteAte.SelectedTests = new int[]{100,110};
remoteAte.Run();
```

Here are the actual Test names and IDs used by this application:

NOTE The file, "TestInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 4 Test IDs and Names

Name	TestID	Description
3.3.1a Tx Preset Calibration (Port 1, Lane 0)	1810	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 0)	2810	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 0)	10810	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 0)	20810	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 0)	11810	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 0)	21810	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 0)	12810	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 0)	22810	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 1)	1811	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 1)	2811	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 1)	10811	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 1)	20811	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 1)	11811	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 1)	21811	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 1)	12811	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 1, Lane 1)	22811	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 0)	1812	The Preset Calibration is used to find the optimized preset.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.1a Tx Preset Calibration (Port 2, Lane 0)	2812	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 0)	10812	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 0)	20812	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 0)	11812	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 0)	21812	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 0)	12812	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 0)	22812	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 1)	1813	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 1)	2813	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 1)	10813	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 1)	20813	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 1)	11813	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 1)	21813	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 1)	12813	The Preset Calibration is used to find the optimized preset.
3.3.1a Tx Preset Calibration (Port 2, Lane 1)	22813	The Preset Calibration is used to find the optimized preset.
3.3.1b Tx CTLE Calibration (Port 1, Lane 0)	1820	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 1, Lane 0)	2820	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 1, Lane 0)	10820	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 1, Lane 0)	20820	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.1b Tx CTLE Calibration (Port 1, Lane 0)	11820	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 1, Lane 0)	21820	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 1, Lane 0)	12820	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 1, Lane 0)	22820	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 1, Lane 1)	1821	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 1, Lane 1)	2821	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 1, Lane 1)	10821	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 1, Lane 1)	20821	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 1, Lane 1)	11821	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 1, Lane 1)	21821	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 1, Lane 1)	12821	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 1, Lane 1)	22821	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 0)	1822	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 0)	2822	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 0)	10822	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 0)	20822	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 0)	11822	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 0)	21822	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 0)	12822	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3.1b Tx CTLE Calibration (Port 2, Lane 0)	22822	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 1)	1823	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 1)	2823	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 1)	10823	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 1)	20823	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 1)	11823	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 1)	21823	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 1)	12823	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.3.1b Tx CTLE Calibration (Port 2, Lane 1)	22823	The CTLE Calibration is used to find the optimized DC gain value for the CTLE.
3.4.10 Tx Total Jitter (Port 1, Lane 0)	2671	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
3.4.10 Tx Total Jitter (Port 1, Lane 0)	21671	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
3.4.10 Tx Total Jitter (Port 1, Lane 0)	1671	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.4.10 Tx Total Jitter (Port 1, Lane 0)	11671	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.4.10 Tx Total Jitter (Port 1, Lane 1)	2672	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
3.4.10 Tx Total Jitter (Port 1, Lane 1)	21672	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
3.4.10 Tx Total Jitter (Port 1, Lane 1)	1672	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.4.10 Tx Total Jitter (Port 1, Lane 1)	11672	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.4.10 Tx Total Jitter (Port 2, Lane 0)	2673	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
3.4.10 Tx Total Jitter (Port 2, Lane 0)	21673	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.10 Tx Total Jitter (Port 2, Lane 0)	1673	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.4.10 Tx Total Jitter (Port 2, Lane 0)	11673	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.4.10 Tx Total Jitter (Port 2, Lane 1)	2674	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
3.4.10 Tx Total Jitter (Port 2, Lane 1)	21674	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
3.4.10 Tx Total Jitter (Port 2, Lane 1)	1674	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.4.10 Tx Total Jitter (Port 2, Lane 1)	11674	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 1, Lane 0)	2871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 1, Lane 0)	21871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 1, Lane 0)	1871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 1, Lane 0)	11871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 1, Lane 1)	2872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 1, Lane 1)	21872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 1, Lane 1)	1872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 1, Lane 1)	11872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 2, Lane 0)	2873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 2, Lane 0)	21873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 2, Lane 0)	1873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 2, Lane 0)	11873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 2, Lane 1)	2874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.11 Tx Uncorrelated Jitter (Port 2, Lane 1)	21874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 2, Lane 1)	1874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.4.11 Tx Uncorrelated Jitter (Port 2, Lane 1)	11874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 0)	2971	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 0)	21971	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 0)	1971	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 0)	11971	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 1)	2972	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 1)	21972	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 1)	1972	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 1)	11972	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 0)	2973	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 0)	21973	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 0)	1973	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 0)	11973	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 1)	2974	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 1)	21974	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 1)	1974	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
3.4.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 1)	11974	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 0)	2981	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 0)	21981	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 0)	1981	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 0)	11981	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 1)	2982	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 1)	21982	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 1)	1982	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 1)	11982	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 0)	2983	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 0)	21983	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 0)	1983	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 0)	11983	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 1)	2984	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 1)	21984	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 1)	1984	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.4.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 1)	11984	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 1, Lane 0)	2121	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 1, Lane 0)	21121	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 1, Lane 0)	1121	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.14 Tx AC Common Mode Voltage (Port 1, Lane 0)	11121	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 1, Lane 1)	2221	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 1, Lane 1)	21221	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 1, Lane 1)	1221	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 1, Lane 1)	11221	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 2, Lane 0)	2321	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 2, Lane 0)	21321	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 2, Lane 0)	1321	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 2, Lane 0)	11321	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 2, Lane 1)	2421	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 2, Lane 1)	21421	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 2, Lane 1)	1421	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
3.4.14 Tx AC Common Mode Voltage (Port 2, Lane 1)	11421	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 1, Lane 0)	2961	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 1, Lane 0)	21961	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 1, Lane 0)	1961	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 1, Lane 0)	11961	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 1, Lane 1)	2962	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 1, Lane 1)	21962	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.14 Tx Duty Cycle Distortion (Port 1, Lane 1)	1962	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 1, Lane 1)	11962	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 2, Lane 0)	2963	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 2, Lane 0)	21963	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 2, Lane 0)	1963	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 2, Lane 0)	11963	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 2, Lane 1)	2964	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 2, Lane 1)	21964	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 2, Lane 1)	1964	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.4.14 Tx Duty Cycle Distortion (Port 2, Lane 1)	11964	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.4.15 Tx Eye Diagram (Port 1, Lane 0)	2131	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
3.4.15 Tx Eye Diagram (Port 1, Lane 0)	21131	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
3.4.15 Tx Eye Diagram (Port 1, Lane 0)	1131	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.4.15 Tx Eye Diagram (Port 1, Lane 0)	11131	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.4.15 Tx Eye Diagram (Port 1, Lane 1)	2231	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
3.4.15 Tx Eye Diagram (Port 1, Lane 1)	21231	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
3.4.15 Tx Eye Diagram (Port 1, Lane 1)	1231	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.4.15 Tx Eye Diagram (Port 1, Lane 1)	11231	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.4.15 Tx Eye Diagram (Port 2, Lane 0)	2331	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.15 Tx Eye Diagram (Port 2, Lane 0)	21331	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
3.4.15 Tx Eye Diagram (Port 2, Lane 0)	1331	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.4.15 Tx Eye Diagram (Port 2, Lane 0)	11331	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.4.15 Tx Eye Diagram (Port 2, Lane 1)	2431	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
3.4.15 Tx Eye Diagram (Port 2, Lane 1)	21431	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
3.4.15 Tx Eye Diagram (Port 2, Lane 1)	1431	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.4.15 Tx Eye Diagram (Port 2, Lane 1)	11431	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.4.16 Tx Total Jitter TP3EQ (Port 1, Lane 0)	2661	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.16 Tx Total Jitter TP3EQ (Port 1, Lane 0)	21661	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.16 Tx Total Jitter TP3EQ (Port 1, Lane 0)	1661	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.16 Tx Total Jitter TP3EQ (Port 1, Lane 0)	11661	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.16 Tx Total Jitter TP3EQ (Port 1, Lane 1)	2662	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.16 Tx Total Jitter TP3EQ (Port 1, Lane 1)	21662	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.16 Tx Total Jitter TP3EQ (Port 1, Lane 1)	1662	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.16 Tx Total Jitter TP3EQ (Port 1, Lane 1)	11662	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.16 Tx Total Jitter TP3EQ (Port 2, Lane 0)	2663	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.16 Tx Total Jitter TP3EQ (Port 2, Lane 0)	21663	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.16 Tx Total Jitter TP3EQ (Port 2, Lane 0)	1663	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.16 Tx Total Jitter TP3EQ (Port 2, Lane 0)	11663	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.16 Tx Total Jitter TP3EQ (Port 2, Lane 1)	2664	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.16 Tx Total Jitter TP3EQ (Port 2, Lane 1)	21664	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.16 Tx Total Jitter TP3EQ (Port 2, Lane 1)	1664	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.16 Tx Total Jitter TP3EQ (Port 2, Lane 1)	11664	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 0)	2771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 0)	21771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 0)	1771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 0)	11771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 1)	2772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 1)	21772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 1)	1772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 1)	11772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 0)	2773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 0)	21773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 0)	1773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 0)	11773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 1)	2774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 1)	21774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 1)	1774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 1)	11774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 0)	2881	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 0)	21881	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 0)	1881	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 0)	11881	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 1)	2882	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 1)	21882	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 1)	1882	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 1)	11882	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 0)	2883	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 0)	21883	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 0)	1883	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 0)	11883	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 1)	2884	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 1)	21884	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 1)	1884	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 1)	11884	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.4.19 Tx Eye Diagram TP3EQ (Port 1, Lane 0)	2991	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
3.4.19 Tx Eye Diagram TP3EQ (Port 1, Lane 0)	21991	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.19 Tx Eye Diagram TP3EQ (Port 1, Lane 0)	1991	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.4.19 Tx Eye Diagram TP3EQ (Port 1, Lane 0)	11991	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.4.19 Tx Eye Diagram TP3EQ (Port 1, Lane 1)	2992	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
3.4.19 Tx Eye Diagram TP3EQ (Port 1, Lane 1)	21992	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
3.4.19 Tx Eye Diagram TP3EQ (Port 1, Lane 1)	1992	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.4.19 Tx Eye Diagram TP3EQ (Port 1, Lane 1)	11992	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.4.19 Tx Eye Diagram TP3EQ (Port 2, Lane 0)	2993	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
3.4.19 Tx Eye Diagram TP3EQ (Port 2, Lane 0)	21993	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
3.4.19 Tx Eye Diagram TP3EQ (Port 2, Lane 0)	1993	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.4.19 Tx Eye Diagram TP3EQ (Port 2, Lane 0)	11993	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.4.19 Tx Eye Diagram TP3EQ (Port 2, Lane 1)	2994	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
3.4.19 Tx Eye Diagram TP3EQ (Port 2, Lane 1)	21994	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
3.4.19 Tx Eye Diagram TP3EQ (Port 2, Lane 1)	1994	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.4.19 Tx Eye Diagram TP3EQ (Port 2, Lane 1)	11994	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.4.1a Tx Equalization Preshoot (Port 1, Lane 0)	2510	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1a Tx Equalization Preshoot (Port 1, Lane 0)	21510	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1a Tx Equalization Preshoot (Port 1, Lane 0)	1510	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1a Tx Equalization Preshoot (Port 1, Lane 0)	11510	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1a Tx Equalization Preshoot (Port 1, Lane 1)	2520	The equalization level at TP1 of a Thunderbolt device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.1a Tx Equalization Preshoot (Port 1, Lane 1)	21520	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1a Tx Equalization Preshoot (Port 1, Lane 1)	1520	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1a Tx Equalization Preshoot (Port 1, Lane 1)	11520	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1a Tx Equalization Preshoot (Port 2, Lane 0)	2530	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1a Tx Equalization Preshoot (Port 2, Lane 0)	21530	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1a Tx Equalization Preshoot (Port 2, Lane 0)	1530	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1a Tx Equalization Preshoot (Port 2, Lane 0)	11530	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1a Tx Equalization Preshoot (Port 2, Lane 1)	2540	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1a Tx Equalization Preshoot (Port 2, Lane 1)	21540	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1a Tx Equalization Preshoot (Port 2, Lane 1)	1540	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1a Tx Equalization Preshoot (Port 2, Lane 1)	11540	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 1, Lane 0)	2610	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 1, Lane 0)	21610	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 1, Lane 0)	1610	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 1, Lane 0)	11610	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 1, Lane 1)	2620	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 1, Lane 1)	21620	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 1, Lane 1)	1620	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 1, Lane 1)	11620	The equalization level at TP1 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.1b Tx Equalization Deemphasis (Port 2, Lane 0)	2630	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 2, Lane 0)	21630	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 2, Lane 0)	1630	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 2, Lane 0)	11630	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 2, Lane 1)	2640	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 2, Lane 1)	21640	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 2, Lane 1)	1640	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1b Tx Equalization Deemphasis (Port 2, Lane 1)	11640	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 1, Lane 0)	2710	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 1, Lane 0)	21710	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 1, Lane 0)	1710	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 1, Lane 0)	11710	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 1, Lane 1)	2720	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 1, Lane 1)	21720	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 1, Lane 1)	1720	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 1, Lane 1)	11720	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 2, Lane 0)	2730	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 2, Lane 0)	21730	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 2, Lane 0)	1730	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.1c Tx Swing Preset 15 (Port 2, Lane 0)	11730	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 2, Lane 1)	2740	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 2, Lane 1)	21740	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 2, Lane 1)	1740	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.
3.4.1c Tx Swing Preset 15 (Port 2, Lane 1)	11740	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 1, Lane 0)	2151	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 1, Lane 0)	21151	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 1, Lane 0)	1151	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 1, Lane 0)	11151	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 1, Lane 1)	2251	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 1, Lane 1)	21251	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 1, Lane 1)	1251	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 1, Lane 1)	11251	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 2, Lane 0)	2351	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 2, Lane 0)	21351	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 2, Lane 0)	1351	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 2, Lane 0)	11351	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 2, Lane 1)	2451	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 2, Lane 1)	21451	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.2a Tx Unit Interval, Min (Port 2, Lane 1)	1451	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2a Tx Unit Interval, Min (Port 2, Lane 1)	11451	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 1, Lane 0)	2152	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 1, Lane 0)	21152	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 1, Lane 0)	1152	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 1, Lane 0)	11152	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 1, Lane 1)	2252	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 1, Lane 1)	21252	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 1, Lane 1)	1252	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 1, Lane 1)	11252	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 2, Lane 0)	2352	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 2, Lane 0)	21352	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 2, Lane 0)	1352	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 2, Lane 0)	11352	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 2, Lane 1)	2452	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 2, Lane 1)	21452	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 2, Lane 1)	1452	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.4.2b Tx Unit Interval, Max (Port 2, Lane 1)	11452	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.3a Tx Unit Interval Mean, Min (Port 1, Lane 0)	2153	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3a Tx Unit Interval Mean, Min (Port 1, Lane 0)	21153	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3a Tx Unit Interval Mean, Min (Port 1, Lane 0)	1153	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3a Tx Unit Interval Mean, Min (Port 1, Lane 0)	11153	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3a Tx Unit Interval Mean, Min (Port 1, Lane 1)	2253	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3a Tx Unit Interval Mean, Min (Port 1, Lane 1)	21253	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3a Tx Unit Interval Mean, Min (Port 1, Lane 1)	1253	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3a Tx Unit Interval Mean, Min (Port 1, Lane 1)	11253	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3a Tx Unit Interval Mean, Min (Port 2, Lane 0)	2353	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3a Tx Unit Interval Mean, Min (Port 2, Lane 0)	21353	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3a Tx Unit Interval Mean, Min (Port 2, Lane 0)	1353	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3a Tx Unit Interval Mean, Min (Port 2, Lane 0)	11353	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3a Tx Unit Interval Mean, Min (Port 2, Lane 1)	2453	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.3a Tx Unit Interval Mean, Min (Port 2, Lane 1)	21453	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3a Tx Unit Interval Mean, Min (Port 2, Lane 1)	1453	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3a Tx Unit Interval Mean, Min (Port 2, Lane 1)	11453	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 1, Lane 0)	2154	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 1, Lane 0)	21154	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 1, Lane 0)	1154	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 1, Lane 0)	11154	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 1, Lane 1)	2254	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 1, Lane 1)	21254	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 1, Lane 1)	1254	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 1, Lane 1)	11254	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 2, Lane 0)	2354	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 2, Lane 0)	21354	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.3b Tx Unit Interval Mean, Max (Port 2, Lane 0)	1354	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 2, Lane 0)	11354	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 2, Lane 1)	2454	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 2, Lane 1)	21454	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 2, Lane 1)	1454	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.3b Tx Unit Interval Mean, Max (Port 2, Lane 1)	11454	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.4.4 Tx SSC Down Spread Range (Port 1, Lane 0)	2165	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.
3.4.4 Tx SSC Down Spread Range (Port 1, Lane 0)	21165	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.
3.4.4 Tx SSC Down Spread Range (Port 1, Lane 0)	1165	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.4.4 Tx SSC Down Spread Range (Port 1, Lane 0)	11165	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.4.4 Tx SSC Down Spread Range (Port 1, Lane 1)	2265	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.
3.4.4 Tx SSC Down Spread Range (Port 1, Lane 1)	21265	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.
3.4.4 Tx SSC Down Spread Range (Port 1, Lane 1)	1265	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.4.4 Tx SSC Down Spread Range (Port 1, Lane 1)	11265	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.4.4 Tx SSC Down Spread Range (Port 2, Lane 0)	2365	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.
3.4.4 Tx SSC Down Spread Range (Port 2, Lane 0)	21365	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.4 Tx SSC Down Spread Range (Port 2, Lane 0)	1365	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.4.4 Tx SSC Down Spread Range (Port 2, Lane 0)	11365	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.4.4 Tx SSC Down Spread Range (Port 2, Lane 1)	2465	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.
3.4.4 Tx SSC Down Spread Range (Port 2, Lane 1)	21465	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.
3.4.4 Tx SSC Down Spread Range (Port 2, Lane 1)	1465	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.4.4 Tx SSC Down Spread Range (Port 2, Lane 1)	11465	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 0)	2162	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 0)	21162	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 0)	1162	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 0)	11162	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 1)	2262	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 1)	21262	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 1)	1262	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 1)	11262	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 0)	2362	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 0)	21362	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 0)	1362	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 0)	11362	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 1)	2462	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 1)	21462	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 1)	1462	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 1)	11462	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 0)	2163	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 0)	21163	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 0)	1163	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 0)	11163	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 1)	2263	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 1)	21263	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 1)	1263	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 1)	11263	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 0)	2363	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 0)	21363	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 0)	1363	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 0)	11363	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 1)	2463	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 1)	21463	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 1)	1463	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.4.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 1)	11463	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.5 Tx SSC Down Spread Rate (Port 1, Lane 0)	2161	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 1, Lane 0)	21161	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 1, Lane 0)	1161	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 1, Lane 0)	11161	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 1, Lane 1)	2261	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 1, Lane 1)	21261	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 1, Lane 1)	1261	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 1, Lane 1)	11261	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 2, Lane 0)	2361	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 2, Lane 0)	21361	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 2, Lane 0)	1361	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 2, Lane 0)	11361	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 2, Lane 1)	2461	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 2, Lane 1)	21461	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 2, Lane 1)	1461	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.4.5 Tx SSC Down Spread Rate (Port 2, Lane 1)	11461	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 1, Lane 0)	2171	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 1, Lane 0)	21171	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 1, Lane 0)	1171	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.6 Tx SSC Phase Deviation (Port 1, Lane 0)	11171	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 1, Lane 1)	2271	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 1, Lane 1)	21271	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 1, Lane 1)	1271	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 1, Lane 1)	11271	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 2, Lane 0)	2371	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 2, Lane 0)	21371	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 2, Lane 0)	1371	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 2, Lane 0)	11371	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 2, Lane 1)	2471	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 2, Lane 1)	21471	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 2, Lane 1)	1471	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
3.4.6 Tx SSC Phase Deviation (Port 2, Lane 1)	11471	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 1, Lane 0)	2172	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 1, Lane 0)	21172	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 1, Lane 0)	1172	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 1, Lane 0)	11172	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 1, Lane 1)	2272	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 1, Lane 1)	21272	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.6b Tx SSC Phase Slew Rate (Port 1, Lane 1)	1272	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 1, Lane 1)	11272	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 2, Lane 0)	2372	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 2, Lane 0)	21372	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 2, Lane 0)	1372	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 2, Lane 0)	11372	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 2, Lane 1)	2472	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 2, Lane 1)	21472	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 2, Lane 1)	1472	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.6b Tx SSC Phase Slew Rate (Port 2, Lane 1)	11472	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.8 Tx Lane to Lane Skew (Port 1, Lane 0/Lane 1)	2410	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt device must be less than the maximum limit.
3.4.8 Tx Lane to Lane Skew (Port 1, Lane 0/Lane 1)	21410	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt device must be less than the maximum limit.
3.4.8 Tx Lane to Lane Skew (Port 1, Lane 0/Lane 1)	1410	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt host must be less than the maximum limit.
3.4.8 Tx Lane to Lane Skew (Port 1, Lane 0/Lane 1)	11410	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt host must be less than the maximum limit.
3.4.8 Tx Lane to Lane Skew (Port 2, Lane 0/Lane 1)	2430	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt device must be less than the maximum limit.
3.4.8 Tx Lane to Lane Skew (Port 2, Lane 0/Lane 1)	21430	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt device must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.8 Tx Lane to Lane Skew (Port 2, Lane 0/Lane 1)	1430	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt host must be less than the maximum limit.
3.4.8 Tx Lane to Lane Skew (Port 2, Lane 0/Lane 1)	11430	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt host must be less than the maximum limit.
3.4.8 Tx SSC Slew Rate (Port 1, Lane 0)	2164	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 1, Lane 0)	21164	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 1, Lane 0)	1164	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 1, Lane 0)	11164	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 1, Lane 1)	2264	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 1, Lane 1)	21264	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 1, Lane 1)	1264	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 1, Lane 1)	11264	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 2, Lane 0)	2364	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 2, Lane 0)	21364	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 2, Lane 0)	1364	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 2, Lane 0)	11364	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 2, Lane 1)	2464	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 2, Lane 1)	21464	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 2, Lane 1)	1464	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.
3.4.8 Tx SSC Slew Rate (Port 2, Lane 1)	11464	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.9a Tx Rise Time (Port 1, Lane 0)	2111	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9a Tx Rise Time (Port 1, Lane 0)	21111	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9a Tx Rise Time (Port 1, Lane 0)	1111	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9a Tx Rise Time (Port 1, Lane 0)	11111	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9a Tx Rise Time (Port 1, Lane 1)	2211	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9a Tx Rise Time (Port 1, Lane 1)	21211	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9a Tx Rise Time (Port 1, Lane 1)	1211	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9a Tx Rise Time (Port 1, Lane 1)	11211	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9a Tx Rise Time (Port 2, Lane 0)	2311	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9a Tx Rise Time (Port 2, Lane 0)	21311	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9a Tx Rise Time (Port 2, Lane 0)	1311	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9a Tx Rise Time (Port 2, Lane 0)	11311	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9a Tx Rise Time (Port 2, Lane 1)	2411	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.9a Tx Rise Time (Port 2, Lane 1)	21411	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9a Tx Rise Time (Port 2, Lane 1)	1411	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9a Tx Rise Time (Port 2, Lane 1)	11411	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 1, Lane 0)	2112	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 1, Lane 0)	21112	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 1, Lane 0)	1112	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 1, Lane 0)	11112	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 1, Lane 1)	2212	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 1, Lane 1)	21212	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 1, Lane 1)	1212	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 1, Lane 1)	11212	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 2, Lane 0)	2312	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 2, Lane 0)	21312	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4.9b Tx Fall Time (Port 2, Lane 0)	1312	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 2, Lane 0)	11312	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 2, Lane 1)	2412	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 2, Lane 1)	21412	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 2, Lane 1)	1412	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.4.9b Tx Fall Time (Port 2, Lane 1)	11412	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.10 Tx Total Jitter (Port 1, Lane 0)	20671	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
3.5.10 Tx Total Jitter (Port 1, Lane 0)	22671	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
3.5.10 Tx Total Jitter (Port 1, Lane 0)	10671	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.5.10 Tx Total Jitter (Port 1, Lane 0)	12671	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.5.10 Tx Total Jitter (Port 1, Lane 1)	20672	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
3.5.10 Tx Total Jitter (Port 1, Lane 1)	22672	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
3.5.10 Tx Total Jitter (Port 1, Lane 1)	10672	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.5.10 Tx Total Jitter (Port 1, Lane 1)	12672	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.5.10 Tx Total Jitter (Port 2, Lane 0)	20673	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
3.5.10 Tx Total Jitter (Port 2, Lane 0)	22673	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.10 Tx Total Jitter (Port 2, Lane 0)	10673	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.5.10 Tx Total Jitter (Port 2, Lane 0)	12673	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.5.10 Tx Total Jitter (Port 2, Lane 1)	20674	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
3.5.10 Tx Total Jitter (Port 2, Lane 1)	22674	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
3.5.10 Tx Total Jitter (Port 2, Lane 1)	10674	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.5.10 Tx Total Jitter (Port 2, Lane 1)	12674	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 1, Lane 0)	20871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 1, Lane 0)	22871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 1, Lane 0)	10871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 1, Lane 0)	12871	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 1, Lane 1)	20872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 1, Lane 1)	22872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 1, Lane 1)	10872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 1, Lane 1)	12872	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 2, Lane 0)	20873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 2, Lane 0)	22873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 2, Lane 0)	10873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 2, Lane 0)	12873	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 2, Lane 1)	20874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.11 Tx Uncorrelated Jitter (Port 2, Lane 1)	22874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt device must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 2, Lane 1)	10874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.5.11 Tx Uncorrelated Jitter (Port 2, Lane 1)	12874	The sum of uncorrelated deterministic jitter and random jitter (UJ) of a Thunderbolt host must be less than maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 0)	20971	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 0)	22971	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 0)	10971	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 0)	12971	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 1)	20972	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 1)	22972	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 1)	10972	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 1)	12972	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 0)	20973	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 0)	22973	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 0)	10973	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 0)	12973	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 1)	20974	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 1)	22974	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 1)	10974	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
3.5.12 Tx Uncorrelated Deterministic Jitter (Port 2, Lane 1)	12974	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 0)	20981	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 0)	22981	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 0)	10981	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 0)	12981	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 1)	20982	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 1)	22982	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 1)	10982	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 1)	12982	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 0)	20983	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 0)	22983	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 0)	10983	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 0)	12983	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 1)	20984	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 1)	22984	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt device must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 1)	10984	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.5.13 Tx Low Frequency Uncorrelated Deterministic Jitter (Port 2, Lane 1)	12984	The sum of low freqeuncy uncorrelated deterministic jitter (UDJ_LF) of a Thunderbolt host must be less than the maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 1, Lane 0)	20121	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 1, Lane 0)	22121	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 1, Lane 0)	10121	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.14 Tx AC Common Mode Voltage (Port 1, Lane 0)	12121	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 1, Lane 1)	20221	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 1, Lane 1)	22221	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 1, Lane 1)	10221	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 1, Lane 1)	12221	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 2, Lane 0)	20321	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 2, Lane 0)	22321	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 2, Lane 0)	10321	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 2, Lane 0)	12321	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 2, Lane 1)	20421	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 2, Lane 1)	22421	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 2, Lane 1)	10421	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
3.5.14 Tx AC Common Mode Voltage (Port 2, Lane 1)	12421	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 1, Lane 0)	20961	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 1, Lane 0)	22961	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 1, Lane 0)	10961	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 1, Lane 0)	12961	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 1, Lane 1)	20962	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 1, Lane 1)	22962	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.14 Tx Duty Cycle Distortion (Port 1, Lane 1)	10962	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 1, Lane 1)	12962	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 2, Lane 0)	20963	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 2, Lane 0)	22963	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 2, Lane 0)	10963	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 2, Lane 0)	12963	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 2, Lane 1)	20964	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 2, Lane 1)	22964	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt device must be less than the maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 2, Lane 1)	10964	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.5.14 Tx Duty Cycle Distortion (Port 2, Lane 1)	12964	The sum of Duty Cycle Distortion (DCD) of a Thunderbolt host must be less than the maximum limit.
3.5.15 Tx Eye Diagram (Port 1, Lane 0)	20131	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
3.5.15 Tx Eye Diagram (Port 1, Lane 0)	22131	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
3.5.15 Tx Eye Diagram (Port 1, Lane 0)	10131	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.5.15 Tx Eye Diagram (Port 1, Lane 0)	12131	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.5.15 Tx Eye Diagram (Port 1, Lane 1)	20231	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
3.5.15 Tx Eye Diagram (Port 1, Lane 1)	22231	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
3.5.15 Tx Eye Diagram (Port 1, Lane 1)	10231	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.5.15 Tx Eye Diagram (Port 1, Lane 1)	12231	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.5.15 Tx Eye Diagram (Port 2, Lane 0)	20331	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.15 Tx Eye Diagram (Port 2, Lane 0)	22331	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
3.5.15 Tx Eye Diagram (Port 2, Lane 0)	10331	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.5.15 Tx Eye Diagram (Port 2, Lane 0)	12331	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.5.15 Tx Eye Diagram (Port 2, Lane 1)	20431	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
3.5.15 Tx Eye Diagram (Port 2, Lane 1)	22431	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
3.5.15 Tx Eye Diagram (Port 2, Lane 1)	10431	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.5.15 Tx Eye Diagram (Port 2, Lane 1)	12431	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
3.5.16 Tx Total Jitter TP3EQ (Port 1, Lane 0)	20661	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.16 Tx Total Jitter TP3EQ (Port 1, Lane 0)	22661	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.16 Tx Total Jitter TP3EQ (Port 1, Lane 0)	10661	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.16 Tx Total Jitter TP3EQ (Port 1, Lane 0)	12661	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.16 Tx Total Jitter TP3EQ (Port 1, Lane 1)	20662	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.16 Tx Total Jitter TP3EQ (Port 1, Lane 1)	22662	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.16 Tx Total Jitter TP3EQ (Port 1, Lane 1)	10662	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.16 Tx Total Jitter TP3EQ (Port 1, Lane 1)	12662	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.16 Tx Total Jitter TP3EQ (Port 2, Lane 0)	20663	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.16 Tx Total Jitter TP3EQ (Port 2, Lane 0)	22663	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.16 Tx Total Jitter TP3EQ (Port 2, Lane 0)	10663	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.16 Tx Total Jitter TP3EQ (Port 2, Lane 0)	12663	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.16 Tx Total Jitter TP3EQ (Port 2, Lane 1)	20664	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.16 Tx Total Jitter TP3EQ (Port 2, Lane 1)	22664	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.16 Tx Total Jitter TP3EQ (Port 2, Lane 1)	10664	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.16 Tx Total Jitter TP3EQ (Port 2, Lane 1)	12664	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 0)	20771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 0)	22771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 0)	10771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 0)	12771	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 1)	20772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 1)	22772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 1)	10772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 1, Lane 1)	12772	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 0)	20773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 0)	22773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 0)	10773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 0)	12773	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 1)	20774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 1)	22774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 1)	10774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.17 Tx Uncorrelated Jitter TP3EQ (Port 2, Lane 1)	12774	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 0)	20881	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 0)	22881	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 0)	10881	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 0)	12881	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 1)	20882	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 1)	22882	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 1)	10882	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 1)	12882	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 0)	20883	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 0)	22883	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 0)	10883	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 0)	12883	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 1)	20884	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 1)	22884	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 1)	10884	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.18 Tx Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 1)	12884	The sum of uncorrelated deterministic jitter (UDJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
3.5.19 Tx Eye Diagram TP3EQ (Port 1, Lane 0)	20991	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
3.5.19 Tx Eye Diagram TP3EQ (Port 1, Lane 0)	22991	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.19 Tx Eye Diagram TP3EQ (Port 1, Lane 0)	10991	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.5.19 Tx Eye Diagram TP3EQ (Port 1, Lane 0)	12991	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.5.19 Tx Eye Diagram TP3EQ (Port 1, Lane 1)	20992	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
3.5.19 Tx Eye Diagram TP3EQ (Port 1, Lane 1)	22992	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
3.5.19 Tx Eye Diagram TP3EQ (Port 1, Lane 1)	10992	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.5.19 Tx Eye Diagram TP3EQ (Port 1, Lane 1)	12992	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.5.19 Tx Eye Diagram TP3EQ (Port 2, Lane 0)	20993	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
3.5.19 Tx Eye Diagram TP3EQ (Port 2, Lane 0)	22993	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
3.5.19 Tx Eye Diagram TP3EQ (Port 2, Lane 0)	10993	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.5.19 Tx Eye Diagram TP3EQ (Port 2, Lane 0)	12993	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.5.19 Tx Eye Diagram TP3EQ (Port 2, Lane 1)	20994	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
3.5.19 Tx Eye Diagram TP3EQ (Port 2, Lane 1)	22994	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
3.5.19 Tx Eye Diagram TP3EQ (Port 2, Lane 1)	10994	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.5.19 Tx Eye Diagram TP3EQ (Port 2, Lane 1)	12994	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
3.5.1a Tx Equalization Preshoot (Port 1, Lane 0)	20510	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1a Tx Equalization Preshoot (Port 1, Lane 0)	22510	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1a Tx Equalization Preshoot (Port 1, Lane 0)	10510	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1a Tx Equalization Preshoot (Port 1, Lane 0)	12510	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1a Tx Equalization Preshoot (Port 1, Lane 1)	20520	The equalization level at TP1 of a Thunderbolt device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.1a Tx Equalization Preshoot (Port 1, Lane 1)	22520	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1a Tx Equalization Preshoot (Port 1, Lane 1)	10520	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1a Tx Equalization Preshoot (Port 1, Lane 1)	12520	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1a Tx Equalization Preshoot (Port 2, Lane 0)	20530	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1a Tx Equalization Preshoot (Port 2, Lane 0)	22530	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1a Tx Equalization Preshoot (Port 2, Lane 0)	10530	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1a Tx Equalization Preshoot (Port 2, Lane 0)	12530	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1a Tx Equalization Preshoot (Port 2, Lane 1)	20540	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1a Tx Equalization Preshoot (Port 2, Lane 1)	22540	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1a Tx Equalization Preshoot (Port 2, Lane 1)	10540	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1a Tx Equalization Preshoot (Port 2, Lane 1)	12540	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 1, Lane 0)	20610	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 1, Lane 0)	22610	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 1, Lane 0)	10610	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 1, Lane 0)	12610	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 1, Lane 1)	20620	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 1, Lane 1)	22620	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 1, Lane 1)	10620	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 1, Lane 1)	12620	The equalization level at TP1 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.1b Tx Equalization Deemphasis (Port 2, Lane 0)	20630	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 2, Lane 0)	22630	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 2, Lane 0)	10630	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 2, Lane 0)	12630	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 2, Lane 1)	20640	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 2, Lane 1)	22640	The equalization level at TP1 of a Thunderbolt device must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 2, Lane 1)	10640	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1b Tx Equalization Deemphasis (Port 2, Lane 1)	12640	The equalization level at TP1 of a Thunderbolt host must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 1, Lane 0)	20710	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 1, Lane 0)	22710	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 1, Lane 0)	10710	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 1, Lane 0)	12710	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 1, Lane 1)	20720	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 1, Lane 1)	22720	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 1, Lane 1)	10720	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 1, Lane 1)	12720	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 2, Lane 0)	20730	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 2, Lane 0)	22730	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 2, Lane 0)	10730	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.1c Tx Swing Preset 15 (Port 2, Lane 0)	12730	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 2, Lane 1)	20740	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 2, Lane 1)	22740	The transmitter swing of Preset 15 of a Thunderbolt Device must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 2, Lane 1)	10740	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.
3.5.1c Tx Swing Preset 15 (Port 2, Lane 1)	12740	The transmitter swing of Preset 15 of a Thunderbolt host must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 1, Lane 0)	20151	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 1, Lane 0)	22151	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 1, Lane 0)	10151	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 1, Lane 0)	12151	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 1, Lane 1)	20251	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 1, Lane 1)	22251	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 1, Lane 1)	10251	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 1, Lane 1)	12251	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 2, Lane 0)	20351	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 2, Lane 0)	22351	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 2, Lane 0)	10351	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 2, Lane 0)	12351	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 2, Lane 1)	20451	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 2, Lane 1)	22451	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.2a Tx Unit Interval, Min (Port 2, Lane 1)	10451	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2a Tx Unit Interval, Min (Port 2, Lane 1)	12451	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 1, Lane 0)	20152	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 1, Lane 0)	22152	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 1, Lane 0)	10152	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 1, Lane 0)	12152	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 1, Lane 1)	20252	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 1, Lane 1)	22252	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 1, Lane 1)	10252	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 1, Lane 1)	12252	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 2, Lane 0)	20352	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 2, Lane 0)	22352	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 2, Lane 0)	10352	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 2, Lane 0)	12352	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 2, Lane 1)	20452	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 2, Lane 1)	22452	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 2, Lane 1)	10452	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
3.5.2b Tx Unit Interval, Max (Port 2, Lane 1)	12452	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.3a Tx Unit Interval Mean, Min (Port 1, Lane 0)	20153	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3a Tx Unit Interval Mean, Min (Port 1, Lane 0)	22153	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3a Tx Unit Interval Mean, Min (Port 1, Lane 0)	10153	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3a Tx Unit Interval Mean, Min (Port 1, Lane 0)	12153	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3a Tx Unit Interval Mean, Min (Port 1, Lane 1)	20253	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3a Tx Unit Interval Mean, Min (Port 1, Lane 1)	22253	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3a Tx Unit Interval Mean, Min (Port 1, Lane 1)	10253	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3a Tx Unit Interval Mean, Min (Port 1, Lane 1)	12253	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3a Tx Unit Interval Mean, Min (Port 2, Lane 0)	20353	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3a Tx Unit Interval Mean, Min (Port 2, Lane 0)	22353	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3a Tx Unit Interval Mean, Min (Port 2, Lane 0)	10353	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3a Tx Unit Interval Mean, Min (Port 2, Lane 0)	12353	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3a Tx Unit Interval Mean, Min (Port 2, Lane 1)	20453	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.3a Tx Unit Interval Mean, Min (Port 2, Lane 1)	22453	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3a Tx Unit Interval Mean, Min (Port 2, Lane 1)	10453	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3a Tx Unit Interval Mean, Min (Port 2, Lane 1)	12453	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 1, Lane 0)	20154	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 1, Lane 0)	22154	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 1, Lane 0)	10154	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 1, Lane 0)	12154	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 1, Lane 1)	20254	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 1, Lane 1)	22254	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 1, Lane 1)	10254	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 1, Lane 1)	12254	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 2, Lane 0)	20354	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 2, Lane 0)	22354	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.3b Tx Unit Interval Mean, Max (Port 2, Lane 0)	10354	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 2, Lane 0)	12354	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 2, Lane 1)	20454	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 2, Lane 1)	22454	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 2, Lane 1)	10454	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.3b Tx Unit Interval Mean, Max (Port 2, Lane 1)	12454	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
3.5.4 Tx SSC Down Spread Range (Port 1, Lane 0)	20165	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.
3.5.4 Tx SSC Down Spread Range (Port 1, Lane 0)	22165	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.
3.5.4 Tx SSC Down Spread Range (Port 1, Lane 0)	10165	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.5.4 Tx SSC Down Spread Range (Port 1, Lane 0)	12165	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.5.4 Tx SSC Down Spread Range (Port 1, Lane 1)	20265	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.
3.5.4 Tx SSC Down Spread Range (Port 1, Lane 1)	22265	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.
3.5.4 Tx SSC Down Spread Range (Port 1, Lane 1)	10265	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.5.4 Tx SSC Down Spread Range (Port 1, Lane 1)	12265	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.5.4 Tx SSC Down Spread Range (Port 2, Lane 0)	20365	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.
3.5.4 Tx SSC Down Spread Range (Port 2, Lane 0)	22365	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.4 Tx SSC Down Spread Range (Port 2, Lane 0)	10365	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.5.4 Tx SSC Down Spread Range (Port 2, Lane 0)	12365	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.5.4 Tx SSC Down Spread Range (Port 2, Lane 1)	20465	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.
3.5.4 Tx SSC Down Spread Range (Port 2, Lane 1)	22465	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt device must be within the specification.
3.5.4 Tx SSC Down Spread Range (Port 2, Lane 1)	10465	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.5.4 Tx SSC Down Spread Range (Port 2, Lane 1)	12465	The spread spectrum clocking (SSC) modulation dynamic range at TP1 of a Thunderbolt host must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 0)	20162	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 0)	22162	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 0)	10162	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 0)	12162	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 1)	20262	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 1)	22262	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 1)	10262	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 1, Lane 1)	12262	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 0)	20362	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 0)	22362	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 0)	10362	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 0)	12362	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 1)	20462	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 1)	22462	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 1)	10462	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4a Tx SSC Down Spread Deviation, Min (Port 2, Lane 1)	12462	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 0)	20163	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 0)	22163	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 0)	10163	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 0)	12163	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 1)	20263	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 1)	22263	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 1)	10263	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 1, Lane 1)	12263	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 0)	20363	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 0)	22363	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 0)	10363	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 0)	12363	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 1)	20463	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 1)	22463	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 1)	10463	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
3.5.4b Tx SSC Down Spread Deviation, Max (Port 2, Lane 1)	12463	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.5 Tx SSC Down Spread Rate (Port 1, Lane 0)	20161	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 1, Lane 0)	22161	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 1, Lane 0)	10161	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 1, Lane 0)	12161	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 1, Lane 1)	20261	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 1, Lane 1)	22261	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 1, Lane 1)	10261	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 1, Lane 1)	12261	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 2, Lane 0)	20361	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 2, Lane 0)	22361	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 2, Lane 0)	10361	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 2, Lane 0)	12361	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 2, Lane 1)	20461	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 2, Lane 1)	22461	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 2, Lane 1)	10461	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.5.5 Tx SSC Down Spread Rate (Port 2, Lane 1)	12461	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 1, Lane 0)	20171	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 1, Lane 0)	22171	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 1, Lane 0)	10171	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.6 Tx SSC Phase Deviation (Port 1, Lane 0)	12171	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 1, Lane 1)	20271	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 1, Lane 1)	22271	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 1, Lane 1)	10271	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 1, Lane 1)	12271	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 2, Lane 0)	20371	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 2, Lane 0)	22371	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 2, Lane 0)	10371	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 2, Lane 0)	12371	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 2, Lane 1)	20471	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 2, Lane 1)	22471	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 2, Lane 1)	10471	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
3.5.6 Tx SSC Phase Deviation (Port 2, Lane 1)	12471	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 1, Lane 0)	20172	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 1, Lane 0)	22172	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 1, Lane 0)	10172	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 1, Lane 0)	12172	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 1, Lane 1)	20272	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 1, Lane 1)	22272	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.6b Tx SSC Phase Slew Rate (Port 1, Lane 1)	10272	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 1, Lane 1)	12272	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 2, Lane 0)	20372	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 2, Lane 0)	22372	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 2, Lane 0)	10372	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 2, Lane 0)	12372	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 2, Lane 1)	20472	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 2, Lane 1)	22472	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 2, Lane 1)	10472	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.6b Tx SSC Phase Slew Rate (Port 2, Lane 1)	12472	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.8 Tx Lane to Lane Skew (Port 1, Lane 0/Lane 1)	20410	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt device must be less than the maximum limit.
3.5.8 Tx Lane to Lane Skew (Port 1, Lane 0/Lane 1)	22410	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt device must be less than the maximum limit.
3.5.8 Tx Lane to Lane Skew (Port 1, Lane 0/Lane 1)	10410	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt host must be less than the maximum limit.
3.5.8 Tx Lane to Lane Skew (Port 1, Lane 0/Lane 1)	12410	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt host must be less than the maximum limit.
3.5.8 Tx Lane to Lane Skew (Port 2, Lane 0/Lane 1)	20430	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt device must be less than the maximum limit.
3.5.8 Tx Lane to Lane Skew (Port 2, Lane 0/Lane 1)	22430	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt device must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.8 Tx Lane to Lane Skew (Port 2, Lane 0/Lane 1)	10430	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt host must be less than the maximum limit.
3.5.8 Tx Lane to Lane Skew (Port 2, Lane 0/Lane 1)	12430	The lane to lane skew between dual transmit signals of the same port group of a Thunderbolt host must be less than the maximum limit.
3.5.8 Tx SSC Slew Rate (Port 1, Lane 0)	20164	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 1, Lane 0)	22164	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 1, Lane 0)	10164	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 1, Lane 0)	12164	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 1, Lane 1)	20264	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 1, Lane 1)	22264	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 1, Lane 1)	10264	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 1, Lane 1)	12264	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 2, Lane 0)	20364	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 2, Lane 0)	22364	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 2, Lane 0)	10364	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 2, Lane 0)	12364	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 2, Lane 1)	20464	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 2, Lane 1)	22464	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt device must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 2, Lane 1)	10464	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.
3.5.8 Tx SSC Slew Rate (Port 2, Lane 1)	12464	The spread spectrum clocking (SSC) slew rate at TP1 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.9a Tx Rise Time (Port 1, Lane 0)	20111	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9a Tx Rise Time (Port 1, Lane 0)	22111	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9a Tx Rise Time (Port 1, Lane 0)	10111	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9a Tx Rise Time (Port 1, Lane 0)	12111	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9a Tx Rise Time (Port 1, Lane 1)	20211	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9a Tx Rise Time (Port 1, Lane 1)	22211	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9a Tx Rise Time (Port 1, Lane 1)	10211	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9a Tx Rise Time (Port 1, Lane 1)	12211	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9a Tx Rise Time (Port 2, Lane 0)	20311	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9a Tx Rise Time (Port 2, Lane 0)	22311	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9a Tx Rise Time (Port 2, Lane 0)	10311	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9a Tx Rise Time (Port 2, Lane 0)	12311	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9a Tx Rise Time (Port 2, Lane 1)	20411	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.9a Tx Rise Time (Port 2, Lane 1)	22411	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9a Tx Rise Time (Port 2, Lane 1)	10411	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9a Tx Rise Time (Port 2, Lane 1)	12411	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 1, Lane 0)	20112	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 1, Lane 0)	22112	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 1, Lane 0)	10112	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 1, Lane 0)	12112	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 1, Lane 1)	20212	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 1, Lane 1)	22212	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 1, Lane 1)	10212	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 1, Lane 1)	12212	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 2, Lane 0)	20312	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 2, Lane 0)	22312	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.5.9b Tx Fall Time (Port 2, Lane 0)	10312	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 2, Lane 0)	12312	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 2, Lane 1)	20412	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 2, Lane 1)	22412	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 2, Lane 1)	10412	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
3.5.9b Tx Fall Time (Port 2, Lane 1)	12412	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.

4 Instruments

The following table shows the instruments used by this application. The name is required by various remote interface methods.

- Instrument Name — The name to use as a parameter in remote interface commands.
- Description — The description of the instrument.

For example, if an application uses an oscilloscope and a pulse generator, then you would expect to see something like this in the table below:

Table 5 Example Instrument Information

Name	Description
scope	The primary oscilloscope.
Pulse	The pulse generator used for Gen 2 tests.

and you would be able to remotely control an instrument using:

```
ARSL syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
arsl -a ipaddress -c "SendScpiCommandCustom 'Command=[scpi
command];Timeout=100;Instrument=pulsegen'"

arsl -a ipaddress -c "SendScpiQueryCustom 'Command=[scpi
query];Timeout=100;Instrument=pulsegen'"


C# syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
SendScpiCommandOptions commandOptions = new SendScpiCommandOptions();
commandOptions.Command = "[scpi command]";
commandOptions.Instrument = "[instrument name]";
commandOptions.Timeout = [timeout];
remoteAte.SendScpiCommand(commandOptions);

SendScpiQueryOptions queryOptions = new SendScpiQueryOptions();
queryOptions.Query = "[scpi query]";
queryOptions.Instrument = "[instrument name]";
```

```
queryOptions.Timeout = [timeout];
remoteAte.SendScpiQuery(queryOptions);
```

Here are the actual instrument names used by this application:

NOTE The file, "InstrumentInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

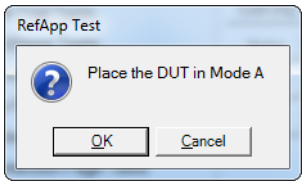
Table 6 Instrument Names

Instrument Name	Description
Infiniium	The primary oscilloscope
JBERTB	N4903B High Performance Serial BERT
JBERTA	N4903A High Performance Serial BERT

5 Message IDs

During the normal course of operation, an application displays multiple message prompts. The application's remote interface exposes a callback capability which enables remote clients to receive the text found in the prompt and to programmatically select the desired response (OK, Cancel, etc.). In order to determine which message is being received, the remote program could parse the message and look for key words. However, because message text is subject to change, a more reliable approach is to use the "message ID" that is attached to the more frequently-seen messages. The following table shows the IDs of the messages that this application may prompt during nominal operation.

For example, if the application may display the following prompt:



then you would expect to see something like this in the table below:

Message	ID	Responses	Usage
DUT mode message	313AEE2F-9EF0-476f-A2EB-29A5C7DE686F	OK=action completed and proceed, Cancel = abort test	App

- Message – A summary of the message in the prompt.
- ID – A unique code that will never change for this prompt, even if the message text changes (assuming the underlying purpose is maintained).
- Responses – The buttons on the prompt and their actions.
- Usage – The scope of the message:
  - "Common" – This message/ID may be used by other apps.

- "App" — This message/ID is unique to this app.
- "<testID>" — This message/ID is unique to this test ID.

A remote client would then structure the code in its message callback handler as shown below to manage message identification:

```
private static void OnSimpleMessage(object sender, MessageEventArgs e)
{
  if (e.ID == "313AEE2F-9EF0-476f-A2EB-29A5C7DE686F")
  {
    // Add code here to set the DUT in Mode A

    e.Response = DialogResult.OK;
  }
}
```

Here are actual message IDs used by this application:

NOTE The file, "MessageInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 7 Message IDs

Message	ID	Responses	Usage
Acq Limit: Can't determine minimum bandwidth	25A86458-151E-413D-B890-FC30CFD5ECAA	OK	Instrument
Activating limit will conflict with existing resutls	31A39751-6019-41de-89DF-59DB239DF978	OK=delete conflicting results, Cancel=cancel activation	Instrument
Already running tests	022467B0-6E08-40eb-B4D4-BBB018FBFBC7	OK	Instrument
App startup aborted	C2B67F67-E5D5-4845-8B63-443781223010	OK	Instrument
Can't set memory depth	FFFF1129-BD83-4318-993E-64C94033CEC4	OK=skip step and continue, Cancel=abort test	Instrument
Channel Setup: Unknown scope channel	CDE944EB-F440-4CB1-AFDC-7596461BCD86	OK	Instrument
Compliance/Debug mode change	9C72A970-8D7D-4b37-9787-48AEEA5DC3F1	OK=change mode, Cancel=abort action	Instrument
Confirmation Required	37437505-160C-4cc8-BA06-093C12994C1E	OK=continue, Cancel=abort test	Instrument
Connection change	879629E6-78FA-4a87-B247-A9DB4F0D7330	Abort=abort run, Retry=connection changed - continue run, Ignore=connection not chagned - continue run	Instrument

Table 7 Message IDs (continued)

Message	ID	Responses	Usage
Debug pause (messages vary)	50B66A97-A6A9-413f-8329-76DFAC492FD6	OK=resume, Cancel=abort run	Instrument
End of run summary	602F9866-F975-42b7-842C-D8447E5E3FCB	OK	Instrument
End of run summary (test aborted)	124580E4-4486-42d4-B908-C6D0FB2AEE93	OK	Instrument
Error during CSV file generation	C88B1C64-8334-4b15-8727-81F5E2BA2ED4	OK	Instrument
Error during app exit	81112706-F720-4787-81D3-B22A9B692B41	OK	Instrument
Expected signal not found	86C74779-322E-4585-A07A-26A2C8FAAC84	Abort=abort test, Retry=retry failed action, Ignore=skip failed step	Instrument
Expected signal not found	7957D5B8-E62D-4224-A7DD-70361E816A43	Retry=retry failed action, Cancel=abort test	Instrument
InfiniiSim: Not available because scope default prevented	B8461A2C-9F5F-4AF3-94C1-DF77080D517A	OK	Instrument
InfiniiSim: Scope doesn't support settings found in project	C9BC2205-8041-448b-AF31-CF602183E989	OK	Instrument
InfiniiSim: Unknown scope channel	4E5ECAF6-867C-47B3-982D-5F07E2090703	OK	Instrument
No test selected	B5D233AD-9EB4-4ac2-A443-A30A13643978	OK	Instrument
PrecisionProbe and InfiniiSim controllers turned off after config change	B4477006-D6D1-4375-9FF7-D8177FFC1BF9	OK	Instrument
PrecisionProbe/PrecisionCable: Not available because scope default prevented	6E60C9F8-8FBF-419C-B70A-B666FBDE3677	OK	Instrument
PrecisionProbe/PrecisionCable: Scope doesn't support settings found in project	2FC3B6FA-E28C-4700-9F46-4ABBA86A0D90	OK	Instrument
PrecisionProbe/PrecisionCable: Switch Controller is enabled	22F46DA8-89AE-4370-A57C-571DCF5BB87E	OK	Instrument
PrecisionProbe/PrecisionCable: Unknown scope channel	6788685B-9E88-47E6-BAE6-862F5BF3C9BA	OK	Instrument
Project loaded as read-only (reason)	98C785F8-D24F-4758-A18D-1CCE61F25371	OK	Instrument

Table 7 Message IDs (continued)

Message	ID	Responses	Usage
Project loaded with errors	58AD7A02-1E63-4d77-BC6C-6EF3E37AAD5B	OK	Instrument
Project not loaded	B2615E9C-5ED7-4db7-AEAF-2BC25C62B656	OK	Instrument
Project save failed (unauthorized access)	89DCC194-6254-4902-AE63-B7CCD12C8B2A	OK	Instrument
Run paused	FE2CF871-6D4A-4080-8FF9-770075590D9F	OK=resume, Cancel=abort run	Instrument
Setting change requires result deletion	8732A3AB-142C-47e5-86EA-DB737F415DDE	OK=delete results; Cancel=abort change	Instrument
Store mode change requires result deletion	884CDFDE-605E-4d04-B8FD-9B181E7FA468	OK=delete results, Cancel=abort change	Instrument
Switch Matrix controller turned off after config change	FC95EBAA-F33F-4eae-90BB-6A6A8F16E2DF	OK	Instrument
Switch Matrix: Auto mode unavailable after config change	6E5589DC-E073-4818-9E8A-782A75898475	OK	Instrument
Switch Matrix: Auto mode unavailable for model, all settings will be reset	F78BD2E2-BF29-42e0-98F8-23B6CE565B08	OK=go auto do reset, Cancel=abort action	Instrument
Switch Matrix: Confirm Auto mode	D5E1A12E-6218-4416-8451-5F9415D924BF	OK=go auto, Cancel=stay manual	Instrument
Switch Matrix: Obsolete items in settings discarded	0C45BD20-E0C2-481e-A3B6-9C1A26C2103A	OK	Instrument
Switch Matrix: Reconnect drivers	047FE44F-B251-49fa-B3C7-5590317230CD	Yes=use saved addresses, No=prompt for new addresses, Cancel=reset all settings	Instrument
Switch Matrix: Remove all InfiniiSim settings	C5560182-73BE-4901-941E-3DAEC9F07B33	OK=remove, Cancel=abort action	Instrument
Switch Matrix: User cancelled settings load	50F3FB70-AA6B-488e-8CFA-62CDA756F746	OK	Instrument
SwitchMatrix: Correction reset due to application route change	95FEA629-3BE1-4288-BA34-426516018B07	OK=Accept new routing, Cancel=Reset switch matrix settings	Instrument
SwitchMatrix: Instrument already connected to another driver	08556148-4D63-4edd-B894-22916F39849A	OK	Instrument
SwitchMatrix: Max num drivers exceeded	7D8994AB-FCC2-4294-87B3-19B972BB6510	OK	Instrument

Table 7 Message IDs (continued)

Message	ID	Responses	Usage
SwitchMatrix: Reset after drive reconnect fail	CF3E93B6-77FA-4FD7-B656-D286BE1C7C75	OK	Instrument
SwitchMatrix: Reset after drive reconnect fail	D298A4B8-F077-49BE-9CB2-AE6C14FB4705	OK	Instrument
SwitchMatrix: Unexpected multi-SPDT module	2723591D-55A9-44F3-9318-B732995D9427	OK	Instrument
SwitchMatrix: Unknown current switch state	ECE6535B-5C1A-4688-9E45-FB255435CC92	OK	Instrument
Unknown EEyeLocation parameter	FCA1C61B-D2EA-4671-AD48-9C080A6C6039	OK	Instrument
Upgrade app to open project	794C6148-ADF4-4b24-895D-74D94B76F8AE	OK	Instrument

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