Keysight D9010ONFC ONFI Test Application

KEYSIGHT TECHNOLOGIES

Methods of Implementation

Notices

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Contents

1 Overview

ONFI Automated Testing—At a Glance 10

Required Equipment and Software 11

Hardware 11
Software 11
Licensing information 11

In This Book 12

See Also 12

2 Installing the Test Application and Licenses

Installing the Test Application 14

Installing the License Key 15

Using Keysight License Manager 5 15
Using Keysight License Manager 6 16

3 Preparing to Take Measurements

Calibrating the Oscilloscope 20

Starting the ONFI Test Application 21

Signal requirements for test availability 23

4 Understanding ONFI Concepts for Measurements

Data Interfaces - Overview 28

Output Slew Rate 30

Input Slew Rate Derating 32

AC Undershoot/Overshoot Requirements 40

DC and Operating Conditions 41

Single-Ended Requirements for Differential DQS Signals 43

VREFQ Tolerance 44

Differential Signaling 45

ONFI Read/Write Separation 46
Threshold Settings 48
Timing Modes & Timing Diagrams 57
Timing Diagrams for NVDDR2/NVDDR3 57
Measuring Timing Parameters to/from Tri-State 61

5 NVDDR2/NVDDR3 Electrical Tests

Setting up the ONFI Test Application to run tests 64
Single-Ended WRITE Cycle Tests for Strobe and Data 65
VSEH(AC) for DQS Plus 65
VSEL(AC) for DQS Plus 67
VSEH(AC) for DQS Minus 68
VSEL(AC) for DQS Minus 69
VIX for Strobe 70
VIH(AC) for DQ 71
VIH(DC) for DQ 72
VIL(AC) for DQ 73
VIL(DC) for DQ 74
Single-Ended READ Cycle Tests for Strobe and Data 75
VOX for Strobe 75
VOH(AC) for DQ 76
VOL(AC) for DQ 77
Single-Ended READ Cycle Tests for RE 78
VOX for RE 78
Single-Ended Command and Address Tests for ALE 79
ALE Overshoot Amplitude 79
ALE Overshoot Area 80
ALE Undershoot Amplitude 81
ALE Undershoot Area 82
Single-Ended Command and Address Tests for CLE 83
CLE Overshoot Amplitude 83
CLE Overshoot Area 84
CLE Undershoot Amplitude 85
CLE Undershoot Area 86
Single-Ended Command and Address Tests for WE 87
WE Overshoot Amplitude 87
WE Overshoot Area 88
WE Undershoot Amplitude 89
WE Undershoot Area 90

Differential WRITE Cycle Tests for Strobe 91
- VIH.diff(AC) for DQS 91
- VIH.diff(DC) for DQS 93
- VIL.diff(AC) for DQS 94
- VIL.diff(DC) for DQS 95

Differential READ Cycle Tests for Strobe 96
- VOH.diff(AC) for DQS 96
- VOL.diff(AC) for DQS 98

6 NVDDR2/NVDDR3 Timing Tests

Setting up the ONFI Test Application to run tests 100

Timing Write Tests 101
- tDQSH 101
- tDQSL 103
- tDS_tight(derate) 105
- tDS_relaxed(derate) 107
- tDH_tight(derate) 109
- tDH_relaxed(derate) 111
- tDS(derate) 113
- tDH(derate) 115
- tDSC(avg) 117
- tDSC(abs) 119
- SRIseR 120
- SRIseF 121
- tDIPW 122
- tWPRE 124
- tWPRE2 125
- tDBS 126
- tCS-Write 127
- tCDQSS 128
- tWPST 129
- tWPSTH 130

Timing Read Tests 131

SROseR 131
SROseF 133
SRORdiff 135
SROFdiff 136
tQH 137
tDQSQ 139
tDVW 141
tQSH 142
tQSL 145
tAC 148
tDQSRE 149
tRC(avg) 150
tRC(abs) 152
tREH(avg) 153
tREH(abs) 155
tRP(avg) 156
tRP(abs) 158
tCR 159
tCS-Read 160
tDBS-Read 161
tRPRE 162
tRPRE2 163
tDQSRH 164
tDQSD 165
tRPST 166
tRPSTH 167

Timing Command and Address Tests 168

tCSD_ALE 168
tCSD_CLE 169
tCALS_CLE 170
tCALH_CLE 171
tCALS_ALE 172
tCALH_ALE 173
tWP 174
tCS 175
tCH 176
tCAS 177
tCAH 178

7 NVDDR2/NVDDR3 Jitter Tests

Setting up the ONFI Test Application to run tests 180

Jitter Tests on Strobe 181
tJITper(DQS) 181
tJITcc(DQS) 184
Jitter Tests on Read Enable 186
tJITper(RE) 186
tJITcc(RE) 189

8 NVDDR2/NVDDR3 Eye-Diagram Tests

Setting up the ONFI Test Application to run tests 192
Read Cycle Tests 193
Eye Diagram for Read DQ 193
Write Cycle Tests 194
Eye Diagram for Write DQ 194

1 Overview

ONFI Automated Testing—At a Glance 10
Required Equipment and Software 11
In This Book 12

KEYSIGHT TECHNOLOGIES

ONFI Automated Testing—At a Glance

The Keysight D9010ONFC ONFI Test Application provides a framework for using Keysight Infiniium Oscilloscope to perform compliance testing on ONFI devices based on ONFI (Joint Electronic Device Engineering Council) specifications. The test application guides you through the process of selecting and configuring tests, making oscilloscope connections, running tests, and evaluating the test results. The Keysight D9010ONFC ONFI Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE **The tests performed by the Keysight D9010ONFC ONFI Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.**

The ONFI test standards and specifications are described in the ONFI document Open NAND Flash Interface Specification Revision 4.2. For more information, refer to the ONFI web site at http://www.ONFI.org.

Required Equipment and Software

In order to run the ONFI automated tests, you need the following equipment and software:

Hardware

- Use one of the following Oscilloscope models. Refer to www.keysight.com for the respective bandwidth ranges.
  - Keysight Infiniium 9000/90000 X-Series or 9000/90000 Series Digital Storage Oscilloscopes
  - Keysight UXR Oscilloscopes
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Precision 3.5 mm BNC to SMA male adapter, Keysight p/n 54855-67604, qty = 2
- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG-316/U or similar, qty = 2, matched length
- Probes or test fixtures
  - E2677A differential solder-in probe head
  - InfiniiMax 116xA or 113xA probe amplifiers
- Keysight also recommends using a second monitor to view the test application.

Software

- The minimum version of Infiniium Oscilloscope Software (see the Keysight D9010ONFC ONFI Test Application Release Notes)
- Keysight D9010ONFC ONFI Test Application software
- Keysight E2688A Serial Data Analysis and Clock Recovery software (for clock recovery)

Licensing information

Refer to the *Data Sheet* pertaining to ONFI Test Application to know about the licenses you must install along with other optional licenses. Visit “http://www.keysight.com/find/D9010ONFC” and in the web page's **Document Library** tab, you may view the associated Data Sheet.

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

The licensing format for Keysight License Manager 6 differs from its predecessors. See “Installing the License Key" on page 15 to see the difference in installing a license key using either of the applications on your machine.

In This Book

This manual describes the tests that are performed by the Keysight D9010ONFC ONFI Test Application in more detail; it contains information from (and refers to) the ONFI specifications.

- Chapter 2, “Installing the Test Application and Licenses” shows how to install and license the automated test application (if it was purchased separately).
- Chapter 3, “Preparing to Take Measurements” describes how to launch the Keysight D9010ONFC ONFI Test Application and gives a brief overview of how it is used.
- Chapter 4, “Understanding ONFI Concepts for Measurements” describes the conceptual information extracted from the ONFI specification with respect to NVDDR2/NVDDR3 SDRAM types.
- Chapter 5, “NVDDR2/NVDDR3 Electrical Tests” describes the Electrical READ and WRITE cycle tests for strobe and data signals.
- Chapter 6, “NVDDR2/NVDDR3 Timing Tests” describes the Timing READ and WRITE cycle tests for strobe, data and read enable signals.
- Chapter 7, “NVDDR2/NVDDR3 Jitter Tests” describes the Jitter tests for strobe and read enable signals.
- Chapter 8, “NVDDR2/NVDDR3 Eye-Diagram Tests” describes the READ and WRITE cycle Eye-Diagram tests for strobe signals.

See Also

The Keysight D9010ONFC ONFI Test Application’s Online Help, which describes:

- Starting the ONFI Test Application
- Creating or Opening a Test Project
- Setting Up the Test Environment
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
- Configuring Automation in the Test Application
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test App

2 Installing the Test Application and Licenses

Installing the Test Application 14
Installing the License Key 15

If you purchased the D9010ONFC ONFI Test Application separate from your Infiniium oscilloscope, you must install the software and license key.

KEYSIGHT TECHNOLOGIES

Installing the Test Application

1. Make sure you have the minimum version of Infiniium Oscilloscope software (see the D9010ONFC release notes). To ensure that you have the minimum version, select **Help > About Infiniium...** from the main menu.
2. To obtain the ONFI Test Application, go to Keysight website: "http://www.keysight.com/find/D9010ONFC".
3. In the web page's **Trials & Licenses** tab, click the **Details and Download** button to view instructions for downloading and installing the application software.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1. Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.
2. Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

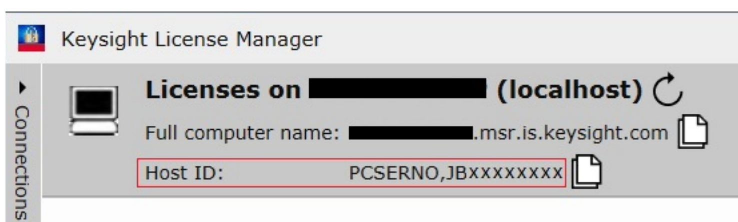

Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1. Save the license files on the machine, where you wish to run the Test Application and its features.
2. Launch Keysight License Manager.
3. From the configuration menu, use one of the options to install each license file.

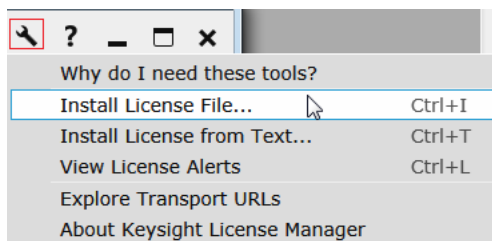

Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1 Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

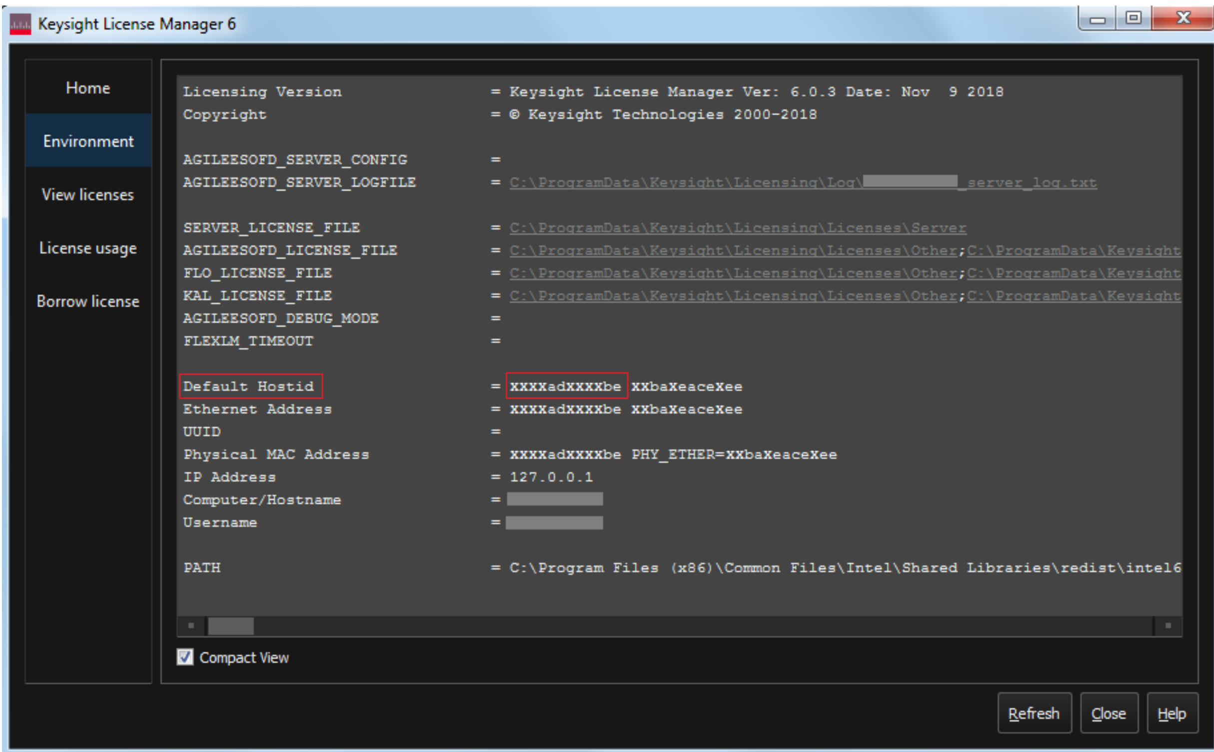

Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.
2 Launch Keysight License Manager 6.
3 From the Home tab, use one of the options to install each license file.

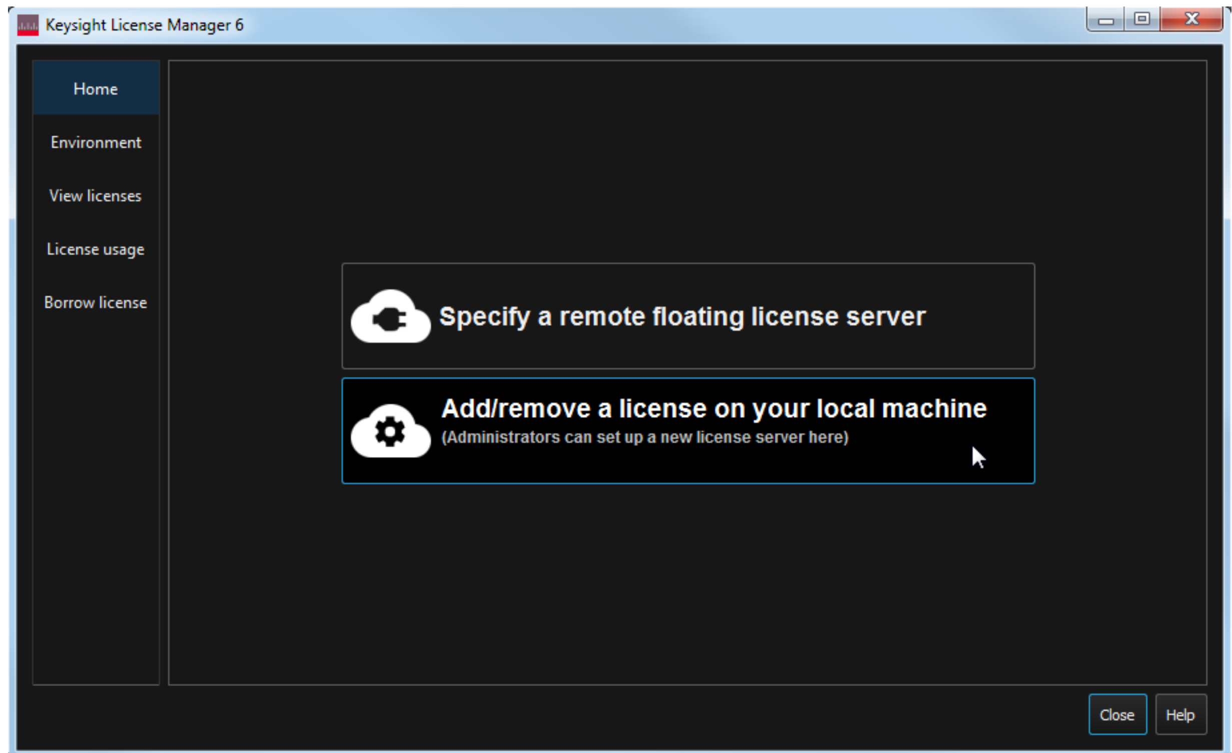

Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

3 Preparing to Take Measurements

Calibrating the Oscilloscope 20
Starting the ONFI Test Application 21
Signal requirements for test availability 23

Before running the automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this application. After the oscilloscope and probe have been calibrated, you are ready to start the ONFI Test Application and perform the measurements.

Calibrating the Oscilloscope

If you have not already calibrated the oscilloscope, refer to the *User Guide* for the respective Oscilloscope you are using.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE If you switch cables between channels or other Oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the ONFI Test Application

1 Ensure that the ONFI Device Under Test (DUT) is operating and set to desired test modes. To start the ONFI Test Application: From the Infiniium Oscilloscope's main menu, select **Analyze > Automated Test Apps > D9010ONFC ONFI Test App**.

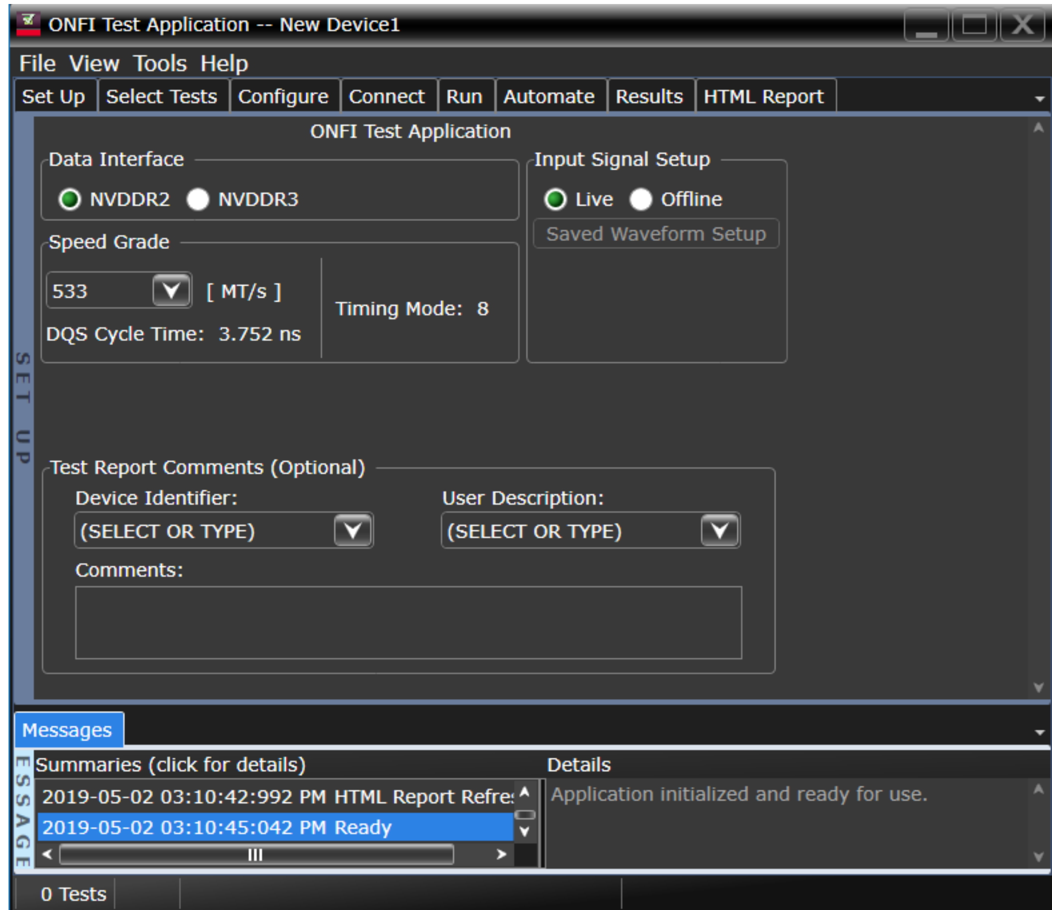

Figure 5 ONFI Test Application Main Window

To understand the functionality of the various features in the user interface of the Test Application, refer to the *Keysight D9010ONFC ONFI Test Application Online Help* available in the Help menu.

The task flow pane and the tabs in the main pane show the steps you take in running the automated tests:

Set Up	Lets you identify and set up the test environment, including information about the device under test. The Test App includes relevant information in the final HTML report.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (for example, channels used in test, voltage levels, etc.).
Connect	Shows you how to connect the oscilloscope to the device under test for the tests that are to be run.
Run	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE

1. In the **Configure** tab, the values for all such Configuration parameters that are Oscilloscope-dependent, will correspond to the Oscilloscope Model (DSOs or UXRs), where you are running the Test Application.

2. When you close the ONFI Test Application, each channel's probe is configured as single-ended or differential depending on the last ONFI test that was run.

Signal requirements for test availability

Table 1 displays a comprehensive list of the tests that correspond to one or more signals in the ONFI Test Application.

Table 1 List of tests and corresponding test signals

NVDDR2/NVDDR3 Tests	Signals based on test definition	Signals required to perform test
VSEH(AC) for DQS Plus	DQS_t	DQS_t, DQ
VSEL(AC) for DQS Plus	DQS_t	DQS_t, DQ
VSEH(AC) for DQS Minus	DQS_c	DQS_c, DQ
VSEL(AC) for DQS Minus	DQS_c	DQS_c, DQ
VIX for Strobe	DQS_t, DQS_c	DQS_t, DQS_c, DQ
VIH(AC) for DQ	DQ	DQS, DQ
VIH(DC) for DQ	DQ	DQS, DQ
VIL(AC) for DQ	DQ	DQS, DQ
VIL(DC) for DQ	DQ	DQS, DQ
VOX for Strobe	DQS_t, DQS_c	DQS_t, DQS_c, DQ
VOH(AC) for DQ	DQ	DQS, DQ
VOL(AC) for DQ	DQ	DQS, DQ
VOX for RE	RE_t, RE_c	DQS, DQ, RE_t, RE_c
ALE Overshoot Amplitude	ALE	ALE
ALE Overshoot Area	ALE	ALE
ALE Undershoot Amplitude	ALE	ALE
ALE Undershoot Area	ALE	ALE
CLE Overshoot Amplitude	CLE	CLE
CLE Overshoot Area	CLE	CLE
CLE Undershoot Amplitude	CLE	CLE
CLE Undershoot Area	CLE	CLE
WE Overshoot Amplitude	WE	WE
WE Overshoot Area	WE	WE
WE Undershoot Amplitude	WE	WE
WE Undershoot Area	WE	WE
VIH.diff(AC) for DQS	DQS	DQS, DQ
VIH.diff(DC) for DQS	DQS	DQS, DQ
VIL.diff(AC) for DQS	DQS	DQS, DQ
VIL.diff(DC) for DQS	DQS	DQS, DQ

NVDDR2/NVDDR3 Tests	Signals based on test definition	Signals required to perform test
VOH.diff(AC) for DQS	DQS	DQS, DQ
VOL.diff(AC) for DQS	DQS	DQS, DQ
tDQSH	DQS	DQS, DQ
tDQSL	DQS	DQS, DQ
tDS_tight(derate)	DQ	DQS, DQ
tDS_relaxed(derate)	DQ	DQS, DQ
tDH_tight(derate)	DQ	DQS, DQ
tDH_relaxed(derate)	DQ	DQS, DQ
tDS(derate)	DQ	DQS, DQ
tDH(derate)	DQ	DQS, DQ
tDSC(avg)	DQS	DQS, DQ
tDSC(abs)	DQS	DQS, DQ
SRIseR	DQ	DQS, DQ
SRIseF	DQ	DQS, DQ
tDIPW	DQ	DQS, DQ
tWPRE	DQS	DQS, DQ
tWPRE2	DQS	DQS, DQ
tDBS	DQS, CE	DQS, DQ, CE
tCS-Write	DQS, CE	DQS, DQ, CE
tCDQSS	DQS	DQS, DQ
tWPST	DQS, CLE	DQS, DQ, CLE, WE
tWPSTH	CLE, WE	DQS, DQ, CLE, WE
SROseR	DQ	DQS, DQ
SROseF	DQ	DQS, DQ
SRORdiff	DQS	DQS, DQ
SROFdiff	DQS	DQS, DQ
tQH	DQS, DQ	DQS, DQ
tDQSQ	DQS, DQ	DQS, DQ
tDVW	DQ	DQS, DQ
tQSH	DQS	DQS, DQ
tQSL	DQS	DQS, DQ
tAC	DQ, RE	DQS, DQ, RE
tDQSRE	DQS, RE	DQS, RE
tRC(avg)	RE	DQ, DQS, RE

NVDDR2/NVDDR3 Tests	Signals based on test definition	Signals required to perform test
tRC(abs)	RE	DQ, DQS, RE
tREH(avg)	RE	DQ, DQS, RE
tREH(abs)	RE	DQ, DQS, RE
tRP(avg)	RE	DQ, DQS, RE
tRP(abs)	RE	DQ, DQS, RE
tCR	CE, RE	CE, RE, DQS, DQ
tCS-Read	CE, RE	CE, RE, DQS, DQ
tDBS-Read	CE, RE	CE, RE, DQS, DQ
tRPRE	RE	DQ, DQS, RE
tRPRE2	RE	DQ, DQS, RE
tDQSRH	DQS, RE	DQS, DQ, RE
tDQSD	DQS, RE	DQS, DQ, RE
tRPST	CE, RE	CE, RE, DQ, DQS
tRPSTH	CE, RE	CE, RE, DQ, DQS
tCSD_ALE	CE, ALE	CE, ALE
tCSD_CLE	CE, CLE	CE, CLE
tCALS_CLE	CLE, WE	CLE, WE
tCALH_CLE	CLE, WE	CLE, WE
tCALS_ALE	ALE, WE	ALE, WE
tCALH_ALE	ALE, WE	ALE, WE
tWP	WE	WE
tCS	CE, WE	CE, WE
tCH	CE, WE	CE, WE
tCAS	Command/Address DQ	WE, Command/Address DQ
tCAH	Command/Address DQ	WE, Command/Address DQ
tJITper(DQS)	DQS	DQS, DQ
tJITcc(DQS)	DQS	DQS, DQ
tJITper(RE)	RE	DQS, DQ, RE
tJITcc(RE)	RE	DQS, DQ, RE
Eye Diagram for Read DQ	DQ	DQS, DQ
Eye Diagram for Write DQ	DQ	DQS, DQ

4 Understanding ONFI Concepts for Measurements

Data Interfaces - Overview / 28
Output Slew Rate / 30
Input Slew Rate Derating / 32
AC Undershoot/Overshoot Requirements / 40
DC and Operating Conditions / 41
Single-Ended Requirements for Differential DQS Signals / 43
VREFQ Tolerance / 44
Differential Signaling / 45
ONFI Read/Write Separation / 46
Timing Modes & Timing Diagrams / 57

Before running the ONFI Test Application automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this ONFI Test Application. After the oscilloscope and probe have been calibrated, you are ready to start the Keysight D9010ONFC ONFI Test Application and perform the measurements.

Data Interfaces - Overview

The current version of the Keysight D9010ONFC ONFI Test Application supports compliance testing of the NV-DDR2 and NV-DDR3 data interfaces.

The NV-DDR2 data interface is double data rate (DDR), that is, it uses the DDR protocol and includes additional capabilities for scaling speed like on-die termination and differential signaling. The NV-DDR3 data interface includes all NV-DDR2 features, but operates at VccQ=1.2V.

The maximum speed of operation for NVDDR2 is 800 MT/s whereas for NVDDR3, maximum speed is 1600 MT/s. If VccQ = 1.8V on power-up, the DUT shall operate in NVDDR2 data interface timing mode 0. If VccQ=1.2V on power up, the DUT shall operate in NVDDR3 data interface timing mode 0.

NOTE

The Keysight D9010ONFC ONFI Test Application Methods of Implementation automatically changes the default values for Vcc and VccQ according to the data interface you select under the **Set Up** tab.

Table 2 describes the signal functionality for NVDDR2/NVDDR3 data interfaces.

Table 2 Signal Assignment for NVDDR2/NVDDR3

Symbol	Type	Description
NVDDR2 / NVDDR3		
ALE	Input	Address Latch Enable
CE_n	Input	Chip Enable
CLE	Input	Command Latch Enable
DQ[7:0]	I/O	Data inputs/outputs
DQS / DQS_t	I/O	Data Strobe
DQS_c	I/O	Data Strobe Complement
RE_n / RE_t	Input	Read Enable
RE_c	Input	Read Enable Complement
WE_n	Input	Write Enable
WP_n	Input	Write Protect
R/B_n	Output	Ready / Busy_n
ZQ	NA	ZQ Calibration

The testing conditions that shall be used to verify compliance with a particular timing mode for devices that support driver strength settings are listed in Table 3. This includes all devices that support the NVDDR2 or NVDDR3 data interfaces.

Table 3 Testing Conditions for Devices that Support Driver Strength Settings

Parameter	NVDDR2/NVDDR3 Single-ended	NVDDR2/NVDDR3 Differential
Positive input transition	VIL (DC) to VIH (AC)	VILdiff (DC) max to VIHdiff (AC) min
Negative input transition	VIH (DC) to VIL (AC)	VIHdiff (DC) min to VILdiff (AC) max
Minimum input slew rate	tIS = 1.0 V/ns	tIS = 2.0 V/ns
Input timing levels	VccQ / 2 if internal VREFQ or external VREFQ	crosspoint
Output timing levels	Vtt	crosspoint

Output Slew Rate

The testing conditions used for output slew rate testing are specified in Table 4. Output slew rate is verified by design and characterization; it may not be subject to production test. The minimum slew rate is the minimum of the rising edge and the falling edge slew rate. The maximum slew rate is the maximum of the rising edge and the falling edge slew rate. Slew rates are measured under normal SSO conditions, with half of the DQ signals per data byte driving high and half of the DQ signals per data byte driving low. The output slew rate is measured per individual DQ signal. The differential parameters are used when the DQS signal is configured to operate as a differential signal. The NV-DDR2 data interface uses the same voltage levels defined in the SSTL_18 standard.

Table 4 Testing Conditions for Output Slew Rate

Parameter	NVDDR2/NVDDR3 Single-Ended	NVDDR2/NVDDR3 Differential
VOL(AC)	Vtt - (VccQ * 0.10)	-
VOH(AC)	Vtt + (VccQ * 0.10)	-
VOLdiff(AC)	-	-0.2 * VccQ
VOHdiff(AC)	-	0.2 * VccQ
Positive output transition	VOL (AC) to VOH (AC)	VOLdiff(AC) to VOHdiff(AC)
Negative output transition	VOH (AC) to VOL (AC)	VOHdiff(AC) to VOLdiff(AC)
tRISE[1]	Time during rising edge from VOL(AC) to VOH(AC)	-
tFALL[1]	Time during falling edge from VOH(AC) to VOL(AC)	-
tRISEdiff[2]	-	Time during rising edge from VOLdiff(AC) to VOHdiff(AC)
tFALLdiff[2]	-	Time during falling edge from VOHdiff(AC) to VOLdiff(AC)
Output slew rate rising edge	[VOH(AC) – VOL(AC)] / tRISE	[VOHdiff(AC) – VOLdiff(AC)] / tRISEdiff
Output slew rate falling edge	[VOH(AC) – VOL(AC)] / tFALL	[VOHdiff(AC) – VOLdiff(AC)] / tFALLdiff

1: Refer to Figure 6

2: Refer to Figure 7

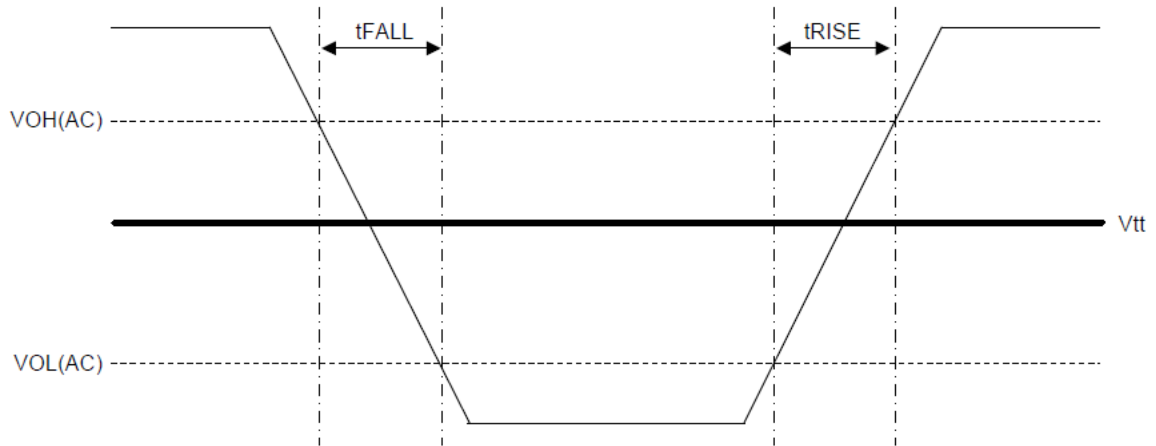

Figure 6 tRISE and tFALL Definition for Output Slew Rate, NV-DDR2/3 (single-ended)

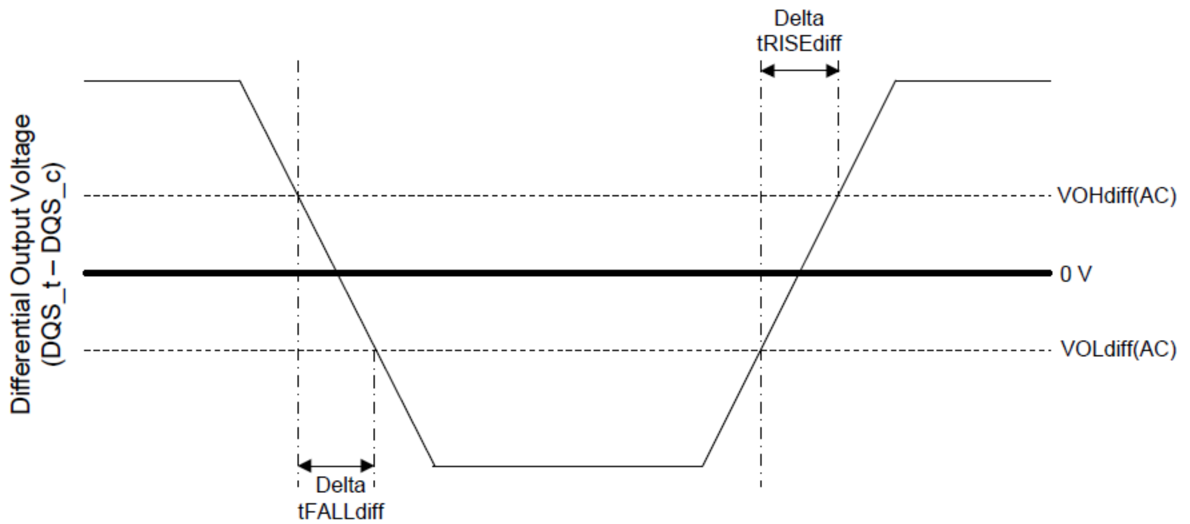

Figure 7 tRISEdiff and tFALLdiff Definition for Output Slew Rate, NV-DDR2/3 (differential)

The output slew rate matching ratio is specified in Table 5. The output slew rate mismatch is determined by the ratio of fast slew rate and slow slew rate. If the rising edge is faster than the falling edge, divide the rising slew rate by the falling slew rate. If the falling is faster than the rising edge, divide the falling slew rate by the rising slew rate.

Table 5 Output Slew Rate Matching Ratio

Parameter	Min.	Max.
Output Slew Rate Matching Ratio, without ZQ Calibration	1.0	1.4
Output Slew Rate Matching Ratio, with ZQ Calibration	1.0	1.3

Input Slew Rate Derating

The minimum and maximum input slew rate requirements that the device shall comply with for the NV-DDR2 and NV-DDR3 data interface are defined in Table 6 for all timing modes. If the input slew rate falls below the minimum value, derating shall be applied.

Table 6 Maximum and minimum input slew rate

Description	Single-Ended	Differential	Unit
Input Slew Rate (min)	1.0	2.0	V/ns
Input Slew Rate (max)	4.5	9.0	V/ns

For DQ signals when used for input, the total data setup time (tDS) and data hold time (tDH) required is calculated by adding a derating value to the tDS and tDH values indicated for the timing mode. To calculate the total data setup time, tDS is incremented by the appropriate Δset derating value. To calculate the total data hold time, tDH is incremented by the appropriate Δhld derating value.

Figure 8 provides the NV-DDR2 derating values when differential DQS (DQS_t/DQS_c) is used.

DQ V/ns	DQS_t/DQS_c Slew Rate Derating VIH/L(AC) = 250 mV, VIH/L(DC) = 125 mV																							
	12		6		4		3		2		1.8		1.6		1.4		1.2		1		0.8		0.6	
	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld
6	-26	-26	-21	-21	-16	-16																		
3	-26	-26	-21	-21	-16	-16	-10	-10																
2			-21	-21	-16	-16	-10	-10	0	0														
1.5					-16	-16	-10	-10	0	0	7	7												
1					-16	-16	-10	-10	0	0	7	7	16	16										
0.9							3	3	14	14	21	21	30	30	41	41								
0.8									31	31	38	38	47	47	58	58	73	73						
0.7											61	61	69	69	80	80	95	95	116	116				
0.6													99	99	110	110	125	125	146	146	176	176		
0.5															152	152	167	167	188	188	218	218	269	269
0.4																	229	229	250	250	282	282	333	333
0.3																			355	355	385	385	436	436

Figure 8 NV-DDR2 Input Slew Rate Derating Values for DQ and differential DQS

Figure 9 provides the NV-DDR2 derating values when single-ended DQS is used.

DQ V/ns	DQS Slew Rate Derating VIH/L(AC) = 250 mV, VIH/L(DC) = 125 mV																									
	6		5		3		2		1.5		1		0.9		0.8		0.7		0.6		0.5		0.4		0.3	
	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld
6	0	0	0	0																						
5	0	0	0	0	0	0																				
4			0	0	0	0	0	0																		
3			0	0	0	0	0	0	0	0																
2					0	0	0	0	0	0	0	0														
1.5					0	0	0	0	0	0	0	0	14	14												
1							0	0	0	0	0	0	14	14	31	31										
0.9									14	14	14	14	28	28	45	45	67	67								
0.8											31	31	45	45	63	63	85	85	115	115						
0.7													67	67	85	85	107	107	137	137	179	179				
0.6															115	115	137	137	167	167	208	208	271	271		
0.5																	179	179	208	208	250	250	313	313	418	418
0.4																			271	271	313	313	375	375	480	480
0.3																					418	418	480	480	594	594

Figure 9 NV-DDR2 Input Slew Rate Derating Values for DQ and single-ended DQS

Figure 10 provides the NV-DDR3 derating values when differential DQS (DQS_t/DQS_c) is used.

DQ V/ns	DQS_t/DQS_c Slew Rate Derating VIH/L(AC) = 150 mV, VIH/L(DC) = 100 mV																							
	12		6		4		3		2		1.8		1.6		1.4		1.2		1		0.8		0.6	
	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld
6	−63	−31	−33	−17	-25	-13																		
3	−63	−31	−33	−17	−25	−13	-17	-8																
2			−33	−17	−25	−13	−17	−8	0	0														
1.5					−25	−13	−17	−8	0	0	6	6												
1					−25	−13	−17	−8	0	0	6	6	13	13										
0.9							−6	3	11	11	17	17	24	24	33	33								
0.8									25	25	31	31	38	38	46	46	58	58						
0.7											48	48	55	55	64	64	76	76	93	93				
0.6													79	79	88	88	100	100	117	117	142	142		
0.5															121	121	133	133	150	150	175	175	217	217
0.4																	183	183	200	200	225	225	267	267
0.3																			283	283	308	308	350	350

Figure 10 NV-DDR3 Input Slew Rate Derating Values for DQ and differential DQS

Figure 11 provides the NV-DDR3 derating values when single-ended DQS is used.

DQ V/ns	DQS Slew Rate Derating VIH/L(AC) = 150 mV, VIH/L(DC) = 100 mV																									
	6		5		3		2		1.5		1		0.9		0.8		0.7		0.6		0.5		0.4		0.3	
	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld	Δ set	Δ hld
6	0	0	0	0	0	0																				
5	0	0	0	0	0	0	0	0																		
3	0	0	0	0	0	0	0	0	0	0																
2			0	0	0	0	0	0	0	0	0	0														
1.5					0	0	0	0	0	0	0	0	11	11												
1							0	0	0	0	0	0	11	11	25	25										
0.9									11	11	11	11	22	22	36	36	54	54								
0.8											25	25	36	36	50	50	68	68	92	92						
0.7													54	54	68	68	86	86	110	110	143	143				
0.6															92	92	110	110	133	133	167	167	217	217		
0.5																	143	143	167	167	200	200	250	250	333	333
0.4																			217	217	250	250	300	300	383	383
0.3																					333	333	383	383	467	467

Figure 11 NV-DDR3 Input Slew Rate Derating Values for DQ and single-ended DQS

NOTE

Shaded areas in each figure above indicate input slew rate combinations that are not supported. For slew rates not explicitly listed in Figures 8 to 11, the derating values should be obtained by linear interpolation.

For NVDDR3, slew rates below 0.4V/ns are not supported for 1066/1200 MT/s operation and slew rates below 1.0V/ns are not supported for >1200MT/s operation.

Table 7 provides the NV-DDR3 derating value when the input timing is measured as a Tsu+Thd window.

Table 7 NV-DDR3 Input Slew Rate Derating Values for DQ Window

DQ Slew Rate	ΔSetup + Hold
≥1.0 V/ns	0 ps
0.9 V/ns	22 ps
0.8 V/ns	50 ps
0.7 V/ns	86 ps
0.6 V/ns	133 ps
0.5 V/ns	200 ps
0.4 V/ns	300 ps

The input differential DQS slew rate measurement is defined in Table 8 and represented pictorially in Figure 12.

Table 8 Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (DQS_t - DQS_c)	VILdiff(DC)	VIHdiff(DC)	[VIHdiff(DC) - VILdiff(DC)] / Delta $t_{RISEdiff}$
Differential input slew rate for falling edge (DQS_t - DQS_c)	VIHdiff(DC)	VILdiff(DC)	[VIHdiff(DC) - VILdiff(DC)] / Delta $t_{FALLdiff}$

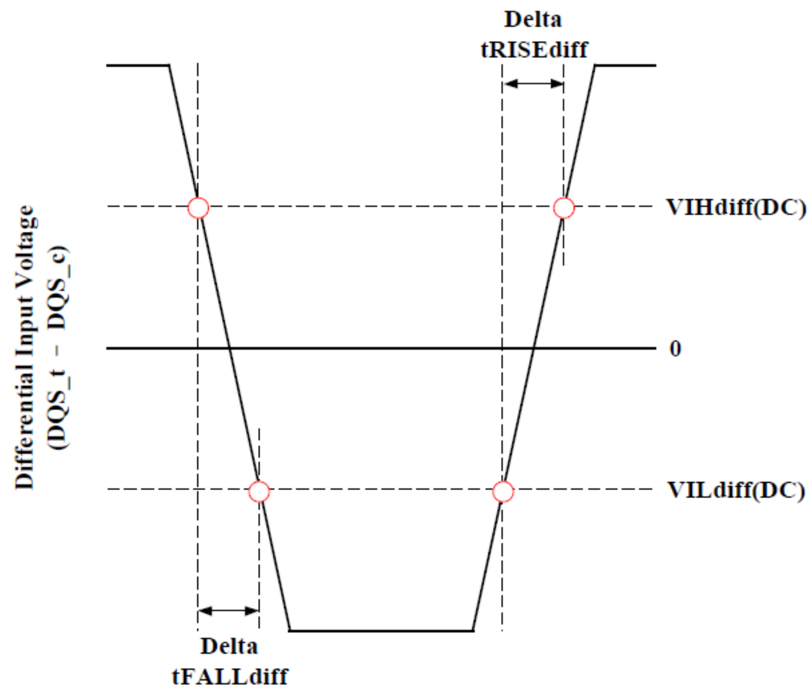

Figure 12 Differential Input Slew Rate Definition for DQS_t, DQS_c

The setup nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREFQ(DC) and the first crossing of VIH(AC) min. The setup nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREFQ(DC) and the first crossing of VIL(AC) max.

If the actual signal is always earlier than the nominal slew rate line between the shaded ‘VREFQ(DC) to AC region’, the derating value uses the nominal slew rate shown in Figure 13.

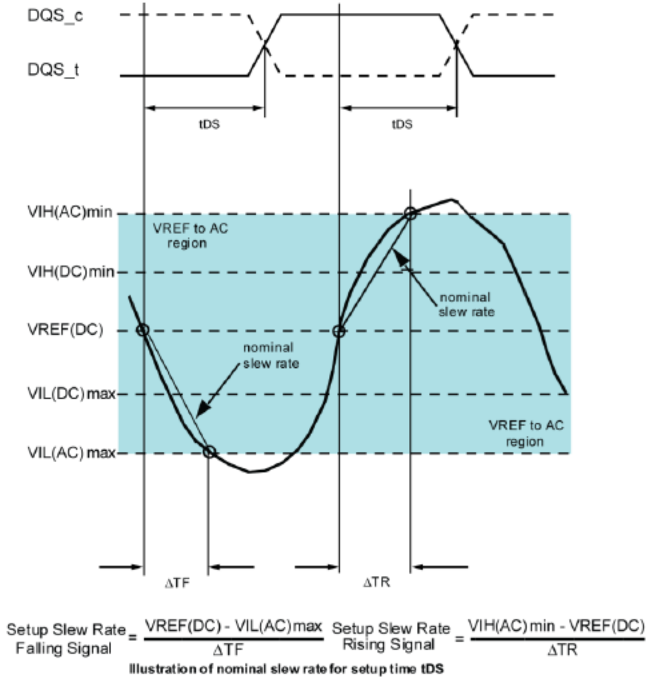

Figure 13 Nominal Slew Rate for Data Setup Time (tDS)

If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREFQ(DC) to AC region', the derating value uses the slew rate of a tangent line to the actual signal from the AC level to the DC level shown in Figure 14.

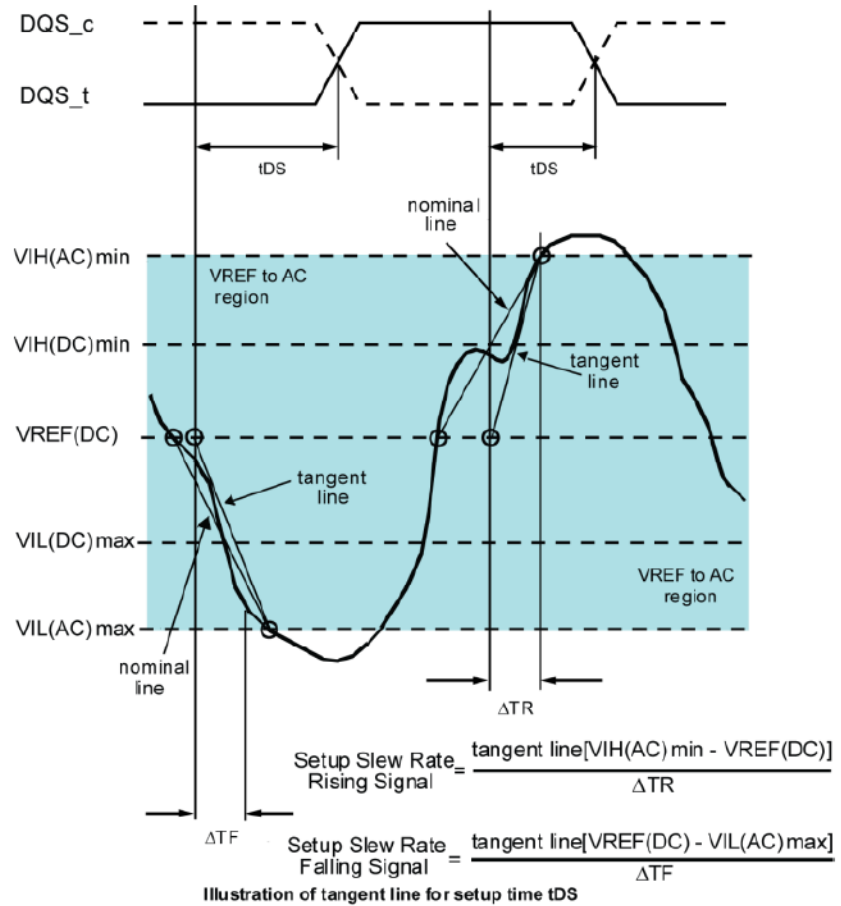

Figure 14 Tangent Line for Data Setup Time (tDS)

The hold nominal slew rate for a rising signal is defined as the slew rate between the first crossing of VIL(DC) max and the first crossing of VREFQ(DC). The hold nominal slew rate for a falling signal is defined as the slew rate between the first crossing of VIH(DC) min and the first crossing of VREFQ(DC).

If the actual signal is always later than the nominal slew rate line between shaded 'DC to VREFQ(DC) region', the derating value uses the nominal slew rate shown in Figure 15.

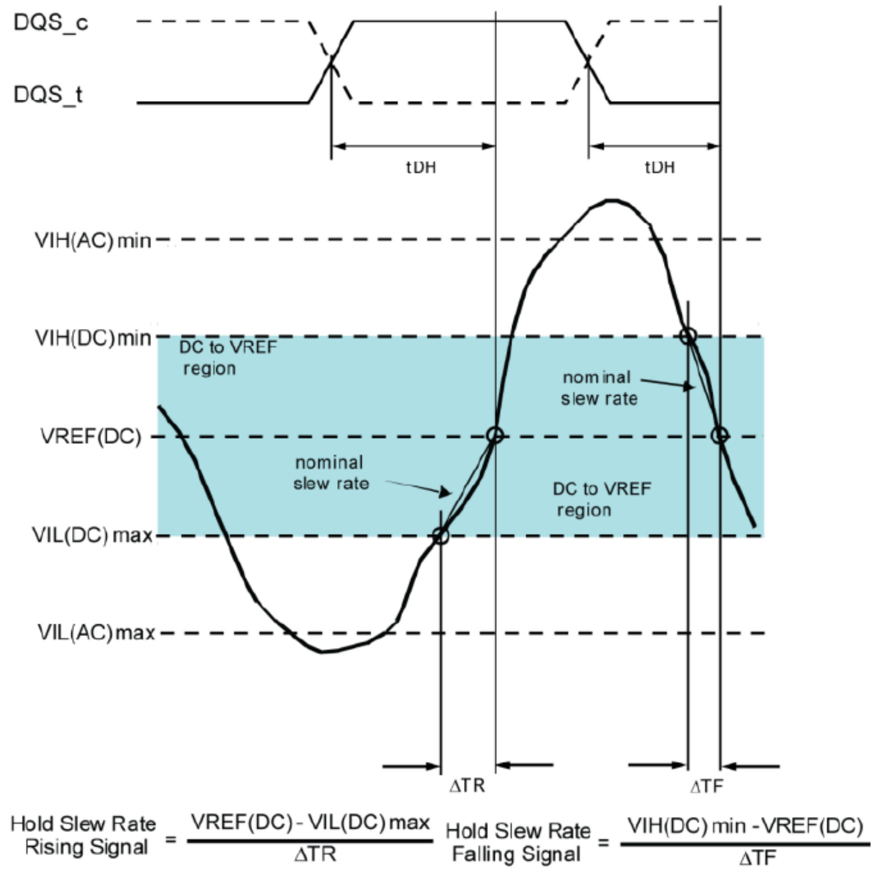

Figure 15 Nominal Slew Rate for Data Hold Time (tDH)

If the actual signal is earlier than the nominal slew rate line anywhere between the shaded 'DC to VREFQ(DC) region', the derating value uses the slew rate of a tangent line to the actual signal from the DC level to the VREFQ(DC) level shown in Figure 16.

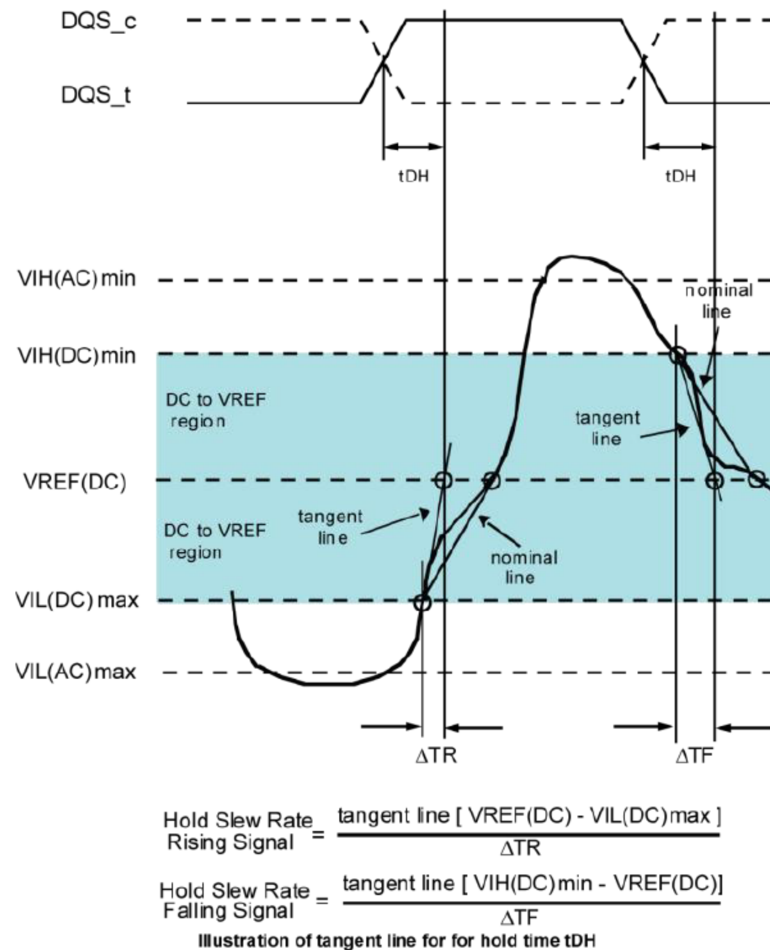

Figure 16 Tangent Line for Data Hold Time (tDH)

If the tangent line is used for derating, the setup and hold values shall be derated from where the tangent line crosses VREFQ(DC), not the actual signal (refer to Figure 14 and Figure 16).

AC Undershoot/Overshoot Requirements

The device may have AC overshoot or undershoot from VccQ and VssQ levels. Table 9 and Table 10 define the maximum values that the AC overshoot or undershoot may attain. The NV-DDR2 values apply for 1.8V VccQ level. The NV-DDR3 values apply for only 1.2V VccQ level. The maximum amplitude allowed for the overshoot area is 1 V for the NV-DDR2 data interfaces and timing modes. The maximum amplitude allowed for the overshoot area is 0.35 V for the NV-DDR3 data interface and timing modes. The maximum amplitude allowed for the undershoot area is 1 V for the NV-DDR2 data interfaces and timing modes. The maximum amplitude allowed for the undershoot area is 0.35 V for the NV-DDR3 data interface and timing modes.

The maximum overshoot area above VccQ and the maximum undershoot area below VssQ is symmetric and varies depending on timing mode, as shown in Table 9 and Table 10. These values apply to the maximum data signaling frequency for a given timing mode. If the data signaling frequency for maximum overshoot or undershoot conditions is less than the selected timing mode, the values for the applicable slower timing mode may be used.

Table 9 AC Overshoot/Undershoot Maximum Values for NVDDR2

Timing Mode	ALE, CLE, WE_n
0-10	3 V-ns

Table 10 AC Overshoot/Undershoot Maximum Values for NVDDR3

Timing Mode	ALE, CLE, WE_n
0-15	3 V-ns

The parameters described in Table 9 and Table 10 are pictorially represented in Figure 17.

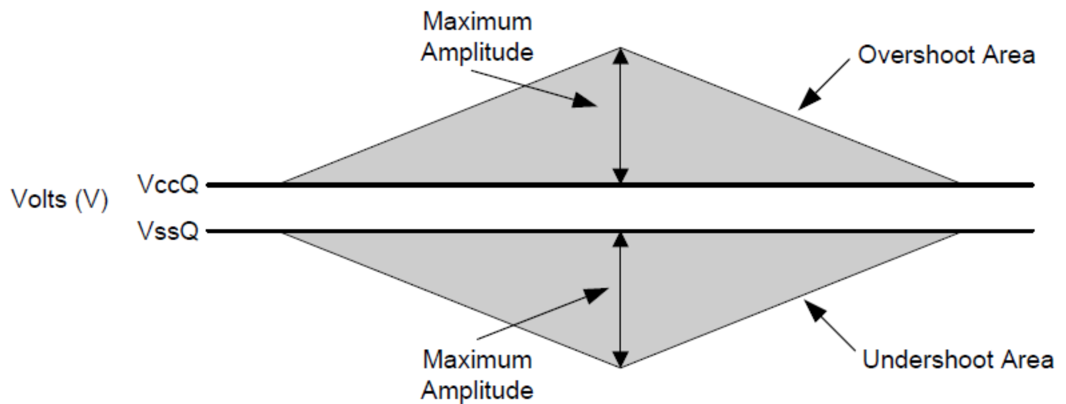

Figure 17 Overshoot/Undershoot Diagram

DC and Operating Conditions

DC signal specifications apply to the CLK, DQ[7:0], DQS, ALE, CLE, and W/R_n signals and only when using the NV-DDR2, or NV-DDR3 data interfaces. For all other signals in NV-DDR2 or NV-DDR3, the AC signal specification shall be met. For signals where DC signal specifications apply, the transition times are measured between VIL (DC) and VIH (AC) for rising input signals and between VIH (DC) and VIL (AC) for falling input signals. The receiver will effectively switch as a result of the signal crossing the AC input level and remain in that state as long as the signal does not ring back above DC input LOW level or below DC input HIGH level.

The parameters in Table 11 and Table 12 apply to power-on default values in the device.

Table 11 DC and Operating Conditions for VccQ of 1.8V (NV-DDR2), measured on VccQ rail

Parameter	Symbol	Min.	Max.	Units
DC Input high voltage	VIH(DC)	VREFQ + 125	VccQ + 300	mV
AC Input high voltage	VIH(AC)	VREFQ + 250	(Note 1)	mV
DC Input low voltage	VIL(DC)	-300	VREFQ - 125	mV
AC Input low voltage	VIL(AC)	(Note 1)	VREFQ - 125	mV
DC Input high voltage (CE_n, WP_n)	VIH(DC)	VccQ * 0.7	VccQ + 300	mV
AC Input high voltage (CE_n, WP_n)	VIH(AC)	VccQ * 0.8	(Note 1)	mV
DC Input low voltage (CE_n, WP_n)	VIL(DC)	-300	VccQ * 0.3	mV
AC Input low voltage (CE_n, WP_n)	VIL(AC)	(Note 1)	VccQ * 0.2	mV

Note 1: Refer to section 2.11 of the ONFI specification version 4.2 for AC Overshoot and Undershoot requirements.

Table 12 DC and Operating Conditions for VccQ of 1.2V (NV-DDR3), measured on VccQ rail

Parameter	Symbol	Min.	Max.	Units
DC Input high voltage	VIH(DC)	VREFQ + 100	VccQ	mV
AC Input high voltage	VIH(AC)	VREFQ + 150	(Note 1)	mV
DC Input low voltage	VIL(DC)	VssQ	VREFQ - 100	mV
AC Input low voltage	VIL(AC)	(Note 1)	VREFQ - 150	mV
DC Input high voltage (CE_n, WP_n)	VIH(DC)	VccQ * 0.7	VccQ	mV
AC Input high voltage (CE_n, WP_n)	VIH(AC)	VccQ * 0.8	(Note 1)	mV
DC Input low voltage (CE_n, WP_n)	VIL(DC)	VssQ	VccQ * 0.3	mV
AC Input low voltage (CE_n, WP_n)	VIL(AC)	(Note 1)	VccQ * 0.2	mV

Note 1: Refer to section 2.11 of the ONFI specification version 4.2 for AC Overshoot and Undershoot requirements.

The differential AC and DC input levels are defined in Table 13. These levels are used to calculate differential signal slew rate, refer to section 4.13 of the ONFI specification version 4.2.

Table 13 Differential DC and AC Input Levels

Parameter	Symbol	Min.	Max.	Units
Differential Input high	VIHdiff (DC)	2 * [VIH(DC) - VREFQ]	(Note 1)	V
Differential Input low	VILdiff (DC)	(Note 1)	2 * [VIL(DC) - VREFQ]	V
Differential Input high AC	VIHdiff (AC)	2 * [VIH(AC) - VREFQ]	(Note 1)	V
Differential Input low AC	VILdiff (AC)	(Note 1)	2 * [VIL(AC) - VREFQ]	V

Note 1: These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) must be within the respective limits [VIH(DC) max, VIL (DC) min] for single-ended signals as well as the limitations for overshoot and undershoot.

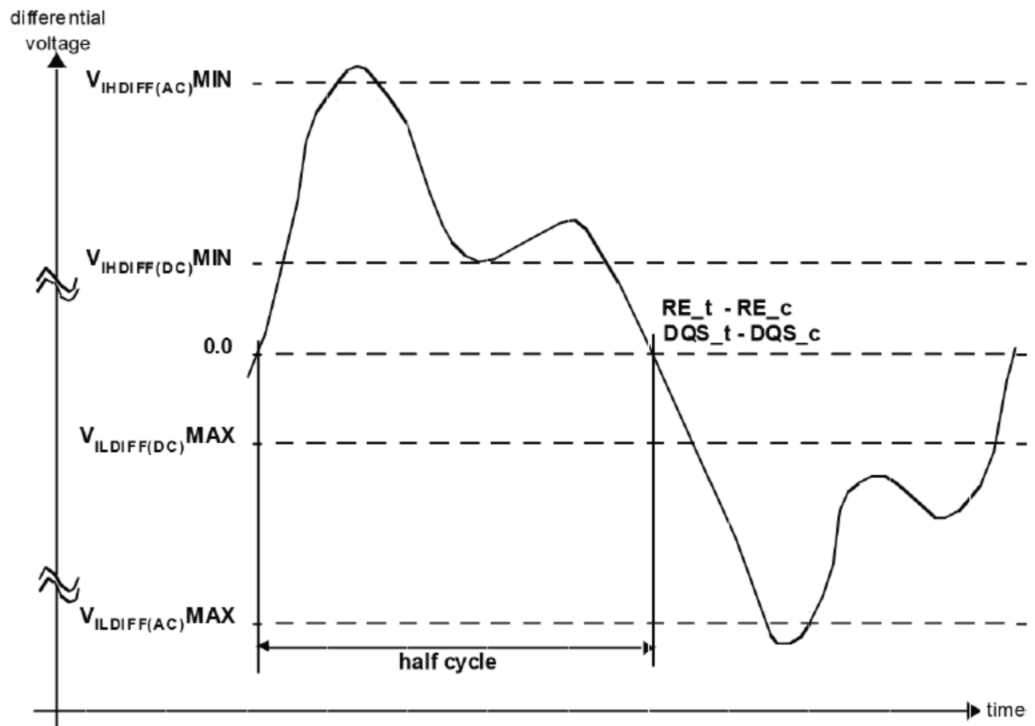

Figure 18 Definition of Differential AC Swing

Single-Ended Requirements for Differential DQS Signals

Each individual component of a differential DQS signal, that is, DQS_t or DQS_c, shall comply with the requirements of single-ended signals. DQS_t or DQS_c shall meet VSEH(AC)min / VSEL(AC)max in every half-cycle preceding and following a valid transition.

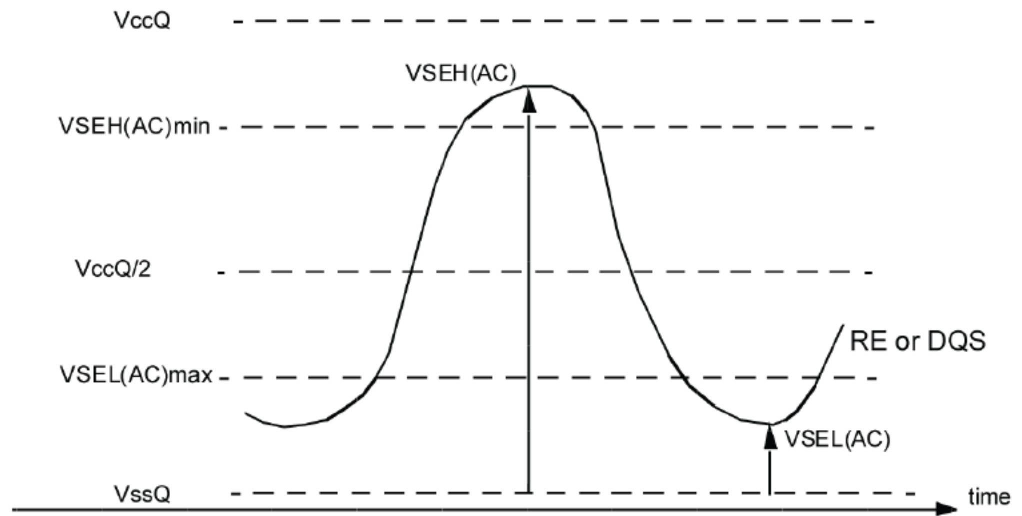

Figure 19 Single-Ended Requirements for Differential DQS Signals

While the requirements for DQ signal and control signals (such as ALE, CLE) are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VccQ/2, which is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals, the requirement to reach VSEL(AC)max and VSEH(AC)min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 14 Single-Ended Levels for RE_t, DQS_t, RE_c, and DQS_c

Parameter	Symbol	Min.	Max.	Units
NVDDR2 Single-Ended high-level	VSEH(AC)	(VccQ / 2) + 0.250	(Note 1)	V
NVDDR2 Single-Ended high-level	VSEL(AC)	(Note 1)	(VccQ / 2) - 0.250	V
NVDDR3 Single-Ended low-level	VSEH(AC)	(VccQ / 2) + 0.150	(Note 1)	V
NVDDR3 Single-Ended low-level	VSEL(AC)	(Note 1)	(VccQ / 2) - 0.150	V

Note 1: These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) must be within the respective limits [VIH(DC) max, VIL (DC) min] for single-ended signals as well as the limitations for overshoot and undershoot.

VREFQ Tolerance

The DC-tolerance limits and AC-noise limits for the reference voltage VREFQ are illustrated in Figure 20. It shows a valid reference voltage VREFQ(t) as a function of time.

VREFQ(DC) is the linear average of VREFQ(t) over a long period of time (for example, 1 sec) and is specified as a fraction of the linear average of VccQ, also measured over a long period of time (for example, 1 sec). This average shall meet the minimum/maximum requirements defined in . VREFQ(t) may temporarily deviate from VREFQ(DC) by no more than ±1% VccQ.

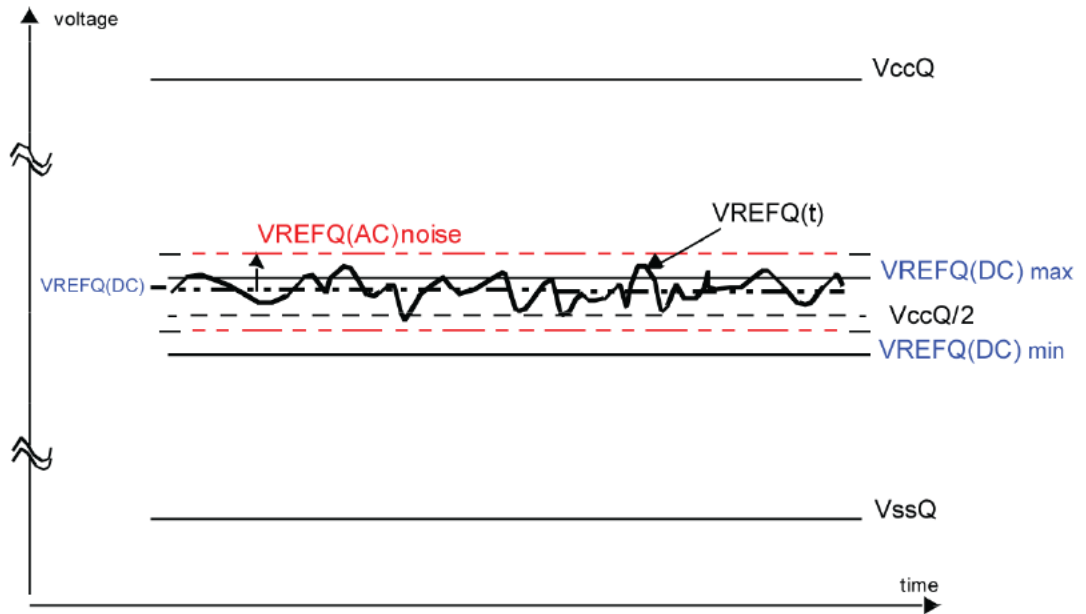

Figure 20 Illustration of VREFQ tolerance and VREFQ(AC)-noise limits

Table 15 VREFQ Specification

Parameter	Symbol	Min.	Max.	Units
Reference Voltage	VREFQ(DC)	0.49 * VccQ	0.51 * VccQ	V

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREFQ.

This clarifies that the setup/hold specification and derating values must include time and voltage associated with VREFQ AC-noise. Timing and voltage effects due to AC-noise on VREFQ up to the specified limit (±1% VccQ) are included in timings and their associated deratings. During any transaction, if the device induces VREFQ noise that is greater than 20 MHz and causes a VREFQ violation, the device shall still meet specifications.

Differential Signaling

Differential signaling may be used to improve signal integrity through enhanced noise immunity. The DUT may support differential RE_n and/or differential DQS signaling.

The differential AC input parameters are specified in Table 16 and Table 17. VIX(AC) indicates the voltage at which differential input signals shall cross. The typical value of VIX(AC) is expected to be 0.5 x VccQ of the transmitting device. VIX(AC) is expected to track variations in VccQ.

Table 16 Differential AC Input Parameters for NVDDR2

Parameter	Symbol	Min.	Max.	Unit
AC differential input cross-point voltage relative to VccQ/2	VIX(AC)	0.50*VccQ - 175	0.50*VccQ + 175	mV

Table 17 Differential AC Input Parameters for NVDDR3

Parameter	Symbol	Min.	Max.	Unit
AC differential input cross-point voltage relative to VccQ/2	VIX(AC)	0.50*VccQ - 120	0.50*VccQ + 120	mV

The differential AC output parameters are specified in Table 18 and Table 19. VOX(AC) indicates the voltage at which differential output signals shall cross.

The typical value of VOX(AC) is expected to be about 0.5 x VccQ of the transmitting device and VOX(AC) is expected to track variations of VccQ. VOX(AC) is measured under normal SSO conditions, with half of the DQ signals per data byte driving high and half of the DQ signals per data byte driving low.

Table 18 Differential AC Output Parameters without ZQ calibration

Parameter	Symbol	Min.	Max.	Unit
AC differential output cross-point voltage	VOX(AC)	0.50*VccQ - 200	0.50*VccQ + 200	mV

Table 19 Differential AC Output Parameters with ZQ calibration

Parameter	Symbol	Min.	Max.	Unit
AC differential output cross-point voltage	VOX(AC)	0.50*VccQ - 150	0.50*VccQ + 150	mV

ONFI Read/Write Separation

Most of the tests must be run on specific Read burst or Write burst region. Therefore, it becomes essential to separate read and write bursts. The Keysight D9010ONFC ONFI Test Application uses the DQS-DQ Phase Difference Burst Triggering Method for Read/Write Separation. This method uses phase difference between DQS and DQ to differentiate between Read and Write.

Figure 21 shows flowchart depicting the process of read and write separation.

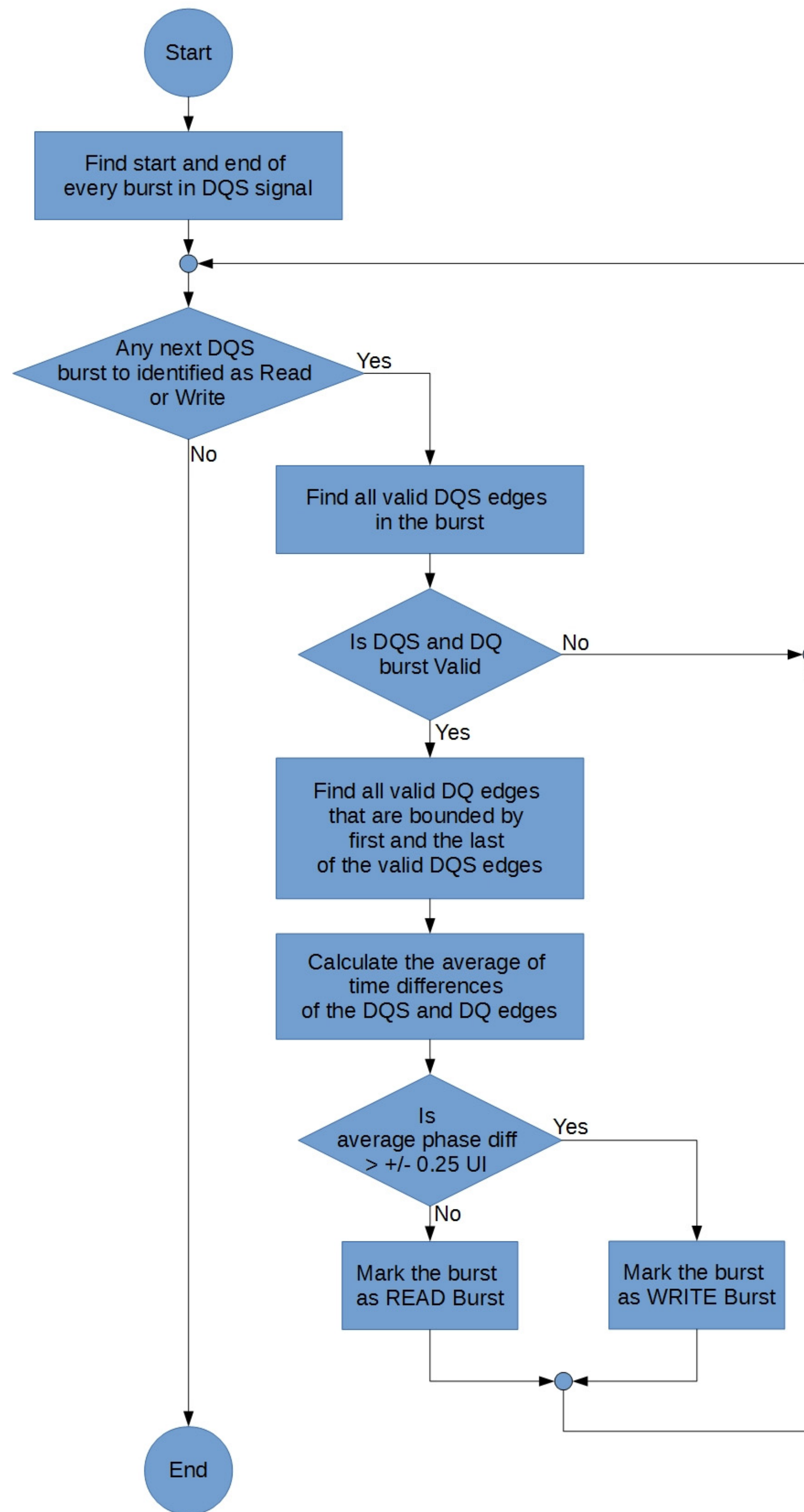

Figure 21 Flowchart depicting DQS-DQ Phase Difference

NOTE

A DQS burst is considered valid when the first edge has more than 2.5 UI of spacing from the start of the signal and the last edge must have more than 2.0 UI spacing towards the end of the signal.

A DQ burst is considered valid if at least one transition occurs. A valid transition must be at a minimum of 250mV.

Threshold Settings

The Keysight D9010ONFC ONFI Test Application consists of two groups of threshold settings in the Configure tab:

- Reade/Write Separation Threshold Settings

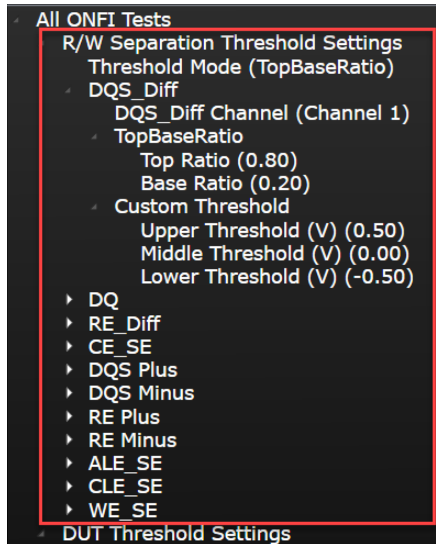

Figure 22 Read/Write Separation Threshold Settings under Configure tab

- DUT Threshold Settings divided into General Settings and Signal Measurement Threshold Settings

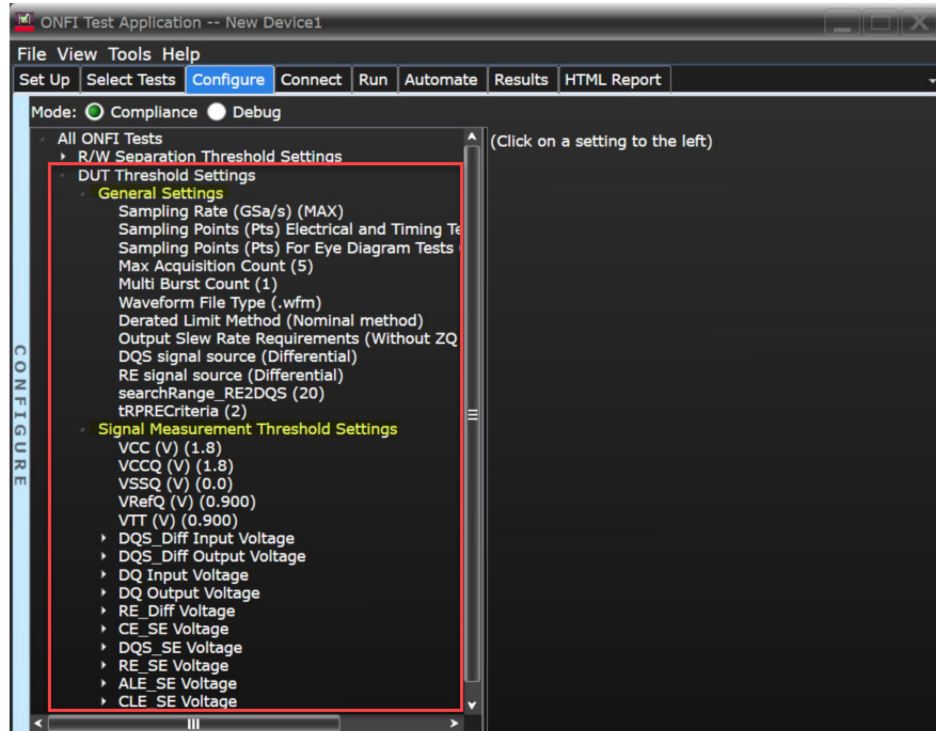

Figure 23 DUT Threshold Settings

Tests that require Read/Write Separation

- Electrical Tests
  - Single-Ended Signals
    - WRITE cycle tests
    - READ cycle tests
  - Differential Signals
    - WRITE cycle tests
    - READ cycle tests
- Timing Tests
  - WRITE cycle tests
  - READ cycle tests
- Jitter Tests
- Eye Diagram Tests

Both Read/Write Separation Threshold Settings and Signal Measurement Threshold Settings affect the test runs on the category of tests listed above.

Basic process flow for tests that require Read/Write Separation

Refer to the block diagram shown in Figure 24 to understand the process flow of tests that require Read/Write Separation:

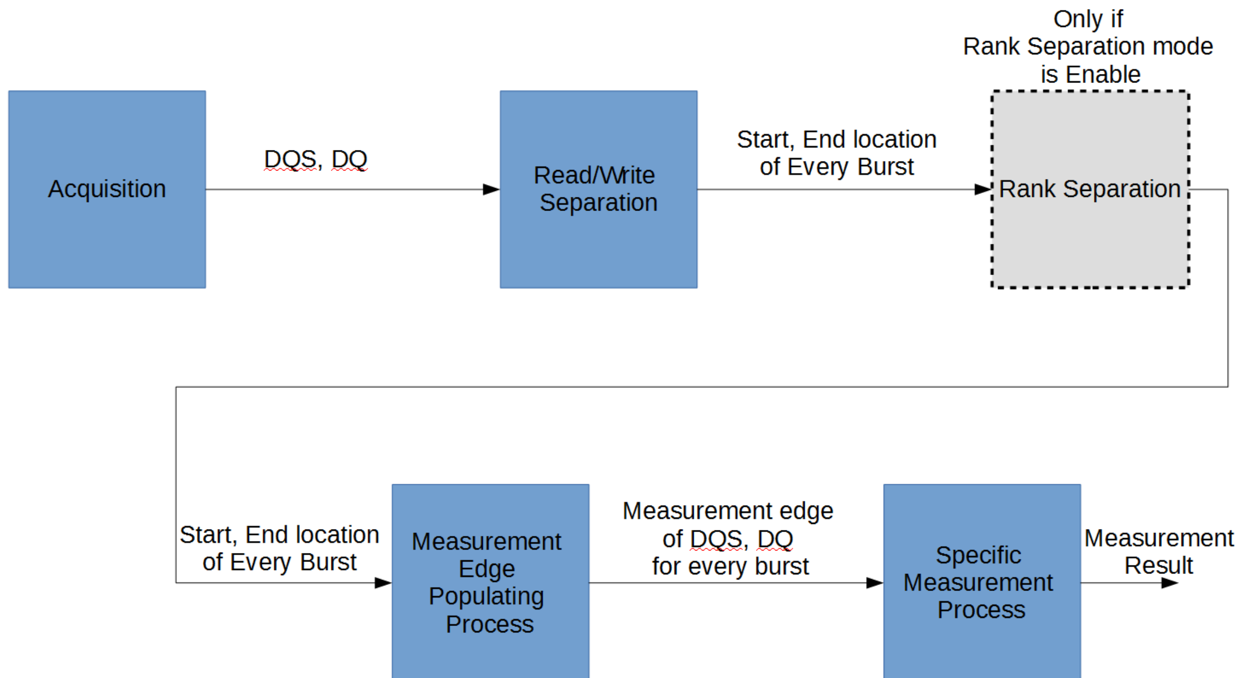

Figure 24 Process flow for tests requiring Read/Write Separation

Each threshold setting has a separate impact on each block in the process flow shown in Figure 24. Table 20 gives a better understanding about whether or not the threshold settings impacts a certain block in the process flow.

Table 20 Impact of Threshold Settings on the Process Flow

Threshold Settings	Acquisition	Read/Write Separation	Rank Separation	Measurement Edge Populating Process	Specific Measurement Process
Read/Write Separation Threshold Settings	No Impact	Impacts	No Impact	No Impact	No Impact
Signal Measurement Threshold Settings	No Impact	No Impact	No Impact	Impacts	Impacts

In a nutshell, Table 20 indicates that Read/Write Separation Threshold Settings affect the Read/Write Separation block only and the Signal Measurement Threshold Settings affect the Measurement Edge Populating Process and Specific Measurement Process blocks.

The objective of using Read/Write Separation Threshold Settings is to define the upper, middle and lower threshold settings on DQS and DQ signals for Read/Write Separation so as to produce a series of bursts. In other words, the correct configuration for Read/Write Separation Threshold Settings yields number of Bursts detected, as shown in Figure 25.

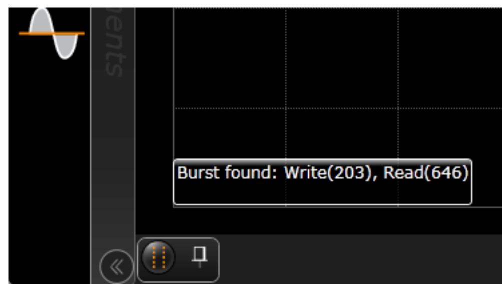

Figure 25 Burst detected for correct Read/Write Separation Threshold Settings

While the signal may have actual bursts, an incorrect configuration for Burst Trigger Threshold Settings does not yield any burst, as shown in Figure 26.

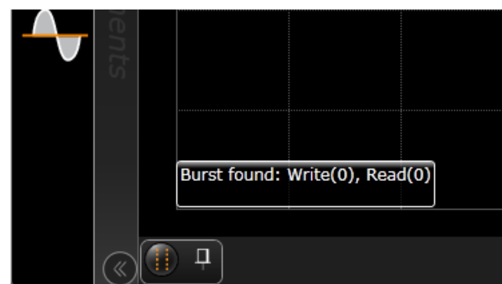

Figure 26 Burst not detected for incorrect Read/Write Separation Threshold Settings

The Read/Write Separation Threshold Settings consists of two modes, namely, TopBase Ratio and Custom Threshold. Figure 27 shows the appearance of the Threshold Mode configuration variable under the Configure tab when TopBaseRatio mode is selected. Figure 31 shows the appearance of the Threshold Mode configuration variable under the Configure tab when Custom Threshold mode is selected.

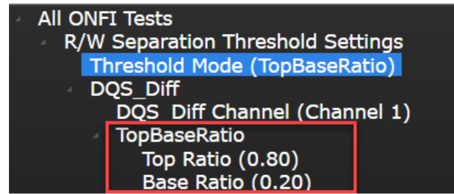

Figure 27 TopBase Ratio mode under Reade/Write Separation Threshold Settings

TopBase Ratio mode In the TopBase Ratio mode, the Compliance Test Application performs VTop and VBase measurements on the DQS and DQ signals. Further, the application calculates the threshold using the equations:

For DQS signals:

$UpperThreshold_{DQS} = TopRatio_{DQS} \times [(VTop_{DQS} - VBase_{DQS}) + VBase_{DQS}]$

$LowerThreshold_{DQS} = BaseRatio_{DQS} \times [(VTop_{DQS} - VBase_{DQS}) + VBase_{DQS}]$

$MiddleThreshold_{DQS} = 0.5 \times (UpperThreshold_{DQS} + LowerThreshold_{DQS})$

For DQ signals:

$UpperThreshold_{DQ} = TopRatio_{DQ} \times [(VTop_{DQ} - VBase_{DQ}) + VBase_{DQ}]$

$LowerThreshold_{DQ} = BaseRatio_{DQ} \times [(VTop_{DQ} - VBase_{DQ}) + VBase_{DQ}]$

$MiddleThreshold_{DQ} = 0.5 \times (UpperThreshold_{DQ} + LowerThreshold_{DQ})$

The TopBase Ratio mode is useful because you do not have to manually evaluate the threshold levels of the signals, which otherwise, may be time consuming. However, in order for this mode to function properly, you must ensure that the following requirements are met:

1 The sufficient amplitude for DQS (Typical minimum range is from 200mV to -200mV. Preferred range is from 400mV to -400mV).
2 The sufficient amplitude for DQ (Typical minimum value is the 200mVpp center at Compliance Vref/Vcent. Preferred value is the 400mVpp center at Compliance Vref/Vcent).
3 The amplitude for Read and Write must be approximately the same, within 20% tolerance.
4 The High Impedance (Idle) level is around the middle level of the burst. If that level is at a higher or lower level than the burst amplitude (as shown in Figure 28), TopBase Ratio mode may not be effective.

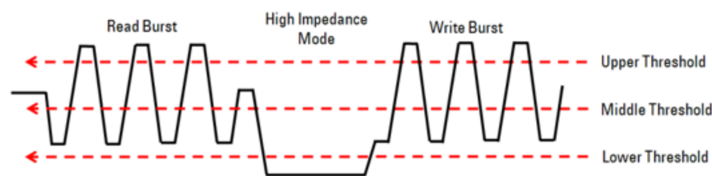

Figure 28 High Impedance (Idle) Level

5 The voltage across High Impedance (Idle) Levels should not exceed the burst amplitude by more than 10%.

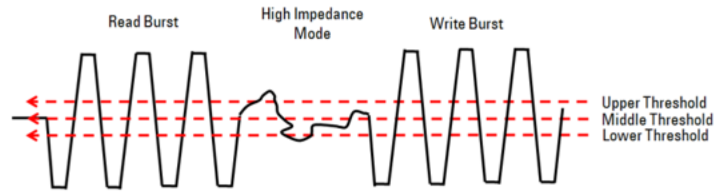

Figure 29 Voltage across High Impedance (Idle) Level

6 Ringing after the burst must be small; preferably within 10% of the burst amplitude.

Figure 30 shows an ideal signal with TopBase Ratio mode set for Burst Trigger Threshold Settings.

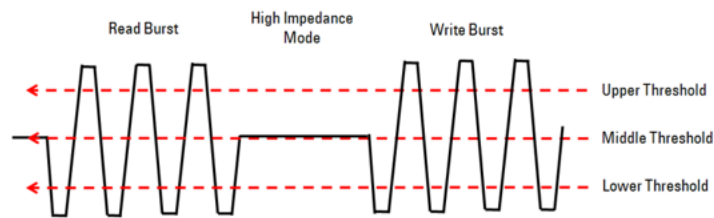

Figure 30 Sample of an ideal signal for TopBase Ratio mode

In case there is an actual burst on the signal but no burst is detected under TopBase Ratio mode of the Burst Trigger Threshold Settings, it indicates that any one of the six conditions defined above have not been met. Therefore, Keysight recommends implementing the Custom Threshold mode in Read/Write Separation Threshold Settings.

Custom Threshold mode Custom Threshold mode relies on your inputs to define the threshold levels of the signals, specially for such signals where applying any algorithm becomes challenging.

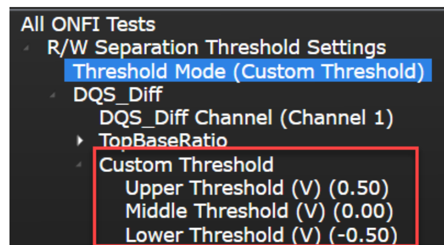

Figure 31 Custom Threshold mode under Read/Write Separation Threshold Settings

In order to implement this mode, you must manually define the upper, middle and lower threshold levels for each Channel according to the configuration value that you have entered.

To understand the advantage of using Custom Threshold mode, let us consider two cases:

1 Non-Ideal High Impedance Voltage – In the signal shown in Figure 32, the amplitude of the high impedance voltage is below the Read and Write amplitude. In such a situation, when the Compliance Test Application automatically determines the appropriate threshold level using the TopBase Ratio mode, the high impedance voltage complicates the algorithm within the application. The upper, middle and lower threshold levels, which are calculated under the TopBase Ratio mode, do not meet the requirements for valid Read and Write bursts. Hence, the

application is unable to determine any valid Read or Write bursts. Eventually, the application is unable to perform any measurements or the measurements are erroneous.

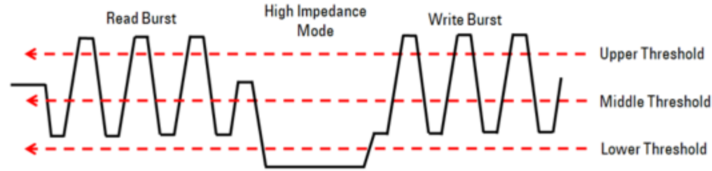

Figure 32 Signal with a non-ideal high impedance voltage amplitude

To avoid such a situation, use the Custom Threshold mode to re-define the Trigger threshold levels that enables the Compliance Test Application to trigger on both Read and Write bursts.

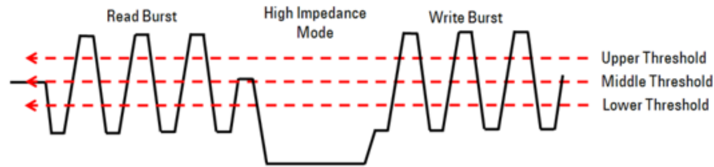

Figure 33 Signal with custom threshold levels defined

2 Different Amplitudes of Read and Write Bursts — In the signal shown in Figure 34, the amplitude of the Read burst is significantly higher than that of the Write burst. In this situation, the Compliance Test Application uses the TopBase Ratio mode to automatically determine the upper, middle and lower threshold levels according to the VTop and VBase measurements performed on the actual signal. With the calculated threshold levels, the application triggers on only the Read burst because the edge meets the threshold condition. However, it does not trigger on the Write burst. Therefore, when the application runs the Write cycle tests, it is unable to find the required Write signals. Eventually, the application performs invalid or erroneous measurements. Note that there may be signals where the amplitude of the Write burst is significantly higher than that of the Read burst. In such cases, the application is unable to find the required Read signals when running tests.

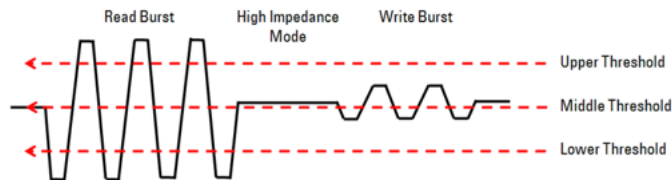

Figure 34 Signal with a non-ideal high impedance voltage amplitude

To avoid such a situation, use the Custom Threshold mode to re-define the Trigger threshold levels that enables the Compliance Test Application to trigger on both Read and Write bursts.

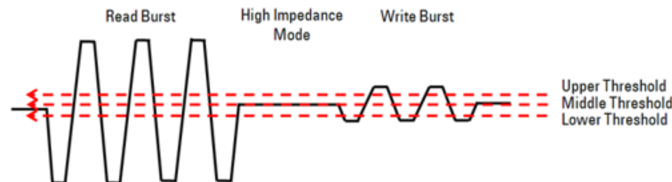

Figure 35 Signal with custom threshold levels defined

Signal Measurement Threshold Settings

For tests that require Read/Write Separation, the Compliance Test Application uses some of the configuration done under Signal Measurement Threshold Settings as the threshold to define the measurement edge, which is used further for specific measurements.

Figure 36 to Figure 37 show the configuration that is used to define the edge threshold for:

1 Differential DQS signal (Write Burst)

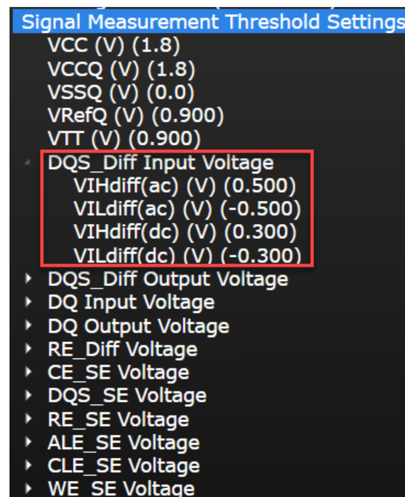

Figure 36 Signal Measurement Threshold Settings for Differential DQS signal (Write Burst)

2 Differential DQS signal (Read Burst)

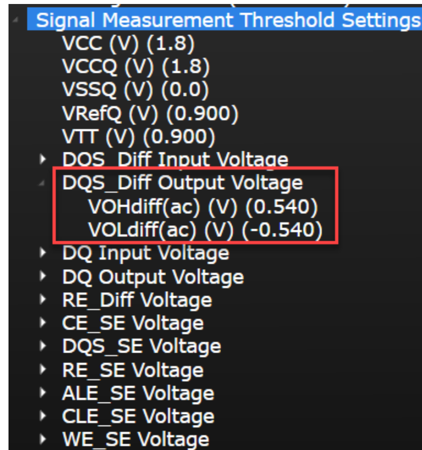

Figure 37 Signal Measurement Threshold Settings for Differential DQS signal (Read Burst)

Following examples describe the dependency of certain tests on the configuration variables:

- Example 1: tDQSH (Write Burst; DQS and DQ signal)

The test procedure for tDQSH states:

1 Acquire and split the read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising and falling DQS crossings in the specified burst.
4 tDQSH is the time starting from a rising edge of the DQS and ending at the following falling edge.
5 Collect all values of the tDQSH measured.
6 Determine the worst result from the set of tDQSH measured.

After identifying the target burst in step 2 of the procedure, it is required that the measurement edge be populated in step 3. Therefore, the configuration variables that defines the measurement edge in step 3 are:

- VIHdiff(ac)
- VILdiff(ac)
- VIHdiff(dc)
- VILdiff(dc)

The middle cross-point level of differential DQS is 0V. Notice that in this case, VIHdiff is considered instead of VOHdiff, as this test involves the Write burst.

Besides, the configuration for DQ signal is also used to check the validity of the burst. If the DQ transition is unable to meet the threshold settings listed below, that burst is considered invalid and is not considered or used for measurements, even if the DQS edge is valid.

- VIH(ac)
- VIL(ac)
- VIH(dc)
- VIL(dc)
- VRefQ

Timing Modes & Timing Diagrams

For the NVDDR2 and NVDDR3 timing modes, the testing conditions defined in Table 3 must be fulfilled. For speeds faster than 200 MT/s, the timing parameters are verified using the optimum drive strength, differential signaling for both RE_n (RE_t/RE_c) and DQS (DQS_t/DQS_c) signals, and external VREFQ. For speeds faster than 533 MT/s, the timing parameters are verified with ZQ calibration performed. For speeds faster than 200 MT/s, you may use alternate drive strength settings, single-ended signaling, and/or internal VREFQ; customized according to your requirements.

For more information about Timing Modes, refer to *Section 4.18.3* of the *ONFI specification rev. 4.2*.

Timing Diagrams for NVDDR2/NVDDR3

The NV-DDR2 and NV-DDR3 timing diagrams show differential (complementary) signaling being used (RE_t/RE_c and DQS_t/DQS_c). Differential signaling is optional. RE_n and RE_t are the same signal; RE_c is not used when differential signaling is disabled. DQS and DQS_t are the same signal; DQS_c is not used when differential signaling is disabled.

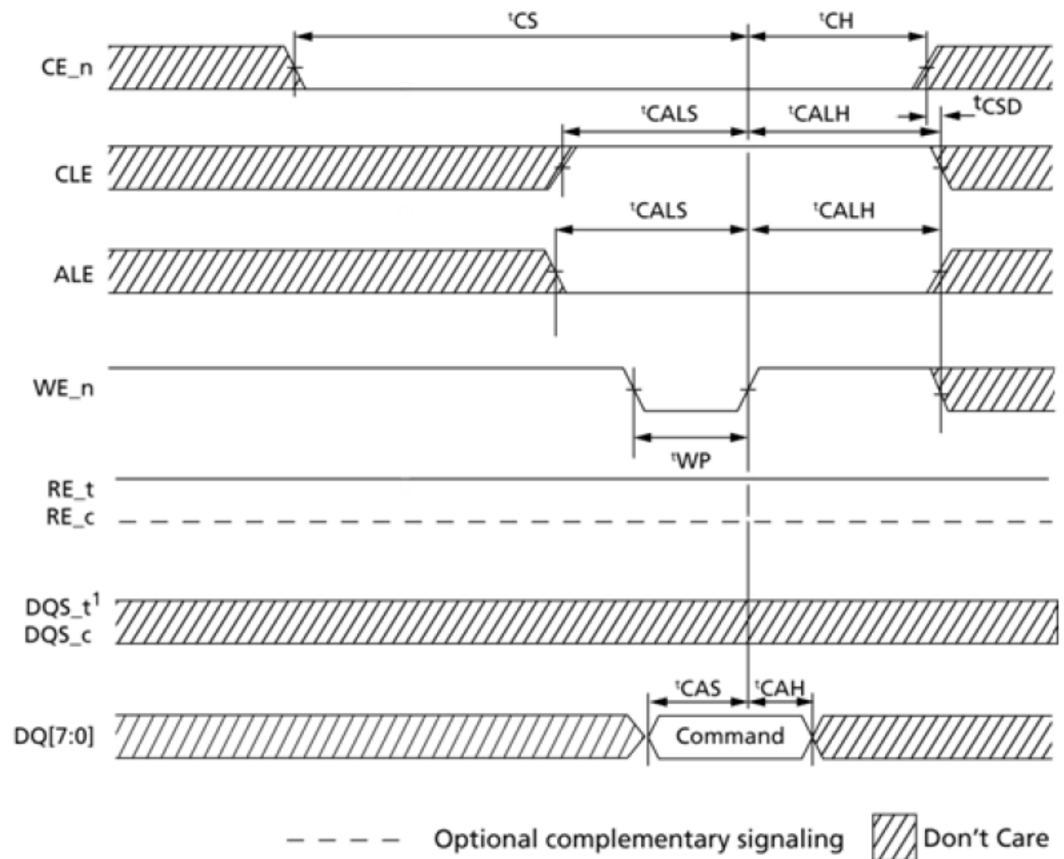

Figure 38 NVDDR2/NVDDR3 Command Cycle Timings

NOTE

When the bus state is not a data input or data output cycle, if ALE, CLE and CE_n are all low (i.e. Idle state), in such conditions, DQS (DQS_t) shall be held high to prevent the DUT from enabling ODT. If ODT is disabled, DQS meets the 'don't care' during Idle states.

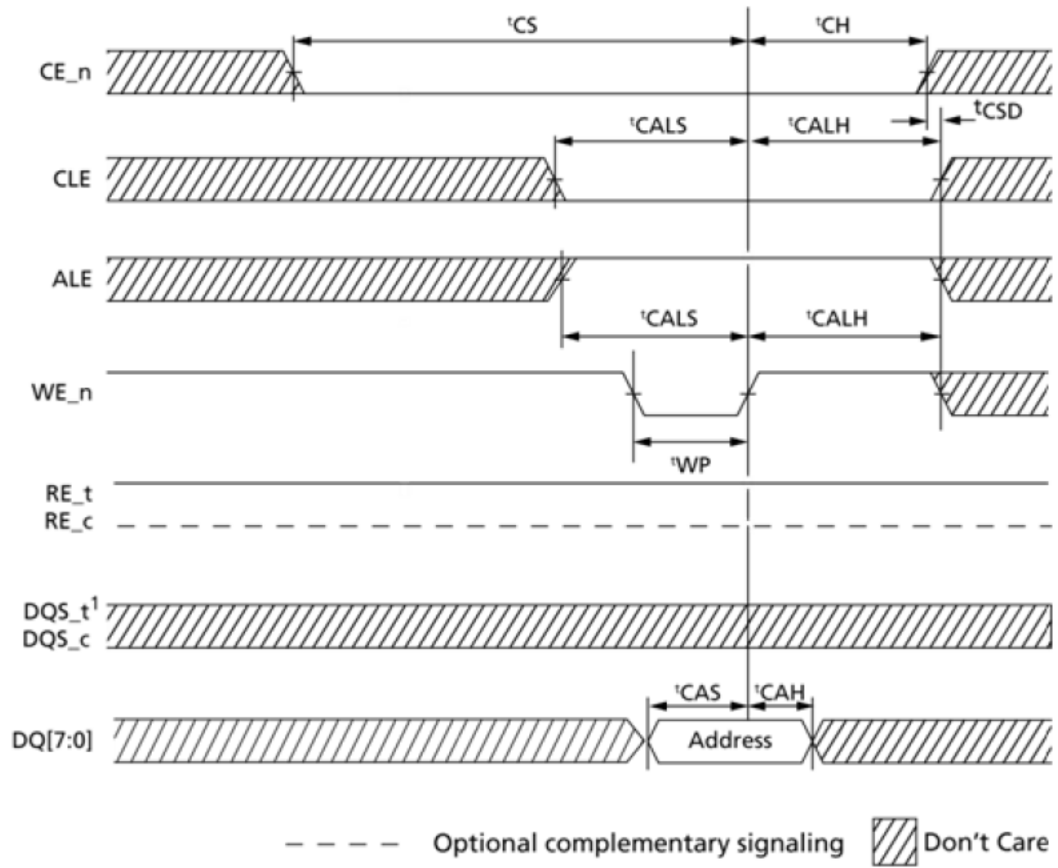

Figure 39 NVDDR2/NVDDR3 Address Cycle Timings

NOTE

When the bus state is not a data input or data output cycle, if ALE, CLE and CE_n are all low (that is, Idle state), in such conditions, DQS (DQS_t) shall be held high to prevent the DUT from enabling ODT. If ODT is disabled, DQS meets the 'don't care' during Idle states.

Data input cycle timing describes timing for data transfers from the host to the DUT (that is, data writes). Data input may be paused by stopping the transitioning of DQS (DQS_t/DQS_c).

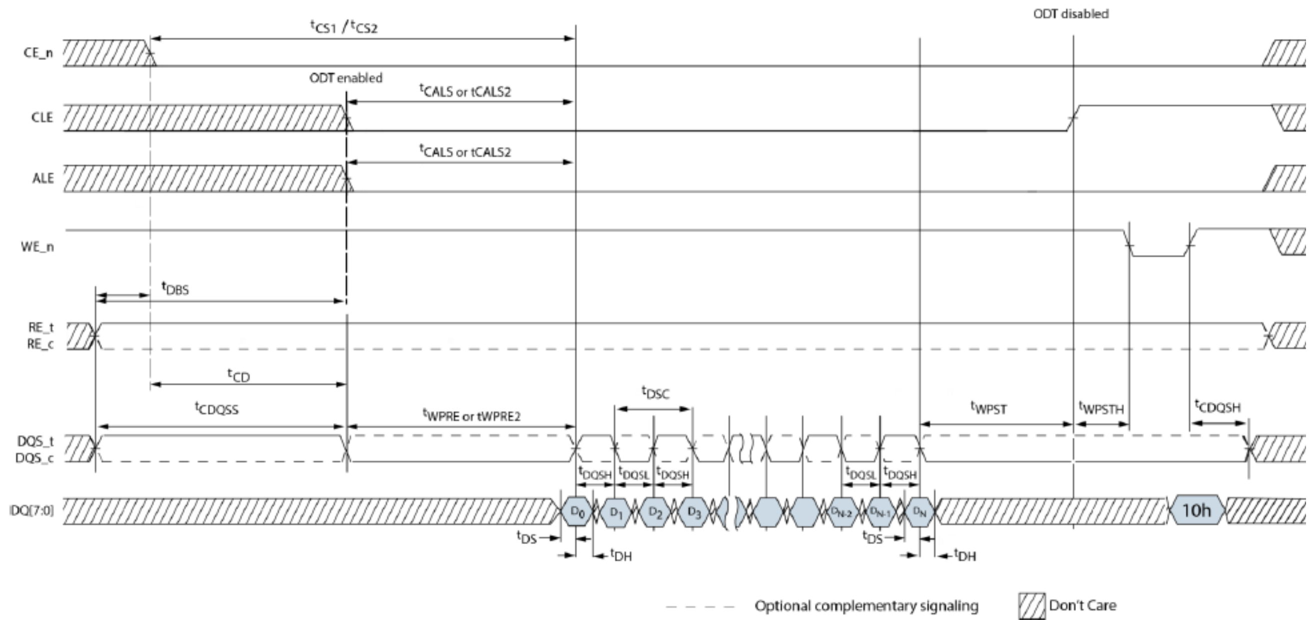

Figure 40 NVDDR2/NVDDR3 Data Input Cycle Timing

Data output cycle timing describes timing for data transfers from the DUT to the host (that is, data reads). Data output may be paused by stopping the transitioning of RE_n (RE_t/RE_c).

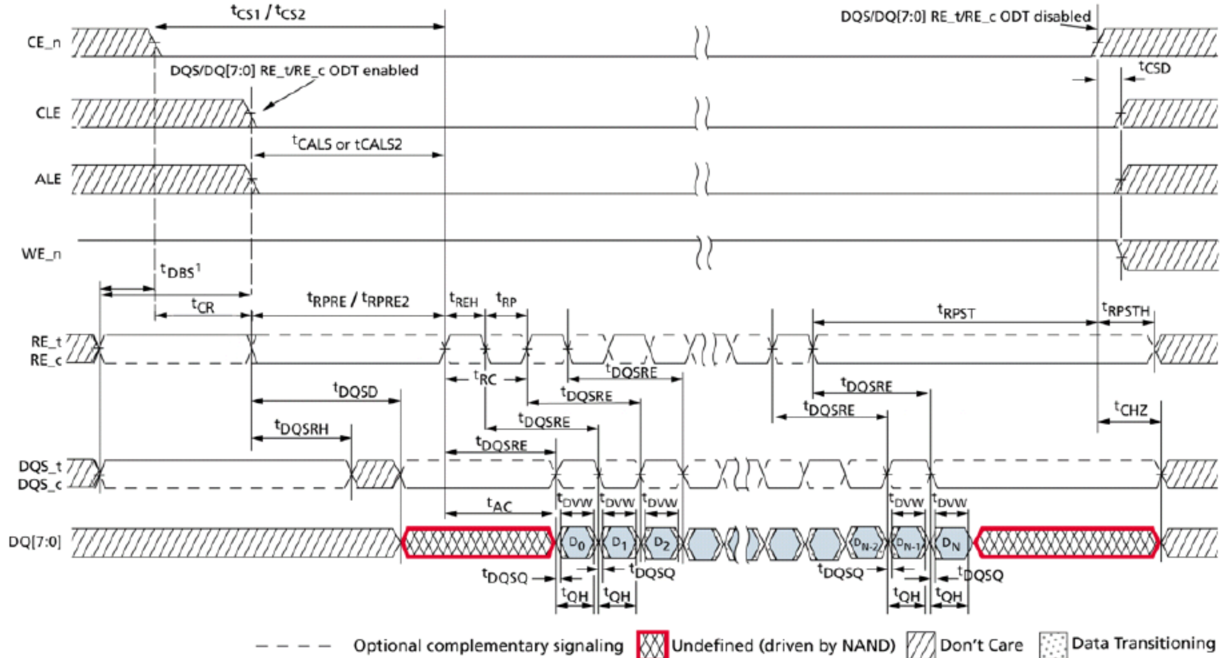

Figure 41 Data output cycle timing (no training on DQ)

Measuring Timing Parameters to/from Tri-State

There are several timing parameters that are measured to or from when:

- The device is no longer driving the NAND bus or a tri-state (hi-Z) condition
- The device begins driving from a tri-state (hi-Z) condition

These timing parameters include: tDQSD, tDQSHZ, tCHZ, tRHZ, and tIR.

This appendix defines a two point method for measuring timing parameters that involve a tri-state condition. Figure 42 defines a method to calculate the point when the device is no longer driving the NAND bus or begins driving by measuring the signal at two different voltages. The voltage measurement points are acceptable across a wide range (x = 20 mV up to x < 1/4 of VccQ). Figure 42 uses tDQSHZ and tDQSD as examples. However, the method should be used for any timing parameter (NV-DDR2, or NV-DDR3) that specifies that the device output is no longer driving the NAND bus or specifies that the device begins driving the NAND bus from a tri-state condition.

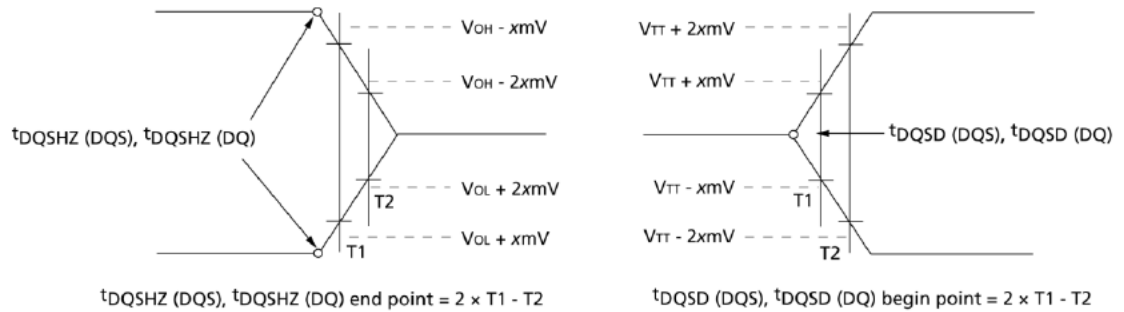

Figure 42 Two point method for measuring timing parameters with tri-state condition

5 NVDDR2/NVDDR3 Electrical Tests

Setting up the ONFI Test Application to run tests / 64
Single-Ended WRITE Cycle Tests for Strobe and Data / 65
Single-Ended READ Cycle Tests for Strobe and Data / 75
Single-Ended READ Cycle Tests for RE / 78
Single-Ended Command and Address Tests for ALE / 79
Single-Ended Command and Address Tests for CLE / 83
Single-Ended Command and Address Tests for WE / 87
Differential WRITE Cycle Tests for Strobe / 91
Differential READ Cycle Tests for Strobe / 96

This section provides the Methods of Implementation (MOIs) for ONFI Electrical tests for Strobe and Data Signals using a Keysight Infiniium Oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the Keysight D9010ONFC ONFI Test Application.

NOTE The test methodology described below for each test is applicable for both NVDDR2 and NVDDR3 data interface types. The NV-DDR3 data interface includes all NV-DDR2 features; however, NVDDR2 operates at VccQ=1.8V whereas NVDDR3 operates at VccQ=1.2V.

KEYSIGHT TECHNOLOGIES

Setting up the ONFI Test Application to run tests

1. Launch the ONFI Test Application as described in "Starting the ONFI Test Application" on page 21.
2. Connect the differential solder-in probe head to the PUTs on the ONFI device.
3. Connect the Oscilloscope probes to any Channels of the Oscilloscope.
4. On the **Set Up** tab of the ONFI Test Application:
   a. Select the required **Data Interface** type.
   b. Select or type a data rate value from the drop-down options in the **Speed Grade** area. The Test Application displays the corresponding **Timing Mode** number automatically.
   c. In the **Input Signal Setup** area, **Live** is selected by default. Select **Offline** to load one or more waveform files located on your machine.
   d. Type in or select the **Device Identifier** as well as **User Description** from the drop-down list. Enter your comments in the **Comments** text box.
5. Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.
6. Start running the selected tests. When performing the Electrical tests for Strobe and Data Signals, the ONFI Test Application will prompt you to make the proper connections. The **Connect** tab in the ONFI Test Application displays the exact number of probe connections. You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the **Configure** tab of the ONFI Test Application.

NOTE

The values for sampling rate and sampling point configuration options in the Configure tab differ for Digital Storage Oscilloscopes and UXR Oscilloscopes.

Sampling Rate (in GSa/s) options in DSOs are 10, 20, 40, 80 and MAX (default); whereas in UXRs, sampling rate (in GSa/s) options are 8, 16, 32, 64 (default), 128 and MAX.

The default option for **Sampling Points (Pts) for Electrical and Timing Tests Only** in DSOs is 2MPts; whereas in UXRs, the default option is 4MPts.

For more information about the functionality of various tabs and running tests using the ONFI Test Application's user interface, refer to the *Keysight D9010ONFC ONFI Test Application Online Help*.

Single-Ended WRITE Cycle Tests for Strobe and Data

Refer to "Understanding ONFI Concepts for Measurements" on page 27 to read about the conceptual information associated with each test.

VSEH(AC) for DQS Plus

Test Overview

The purpose of this test is to verify that the maximum Voltage of the high pulse must be within the conformance limit of the VSEH(AC) value as specified in the ONFI specification.

The value of VccQ, which directly affects the conformance upper limit is defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change this value.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS_plus (DQS_t)

Signals required to perform the test on the oscilloscope:

- DQS_plus (DQS_t)
- DQ

Test Definition Notes from the Specification

Table 21 Single-ended high level for DQS Plus

Symbol	Parameter	Min	Max	Units
VSEH(AC)	NV-DDR2 Single-Ended high level	(VccQ/2) + 0.250	Note 1[a]	V
VSEH(AC)	NV-DDR3 Single-Ended high level	(VccQ/2) + 0.150	Note 1[a]	V

a: Refer to Tabe 17 of the ONFI Specification Revision 4.2. These values are not defined. However, the single-ended signals RE_t, RE_c, DQS_t, DQS_c, shall be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Test References

See *Figure 25* and *Table 17* in *Section 2.12.1* of the *Open NAND Flash Interface Specification Revision 4.2*.

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid strobe positive pulses in this burst. A valid strobe positive pulse starts at the VREFQ crossing on a valid strobe rising edge and ends at the VREFQ crossing on the following valid strobe falling edge.
4. For the first valid strobe positive pulse, zoom in on the pulse so that it appears on the Oscilloscope's display and measure TMAX.
5. Measure VTIME at the found TMAX to get the maximum Voltage of the pulse. Consider VTIME measurement result as the VSEH(AC) value.
6. Continue the previous step for the rest of the valid strobe positive pulses that were found in the burst.
7. Determine the worst result from the set of VSEH(AC) measured.

Expected / Observable Results

The worst measured VSEH(AC) for DQS Plus must be within the specification limits.

VSEL(AC) for DQS Plus

Test Overview

The purpose of this test is to verify that the minimum Voltage of the high pulse must be within the conformance limit of the VSEL(AC) value as specified in the ONFI specification.

The value of VccQ, which directly affects the conformance upper limit is defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change this value.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS_plus (DQS_t)

Signals required to perform the test on the Oscilloscope:

- DQS_plus (DQS_t)
- DQ

Test Definition Notes from the Specification

Table 22 Single-ended low level for DQS Plus

Symbol	Parameter	Min	Max	Units
VSEL(AC)	NV-DDR2 Single-Ended low level	Note 1[a]	(VccQ/2) - 0.250	V
VSEL(AC)	NV-DDR3 Single-Ended low level	Note 1[a]	(VccQ/2) - 0.150	V

a: Refer to Tabe 17 of the ONFI Specification Revision 4.2. These values are not defined. However, the single-ended signals RE_t, RE_c, DQS_t, DQS_c, shall be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Test References

See *Figure 25* and *Table 17* in *Section 2.12.1* of the *Open NAND Flash Interface Specification Revision 4.2*.

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid strobe negative pulses in this burst. A valid strobe negative pulse starts at the VREFQ crossing on a valid strobe falling edge and ends at the VREFQ crossing on the following valid strobe rising edge.
4. For the first valid strobe negative pulse, zoom in on the pulse so that it appears on the Oscilloscope's display and measure TMIN.
5. Measure VTIME at the found TMIN to get the minimum Voltage of the pulse. Consider the VTIME measurement result as the VSEL(AC) value.
6. Continue the previous step for the rest of the valid strobe negative pulses that were found in the burst.
7. Determine the worst result from the set of VSEL(AC) measured.

Expected/Observable Results

The worst measured VSEL(AC) for DQS Plus must be within the specification limits.

VSEH(AC) for DQS Minus

Test Overview

The purpose of this test is to verify that the maximum Voltage of the low pulse must be within the conformance limit of the VSEH(AC) value as specified in the ONFI specification.

The value of VccQ, which directly affects the conformance upper limit is defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change this value.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS_minus (DQS_c)

Signals required to perform the test on the oscilloscope:

- DQS_minus (DQS_c)
- DQ

Test Definition Notes from the Specification

Table 23 Single-ended high level for DQS Minus

Symbol	Parameter	Min	Max	Units
VSEH(AC)	NV-DDR2 Single-Ended high level	(VccQ/2) + 0.250	Note 1[a]	V
VSEH(AC)	NV-DDR3 Single-Ended high level	(VccQ/2) + 0.150	Note 1[a]	V

a: Refer to Tabe 17 of the ONFI Specification Revision 4.2. These values are not defined. However, the single-ended signals RE_t, RE_c, DQS_t, DQS_c, shall be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Test References

See *Figure 25* and *Table 17* in *Section 2.12.1* of the *Open NAND Flash Interface Specification Revision 4.2*.

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid strobe positive pulses in this burst. A valid strobe positive pulse starts at the V_{QREF} crossing on a valid strobe rising edge and ends at the V_{QREF} crossing on the following valid strobe falling edge.
4. For the first valid strobe positive pulse, zoom in on the pulse so that it appears on the Oscilloscope's display and measure TMAX.
5. Measure VTIME at the found TMAX to get the maximum Voltage of the pulse. Consider VTIME measurement result as the VSEH(AC) value.
6. Continue the previous step for the rest of the valid strobe positive pulses that were found in the burst.
7. Determine the worst result from the set of VSEH(AC) measured.

Expected / Observable Results

The worst measured VSEH(AC) for DQS Minus must be within the specification limits.

VSEL(AC) for DQS Minus

Test Overview

The purpose of this test is to verify that the minimum Voltage of the low pulse must be within the conformance limit of the VSEL(AC) value as specified in the ONFI specification.

The value of VccQ, which directly affects the conformance upper limit is defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change this value.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS_minus (DQS_c)

Signals required to perform the test on the Oscilloscope:

- DQS_minus (DQS_c)
- DQ

Test Definition Notes from the Specification

Table 24 Single-ended low level for DQS Minus

Symbol	Parameter	Min	Max	Units
VSEL(AC)	NV-DDR2 Single-Ended low level	Note 1[a]	(VccQ/2) - 0.250	V
VSEL(AC)	NV-DDR3 Single-Ended low level	Note 1[a]	(VccQ/2) - 0.150	V

a: Refer to Tabe 17 of the ONFI Specification Revision 4.2. These values are not defined. However, the single-ended signals RE_t, RE_c, DQS_t, DQS_c, shall be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Test References

See *Figure 25* and *Table 17* in *Section 2.12.1* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid strobe negative pulses in this burst. A valid strobe negative pulse starts at the VREFQ crossing on a valid strobe falling edge and ends at the VREFQ crossing on the following valid strobe rising edge.
4 For the first valid strobe negative pulse, zoom in on the pulse so that it appears on the Oscilloscope’s display and measure TMIN.
5 Measure VTIME at the found TMIN to get the minimum Voltage of the pulse. Consider the VTIME measurement result as the VSEL(AC) value.
6 Continue the previous step for the rest of the valid strobe negative pulses that were found in the burst.
7 Determine the worst result from the set of VSEL(AC) measured.

Expected/Observable Results

The worst measured VSEL(AC) for DQS Minus must be within the specification limits.

VIX for Strobe

Test Overview

The purpose of this test is to verify the crossing point of the input differential test signal pair is within the conformance limits of the VIX as specified in the ONFI specification.

The value of VccQ, which directly affects the conformance upper limit is defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change this value.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS_plus (DQS_t), DQS_minus (DQS_c)

Signals required to perform the test on the oscilloscope:

- DQS_plus (DQS_t), DQS_minus (DQS_c)
- DQ

Test Definition Notes from the Specification

Table 25 Cross Point Voltage for Differential Input Signals

Symbol	Parameter	Min	Max	Units
VIX(AC)	AC differential input cross-point Voltage relative to VccQ / 2	(NV-DDR2) 0.50 x VccQ - 175	(NV-DDR2) 0.50 x VccQ + 175	mV
		(NV-DDR3) 0.50 x VccQ - 120	(NV-DDR3) 0.50 x VccQ + 120	

Test References

See *Table 68* in *Section 4.14* of the *Open NAND Flash Interface Specification Revision 4.2*.

Measurement Algorithm

1. Obtain sample or acquire data waveforms.
2. Use Subtract function to generate the differential waveform from two source input.
3. Split read and write burst of the acquired signal.
4. Take the first valid WRITE burst found.
5. Find all differential DQS crossings that cross 0V.
6. Use VTIME to get the actual crossing point Voltage value using the timestamps obtained.
7. For each cross point Voltage value, typical value of VIX(AC) is calculated as:
   VIX(AC) = VccQ/2
8. Determine the worst result from the set of VIX(AC) measured.

Expected / Observable Results

The measured crossing point value for the differential test signal pair should be within the conformance limits of the VIX value.

VIH(AC) for DQ

Test Overview

The purpose of this test is to verify that the input high level Voltage value of the test signal within a valid sampling window is greater than the conformance limits of the VIH(AC) value specified in the ONFI specification.

The value of VccQ and VrefQ, which directly affect the conformance upper limit, are defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change these values.

Signals of Interest

Based on the test definition (Write cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 26 AC Input High Voltage for DQ

Symbol	Parameter	Min	Max	Units
VIH(AC)	NVDDR-2 AC Input High Voltage	VREFQ + 250	Note 1[a]	mV
VIH(AC)	NVDDR-3 AC Input High Voltage	VREFQ + 150	Note 1[a]	mV

a: Refer to Table 13 & 14, which direct to section 2.11 for AC Overshoot and Undershoot requirements of the ONFI Specification Revision 4.2.

Test References

See *Tables 13 & 14* in *Section 2.12* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid positive pulses. A valid positive pulse starts at VREFQ crossing at valid rising edge and ends at VREFQ crossing at the following valid falling edge.
4. Zoom in on the first valid positive pulse and perform VTOP measurement. Note the VTOP measurement result value as VIH(AC).
5. Continue the previous step with the rest of the valid positive pulses that were found in the burst.
6. Determine the worst result from the set of VIH(AC) measured.

Expected / Observable Results

The value of the Input High Level Voltage of the test signal must be greater than or equal to the VIH(AC) value in the specification.

VIH(DC) for DQ

Test Overview

The purpose of this test is to verify that the input high level Voltage value of the test signal within a valid sampling window is within the conformance limits of the VIH(DC) value specified in the ONFI specification.

The values of VccQ and VrefQ, which directly affect the conformance upper limit, are defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change these values.

Signals of Interest

Based on the test definition (Write cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 27 DC Input High Voltage for DQ

Symbol	Parameter	Min	Max	Units
VIH(DC)	NV-DDR2 DC Input High Voltage	VREFQ + 125	VccQ + 300	mV
VIH(DC)	NV-DDR3 DC Input High Voltage	VREFQ + 100	VccQ	mV

Test References

See *Tables 13 & 14* in *Section 2.12* of the *Open NAND Flash Interface Specification Revision 4.2*.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid positive pulses. A valid positive pulse starts at VREFQ crossing at valid rising edge and ends at VREFQ crossing at the following valid falling edge.
4. Zoom in on the first valid positive pulse and perform VTOP measurement. Note the VTOP measurement result value as VIH(DC).
5. Continue the previous step with the rest of the valid positive pulses that were found in the burst.
6. Determine the worst result from the set of VIH(DC) measured.

Expected / Observable Results

The value of the Input High Level Voltage of the test signal must be within the specification limit of VIH(DC).

VIL(AC) for DQ

Test Overview

The purpose of this test is to verify that the input low level Voltage of the test signal within a valid sampling window is lower than the conformance limits of the VIL(AC) value specified in the ONFI specification.

The values of VccQ and VrefQ, which directly affect the conformance upper limit, are defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change these values.

Signals of Interest

Based on the test definition (Write cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 28 AC Input Low Voltage for DQ

Symbol	Parameter	Min	Max	Units
VIL(AC)	NV-DDR2 AC Input Low Voltage	Note 1[a]	VREFQ - 250	mV
VIL(AC)	NV-DDR3 AC Input Low Voltage	Note 1[a]	VREFQ - 150	mV

a: Refer to Tables 13 & 14, which direct to section 2.11 for AC Overshoot and Undershoot requirements of the ONFI Specification Revision 4.2.

Test References

See *Tables 13 & 14* in *Section 2.12* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid negative pulses. A valid negative pulse starts at VREFQ crossing at valid falling edge and ends at VREFQ crossing at the following valid rising edge.
4. Zoom in on the first valid negative pulse and perform VBASE measurement. Take the VBASE measurement result as VIL(AC) value.
5. Continue the previous step with the rest of the valid negative pulses that were found in the burst.
6. Determine the worst result from the set of VIL(AC) measured.

Expected / Observable Results

The value of the Input Low Level Voltage of the test signal must be lower than or equal to the VIL(AC) value in the specification.

VIL(DC) for DQ

Test Overview

The purpose of this test is to verify that the input low level Voltage of the test signal within a valid sampling window is within the conformance limits of the VIL(DC) value specified in the ONFI specification.

The values of VccQ and VrefQ, which directly affect the conformance upper limit, are defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change these values.

Signals of Interest

Based on the test definition (Write cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 29 DC Input Low Voltage for DQ

Symbol	Parameter	Min	Max	Units
VIL(DC)	NV-DDR2 DC Input Low Voltage	-300	VREFQ - 125	mV
VIL(DC)	NV-DDR3 DC Input Low Voltage	VssQ	VREFQ - 100	mV

Test References

See *Tables 13 & 14* in *Section 2.12* of the *Open NAND Flash Interface Specification Revision 4.2*.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid negative pulses. A valid negative pulse starts at VREFQ crossing at valid falling edge and ends at VREFQ crossing at the following valid rising edge.
4. Zoom in on the first valid negative pulse and perform VBASE measurement. Take the VBASE measurement result as VIL(DC) value.
5. Continue the previous step with the rest of the valid negative pulses that were found in the burst.
6. Determine the worst result from the set of VIL(DC) measured.

Expected / Observable Results

The value of the Input Low Level Voltage of the test signal must be within the specification limit of VIL(DC).

Single-Ended READ Cycle Tests for Strobe and Data

Refer to "Understanding ONFI Concepts for Measurements" on page 27 to read about the conceptual information associated with each test.

VOX for Strobe

Test Overview

The purpose of this test is to verify the crossing point of the output differential test signal pair is within the conformance limits of the VOX as specified in the ONFI specification.

The value of VccQ, which directly affects the conformance upper limit is defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change this value.

Signals of Interest

Based on the test definition (Read cycle only):

- DQS_plus (DQS_t), DQS_minus (DQS_c)

Signals required to perform the test on the Oscilloscope:

- DQS_plus (DQS_t), DQS_minus (DQS_c)
- DQ

Test Definition Notes from the Specification

Table 30 Cross Point Voltage for Differential Output Signals

Symbol	Parameter	Min	Max	Units
VOX(AC)	AC differential output cross-point Voltage	0.50 x VccQ - 200	0.50 x VccQ + 200	mV

Test References

See *Table 69* in *Section 4.14* of the *Open NAND Flash Interface Specification Revision 4.2*.

Measurement Algorithm

1. Obtain sample or acquire data waveforms.
2. Use Subtract function to generate the differential waveform from two source inputs.
3. Split read and write burst of the acquired signal.
4. Take the first valid READ burst found.
5. Find all differential DQS crossings that cross 0V.
6. Use V_{TIME} to get the actual crossing point Voltage value using the timestamps obtained.
7. For each cross point Voltage value, typical value of VOX(AC) is calculated as:
   VOX(AC) = VccQ/2
8. Determine the worst result from the set of VOX(AC) measured.

Expected / Observable Results

The measured crossing point value for the differential test signal pair should be within the conformance limits of the VOX value.

VOH(AC) for DQ

Test Overview

The purpose of this test is to verify that the output high level Voltage value of the test signal within a valid sampling window is greater than the conformance limits of the VOH(AC) value specified in the ONFI specification.

The values of VccQ and VTT, which directly affect the conformance upper limit, are defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change these values.

Signals of Interest

Based on the test definition (Read cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 31 AC Output High Voltage for DQ

Symbol	Parameter	NV-DDR2 / NV-DDR3 Values	Units
VOH(AC)	AC Output High Voltage	VTT + (VccQ * 0.10)	mV

Test References

See *Table 43* in *Section 4.9* of the *Open NAND Flash Interface Specification Revision 4.2*.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid positive pulses. A valid positive pulse starts at VREFQ crossing at valid rising edge and ends at VREFQ crossing at the following valid falling edge.
4. Zoom in on the first valid positive pulse and perform VTOP measurement. Note the VTOP measurement result value as VOH(AC).
5. Continue the previous step with the rest of the valid positive pulses that were found in the burst.
6. Determine the worst result from the set of VOH(AC) measured.

Expected / Observable Results

The value of the Output High Level Voltage of the test signal must be greater than or equal to the VOH value in the specification.

VOL(AC) for DQ

Test Overview

The purpose of this test is to verify that the output low level Voltage of the test signal within a valid sampling window is lower than the conformance limits of the VOL(AC) value specified in the ONFI specification.

The values of VccQ and VTT, which directly affect the conformance upper limit, are defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change these values.

Signals of Interest

Based on the test definition (Read cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 32 AC Output Low Voltage for DQ

Symbol	Parameter	NV-DDR2 / NV-DDR3 Values	Units
VOL(AC)	AC Output Low Voltage	VTT - (VccQ * 0.10)	mV

Test References

See *Table 43* in *Section 4.9* of the *Open NAND Flash Interface Specification Revision 4.2*.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid negative pulses. A valid negative pulse starts at VREFQ crossing at valid falling edge and ends at VREFQ crossing at the following valid rising edge.
4 Zoom in on the first valid negative pulse and perform VBASE measurement. Take the VBASE measurement result as VOL(AC) value.
5 Continue the previous step with the rest of the valid negative pulses that were found in the burst.
6 Determine the worst result from the set of VOL(AC) measured.

Expected / Observable Results

The value of the Output Low Level Voltage of the test signal must be lower than or equal to the minimum VOL value.

Single-Ended READ Cycle Tests for RE

Refer to "Understanding ONFI Concepts for Measurements" on page 27 to read about the conceptual information associated with each test.

VOX for RE

Test Overview

The purpose of this test is to verify the crossing point of the output Read Enable (RE) differential test signal pair is within the conformance limits of the VOX as specified in the ONFI specification.

The value of VccQ, which directly affects the conformance upper limit is defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change this value.

Signals of Interest

Based on the test definition (Read cycle only):

- RE_plus (RE_t), RE_minus (RE_c)

Signals required to perform the test on the Oscilloscope:

- RE_plus (RE_t), RE_minus (RE_c)
- DQS, DQ

Test Definition Notes from the Specification

Table 33 Cross Point Voltage for Differential RE Signals

Symbol	Parameter	Min	Max	Units
VOX(AC)	AC differential output cross-point Voltage	0.50 x VccQ - 200	0.50 x VccQ + 200	mV

Test References

See *Table 69* in *Section 4.14* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Obtain sample or acquire data waveforms.
2. Use Subtract function to generate the differential waveform from two source inputs.
3. Split read and write burst of the acquired signal.
4. Take the first valid READ burst found.
5. Find all differential RE crossings that cross 0V within the burst.
6. Use V_{TIME} to get the actual crossing point Voltage value using the timestamps obtained.
7. For each cross point Voltage value, typical value of VOX(AC) is calculated as:
   VOX(AC) = VccQ/2
8. Determine the worst result from the set of VOX(AC) measured.

Expected / Observable Results

The measured crossing point value for the differential test signal pair should be within the conformance limits of the VOX value.

Single-Ended Command and Address Tests for ALE

Refer to "Understanding ONFI Concepts for Measurements" on page 27 to read about the conceptual information associated with each test.

ALE Overshoot Amplitude

Test Overview

The purpose of this test is to verify that the amplitude allowed for the overshoot area is less than or equal to 1V for the NV-DDR2 data interfaces and timing modes whereas, the maximum amplitude allowed for the overshoot area is 0.35V for the NV-DDR3 data interface and timing modes.

Signals of Interest

Based on the test definition:

- ALE

Signals required to perform the test on the Oscilloscope:

- ALE

Test Definition Notes from the Specification

Refer to "Understanding ONFI Concepts for Measurements" on page 27.

Test References

See *Table 8* & *Figure 23: Overshoot/Undershoot Diagram* in *Section 2.11* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1 Set the number of sampling points in the **Sampling Points (Pts) for Electrical and Timing Tests Only** in the **Configure** tab of the Compliance Test Application:

- For Digital Storage Oscilloscopes, default configuration is 2MPts.
- For UXR Oscilloscopes, default configuration is 4MPts.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use VMAX to get the time-stamp of maximum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to maximize the peak area.

5 Find the edges before and after the Overshoot Point at VccQ to calculate the maximum overshoot length duration.

6 Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = VMAX - VccQ

7 Compare test results with the compliance test limits.

Expected / Observable Results

The measured amplitude allowed for the overshoot area should be within the conformance limits as defined in the specification.

ALE Overshoot Area

Test Overview

The purpose of this test is to verify that the overshoot area is less than or equal to 3V-ns for both NV-DDR2 and NV-DDR3 data interfaces and timing modes.

Signals of Interest

Based on the test definition:

- ALE

Signals required to perform the test on the Oscilloscope:

- ALE

Test Definition Notes from the Specification

Refer to "AC Undershoot/Overshoot Requirements" on page 40.

Test References

See *Table 8* & *Figure 23: Overshoot/Undershoot Diagram* in *Section 2.11* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1 Run "ALE Overshoot Amplitude" on page 79 as a pre-requisite to this test.

2 Using the Overshoot Amplitude calculated earlier, calculate Overshoot area (V-ns).

   a Use the overshoot width as the triangle base and the overshoot amplitude as the triangle height.

   b Calculate Overshoot area using the equation:

   Overshoot Area = 0.5 x base x height

3 Compare test results with the compliance test limits.

4 Repeat steps 2 and 3 for each timing mode.

Expected / Observable Results

The measured overshoot area should be within the conformance limits as defined in the specification.

ALE Undershoot Amplitude

Test Overview

The purpose of this test is to verify that the amplitude allowed for the undershoot area is less than or equal to 1V for the NV-DDR2 data interfaces and timing modes whereas, the maximum amplitude allowed for the undershoot area is 0.35V for the NV-DDR3 data interface and timing modes.

Signals of Interest

Based on the test definition:

- ALE

Signals required to perform the test on the Oscilloscope:

- ALE

Test Definition Notes from the Specification

Refer to "AC Undershoot/Overshoot Requirements" on page 40.

Test References

See *Table 8* & *Figure 23: Overshoot/Undershoot Diagram* in *Section 2.11* of the *Open NAND Flash Interface Specification Revision 4.2*.

Measurement Algorithm

1. Set the number of sampling points in the **Sampling Points (Pts) for Electrical and Timing Tests Only** in the **Configure** tab of the Compliance Test Application:
   - For Digital Storage Oscilloscopes, default configuration is 2MPts.
   - For UXR Oscilloscopes, default configuration is 4MPts.
2. Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
3. Use VMIN to get the time-stamp of minimum voltage on all regions of the acquired waveform.
4. Perform manual zoom on the waveform to maximize the peak area.
5. Find the edges before and after the undershoot point at VssQ to calculate the maximum undershoot length duration.
6. Calculate Undershoot Amplitude using the equation:

   Undershoot Amplitude = VssQ - VMIN
7. Compare test results with the compliance test limits.

Expected / Observable Results

The measured amplitude allowed for the undershoot area should be within the conformance limits as defined in the specification.

ALE Undershoot Area

Test Overview

The purpose of this test is to verify that the undershoot area is less than or equal to 3V-ns for both NV-DDR2 and NV-DDR3 data interfaces and timing modes.

Signals of Interest

Based on the test definition:

- ALE

Signals required to perform the test on the Oscilloscope:

- ALE

Test Definition Notes from the Specification

Refer to "AC Undershoot/Overshoot Requirements" on page 40.

Test References

See *Table 8* & *Figure 23: Overshoot/Undershoot Diagram* in *Section 2.11* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Run "ALE Undershoot Amplitude" on page 81 as a pre-requisite to this test.
2. Using the Undershoot Amplitude calculated earlier, calculate Undershoot area (V-ns).
   a. Use the undershoot width as the triangle base and the undershoot amplitude as the triangle height.
   b. Calculate Undershoot area using the equation:

   Undershoot Area = 0.5 x base x height
3. Compare test results with the compliance test limits.
4. Repeat steps 2 and 3 for each timing mode.

Expected / Observable Results

The measured undershoot area should be within the conformance limits as defined in the specification.

Single-Ended Command and Address Tests for CLE

Refer to "Understanding ONFI Concepts for Measurements" on page 27 to read about the conceptual information associated with each test.

CLE Overshoot Amplitude

Test Overview

The purpose of this test is to verify that the amplitude allowed for the overshoot area is less than or equal to 1V for the NV-DDR2 data interfaces and timing modes whereas, the maximum amplitude allowed for the overshoot area is 0.35V for the NV-DDR3 data interface and timing modes.

Signals of Interest

Based on the test definition:

- CLE

Signals required to perform the test on the Oscilloscope:

- CLE

Test Definition Notes from the Specification

Refer to "AC Undershoot/Overshoot Requirements" on page 40.

Test References

See *Table 8* & *Figure 23: Overshoot/Undershoot Diagram* in *Section 2.11* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1 Set the number of sampling points in the **Sampling Points (Pts) for Electrical and Timing Tests Only** in the **Configure** tab of the Compliance Test Application:

- For Digital Storage Oscilloscopes, default configuration is 2MPts.
- For UXR Oscilloscopes, default configuration is 4MPts.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use VMAX to get the time-stamp of maximum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to maximize the peak area.

5 Find the edges before and after the Overshoot Point at VccQ to calculate the maximum overshoot length duration.

6 Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = VMAX - VccQ

7 Compare test results with the compliance test limits.

Expected / Observable Results

The measured amplitude allowed for the overshoot area should be within the conformance limits as defined in the specification.

CLE Overshoot Area

Test Overview

The purpose of this test is to verify that the overshoot area is less than or equal to 3V-ns for both NV-DDR2 and NV-DDR3 data interfaces and timing modes.

Signals of Interest

Based on the test definition:

- CLE

Signals required to perform the test on the Oscilloscope:

- CLE

Test Definition Notes from the Specification

Refer to "AC Undershoot/Overshoot Requirements" on page 40.

Test References

See *Table 8* & *Figure 23: Overshoot/Undershoot Diagram* in *Section 2.11* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Run "CLE Overshoot Amplitude" on page 83 as a pre-requisite to this test.
2. Using the Overshoot Amplitude calculated earlier, calculate Overshoot area (V-ns).
   a Use the overshoot width as the triangle base and the overshoot amplitude as the triangle height.
   b Calculate Overshoot area using the equation:
   Overshoot Area = 0.5 x base x height
3. Compare test results with the compliance test limits.
4. Repeat steps 2 and 3 for each timing mode.

Expected / Observable Results

The measured overshoot area should be within the conformance limits as defined in the specification.

CLE Undershoot Amplitude

Test Overview

The purpose of this test is to verify that the amplitude allowed for the undershoot area is less than or equal to 1V for the NV-DDR2 data interfaces and timing modes whereas, the maximum amplitude allowed for the undershoot area is 0.35V for the NV-DDR3 data interface and timing modes.

Signals of Interest

Based on the test definition:

- CLE

Signals required to perform the test on the Oscilloscope:

- CLE

Test Definition Notes from the Specification

Refer to "AC Undershoot/Overshoot Requirements" on page 40.

Test References

See *Table 8* & *Figure 23: Overshoot/Undershoot Diagram* in *Section 2.11* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1 Set the number of sampling points in the **Sampling Points (Pts) for Electrical and Timing Tests Only** in the **Configure** tab of the Compliance Test Application:

- For Digital Storage Oscilloscopes, default configuration is 2MPts.
- For UXR Oscilloscopes, default configuration is 4MPts.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use VMIN to get the time-stamp of minimum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to maximize the peak area.

5 Find the edges before and after the undershoot point at VssQ to calculate the maximum undershoot length duration.

6 Calculate Undershoot Amplitude using the equation:

Undershoot Amplitude = VssQ - VMIN

7 Compare test results with the compliance test limits.

Expected / Observable Results

The measured amplitude allowed for the undershoot area should be within the conformance limits as defined in the specification.

CLE Undershoot Area

Test Overview

The purpose of this test is to verify that the undershoot area is less than or equal to 3V-ns for both NV-DDR2 and NV-DDR3 data interfaces and timing modes.

Signals of Interest

Based on the test definition:

- CLE

Signals required to perform the test on the Oscilloscope:

- CLE

Test Definition Notes from the Specification

Refer to "AC Undershoot/Overshoot Requirements" on page 40.

Test References

See *Table 8* & *Figure 23: Overshoot/Undershoot Diagram* in *Section 2.11* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Run "CLE Undershoot Amplitude" on page 85 as a pre-requisite to this test.
2. Using the Undershoot Amplitude calculated earlier, calculate Undershoot area (V-ns).
   a. Use the undershoot width as the triangle base and the undershoot amplitude as the triangle height.
   b. Calculate Undershoot area using the equation:

   Undershoot Area = 0.5 x base x height
3. Compare test results with the compliance test limits.
4. Repeat steps 2 and 3 for each timing mode.

Expected / Observable Results

The measured undershoot area should be within the conformance limits as defined in the specification.

Single-Ended Command and Address Tests for WE

Refer to "Understanding ONFI Concepts for Measurements" on page 27 to read about the conceptual information associated with each test.

WE Overshoot Amplitude

Test Overview

The purpose of this test is to verify that the amplitude allowed for the overshoot area is less than or equal to 1V for the NV-DDR2 data interfaces and timing modes whereas, the maximum amplitude allowed for the overshoot area is 0.35V for the NV-DDR3 data interface and timing modes.

Signals of Interest

Based on the test definition:

- WE

Signals required to perform the test on the Oscilloscope:

- WE

Test Definition Notes from the Specification

Refer to "AC Undershoot/Overshoot Requirements" on page 40.

Test References

See *Table 8* & *Figure 23: Overshoot/Undershoot Diagram* in *Section 2.11* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Set the number of sampling points in the **Sampling Points (Pts) for Electrical and Timing Tests Only** in the **Configure** tab of the Compliance Test Application:
   - For Digital Storage Oscilloscopes, default configuration is 2MPts.
   - For UXR Oscilloscopes, default configuration is 4MPts.
2. Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
3. Use VMAX to get the time-stamp of maximum voltage on all regions of the acquired waveform.
4. Perform manual zoom on the waveform to maximize the peak area.
5. Find the edges before and after the Overshoot Point at VccQ to calculate the maximum overshoot length duration.
6. Calculate Overshoot Amplitude using the equation:

   Overshoot Amplitude = VMAX - VccQ
7. Compare test results with the compliance test limits.

Expected / Observable Results

The measured amplitude allowed for the overshoot area should be within the conformance limits as defined in the specification.

WE Overshoot Area

Test Overview

The purpose of this test is to verify that the overshoot area is less than or equal to 3V-ns for both NV-DDR2 and NV-DDR3 data interfaces and timing modes.

Signals of Interest

Based on the test definition:

- WE

Signals required to perform the test on the Oscilloscope:

- WE

Test Definition Notes from the Specification

Refer to "AC Undershoot/Overshoot Requirements" on page 40.

Test References

See *Table 8* & *Figure 23: Overshoot/Undershoot Diagram* in *Section 2.11* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1 Run "WE Overshoot Amplitude" on page 87 as a pre-requisite to this test.

2 Using the Overshoot Amplitude calculated earlier, calculate Overshoot area (V-ns).

   a Use the overshoot width as the triangle base and the overshoot amplitude as the triangle height.

   b Calculate Overshoot area using the equation:

   Overshoot Area = 0.5 x base x height

3 Compare test results with the compliance test limits.

4 Repeat steps 2 and 3 for each timing mode.

Expected / Observable Results

The measured overshoot area should be within the conformance limits as defined in the specification.

WE Undershoot Amplitude

Test Overview

The purpose of this test is to verify that the amplitude allowed for the undershoot area is less than or equal to 1V for the NV-DDR2 data interfaces and timing modes whereas, the maximum amplitude allowed for the undershoot area is 0.35V for the NV-DDR3 data interface and timing modes.

Signals of Interest

Based on the test definition:

- WE

Signals required to perform the test on the Oscilloscope:

- WE

Test Definition Notes from the Specification

Refer to "AC Undershoot/Overshoot Requirements" on page 40.

Test References

See *Table 8* & *Figure 23: Overshoot/Undershoot Diagram* in *Section 2.11* of the *Open NAND Flash Interface Specification Revision 4.2*.

Measurement Algorithm

1 Set the number of sampling points in the **Sampling Points (Pts) for Electrical and Timing Tests Only** in the **Configure** tab of the Compliance Test Application:

- For Digital Storage Oscilloscopes, default configuration is 2MPts.
- For UXR Oscilloscopes, default configuration is 4MPts.

2 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

3 Use VMIN to get the time-stamp of minimum voltage on all regions of the acquired waveform.

4 Perform manual zoom on the waveform to maximize the peak area.

5 Find the edges before and after the undershoot point at VssQ to calculate the maximum undershoot length duration.

6 Calculate Undershoot Amplitude using the equation:

Undershoot Amplitude = VssQ - VMIN

7 Compare test results with the compliance test limits.

Expected / Observable Results

The measured amplitude allowed for the undershoot area should be within the conformance limits as defined in the specification.

WE Undershoot Area

Test Overview

The purpose of this test is to verify that the undershoot area is less than or equal to 3V-ns for both NV-DDR2 and NV-DDR3 data interfaces and timing modes.

Signals of Interest

Based on the test definition:

- WE

Signals required to perform the test on the Oscilloscope:

- WE

Test Definition Notes from the Specification

Refer to "AC Undershoot/Overshoot Requirements" on page 40.

Test References

See *Table 8* & *Figure 23: Overshoot/Undershoot Diagram* in *Section 2.11* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1 Run "WE Undershoot Amplitude" on page 89 as a pre-requisite to this test.

2 Using the Undershoot Amplitude calculated earlier, calculate Undershoot area (V-ns).

   a Use the undershoot width as the triangle base and the undershoot amplitude as the triangle height.

   b Calculate Undershoot area using the equation:

   Undershoot Area = 0.5 x base x height

3 Compare test results with the compliance test limits.

4 Repeat steps 2 and 3 for each timing mode.

Expected / Observable Results

The measured undershoot area should be within the conformance limits as defined in the specification.

Differential WRITE Cycle Tests for Strobe

Refer to “Understanding ONFI Concepts for Measurements” on page 27 to read about the conceptual information associated with each test.

VIH.diff(AC) for DQS

Test Overview

The purpose of this test is to verify that the high level Voltage value of the test signal within a valid sampling window must be within the conformance limit of the VIH.diff(AC) value as specified in the ONFI specification.

The value of VRefQ, which directly affects the conformance upper limit is defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change this value.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 34 Differential AC Input High Voltage for DQS

Symbol	Parameter	Min	Max	Units
VIHdiff(AC)	Differential Input High AC	2 x [VIH(AC) - VREFQ]	Note 1[a]	V

a: Refer to Table 16 of the ONFI Specification Revision 4.2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [VIH(DC) max, VIL (DC) min] for single-ended signals as well as the limitations for overshoot and undershoot in Table 13.

Test References

See *Table 16* in *Section 2.12* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid Strobe positive pulses in this burst. A valid Strobe positive pulse starts at the 0V crossing on a valid Strobe rising edge and ends at the 0V crossing on the following valid Strobe falling edge.
4. For the first valid Strobe positive pulse, zoom in on the pulse so that it appears on the Oscilloscope’s display and perform the VTOP measurement. Take the VTOP measurement result as the VIH.diff(AC) value.
5. Continue the previous step for the rest of the valid Strobe positive pulses found in the burst.
6. Determine the worst result from the set of VIH.diff(AC) measured.

Expected / Observable Results

The worst measured Input High Voltage VIH.diff(AC) must meet the limits defined in the ONFI specification.

VIH.diff(DC) for DQS

Test Overview

The purpose of this test is to verify that the high level Voltage value of the test signal within a valid sampling window must be within the conformance limit of the VIH.diff(DC) value as specified in the ONFI specification.

The value of VRefQ, which directly affects the conformance upper limit is defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change this value.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 35 Differential DC Input High Voltage for DQS

Symbol	Parameter	Min	Max	Units
VIHdiff(DC)	Differential Input High	2 x [VIH(DC) - VREFQ]	Note 1[a]	V

a: Refer to Table 16 of the ONFI Specification Revision 4.2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [VIH(DC) max, VIL (DC) min] for single-ended signals as well as the limitations for overshoot and undershoot in Table 13.

Test References

See *Table 16* in *Section 2.12* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid Strobe positive pulses in this burst. A valid Strobe positive pulse starts at the 0V crossing on a valid Strobe rising edge and ends at the 0V crossing on the following valid Strobe falling edge.
4. For the first valid Strobe positive pulse, zoom in on the pulse so that it appears on the Oscilloscope’s display and perform the VTOP measurement. Take the VTOP measurement result as the VIH.diff(DC) value.
5. Continue the previous step for the rest of the valid Strobe positive pulses found in the burst.
6. Determine the worst result from the set of VIH.diff(DC) measured.

Expected / Observable Results

The worst measured Input High Voltage VIH.diff(DC) must meet the limits defined in the ONFI specification.

VIL.diff(AC) for DQS

Test Overview

The purpose of this test is to verify that the low level Voltage value of the test signal within a valid sampling window must be within the conformance limit of the VIL.diff(AC) value as specified in the ONFI specification.

The value of VRefQ, which directly affects the conformance upper limit is defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change this value.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 36 Differential AC Input Low Voltage for DQS

Symbol	Parameter	Min	Max	Units
VILdiff(AC)	Differential Input Low AC	Note 1[a]	2 x [VIL(AC) - VREFQ]	V

a: Refer to Table 16 of the ONFI Specification Revision 4.2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [VIH(DC) max, VIL (DC) min] for single-ended signals as well as the limitations for overshoot and undershoot in Table 13.

Test References

See *Table 16* in *Section 2.12* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid Strobe negative pulses in this burst. A valid Strobe negative pulse starts at the 0V crossing on a valid Strobe falling edge and ends at the 0V crossing on the following valid Strobe rising edge.
4. For the first valid Strobe negative pulse, zoom in on the pulse so that it appears on the oscilloscope’s display and perform the VBASE measurement. Take the VBASE measurement result as the VIL.diff(AC) value.
5. Continue the previous step for the rest of the valid Strobe negative pulses found in the burst.
6. Determine the worst result from the set of VIL.diff(AC) measured.

Expected / Observable Results

The worst measured Input Low Voltage VIL.diff(AC) must meet the limits defined in the ONFI specification.

VIL.diff(DC) for DQS

Test Overview

The purpose of this test is to verify that the low level Voltage value of the test signal within a valid sampling window must be within the conformance limit of the VIL.diff(DC) value as specified in the ONFI specification.

The value of VRefQ, which directly affects the conformance upper limit is defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change this value.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 37 Differential DC Input Low Voltage for DQS

Symbol	Parameter	Min	Max	Units
VILdiff (DC)	Differential Input Low	Note 1[a]	2 x [VIL(DC) - VREFQ]	V

a: Refer to Table 16 of the ONFI Specification Revision 4.2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [VIH(DC) max, VIL (DC) min] for single-ended signals as well as the limitations for overshoot and undershoot in Table 13.

Test References

See *Table 16* in *Section 2.12* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe negative pulses in this burst. A valid Strobe negative pulse starts at the 0V crossing on a valid Strobe falling edge and ends at the 0V crossing on the following valid Strobe rising edge.
4 For the first valid Strobe negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the VBASE measurement. Take the VBASE measurement result as the VIL.diff(DC) value.
5 Continue the previous step for the rest of the valid Strobe negative pulses found in the burst.
6 Determine the worst result from the set of VIL.diff(DC) measured.

Expected / Observable Results

The worst measured Input Low Voltage VIL.diff(DC) must meet the limits defined in the ONFI specification.

Differential READ Cycle Tests for Strobe

Refer to "Understanding ONFI Concepts for Measurements" on page 27 to read about the conceptual information associated with each test.

VOH.diff(AC) for DQS

Test Overview

The purpose of this test is to verify that the high level Voltage value of the test signal within a valid sampling window must be within the conformance limit of the VOH.diff(AC) value as specified in the ONFI specification.

The value of VccQ, which directly affects the conformance upper limit is defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change this value.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 38 Differential AC Output High Voltage for DQS

Symbol	Parameter	Value	Units
VOH.diff(AC)	AC Output High Voltage	0.2 * VccQ	mV

Test References

See *Table 43* in *Section 4.9* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid Strobe positive pulses in this burst. A valid Strobe positive pulse starts at the 0V crossing on a valid Strobe rising edge and ends at the 0V crossing on the following valid Strobe falling edge.
4. For the first valid positive pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the VTOP measurement. Take the VTOP measurement result as the VOH.diff(AC) value.
5. Continue the previous step for the rest of the valid Strobe positive pulses that were found in the burst.
6. Determine the worst result from the set of VOH.diff(AC) measured.

Expected / Observable Results

The worst measured Output High Voltage VOH.diff(AC) must meet the limits defined in the ONFI specification.

VOL.diff(AC) for DQS

Test Overview

The purpose of this test is to verify that the low level Voltage value of the test signal within a valid sampling window must be within the conformance limit of the VOL.diff(AC) value as specified in the ONFI specification.

The value of VccQ, which directly affects the conformance upper limit is defaulted to the values corresponding to the selected ONFI data interface types. However, you have the flexibility to change this value.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 39 Differential AC Output Low Voltage for DQS

Symbol	Parameter	Value	Units
VOL.diff(AC)	AC Output Low Voltage	-0.2 * VccQ	mV

Test References

See *Table 43* in *Section 4.9* of the *Open NAND Flash Interface Specification Revision 4.2*.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid Strobe negative pulses in this burst. A valid Strobe negative pulse starts at the 0V crossing on a valid Strobe falling edge and ends at the 0V crossing on the following valid Strobe rising edge.
4 For the first valid negative pulse, zoom in on the pulse so that it appears on the Oscilloscope's display and perform the VBASE measurement. Take the VBASE measurement result as the VOL.diff(AC) value.
5 Continue the previous step for the rest of the valid Strobe negative pulses that were found in the burst.
6 Determine the worst result from the set of VOL.diff(AC) measured.

Expected / Observable Results

The worst measured Output Low Voltage VOL.diff(AC) must meet the limits defined in the ONFI specification.

6 NVDDR2/NVDDR3 Timing Tests

Setting up the ONFI Test Application to run tests / 100
Timing Write Tests / 101
Timing Read Tests / 131
Timing Command and Address Tests / 168

This section provides the Methods of Implementation (MOIs) for ONFI Timing tests for Strobe, Data, Read-Enable and Chip-Enable signals using a Keysight Infiniium Oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the Keysight D9010ONFC ONFI Test Application.

NOTE The test methodology described below for each test is applicable for both NVDDR2 and NVDDR3 data interface types. The NV-DDR3 data interface includes all NV-DDR2 features; however, NVDDR2 operates at VccQ=1.8V whereas NVDDR3 operates at VccQ=1.2V.

Setting up the ONFI Test Application to run tests

1. Launch the ONFI Test Application as described in "Starting the ONFI Test Application" on page 21.
2. Connect the differential solder-in probe head to the PUTs on the ONFI device.
3. Connect the Oscilloscope probes to any Channels of the Oscilloscope.
4. On the **Set Up** tab of the ONFI Test Application:
   a. Select the required **Data Interface** type.
   b. Select or type a data rate value from the drop-down options in the **Speed Grade** area. The Test Application displays the corresponding **Timing Mode** number automatically.
   c. In the **Input Signal Setup** area, **Live** is selected by default. Select **Offline** to load one or more waveform files located on your machine.
   d. Type in or select the **Device Identifier** as well as **User Description** from the drop-down list. Enter your comments in the **Comments** text box.
5. Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.
6. Start running the selected tests. When performing the Electrical tests for Strobe and Data Signals, the ONFI Test Application will prompt you to make the proper connections. The **Connect** tab in the ONFI Test Application displays the exact number of probe connections. You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the **Configure** tab of the ONFI Test Application.

NOTE

The values for sampling rate and sampling point configuration options in the **Configure** tab differ for Digital Storage Oscilloscopes and UXR Oscilloscopes.

Sampling Rate (in GSa/s) options in DSOs are 10, 20, 40, 80 and MAX (default); whereas in UXRs, sampling rate (in GSa/s) options are 8, 16, 32, 64 (default), 128 and MAX.

The default option for **Sampling Points (Pts) for Electrical and Timing Tests Only** in DSOs is 2MPts; whereas in UXRs, the default option is 4MPts.

For more information about the functionality of various tabs and running tests using the ONFI Test Application's user interface, refer to the *Keysight D9010ONFC ONFI Test Application Online Help*.

Timing Write Tests

Refer to "Understanding ONFI Concepts for Measurements" on page 27 to read about the conceptual information associated with each test.

tDQSH

Test Overview

The purpose of this test is to verify that the width of the high level pulse of the data strobe signal is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 40 Timing Mode specific values for tDQSH

NV-DDR2/NV-DDR3 Data Input values for tDQSH			
Timing Mode #	Data Rate in MT/s	Minimum tDQSH in tDSC(avg)	Maximum tDQSH in tDSC(avg)
Mode 0	~ 66	0.45	–
Mode 1	80	0.45	–
Mode 2	~ 132	0.45	–
Mode 3	~ 166	0.45	–
Mode 4	200	0.45	–
Mode 5	~ 266	0.45	–
Mode 6	~ 332	0.45	–
Mode 7	400	0.45	–
Mode 8	~ 534	0.45	–
Mode 9	~ 666	0.45	–
Mode 10	800	0.45	–
Mode 11	~1066	0.45	–
Mode 12	1200	0.45	–
Mode 13	~1334	0.448	–
Mode 14	~1466	0.445	–
Mode 15	1600	0.444	–

Test References

See *Table 93* in *Section 4.18.3* and *Figure 75* in *Section 4.19.3.3* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising and falling DQS crossings in the WRITE burst that was found.
4. Measure all tDQSH values. Here, tDQSH is the time starting from a rising edge of the DQS and ending at the following falling edge.
5. Determine the worst result from the set of tDQSH measured.

Expected / Observable Results

The measured p-width of the data strobe signal must be within the conformance limits of the ONFI specification.

tDQSL

Test Overview

The purpose of this test is to verify that the width of the low level pulse of the data strobe signal is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 41 Timing Mode specific values for tDQSL

NV-DDR2/NV-DDR3 Data Input values for tDQSL			
Timing Mode #	Data Rate in MT/s	Minimum tDQSL in tDSC(avg)	Maximum tDQSL in tDSC(avg)
Mode 0	~ 66	0.45	–
Mode 1	80	0.45	–
Mode 2	~ 132	0.45	–
Mode 3	~ 166	0.45	–
Mode 4	200	0.45	–
Mode 5	~ 266	0.45	–
Mode 6	~ 332	0.45	–
Mode 7	400	0.45	–
Mode 8	~ 534	0.45	–
Mode 9	~ 666	0.45	–
Mode 10	800	0.45	–
Mode 11	~1066	0.45	–
Mode 12	1200	0.45	–
Mode 13	~1334	0.448	–
Mode 14	~1466	0.445	–
Mode 15	1600	0.444	–

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising and falling DQS crossings in the WRITE burst that was found.
4. Measure all tDQSL values. Here, tDQSL is the time starting from a falling edge of the DQS and ending at the following rising edge.
5. Determine the worst result from the set of tDQSL measured.

Expected / Observable Results

The measured n-width of the data strobe signal must be within the conformance limits of the ONFI specification.

tDS_tight(derate)

Test Overview

The purpose of this test is to verify that the time interval (tDS_tight) from Data (DQ rising/falling edge) setup time to the associated DQS crossing edge must be within the conformance limit as specified in the ONFI Specification.

NOTE

This test is available for Timing Mode # 4 to 10 only (for NV-DDR2) and Timing Mode # 4 to 12 only (for NV-DDR3). For Timing Mode # 0 to 3, the **Select Tests** tab of the ONFI Compliance Test Application displays tDS(derate) test instead of tDS_tight(derate) and tDS_relaxed(derate) tests.

Signals of Interest

Based on the test definition (Write cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 42 Timing Mode specific values for tDS_tight(derate)

NV-DDR2/NV-DDR3 Data Input values for tDS_tight(derate)			
Timing Mode #	Data Rate in MT/s	Minimum tDS_tight(derate) in ns	Maximum tDS_tight(derate) in ns
Mode 4	200	0.7	–
Mode 5	~ 266	0.5	–
Mode 6	~ 332	0.4	–
Mode 7	400	0.35	–
Mode 8	~ 534	0.3	–
Mode 9	~ 666	0.24	–
Mode 10	800	0.2	–
Mode 11	~1066	0.190	–
Mode 12	1200	0.175	–
Mode 13	~1334	–	–
Mode 14	~1466	–	–
Mode 15	1600	–	–

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising DQ crossings that cross VIH(AC) in the said burst.
4. Find all valid falling DQ crossings that cross VIL(AC) in the same burst.
5. For all DQ crossings found, locate all next DQS crossings that cross 0V.
6. Measure all tDS values. Here, tDS is defined as the time between the DQ crossing and the DQS crossing.
7. Find the worst tDS among the measured values and report the value as the test result.
8. Measure the mean slew rate for all the DQ and DQS edges. The Slew Rate Method can be selected from the Derated Limit Method (either Nominal or Tangent Method).
9. Use the mean slew rate for DQ and DQS to determine the ΔtDS derating value based on the derating tables.
10. The final result for the tDS test can be calculated as:

    tDS_tight(derate) = Measured tDS + ΔtDS.
11. Compare the final result with the pass limits.

Expected / Observable Results

The measured tDS_tight(derate) must be within the conformance limits of the ONFI specification.

tDS_relaxed(derate)

Test Overview

The purpose of this test is to verify that the time interval (tDS_relaxed) from Data (DQ rising/falling edge) setup time to the associated DQS crossing edge must be within the conformance limit as specified in the ONFI Specification.

NOTE

This test is available for Timing Mode # 4 to 10 only (for NV-DDR2) and Timing Mode # 4 to 12 only (for NV-DDR3). For Timing Mode # 0 to 3, the Select Tests tab of the ONFI Compliance Test Application displays tDS(derate) test instead of tDS_tight(derate) and tDS_relaxed(derate) tests.

Signals of Interest

Based on the test definition (Write cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 43 Timing Mode specific values for tDS_relaxed(derate)

NV-DDR2/NV-DDR3 Data Input values for tDS_relaxed(derate)			
Timing Mode #	Data Rate in MT/s	Minimum tDS_relaxed(derate) in ns	Maximum tDS_relaxed(derate) in ns
Mode 4	200	0.9	–
Mode 5	~ 266	0.75	–
Mode 6	~ 332	0.55	–
Mode 7	400	0.40	–
Mode 8	~ 534	0.35	–
Mode 9	~ 666	0.31	–
Mode 10	800	0.26	–
Mode 11	~1066	0.25	–
Mode 12	1200	0.23	–
Mode 13	~1334	–	–
Mode 14	~1466	–	–
Mode 15	1600	–	–

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising DQ crossings that cross VIH(AC) in the said burst.
4. Find all valid falling DQ crossings that cross VIL(AC) in the same burst.
5. For all DQ crossings found, locate all next DQS crossings that cross 0V.
6. Measure all tDS values. Here, tDS is defined as the time between the DQ crossing and the DQS crossing.
7. Find the worst tDS among the measured values and report the value as the test result.
8. Measure the mean slew rate for all the DQ and DQS edges. The Slew Rate Method can be selected from the Derated Limit Method (either Nominal or Tangent Method).
9. Use the mean slew rate for DQ and DQS to determine the ΔtDS derating value based on the derating tables.
10. The final result for the tDS test can be calculated as:

    tDS_relaxed(derate) = Measured tDS + ΔtDS.
11. Compare the final result with the pass limits.

Expected / Observable Results

The measured tDS_relaxed(derate) must be within the conformance limits of the ONFI specification.

tDH_tight(derate)

Test Overview

The purpose of this test is to verify that the time interval (tDH_tight) from Data (DQ rising/falling edge) hold time to the associated DQS crossing edge must be within the conformance limit as specified in the ONFI Specification.

NOTE

This test is available for Timing Mode # 4 to 10 only (for NV-DDR2) and Timing Mode # 4 to 12 only (for NV-DDR3). For Timing Mode # 0 to 3, the **Select Tests** tab of the ONFI Compliance Test Application displays tDH(derate) test instead of tDH_tight(derate) and tDH_relaxed(derate) tests.

Signals of Interest

Based on the test definition (Write cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 44 Timing Mode specific values for tDH_tight(derate)

NV-DDR2/NV-DDR3 Data Input values for tDH_tight(derate)			
Timing Mode #	Data Rate in MT/s	Minimum tDH_tight(derate) in ns	Maximum tDH_tight(derate) in ns
Mode 4	200	0.7	–
Mode 5	~ 266	0.5	–
Mode 6	~ 332	0.4	–
Mode 7	400	0.35	–
Mode 8	~ 534	0.3	–
Mode 9	~ 666	0.24	–
Mode 10	800	0.2	–
Mode 11	~1066	0.190	–
Mode 12	1200	0.175	–
Mode 13	~1334	–	–
Mode 14	~1466	–	–
Mode 15	1600	–	–

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising DQ crossings that cross VIH(AC) in the said burst.
4. Find all valid falling DQ crossings that cross VIL(AC) in the same burst.
5. For all DQ crossings found, locate all next DQS crossings that cross 0V.
6. Measure all tDH values. Here, tDH is defined as the time between the DQ crossing and the DQS crossing.
7. Find the worst tDH among the measured values and report the value as the test result.
8. Measure the mean slew rate for all the DQ and DQS edges. The Slew Rate Method can be selected from the Derated Limit Method (either Nominal or Tangent Method).
9. Use the mean slew rate for DQ and DQS to determine the ΔtDH derating value based on the derating tables.
10. The final result for the tDH test can be calculated as:

    tDH_tight(derate) = Measured tDH + ΔtDH.
11. Compare the final result with the pass limits.

Expected / Observable Results

The measured tDH_tight(derate) must be within the conformance limits of the ONFI specification.

tDH_relaxed(derate)

Test Overview

The purpose of this test is to verify that the time interval (tDH_relaxed) from Data (DQ rising/falling edge) hold time to the associated DQS crossing edge must be within the conformance limit as specified in the ONFI Specification.

NOTE This test is available for Timing Mode # 4 to 10 only (for NV-DDR2) and Timing Mode # 4 to 12 only (for NV-DDR3). For Timing Mode # 0 to 3, the **Select Tests** tab of the ONFI Compliance Test Application displays tDH(derate) test instead of tDH_tight(derate) and tDH_relaxed(derate) tests.

Signals of Interest

Based on the test definition (Write cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 45 Timing Mode specific values for tDH_relaxed(derate)

NV-DDR2/NV-DDR3 Data Input values for tDH_relaxed(derate)			
Timing Mode #	Data Rate in MT/s	Minimum tDH_relaxed(derate) in ns	Maximum tDH_relaxed(derate) in ns
Mode 4	200	0.9	–
Mode 5	~ 266	0.75	–
Mode 6	~ 332	0.55	–
Mode 7	400	0.40	–
Mode 8	~ 534	0.35	–
Mode 9	~ 666	0.31	–
Mode 10	800	0.26	–
Mode 11	~1066	0.25	–
Mode 12	1200	0.23	–
Mode 13	~1334	–	–
Mode 14	~1466	–	–
Mode 15	1600	–	–

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising DQ crossings that cross VIH(AC) in the said burst.
4. Find all valid falling DQ crossings that cross VIL(AC) in the same burst.
5. For all DQ crossings found, locate all next DQS crossings that cross 0V.
6. Measure all tDH values. Here, tDH is defined as the time between the DQ crossing and the DQS crossing.
7. Find the worst tDH among the measured values and report the value as the test result.
8. Measure the mean slew rate for all the DQ and DQS edges. The Slew Rate Method can be selected from the Derated Limit Method (either Nominal or Tangent Method).
9. Use the mean slew rate for DQ and DQS to determine the ΔtDH derating value based on the derating tables.
10. The final result for the tDH test can be calculated as:

    tDH_relaxed(derate) = Measured tDH + ΔtDH.
11. Compare the final result with the pass limits.

Expected / Observable Results

The measured tDH_relaxed(derate) must be within the conformance limits of the ONFI specification.

tDS(derate)

Test Overview

The purpose of this test is to verify that the time interval (tDS) from Data (DQ rising/falling edge) setup time to the associated DQS crossing edge must be within the conformance limit as specified in the ONFI Specification.

NOTE This test is available for Timing Mode # 0 to 3 only. For Timing Mode # 4 to 10 (for NV-DDR2) and Timing Mode # 4 to 12 (for NV-DDR3), the **Select Tests** tab of the ONFI Compliance Test Application displays tDS_tight(derate) and tDS_relaxed(derate) tests instead of tDS(derate) test.

Signals of Interest

Based on the test definition (Write cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 46 Timing Mode specific values for tDS(derate)

NV-DDR2/NV-DDR3 Data Input values for tDS(derate)			
Timing Mode #	Data Rate in MT/s	Minimum tDS(derate) in ns	Maximum tDS(derate) in ns
Mode 0	~ 66	4.0	–
Mode 1	80	3.3	–
Mode 2	~ 132	2.0	–
Mode 3	~ 166	1.1	–

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising DQ crossings that cross VIH(AC) in the said burst.
4. Find all valid falling DQ crossings that cross VIL(AC) in the same burst.
5. For all DQ crossings found, locate all next DQS crossings that cross 0V.
6. Measure all tDS values. Here, tDS is defined as the time between the DQ crossing and the DQS crossing.
7. Find the worst tDS among the measured values and report the value as the test result.
8. Measure the mean slew rate for all the DQ and DQS edges. The Slew Rate Method can be selected from the Derated Limit Method (either Nominal or Tangent Method).
9. Use the mean slew rate for DQ and DQS to determine the ΔtDS derating value based on the derating tables.
10. The final result for the tDS test can be calculated as:

    tDS(derate) = Measured tDS + ΔtDS.
11. Compare the final result with the pass limits.

Expected / Observable Results

The measured value of tDS(derate) must be within the conformance limits of the ONFI specification.

tDH(derate)

Test Overview

The purpose of this test is to verify that the time interval tDH from Data (DQ rising/falling edge) hold time to the associated DQS crossing edge must be within the conformance limit as specified in the ONFI Specification.

NOTE This test is available for Timing Mode # 0 to 3 only. For Timing Mode # 4 to 10 (for NV-DDR2) and Timing Mode # 4 to 12 (for NV-DDR3), the **Select Tests** tab of the ONFI Compliance Test Application displays tDH_tight(derate) and tDH_relaxed(derate) tests instead of tDH(derate) test.

Signals of Interest

Based on the test definition (Write cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 47 Timing Mode specific values for tDH(derate)

NV-DDR2/NV-DDR3 Data Input values for tDH(derate)			
Timing Mode #	Data Rate in MT/s	Minimum tDH(derate) in ns	Maximum tDH(derate) in ns
Mode 0	~ 66	4.0	–
Mode 1	80	3.3	–
Mode 2	~ 132	2.0	–
Mode 3	~ 166	1.1	–

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising DQ crossings that cross VIH(AC) in the said burst.
4. Find all valid falling DQ crossings that cross VIL(AC) in the same burst.
5. For all DQ crossings found, locate all next DQS crossings that cross 0V.
6. Measure all tDH values. Here, tDH is defined as the time between the DQ crossing and the DQS crossing.
7. Find the worst tDH among the measured values and report the value as the test result.
8. Measure the mean slew rate for all the DQ and DQS edges. The Slew Rate Method can be selected from the Derated Limit Method (either Nominal or Tangent Method).
9. Use the mean slew rate for DQ and DQS to determine the ΔtDH derating value based on the derating tables.
10. The final result for the tDH test can be calculated as:

    tDH(derate) = Measured tDH + ΔtDH.
11. Compare the final result with the pass limits.

Expected / Observable Results

The measured value of tDH(derate) must be within the conformance limits of the ONFI specification.

tDSC(avg)

Test Overview

The purpose of this test is to measure the average write cycle time of the Data Strobe signal over any 200 consecutive periods.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 48 Timing Mode specific values for tDSC(avg)

NV-DDR2/NV-DDR3 values for tDSC(avg)			
Timing Mode #	Data Rate in MT/s	Minimum tDSC(avg) in ns	Maximum tDSC(avg) in ns
Mode 0	~ 66	30	–
Mode 1	80	25	–
Mode 2	~ 132	15	–
Mode 3	~ 166	12	–
Mode 4	200	10	–
Mode 5	~ 266	7.5	–
Mode 6	~ 332	6	–
Mode 7	400	5	–
Mode 8	~ 534	3.75	–
Mode 9	~ 666	3	–
Mode 10	800	2.5	–
Mode 11	~1066	1.875	–
Mode 12	1200	1.667	–
Mode 13	~1334	1.5	–
Mode 14	~1466	1.364	–
Mode 15	1600	1.25	–

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

As an example, consider the input test signal with a frequency of 1KHz and 202 cycles acquired.

This measurement measures the difference between every period inside a 200 cycle window with the average of the whole window. The average is measured between consecutive falling edges of the Data Strobe signal.

1. Measure the average for periods 1-200.
2. Measure the difference between period #1 and the average. Save the result as a measurement result.
3. Measure the difference between period #2 and the average. Save the result.
4. Continue measuring the difference between each period and the average until period #200 is compared to the average (therefore, 200 measurements are generated).
5. Slide the window by one and measure the average for periods 2-201.
6. Compare period #2 with the new average.
7. Continue measuring the difference between each period and the average until period #201 is compared to the average (therefore, 200 more measurements are generated, making a total of 400 measurements).
8. Slide the window by one and measure the average for periods 3-202.
9. Compare period #3 with the new average.
10. Continue measuring the difference between each period and the average until period #202.

Expected / Observable Results

The wost value of tDSC(avg) measurement must be within the conformance limits as specified in the ONFI specification.

tDSC(abs)

Test Overview

The purpose of this test is to measure the absolute write cycle time of the Data Strobe signal over all available periods.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 49 Constant Timing Parameter values for tDSC(abs)

Symbol	Min	Max	Units
tDSC(abs)	tDSC(avg) + tJITper(DQS)min	tDSC(avg) + tJITper(DQS)max	ns

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

As an example, consider the input test signal with a frequency of 1KHz and 202 cycles acquired.

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid WRITE burst found.
3 Measure the absolute period from the rising edge to the next consecutive rising edge of the Data Strobe signal over all write cycles.
4 Calculate the minimum and maximum values for tDSC(abs) using the equations:

   tDSC(abs)min = tDSC(avg) + tJITper(DQS)min

   tDSC(abs)max = tDSC(avg) + tJITper(DQS)max

5 Report the worst tDSC(abs) value as the final test result.

Expected / Observable Results

The wost value of tDSC(abs) must be within the conformance limits as specified in the ONFI specification.

SRIseR

Test Overview

The purpose of this test is to verify that the single-ended input slew rate for the rising edge of the write cycle of test signal must be within the conformance limits as specified in the ONFI specification.

Signals of Interest

Based on the test definition (Write cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 50 Maximum and Minimum Single-ended Input Slew Rate for Rising Edge

Symbol	Min	Max	Units
SRIseR	1.0	4.5	V/ns

Test References

See *Table 62* in *Section 4.13.2* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid Strobe rising edges in this burst. A valid Strobe rising edge starts at the last crossing of VREFQ crossing and the first crossing of VIH(AC).
4 For all valid Strobe rising edges, find the transition time, tRISE, which is the time that starts at the last crossing of VREFQ crossing and the first crossing of VIH(AC).
5 Calculate SRIseR = [VIH(AC) – VREFQ] / tRISE.
6 Determine the worst result from the set of SRIseR values that are measured.

Expected / Observable Results

The worst measured SRIseR must be within the conformance limits of the ONFI specification.

SRIseF

Test Overview

The purpose of this test is to verify that the single-ended input slew rate for the falling edge of the write cycle of test signal must be within the conformance limits as specified in the ONFI specification.

Signals of Interest

Based on the test definition (Write cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 51 Maximum and Minimum Single-ended Input Slew Rate for Falling Edge

Symbol	Min	Max	Units
SRIseF	1.0	4.5	V/ns

Test References

See *Table 62* in *Section 4.13.2* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid Strobe falling edges in this burst. A valid Strobe falling edge starts at the last crossing of VREFQ crossing and the first crossing of VIL(AC).
4. For all valid Strobe falling edges, find the transition time, tFALL, which is the time that starts at the last crossing of VREFQ crossing and the first crossing of VIL(AC).
5. Calculate SRIseF = [VREFQ – VIL(AC)] / tFALL.
6. Determine the worst result from the set of SRIseF values that are measured.

Expected / Observable Results

The worst measured SRIseF must be within the conformance limits of the ONFI specification.

tDIPW

Test Overview

The purpose of this test is to verify that the DQ input pulse width is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Write cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 52 Timing Mode specific values for tDIPW

NV-DDR2/NV-DDR3 Data Input values for tDIPW			
Timing Mode #	Data Rate in MT/s	Minimum tDIPW in tDSC(avg)	Maximum tDIPW in tDSC(avg)
Mode 0	~ 66	0.31	–
Mode 1	80	0.31	–
Mode 2	~ 132	0.31	–
Mode 3	~ 166	0.31	–
Mode 4	200	0.31	–
Mode 5	~ 266	0.31	–
Mode 6	~ 332	0.31	–
Mode 7	400	0.31	–
Mode 8	~ 534	0.31	–
Mode 9	~ 666	0.31	–
Mode 10	800	0.31	–
Mode 11	~1066	0.33	–
Mode 12	1200	0.33	–
Mode 13	~1334	0.33	–
Mode 14	~1466	0.33	–
Mode 15	1600	0.33	–

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the DQ Input signal.
2. Take the first valid WRITE burst found..
3. On the burst that is found, measure the width of the DQ pulse between the first crossing of VREFQ(DC) and the consecutive crossing of VREFQ(DC). Record this value as tDIPW.
4. Determine the worst result from the set of tDIPW measured.

Expected / Observable Results

The measured tDIPW must be within the conformance limits of the ONFI specification.

tWPRE

Test Overview

The purpose of this test is to verify that the time when the DQS starts to drive low (first preamble behavior) to the first DQS signal crossing for the Write cycle, is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 53 Constant Timing Parameter Values for tWPRE

Symbol	Parameter	Min	Max	Units
tWPRE	NV-DDR2/NV-DDR3 Write Preamble Time	15	–	ns

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find tLZBeginPoint of the said burst.
4. Find the first rising edge on DQS of the found burst.
5. Report the value of tWPRE. Here, tWPRE is the time between the rising DQS edge's crossings and the tLZBeginPoint found.

Expected / Observable Results

The measured tWPRE must be within the conformance limits of the ONFI specification.

tWPRE2

Test Overview

The purpose of this test is to verify that the time when the DQS write preamble (with ODT enabled) starts to drive low (second preamble behavior) to the first DQS signal crossing for the Write cycle, is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 54 Constant Timing Parameter Values for tWPRE2

Symbol	Parameter	Min	Max	Units
tWPRE2	NV-DDR2/NV-DDR3 Write Second Preamble Time	25	–	ns

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find tLZBeginPoint of the said burst.
4. Find the first rising edge on DQS of the found burst.
5. With ODT enabled, report the value of tWPRE2. Here, tWPRE2 is the time between the rising DQS edge’s crossings and the tLZBeginPoint found.

Expected / Observable Results

The measured tWPRE2 must be within the conformance limits of the ONFI specification.

tDBS

Test Overview

The purpose of this test is to measure the DQS (DQS_t) high setup to CE_n low during data burst.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS, CE

Signals required to perform the test on the Oscilloscope:

- DQS, CE
- DQ

Test Definition Notes from the Specification

Table 55 Constant Timing Parameter Values for tDBS

Symbol	Min	Max	Units
tDBS	5	–	ns

Test References

See Table 91 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising and falling DQS crossings in the WRITE burst that was found.
4. Measure all tDBS values. Here, tDBS is the setup time from the start of the DQS (DQS_t) high signal to the falling edge (start of CE_n low) of the Chip Enable signal during data burst.

Expected / Observable Results

The measured value of tDBS for the Data Strobe signal must be within the conformance limits of the ONFI specification.

tCS-Write

Test Overview

The purpose of this test is to measure the CE_n setup time for data burst with ODT disabled.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS, CE

Signals required to perform the test on the Oscilloscope:

- DQS, CE
- DQ

Test Definition Notes from the Specification

Table 56 Constant Timing Parameter Values for tCS-Write

Symbol	Parameter	Min	Max	Units
tCS	CE_n setup time	20	–	ns

Test References

See Table 91 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire a DQS signal and find the first valid WRITE burst on it.
2. Measure tCS-write as the time difference between the falling edge of the CE_n signal and the rising edge (end of preamble) of the first valid WRITE burst found on the DQS signal.

Expected / Observable Results

The measured value of tCS-Write must be within the conformance limits as specified in the ONFI specification.

tCDQSS

Test Overview

The purpose of this test is to measure the setup time for the data input start pulse on the Data Strobe signal.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 57 Constant Timing Parameter Values for tCDQSS

Symbol	Min	Max	Units
tCDQSS	30	–	ns

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising and falling DQS crossings in the WRITE burst that was found.
4. Measure all tCDQSS values. Here, tCDQSS is the setup time from the start of the Write Preamble of the DQS signal to the immediately prior DQS rising edge.
5. Determine the worst result from the set of tCDQSS measured.

Expected / Observable Results

The measured value of tCDQSS for the Data Strobe signal must be within the conformance limits of the ONFI specification.

tWPST

Test Overview

The purpose of this test is to verify that the DQS Write Postamble time is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Write cycle only):

- DQS, CLE

Signals required to perform the test on the Oscilloscope:

- DQS
- CLE
- WE
- DQ

Test Definition Notes from the Specification

Table 58 Constant Timing Parameter Values for tWPST

Symbol	Parameter	Min	Max	Units
tWPST	NV-DDR2/NV-DDR3 Write Postamble Time	6.5	–	ns

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1 Acquire and split the Read and Write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Measure the difference between the final falling edge of WRITE burst up to the rising edge of the CE signal.
4 Report the value of tWPST. Here, tWPST is the time between the final falling edge of the DQS crossing and the rising edge of the CLE signal.

Expected / Observable Results

The measured tWPST must be within the conformance limits of the ONFI specification.

tWPSTH

Test Overview

The purpose of this test is to verify that the DQS Write Postamble Hold time is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Write cycle only):

- CLE, WE

Signals required to perform the test on the Oscilloscope:

- DQS
- CLE
- WE
- DQ

Test Definition Notes from the Specification

Table 59 Constant Timing Parameter Values for tWPSTH

Symbol	Parameter	Min	Max	Units
tWPSTH	NV-DDR2/NV-DDR3 Write Postamble Hold Time	25	–	ns

Test References

See Table 93 in Section 4.18.3 and Figure 75 in Section 4.19.3.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Get the last DQS edge.
4. From the last DQS edge, find the next CLE rising edge.
5. From the CLE rising edge, find the next WE falling edge.
6. The time difference between the CLE rising edge and the next WE falling edge is tWPSTH.

Expected / Observable Results

The measured tWPSTH must be within the conformance limits of the ONFI specification.

Timing Read Tests

Refer to "Understanding ONFI Concepts for Measurements" on page 27 to read about the conceptual information associated with each test.

SROseR

Test Overview

The purpose of this test is to verify that the single-ended output slew rate for the rising edge of the read cycle of test signal must be within the conformance limits as specified in the ONFI specification.

Signals of Interest

Based on the test definition (Read cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 60 NVDDr2 maximum and minimum single-ended output slew rate for rising edge without ZQ calibration

Symbol	Description	Min	Max	Unit
SROseR	50 Ohms	0.60	4.0	V/ns

Table 61 NVDDr2 maximum and minimum single-ended output slew rate for rising edge with ZQ calibration

Symbol	Description	Min	Max	Unit
SROseR	50 Ohms	0.90	3.5	V/ns

Table 62 NVDDr3 maximum and minimum single-ended output slew rate for rising edge with ZQ calibration

Symbol	Description	Min	Max	Unit
SROseR	50 Ohms	0.60	3.5	V/ns

Test References

- See *Table 34, Table 36, Table 38,* and *Figure 40* in *Section 4.9* of the *Open NAND Flash Interface Specification Revision 4.0.*

  or

- See *Table 37, Table 39, Table 41, Table 43,* and *Figure 43* in *Section 4.9* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid Strobe rising edges in this burst. A valid Strobe rising edge starts at the rising edge of VOL(AC) to the rising edge of VOH(AC).
4. For all valid Strobe rising edges, find the transition time, tRISE, which is the time during rising edge of VOL(AC) to VOH(AC).
5. Calculate SROseR = [VOH(AC) – VOL(AC)] / tRISE.
6. Determine the worst result from the set of SROseR values that are measured.

Expected / Observable Results

The worst measured SROseR must be within the conformance limits of the ONFI specification.

SROseF

Test Overview

The purpose of this test is to verify that the single-ended output slew rate for the falling edge of the read cycle of test signal must be within the conformance limits as specified in the ONFI specification.

Signals of Interest

Based on the test definition (Read cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 63 NVDDr2 maximum and minimum single-ended output slew rate for rising edge without ZQ calibration

Symbol	Description	Min	Max	Unit
SROseF	50 Ohms	0.60	4.0	V/ns

Table 64 NVDDr2 maximum and minimum single-ended output slew rate for rising edge with ZQ calibration

Symbol	Description	Min	Max	Unit
SROseF	50 Ohms	0.90	3.5	V/ns

Table 65 NVDDr3 maximum and minimum single-ended output slew rate for rising edge with ZQ calibration

Symbol	Description	Min	Max	Unit
SROseF	50 Ohms	0.60	3.5	V/ns

Test References

- See *Table 34, Table 36, Table 38,* and *Figure 40* in *Section 4.9* of the *Open NAND Flash Interface Specification Revision 4.0.*

  or

- See *Table 37, Table 39, Table 41, Table 43,* and *Figure 43* in *Section 4.9* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid Strobe falling edges in this burst. A valid Strobe falling edge starts at the falling edge of VOH(AC) to the falling edge of VOL(AC).
4 For all valid Strobe falling edges, find the transition time, tFALL, which is the time during falling edge of VOH(AC) to VOL(AC).
5 Calculate SROseF = [VOH(AC) – VOL(AC)] / tFALL.
6 Determine the worst result from the set of SROseF values that are measured.

Expected / Observable Results

The worst measured SROseF must be within the conformance limits of the ONFI specification.

SRORdiff

Test Overview

The purpose of this test is to verify that the differential output slew rate for rising edge on the read cycle of the test signal must be within the conformance limit of the SRORdiff value as specified in the ONFI specification.

Signals of Interest

Based on the test definition (Read cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 66 Differential Output Slew Rate Rising Edge

Symbol	Parameter	Value	Units
SRORdiff	Differential Output Slew Rate Rising Edge	[VOHdiff(AC) – VOLdiff(AC)] / tRISEdiff	V/ns

Test References

See *Table 43* and *Figure 44* in *Section 4.9* of the *Open NAND Flash Interface Specification Revision 4.2*.

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid Strobe rising edges in this burst. A valid Strobe rising edge starts at the VOLdiff(AC) crossing and ends at the following VOHdiff(AC) crossing.
4. For all valid Strobe rising edges, find the transition time, tRISEdiff, which is the time that starts at the VOLdiff(AC) crossing and ends at the following VOHdiff(AC) crossing.
5. Calculate SRORdiff = [VOHdiff(AC) – VOLdiff(AC)] / tRISEdiff.
6. Determine the worst result from the set of SRORdiff values that are measured.

Expected / Observable Results

The worst measured SRORdiff must be within the conformance limits of the ONFI specification.

SROFdiff

Test Overview

The purpose of this test is to verify that the differential output slew rate for falling edge on the read cycle of the test signal must be within the conformance limit of the SROFdiff value as specified in the ONFI specification.

Signals of Interest

Based on the test definition (Read cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 67 Differential Output Slew Rate Falling Edge

Symbol	Parameter	Value	Units
SROFdiff	Differential Output Slew Rate Falling Edge	[VOHdiff(AC) – VOLdiff(AC)] / tFALLdiff	V/ns

Test References

See *Table 43* and *Figure 44* in *Section 4.9* of the *Open NAND Flash Interface Specification Revision 4.2*.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid Strobe falling edges in this burst. A valid Strobe falling edge starts at the VOHdiff(AC) crossing and ends at the following VOLdiff(AC) crossing.
4. For all valid Strobe falling edges, find the transition time, tFALLdiff, which is the time that starts at the VOHdiff(AC) crossing and ends at the following VOLdiff(AC) crossing.
5. Calculate SROFdiff = [VOHdiff(AC) – VOLdiff(AC)] / tFALLdiff.
6. Determine the worst result from the set of SROFdiff values that are measured.

Expected / Observable Results

The worst measured SROFdiff must be within the conformance limits of the ONFI specification.

tQH

Test Overview

The purpose of this test is to verify that the time interval from each DQS crossing (rising and falling edge) to the consecutive starting point of Data output hold time (DQ crossings) is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Read cycle only):

- DQS, DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 68 Constant Timing Parameter Values for tQH

Symbol	Parameter	Min	Max	Units
tQH	NV-DDR2/NV-DDR3 DQ-DQS hold time, DQS to first DQ to go non-valid, per access	0.37	–	tRC(avg)

Table 69 Timing Mode specific values for tRC(avg)

NV-DDR2 Data Input values for tRC(avg)			
Timing Mode #	Data Rate in MT/s	Minimum tRC(avg) in ns	Maximum tRC(avg) in ns
Mode 0	~ 66	30	–
Mode 1	80	25	–
Mode 2	~ 132	15	–
Mode 3	~ 166	12	–
Mode 4	200	10	–
Mode 5	~ 266	7.5	–
Mode 6	~ 332	6	–
Mode 7	400	5	–
Mode 8	~ 534	3.75	–
Mode 9	~ 666	3	–
Mode 10	800	2.5	–
Mode 11	~1066	1.875	–
Mode 12	1200	1.667	–
Mode 13	~1334	1.5	–
Mode 14	~1466	1.364	–
Mode 15	1600	1.25	–

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid rising and falling DQS crossings in the said burst.
4. For all DQS crossings found, locate the consecutive starting point of the nearest DQ output hold time.
5. Measure the time difference between the DQS crossing (rising and falling) and consecutive starting point of the nearest DQ output hold time as tQH.
6. Determine the worst result from the set of tQH values that are measured.

Expected / Observable Results

The worst value of tQH must be within the conformance limits of the ONFI specification.

tDQSQ

Test Overview

The purpose of this test is to verify that the measured skew between the starting edges of the DQ signal and the DQS transitions (rising and falling edges) is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Read cycle only):

- DQS, DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 70 Timing Mode specific values for tDQSQ

NV-DDR2/NV-DDR3 Data Output values for tDQSQ			
Timing Mode #	Data Rate in MT/s	Minimum tDQSQ in ns	Maximum tDQSQ in ns
Mode 0	~ 66	–	2.5
Mode 1	80	–	2.0
Mode 2	~ 132	–	1.4
Mode 3	~ 166	–	1.0
Mode 4	200	–	0.8
Mode 5	~ 266	–	0.6
Mode 6	~ 332	–	0.5
Mode 7	400	–	0.4
Mode 8	~ 534	–	0.35
Mode 9	~ 666	–	0.3
Mode 10	800	–	0.25
Mode 11	~1066	–	0.188
Mode 12	1200	–	0.167
Mode 13	~1334	–	0.150
Mode 14	~1466	–	0.136
Mode 15	1600	–	0.125

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid DQS transitions and locate the nearest starting edge of the DQ output in the burst.
4 Measure skew from each rising and falling edge of DQS to the nearest starting edge of the DQ signal, respectively.
5 Determine the worst result from the set of tDQSQ values that are measured.

Expected / Observable Results

The worst measured value of tDQSQ must be within the conformance limits of the ONFI specification.

tDVW

Test Overview

The purpose of this test is to verify that the time interval of the valid output window of the Data signal is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Read cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 71 Constant Timing Parameter Values for tDVW

Symbol	Parameter	Min	Max	Units
tDVW	NV-DDR2/NV-DDR3 Output data valid window	tDVW = tQH - tDQSQ		ns

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid rising and falling DQ crossings in the said burst.
4. Measure the time interval between the starting and ending edges of the DQ signal as tDVW. You may calculate tDVW using the equation:

   tDVW = tQH - tDQSQ
5. Determine the worst result from the set of tDVW values that are measured.

Expected / Observable Results

The worst measured value of tDVW must be within the conformance limits of the ONFI specification.

tQSH

Test Overview

The purpose of this test is to verify that the time interval for the high pulse of the Data Strobe output signal (if differential DQS Plus signal is high) is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Read cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 72 Constant Timing Parameter Values for tQSH

Symbol	Parameter	Min	Max	Units
tQSH	NV-DDR2/NV-DDR3 DQS output high time (if differential, DQS_t is high)	0.37	–	tRC(avg)

Table 73 Timing Mode specific values for tRC(avg)

NV-DDR2/NV-DDR3 Data Input values for tRC(avg)			
Timing Mode #	Data Rate in MT/s	Minimum tRC(avg) in ns	Maximum tRC(avg) in ns
Mode 0	~ 66	30	–
Mode 1	80	25	–
Mode 2	~ 132	15	–
Mode 3	~ 166	12	–
Mode 4	200	10	–
Mode 5	~ 266	7.5	–
Mode 6	~ 332	6	–
Mode 7	400	5	–
Mode 8	~ 534	3.75	–
Mode 9	~ 666	3	–
Mode 10	800	2.5	–
Mode 11	~1066	1.875	–
Mode 12	1200	1.667	–
Mode 13	~1334	1.5	–
Mode 14	~1466	1.364	–
Mode 15	1600	1.25	–

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid rising and falling DQS crossings in the said burst.
4. For all DQS crossings found, measure the time interval between the rising and falling edges for the high pulse of the output Data Strobe signal.
5. Determine the worst result from the set of tQSH values that are measured.

Expected / Observable Results

The measured time interval for the high pulse of the Data Strobe output signal (if differential DQS Plus signal is high) must be within the conformance limits of the ONFI specification.

tQSL

Test Overview

The purpose of this test is to verify that the time interval for the low pulse of the Data Strobe output signal (if differential DQS Plus signal is low) is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Read cycle only):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 74 Constant Timing Parameter Values for tQSL

Symbol	Parameter	Min	Max	Units
tQSL	NV-DDR2/NV-DDR3 DQS output high time (if differential, DQS_t is low)	0.37	–	tRC(avg)

Table 75 Timing Mode specific values for tRC(avg)

NV-DDR2/NV-DDR3 Data Input values for tRC(avg)			
Timing Mode #	Data Rate in MT/s	Minimum tRC(avg) in ns	Maximum tRC(avg) in ns
Mode 0	~ 66	30	–
Mode 1	80	25	–
Mode 2	~ 132	15	–
Mode 3	~ 166	12	–
Mode 4	200	10	–
Mode 5	~ 266	7.5	–
Mode 6	~ 332	6	–
Mode 7	400	5	–
Mode 8	~ 534	3.75	–
Mode 9	~ 666	3	–
Mode 10	800	2.5	–
Mode 11	~1066	1.875	–
Mode 12	1200	1.667	–
Mode 13	~1334	1.5	–
Mode 14	~1466	1.364	–
Mode 15	1600	1.25	–

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid rising and falling DQS crossings in the said burst.
4. For all DQS crossings found, measure the time interval between the falling and rising edges for the low pulse of the output Data Strobe signal.
5. Determine the worst result from the set of tQSL values that are measured.

Expected / Observable Results

The measured time interval for the low pulse of the Data Strobe output signal (if differential DQS Plus signal is low) must be within the conformance limits of the ONFI specification.

tAC

Test Overview

The purpose of this test is to verify that the time interval from Read Enable signal transition (end of Read preamble) to the starting edge of the valid data window of the DQ signal is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Read cycle only):

- DQ, RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- RE

Test Definition Notes from the Specification

Table 76 Constant Timing Parameter Values for tAC

Symbol	Parameter	Min	Max	Units
tAC	NV-DDR2/NV-DDR3 Access window of DQ[7:0] from RE_n (RE_t/RE_c crosspoint)	2	25	ns

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid READ burst found.
3. Find the first starting edge of the DQ signal in the said burst.
4. Measure the time interval from the end of Read Preamble (or RE signal transition) to the first starting (rising/falling) edge of the DQ signal.
5. Report the measured value as tAC.

Expected / Observable Results

The measured value of tAC must be within the conformance limits of the ONFI specification.

tDQSRE

Test Overview

The purpose of this test is to verify that the time interval between each Read Enable signal transition (rising/falling) to each corresponding Data Strobe signal transition (rising/falling) is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Read cycle only):

- DQS, RE

Signals required to perform the test on the Oscilloscope:

- DQS
- RE

Test Definition Notes from the Specification

Table 77 Constant Timing Parameter Values for tDQSRE

Symbol	Parameter	Min	Max	Units
tDQSRE	NV-DDR2/NV-DDR3 Access window of DQS from RE_n (RE_t/RE_c)	2	25	ns

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take all valid READ bursts found.
3. For each crossing (rising and falling edge) of the DQS signal, locate the preceding rising and falling RE signal crossings in the said burst.
4. Measure the time interval between each crossing (rising/falling) of the Read Enable signal and the subsequent crossing (rising/falling) of the DQS signal.
5. Determine the worst result from the set of tDQSRE values that are measured.

Expected / Observable Results

The worst measured value of tDQSRE must be within the conformance limits of the ONFI specification.

tRC(avg)

Test Overview

The purpose of this test is to measure the average read cycle time of the Read Enable signal over any 200 consecutive periods.

Signals of Interest

Based on the test definition (Read cycle only):

- RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- RE

Test Definition Notes from the Specification

Table 78 Timing Mode specific values for average read cycle time

NV-DDR2/NV-DDR3 Data Input values for tRC(avg)			
Timing Mode #	Data Rate in MT/s	Minimum tRC(avg) in ns	Maximum tRC(avg) in ns
Mode 0	~ 66	30	–
Mode 1	80	25	–
Mode 2	~ 132	15	–
Mode 3	~ 166	12	–
Mode 4	200	10	–
Mode 5	~ 266	7.5	–
Mode 6	~ 332	6	–
Mode 7	400	5	–
Mode 8	~ 534	3.75	–
Mode 9	~ 666	3	–
Mode 10	800	2.5	–
Mode 11	~1066	1.875	–
Mode 12	1200	1.667	–
Mode 13	~1334	1.5	–
Mode 14	~1466	1.364	–
Mode 15	1600	1.25	–

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

As an example, consider the input test signal with a frequency of 1KHz and 202 cycles acquired.

This measurement measures the difference between every period inside a 200 cycle window with the average of the whole window. The average is measured between consecutive rising edges of the Read Enable signal.

1. Measure the average for periods 1-200.
2. Measure the difference between period #1 and the average. Save the result as a measurement result.
3. Measure the difference between period #2 and the average. Save the result.
4. Continue measuring the difference between each period and the average until period #200 is compared to the average (therefore, 200 measurements are generated).
5. Slide the window by one and measure the average for periods 2-201.
6. Compare period #2 with the new average.
7. Continue measuring the difference between each period and the average until period #201 is compared to the average (therefore, 200 more measurements are generated, making a total of 400 measurements).
8. Slide the window by one and measure the average for periods 3-202.
9. Compare period #3 with the new average.
10. Continue measuring the difference between each period and the average until period #202.

Expected / Observable Results

The wost measured value of tRC(avg) must be within the conformance limits as specified in the ONFI specification.

tRC(abs)

Test Overview

The purpose of this test is to measure the absolute read cycle time of the Read Enable signal over all available periods.

Signals of Interest

Based on the test definition (Read cycle only):

- RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- RE

Test Definition Notes from the Specification

Table 79 Constant Timing Parameter values for Data Strobe absolute read cycle period

Symbol	Min	Max	Units
tRC(abs)	tRC(avg) + tJITper(RE_n)min	tRC(avg) + tJITper(RE_n)max	ns

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

As an example, consider the input test signal with a frequency of 1KHz and 202 cycles acquired.

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid READ burst found.
3. Measure the absolute period between the consecutive rising edges over all read cycles of the Read Enable signal.
4. Calculate the minimum and maximum values for tRC(abs) using the equations:

   tRC(abs)min = tRC(avg) + tJITper(RE_n)min

   tRC(abs)max = tRC(avg) + tJITper(RE_n)max
5. Report the worst tRC(abs) value as the final test result.

Expected / Observable Results

The wost value of tRC(abs) must be within the conformance limits as specified in the ONFI specification.

tREH(avg)

Test Overview

The purpose of this test is to measure the average width of the high level pulse of the Read Enable signal over any 200 consecutive periods.

Signals of Interest

Based on the test definition (Read cycle only):

- RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- RE

Test Definition Notes from the Specification

Table 80 Constant Timing Parameter Values for average high level width of read cycle

Symbol	Parameter	Min	Max	Units
tREH(avg)	NV-DDR2/NV-DDR3 Average RE_n/RE_t high level width	0.45	0.55	tRC(avg)

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

As an example, consider the input test signal with a frequency of 1KHz and 202 cycles acquired.

This measurement measures the difference between every period inside a 200 cycle window with the average of the whole window. The average is measured over the time difference between each rising and consecutive falling edge for each high pulse of the Read Enable signal.

1 Measure the average for periods 1-200.
2 Measure the difference between period #1 and the average. Save the result as a measurement result.
3 Measure the difference between period #2 and the average. Save the result.
4 Continue measuring the difference between each period and the average until period #200 is compared to the average (therefore, 200 measurements are generated).
5 Slide the window by one and measure the average for periods 2-201.
6 Compare period #2 with the new average.
7 Continue measuring the difference between each period and the average until period #201 is compared to the average (therefore, 200 more measurements are generated, making a total of 400 measurements).
8 Slide the window by one and measure the average for periods 3-202.
9 Compare period #3 with the new average.
10 Continue measuring the difference between each period and the average until period #202.

Expected / Observable Results

The wost measured value of tREH(avg) must be within the conformance limits as specified in the ONFI specification.

tREH(abs)

Test Overview

The purpose of this test is to measure the absolute width of the high level pulse of the Read Enable signal over all available cycles.

Signals of Interest

Based on the test definition (Read cycle only):

- RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- RE

Test Definition Notes from the Specification

Table 81 Constant Timing Parameter values for absolute read cycle high level width

Symbol	Parameter	Min	Max	Units
tREH(abs)	NV-DDR2/NV-DDR3 Absolute RE_n/RE_t high level width	0.43	–	tRC(avg)

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

As an example, consider the input test signal with a frequency of 1KHz and 202 cycles acquired.

1. Acquire a Read Enable signal and find a valid Read burst on it.
2. Measure the absolute width as the time difference between each rising and consecutive falling edge for each high pulse of the Read Enable signal.
3. Report the worst value of tREH(abs) as the final test result.

Expected / Observable Results

The worst measured value of tREH(abs) must be within the conformance limits as specified in the ONFI specification.

tRP(avg)

Test Overview

The purpose of this test is to measure the average width of the low level pulse of the Read Enable signal over any 200 consecutive periods.

Signals of Interest

Based on the test definition (Read cycle only):

- RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- RE

Test Definition Notes from the Specification

Table 82 Constant Timing Parameter values for average low level width

Symbol	Parameter	Min	Max	Units
tRP(avg)	NV-DDR2/NV-DDR3 Average RE_n/RE_t low level width	0.45	0.55	tRC(avg)

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

As an example, consider the input test signal with a frequency of 1KHz and 202 cycles acquired.

This measurement measures the difference between every period inside a 200 cycle window with the average of the whole window. The average is measured over the time difference between each falling and consecutive rising edge for each low pulse of the Read Enable signal.

1. Measure the average for periods 1-200.
2. Measure the difference between period #1 and the average. Save the result as a measurement result.
3. Measure the difference between period #2 and the average. Save the result.
4. Continue measuring the difference between each period and the average until period #200 is compared to the average (therefore, 200 measurements are generated).
5. Slide the window by one and measure the average for periods 2-201.
6. Compare period #2 with the new average.
7. Continue measuring the difference between each period and the average until period #201 is compared to the average (therefore, 200 more measurements are generated, making a total of 400 measurements).
8. Slide the window by one and measure the average for periods 3-202.
9. Compare period #3 with the new average.
10. Continue measuring the difference between each period and the average until period #202.

Expected / Observable Results

The worst measured value of tRP(avg) must be within the conformance limits as specified in the ONFI specification.

tRP(abs)

Test Overview

The purpose of this test is to measure the absolute width of the low level pulse of the Read Enable signal over all available cycles.

Signals of Interest

Based on the test definition (Read cycle only):

- RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- RE

Test Definition Notes from the Specification

Table 83 Constant Timing Parameter values for absolute read cycle low level width

Symbol	Parameter	Min	Max	Units
tRP(abs)	NV-DDR2/NV-DDR3 Absolute RE_n/RE_t low level width	0.43	–	tRC(avg)

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

As an example, consider the input test signal with a frequency of 1KHz and 202 cycles acquired.

1 Acquire a Read Enable signal and find a valid Read burst on it.
2 Measure the absolute width as the time difference between each falling and consecutive rising edge for each low pulse of the Read Enable signal.
3 Report the worst tRP(abs) value as the final test result.

Expected / Observable Results

The worst measured value of tRP(abs) must be within the conformance limits as specified in the ONFI specification.

tCR

Test Overview

The purpose of this test is to measure the time difference between the falling edge of the Chip Enable signal and the start of the read preamble.

Signals of Interest

Based on the test definition (Read cycle only):

- CE, RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- CE
- RE

Test Definition Notes from the Specification

Table 84 Constant Timing Parameter Values for tCR

Symbol	Parameter	Min	Max	Units
tCR	CE_n to (RE_n low or RE_t/RE_c crosspoint)	10	–	ns

Test References

See Table 91 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire a Read Enable signal.
2. Measure tCR as the time difference between the falling edge of the CE_n signal and the consecutive starting edge (RE_t/RE_c crosspoint) of the Read preamble.

Expected / Observable Results

The measured value of tCR must be within the conformance limits as specified in the ONFI specification.

tCS-Read

Test Overview

The purpose of this test is to measure the CE_n setup time for data burst with ODT disabled.

Signals of Interest

Based on the test definition (Read cycle only):

- CE, RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- CE
- RE

Test Definition Notes from the Specification

Table 85 Constant Timing Parameter Values for tCS-Read

Symbol	Parameter	Min	Max	Units
tCS	CE_n setup time	20	–	ns

Test References

See Table 91 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1 Acquire a Read Enable signal and find the first valid READ burst on it.
2 Measure tCS-Read as the time difference between the falling edge of the CE_n signal and the rising edge (end of preamble) of the first valid READ burst found on the RE_n signal.

Expected / Observable Results

The measured value of tCS-Read must be within the conformance limits as specified in the ONFI specification.

tDBS-Read

Test Overview

The purpose of this test is to measure the RE_n (RE_t) high setup to CE_n low during data burst.

Signals of Interest

Based on the test definition (Read cycle only):

- CE, RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- CE
- RE

Test Definition Notes from the Specification

Table 86 Constant Timing Parameter Values for tDBS-Read

Symbol	Min	Max	Units
tDBS	5	–	ns

Test References

See Table 91 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid rising and falling RE_n crossings in the READ burst that was found.
4. Measure all tDBS-Read values. Here, tDBS-Read is the setup time from the start of the RE_n (RE_t) high signal to the falling edge (start of CE_n low) of the Chip Enable signal during data burst.

Expected / Observable Results

The measured value of tDBS for the Read Enable signal must be within the conformance limits of the ONFI specification.

tRPRE

Test Overview

The purpose of this test is to verify that the time to transition from the falling edge to the rising edge of the Read Enable signal (first preamble behavior), is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Read cycle only):

- RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- RE

Test Definition Notes from the Specification

Table 87 Constant Timing Parameter Values for tRPRE

Symbol	Parameter	Min	Max	Units
tRPRE	NV-DDR2/NV-DDR3 Read Preamble Time	15	–	ns

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire a Read Enable signal and find a valid Read burst on it.
2. Measure the transition time from the falling edge to the rising edge of the burst as tRPRE.
3. Report the measured value of tRPRE.

Expected / Observable Results

The measured value of tRPRE must be within the conformance limits of the ONFI specification.

tRPRE2

Test Overview

The purpose of this test is to verify that the time to transition from the falling edge to the rising edge of the Read Enable signal with ODT enabled (second preamble behavior), is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Read cycle only):

- RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- RE

Test Definition Notes from the Specification

Table 88 Constant Timing Parameter Values for tRPRE2

Symbol	Parameter	Min	Max	Units
tRPRE2	NV-DDR2/NV-DDR3 Read Preamble Time with ODT enabled	25	–	ns

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1 Acquire a Read Enable signal and find a valid Read burst on it.
2 With ODT enabled, measure the transition time from the falling edge to the rising edge of the burst as tRPRE2.
3 Report the measured value of tRPRE2.

Expected / Observable Results

The measured value of tRPRE2 must be within the conformance limits of the ONFI specification.

tDQSRH

Test Overview

The purpose of this test is to verify that the hold time between the start of the Read Preamble to the start of the undefined Data Strobe signal is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Read cycle only):

- DQS, RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- RE

Test Definition Notes from the Specification

Table 89 Constant Timing Parameter Values for tDQSRH

Symbol	Parameter	Min	Max	Units
tDQSRH	NV-DDR2/NV-DDR3 DQS hold time after (RE_n low or RE_t/RE_c crosspoint)	5	–	ns

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid rising and falling DQS crossings in the said burst.
4. For all DQS crossings found, locate the undefined edges.
5. Measure the time difference between the start of the Read Preamble to the start of the undefined edge of the DQS signal.
6. Report the measured values of tDQSRH.

Expected / Observable Results

The measured value of tDQSRH must be within the conformance limits of the ONFI specification.

tDQSD

Test Overview

The purpose of this test is to verify that the time interval between the start of the Read Preamble to the start of the valid Data Strobe signal/Data signal that is driven by device is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Read cycle only):

- DQS, RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- RE

Test Definition Notes from the Specification

Table 90 Constant Timing Parameter Values for tDQSD

Symbol	Parameter	Min	Max	Units
tDQSD	NV-DDR2/NV-DDR3 (RE_n low or RE_t/RE_c crosspoint) to DQS/DQ driven by device	5	18	ns

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid rising and falling DQ and DQS crossings in the said burst.
4. For all DQ and DQS crossings found, measure the time difference between the start of the Read Preamble to the end of the undefined edges of the DQS signal.
5. Report the measured value as tDQSD.

Expected / Observable Results

The measured value of tDQSD must be within the conformance limits of the ONFI specification.

tRPST

Test Overview

The purpose of this test is to verify that the Postamble time of the Read Enable signal is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Read cycle only):

- CE, RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- CE
- RE

Test Definition Notes from the Specification

Table 91 Constant Timing Parameter Values for tRPST

Symbol	Parameter	Min	Max	Units
tRPST	NV-DDR2/NV-DDR3 Read Postamble Time	tDQSRE + 0.5*tRC	–	ns

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid READ burst found.
3. Measure the time difference between the final edge of the RE burst to the start of the CE High signal as tRPST.
4. Report the measured value of tRPST.

Expected / Observable Results

The measured value of tRPST must be within the conformance limits of the ONFI specification.

tRPSTH

Test Overview

The purpose of this test is to verify that the Postamble Hold time of the Read Enable signal is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition (Read cycle only):

- CE, RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- CE
- RE

Test Definition Notes from the Specification

Table 92 Constant Timing Parameter Values for tRPSTH

Symbol	Parameter	Min	Max	Units
tRPSTH	NV-DDR2/NV-DDR3 Read Postamble Hold Time	15	–	ns

Test References

See Table 94 in Section 4.18.3 and Figure 77 in Section 4.19.3.4 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1 Acquire and split the Read and Write bursts of the acquired signal.
2 Take the first valid READ burst found.
3 Measure the time difference between the start of the CE_n high signal to the consecutive rising edge of the RE_n signal.
4 Report all values of tRPSTH.

Expected / Observable Results

The measured value of tRPSTH must be within the conformance limits of the ONFI specification.

Timing Command and Address Tests

Refer to "Understanding ONFI Concepts for Measurements" on page 27 to read about the conceptual information associated with each test.

tCSD_ALE

Test Overview

The purpose of this test is to verify that the hold time duration of the Address Latch Enable signal from the rising edge of the Chip Enable signal, is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition:

- CE, ALE

Signals required to perform the test on the Oscilloscope:

- CE
- ALE

Test Definition Notes from the Specification

Table 93 Constant Timing Parameter Values for tCSD_ALE

Symbol	Parameter	Min	Max	Units
tCSD_ALE	ALE hold time from CE_n high	10	–	ns

Test References

See *Table 91 in Section 4.18.3* and *Figures 73 & 74* in *Section 4.19.3* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Acquire the signal under test.
2. Measure all tCSD_ALE values. Here, tCSD_ALE is the time starting from the rising edge of the CE_n signal to the rising edge of the Address Latch Enable signal.
3. Report the worst value of tCSD_ALE.

Expected / Observable Results

The worst hold time of the Address Latch Enable signal must be within the conformance limits of the ONFI specification.

tCSD_CLE

Test Overview

The purpose of this test is to verify that the hold time duration of the Command Latch Enable signal from the rising edge of the Chip Enable signal, is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition:

- CE, CLE

Signals required to perform the test on the Oscilloscope:

- CE
- CLE

Test Definition Notes from the Specification

Table 94 Constant Timing Parameter Values for tCSD_CLE

Symbol	Parameter	Min	Max	Units
tCSD_CLE	CLE hold time from CE_n high	10	–	ns

Test References

See *Table 91* in *Section 4.18.3* and *Figures 73 & 74* in *Section 4.19.3* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

1. Acquire the signal under test.
2. Measure all tCSD_CLE values. Here, tCSD_CLE is the time starting from the rising edge of the CE_n signal to the rising edge of the Command Latch Enable signal.
3. Report the worst value of tCSD_CLE.

Expected / Observable Results

The worst hold time of the Command Latch Enable signal must be within the conformance limits of the ONFI specification.

tCALS_CLE

Test Overview

The purpose of this test is to verify that the setup time of the Command Latch Enable signal (with respect to the rising edge of the Write Enable signal) is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition:

- WE, CLE

Signals required to perform the test on the Oscilloscope:

- WE
- CLE

Test Definition Notes from the Specification

Table 95 Constant Timing Parameter Values for tCALS_CLE

Symbol	Parameter	Min	Max	Units
tCALS	CLE setup time	15	–	ns

Test References

See Table 91 in Section 4.18.3 and Figures 73 & 74 in Section 4.19.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1 Acquire the signal under test.
2 Measure all tCALS_CLE values. Here, tCALS_CLE is the setup time of the Command Latch Enable starting from the rising edge of the CLE signal to the rising edge of the Write Enable signal.
3 Report the worst value of tCALS_CLE.

Expected / Observable Results

The worst setup time of the Command Latch Enable signal must be within the conformance limits of the ONFI specification.

tCALH_CLE

Test Overview

The purpose of this test is to verify that the hold time of the Command Latch Enable signal (with respect to the falling edge of the Write Enable signal) is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition:

- WE, CLE

Signals required to perform the test on the Oscilloscope:

- WE
- CLE

Test Definition Notes from the Specification

Table 96 Constant Timing Parameter Values for tCALH_CLE

Symbol	Parameter	Min	Max	Units
tCALH	CLE hold time	5	–	ns

Test References

See Table 91 in Section 4.18.3 and Figures 73 & 74 in Section 4.19.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1 Acquire the signal under test.
2 Measure all tCALH_CLE values. Here, tCALH_CLE is the hold time of the Command Latch Enable starting from the rising edge of the Write Enable signal to the falling edge of the CLE signal.
3 Report the worst value of tCALH_CLE.

Expected / Observable Results

The worst hold time of the Command Latch Enable signal must be within the conformance limits of the ONFI specification.

tCALS_ALE

Test Overview

The purpose of this test is to verify that the setup time of the Address Latch Enable signal (with respect to the rising edge of the Write Enable signal) is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition:

- WE, ALE

Signals required to perform the test on the Oscilloscope:

- WE
- ALE

Test Definition Notes from the Specification

Table 97 Constant Timing Parameter Values for tCALS_ALE

Symbol	Parameter	Min	Max	Units
tCALS	ALE setup time	15	–	ns

Test References

See Table 91 in Section 4.18.3 and Figures 73 & 74 in Section 4.19.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1 Acquire the signal under test.
2 Measure all tCALS_ALE values. Here, tCALS_ALE is the setup time of the Address Latch Enable starting from the rising edge of the ALE signal to the rising edge of the Write Enable signal.
3 Report the worst value of tCALS_ALE.

Expected / Observable Results

The worst setup time of the Address Latch Enable signal must be within the conformance limits of the ONFI specification.

tCALH_ALE

Test Overview

The purpose of this test is to verify that the hold time of the Address Latch Enable signal (with respect to the falling edge of the Write Enable signal) is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition:

- WE, ALE

Signals required to perform the test on the Oscilloscope:

- WE
- ALE

Test Definition Notes from the Specification

Table 98 Constant Timing Parameter Values for tCALH_ALE

Symbol	Parameter	Min	Max	Units
tCALH	ALE hold time	5	–	ns

Test References

See Table 91 in Section 4.18.3 and Figures 73 & 74 in Section 4.19.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1 Acquire the signal under test.
2 Measure all tCALH_ALE values. Here, tCALH_ALE is the hold time of the Address Latch Enable starting from the rising edge of the Write Enable signal to the falling edge of the ALE signal.
3 Report the worst value of tCALH_ALE.

Expected / Observable Results

The worst hold time of the Address Latch Enable signal must be within the conformance limits of the ONFI specification.

tWP

Test Overview

The purpose of this test is to measure the pulse width of the Write Enable signal.

Signals of Interest

Based on the test definition:

- WE

Signals required to perform the test on the Oscilloscope:

- WE

Test Definition Notes from the Specification

Table 99 Constant Timing Parameter values for tWP

Symbol	Min	Max	Units
tWP	11	–	ns

Test References

See Table 91 in Section 4.18.3 and Figures 73 & 74 in Section 4.19.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1 Acquire the Write Enable signal.
2 Measure the pulse width from the falling edge to the consecutive rising edge of the Write Enable signal.
3 Report the pulse width value as tWP.

Expected / Observable Results

The worst value of tWP must be within the conformance limits as specified in the ONFI specification.

tCS

Test Overview

The purpose of this test is to verify that the setup time of the Chip Enable signal (with respect to the rising edge of the Write Enable signal) is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition:

- WE, CE

Signals required to perform the test on the Oscilloscope:

- WE
- CE

Test Definition Notes from the Specification

Table 100 Constant Timing Parameter Values for tCS

Symbol	Parameter	Min	Max	Units
tCS	CE setup time	20	–	ns

Test References

See Table 91 in Section 4.18.3 and Figures 73 & 74 in Section 4.19.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire the signal under test.
2. Measure all tCS values. Here, tCS is the setup time of the Chip Enable signal starting from the falling edge (1-to-0 transition) of the CE_n signal to the next rising edge (0-to-1 transition) of the Write Enable signal.
3. Report the worst value of tCS.

Expected / Observable Results

The worst setup time of the Chip Enable signal must be within the conformance limits of the ONFI specification.

tCH

Test Overview

The purpose of this test is to verify that the hold time of the Chip Enable signal (with respect to the rising edge of the Write Enable signal) is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition:

- WE, CE

Signals required to perform the test on the Oscilloscope:

- WE
- CE

Test Definition Notes from the Specification

Table 101 Constant Timing Parameter Values for tCH

Symbol	Parameter	Min	Max	Units
tCH	CE hold time	5	–	ns

Test References

See Table 91 in Section 4.18.3 and Figures 73 & 74 in Section 4.19.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire the signal under test.
2. Measure all tCH values. Here, tCH is the hold time of the Chip Enable signal starting from the rising edge (0-to-1 transition) of the Write Enable signal to the consecutive rising edge (0-to-1 transition) of the CE_n signal.
3. Report the worst value of tCH.

Expected / Observable Results

The worst hold time of the Chip Enable signal must be within the conformance limits of the ONFI specification.

tCAS

Test Overview

The purpose of this test is to verify that the setup time of the Command/Address DQ signal (with respect to the Write Enable signal) is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition:

- Command/Address DQ

Signals required to perform the test on the oscilloscope:

- WE
- Command/Address DQ

Test Definition Notes from the Specification

Table 102 Constant Timing Parameter Values for tCAS

Symbol	Parameter	Min	Max	Units
tCAS	Command/Address DQ setup time	5	–	ns

Test References

See Table 91 in Section 4.18.3 and Figures 73 & 74 in Section 4.19.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1. Acquire the signal under test.
2. Measure all tCAS values. Here, tCAS is the setup time of the Command/Address signal starting from the initial crossing point of the DQ signal to the next rising edge (0-to-1 transition) of the Write Enable signal.
3. Report the worst value of tCAS.

Expected / Observable Results

The worst setup time of the Command/Address DQ signal must be within the conformance limits of the ONFI specification.

tCAH

Test Overview

The purpose of this test is to verify that the hold time of the Command/Address DQ signal (with respect to the Write Enable signal) is within the conformance limit as specified in the ONFI Specification.

Signals of Interest

Based on the test definition:

- Command/Address DQ

Signals required to perform the test on the oscilloscope:

- WE
- Command/Address DQ

Test Definition Notes from the Specification

Table 103 Constant Timing Parameter Values for tCAH

Symbol	Parameter	Min	Max	Units
tCAH	Command/Address DQ hold time	5	–	ns

Test References

See Table 91 in Section 4.18.3 and Figures 73 & 74 in Section 4.19.3 of the Open NAND Flash Interface Specification Revision 4.2.

Measurement Algorithm

1 Acquire the signal under test.
2 Measure all tCAH values. Here, tCAH is the hold time of the Command/Address signal starting from the rising edge (0-to-1 transition) of the Write Enable signal to the final crossing point of the DQ signal.
3 Report the worst value of tCAH.

Expected / Observable Results

The worst hold time of the Command/Address DQ signal must be within the conformance limits of the ONFI specification.

7 NVDDR2/NVDDR3 Jitter Tests

Setting up the ONFI Test Application to run tests / 180
Jitter Tests on Strobe / 181
Jitter Tests on Read Enable / 186

This section provides the Methods of Implementation (MOIs) for Clock Timing tests using a Keysight Infiniium Oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the Keysight D9010ONFC ONFI Test Application.

NOTE The test methodology described below for each test is applicable for both NVDDR2 and NVDDR3 data interface types. The NV-DDR3 data interface includes all NV-DDR2 features; however, NVDDR2 operates at VccQ=1.8V whereas NVDDR3 operates at VccQ=1.2V.

Setting up the ONFI Test Application to run tests

1 Launch the ONFI Test Application as described in "Starting the ONFI Test Application" on page 21.
2 Connect the differential solder-in probe head to the PUTs on the ONFI device.
3 Connect the Oscilloscope probes to any Channels of the Oscilloscope.
4 On the **Set Up** tab of the ONFI Test Application:
   a Select the required **Data Interface** type.
   b Select or type a data rate value from the drop-down options in the **Speed Grade** area. The Test Application displays the corresponding **Timing Mode** number automatically.
   c In the **Input Signal Setup** area, **Live** is selected by default. Select **Offline** to load one or more waveform files located on your machine.
   d Type in or select the **Device Identifier** as well as **User Description** from the drop-down list. Enter your comments in the **Comments** text box.
5 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.
6 Start running the selected tests. When performing the Electrical tests for Strobe and Data Signals, the ONFI Test Application will prompt you to make the proper connections. The **Connect** tab in the ONFI Test Application displays the exact number of probe connections. You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the **Configure** tab of the ONFI Test Application.

NOTE

The values for sampling rate and sampling point configuration options in the **Configure** tab differ for Digital Storage Oscilloscopes and UXR Oscilloscopes.

Sampling Rate (in GSa/s) options in DSOs are 10, 20, 40, 80 and MAX (default); whereas in UXRs, sampling rate (in GSa/s) options are 8, 16, 32, 64 (default), 128 and MAX.

The default option for **Sampling Points (Pts) for Electrical and Timing Tests Only** in DSOs is 2MPts; whereas in UXRs, the default option is 4MPts.

For more information about the functionality of various tabs and running tests using the ONFI Test Application's user interface, refer to the *Keysight D9010ONFC ONFI Test Application Online Help*.

Jitter Tests on Strobe

Refer to "Understanding ONFI Concepts for Measurements" on page 27 to read about the conceptual information associated with each test.

tJITper(DQS)

This test is applicable to the Rising Edge measurement. The period jitter (tJITper) is the maximum deviation in the tRC or tDSC period from the average or nominal tRC or tDSC period. It is allowed in either the positive or negative direction. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock.

Signals of Interest

Based on the test definition (Read or Write):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 104 Timing Mode specific values for Clock Timing Jitter

NV-DDR2/NV-DDR3 Jitter values for tJITper(DQS)			
Timing Mode #	Data Rate in MT/s	Minimum tJITper(DQS) in ns	Maximum tJITper(DQS) in ns
Mode 0	~ 66	-2.4	2.4
Mode 1	80	-2.0	2.0
Mode 2	~ 132	-1.2	1.2
Mode 3	~ 166	-1.0	1.0
Mode 4	200	-0.80	0.80
Mode 5	~ 266	-0.60	0.60
Mode 6	~ 332	-0.48	0.48
Mode 7	400	-0.40	0.40
Mode 8	~ 534	-0.30	0.30
Mode 9	~ 666	-0.24	0.24
Mode 10	800	-0.20	-0.20
Mode 11	~1066	-0.094	0.094
Mode 12	1200	-0.083	0.083
Mode 13	~1334	-0.078	0.078
Mode 14	~1466	-0.075	0.075
Mode 15	1600	-0.070	0.070

Test References

See *Table 92* in *Section 4.18.3* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

As an example, consider the input test signal with a frequency of 1KHz and 202 cycles acquired.

This measurement measures the difference between every period inside a 200 cycle window with the average of the whole window.

1. Measure the average for periods 1-200.
2. Measure the difference between period #1 and the average. Save the result as a measurement result.
3. Measure the difference between period #2 and the average. Save the result.
4. Continue measuring the difference between each period and the average until period #200 is compared to the average (therefore, 200 measurements are generated).
5. Slide the window by one and measure the average for periods 2-201.
6. Compare period #2 with the new average.
7. Continue measuring the difference between each period and the average until period #201 is compared to the average (therefore, 200 more measurements are generated, making a total of 400 measurements).
8. Slide the window by one and measure the average for periods 3-202.
9. Compare period #3 with the new average.
10. Continue measuring the difference between each period and the average until period #202 (therefore, 200 more measurements are generated, making a total of 600 measurements).
11. Check these 600 measurements for the smallest and largest worst case values.
12. Compare test results with the compliance test limits.

Expected / Observable Results

The tJITper(DQS) measurement value must be within the conformance limits as specified in the ONFI specification.

tJITcc(DQS)

This test is applicable to the Rising Edge Measurement. The cycle-to-cycle jitter (tJITcc) is the amount the clock period can deviate from one cycle to the next. The purpose of this test is to measure the difference in the clock period between two consecutive clock cycles. The tJIT(cc) Rising Edge Measurement measures the clock period from the rising edge of a clock cycle to the next rising edge.

Signals of Interest

Based on the test definition (Read or Write):

- DQS

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test Definition Notes from the Specification

Table 105 Timing Mode specific values for Cycle-to-Cycle Jitter

NV-DDR2/NV-DDR3 Jitter values for tJITcc(DQS)			
Timing Mode #	Data Rate in MT/s	Minimum tJITcc(DQS) in ns	Maximum tJITcc(DQS) in ns
Mode 0	~ 66	–	4.8
Mode 1	80	–	4.0
Mode 2	~ 132	–	2.4
Mode 3	~ 166	–	2.0
Mode 4	200	–	1.6
Mode 5	~ 266	–	1.2
Mode 6	~ 332	–	0.96
Mode 7	400	–	0.80
Mode 8	~ 534	–	0.6
Mode 9	~ 666	–	0.48
Mode 10	800	–	0.4
Mode 11	~1066	–	0.188
Mode 12	1200	–	0.167
Mode 13	~1334	–	0.156
Mode 14	~1466	–	0.150
Mode 15	1600	–	0.140

Test References

See *Table 92* in *Section 4.18.3* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

As an example, consider the input test signal with a frequency of 1KHz and 202 cycles acquired.

1 Measure the difference between every adjacent pair of periods.
2 Generate 201 measurement results.
3 Check the results for the smallest and largest worst case values.
4 Compare the test results against the compliance test limits.

Expected / Observable Results

The tJITcc(DQS) measurement value must be within the conformance limits as specified in the ONFI specification.

Jitter Tests on Read Enable

Refer to “Understanding ONFI Concepts for Measurements” on page 27 to read about the conceptual information associated with each test.

tJITper(RE)

This test is applicable to the Rising Edge measurement. The period jitter (tJITper) is the maximum deviation in the tRC or tDSC period from the average or nominal tRC or tDSC period. It is allowed in either the positive or negative direction. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock.

Signals of Interest

Based on the test definition (Read or Write):

- RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- RE

Test Definition Notes from the Specification

Table 106 Timing Mode specific values for Clock Timing Jitter

NV-DDR2/NV-DDR3 Jitter values for tJITper(RE)			
Timing Mode #	Data Rate in MT/s	Minimum tJITper(RE) in ns	Maximum tJITper(RE) in ns
Mode 0	~ 66	-1.8	1.8
Mode 1	80	-1.5	1.5
Mode 2	~ 132	-0.90	0.90
Mode 3	~ 166	-0.75	0.75
Mode 4	200	-0.60	0.60
Mode 5	~ 266	-0.45	0.45
Mode 6	~ 332	-0.36	0.36
Mode 7	400	-0.30	0.30
Mode 8	~ 534	-0.225	0.225
Mode 9	~ 666	-0.18	0.18
Mode 10	800	-0.15	0.15
Mode 11	~1066	-0.094	0.094
Mode 12	1200	-0.083	0.083
Mode 13	~1334	-0.078	0.078
Mode 14	~1466	-0.075	0.075
Mode 15	1600	-0.070	0.070

Test References

See *Table 92* in *Section 4.18.3* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

As an example, consider the input test signal with a frequency of 1KHz and 202 cycles acquired.

This measurement measures the difference between every period inside a 200 cycle window with the average of the whole window.

1 Measure the average for periods 1-200.
2 Measure the difference between period #1 and the average. Save the result as a measurement result.
3 Measure the difference between period #2 and the average. Save the result.
4 Continue measuring the difference between each period and the average until period #200 is compared to the average (therefore, 200 measurements are generated).
5 Slide the window by one and measure the average for periods 2-201.
6 Compare period #2 with the new average.
7 Continue measuring the difference between each period and the average until period #201 is compared to the average (therefore, 200 more measurements are generated, making a total of 400 measurements).
8 Slide the window by one and measure the average for periods 3-202.
9 Compare period #3 with the new average.
10 Continue measuring the difference between each period and the average until period #202 (therefore, 200 more measurements are generated, making a total of 600 measurements).
11 Check these 600 measurements for the smallest and largest worst case values.
12 Compare test results with the compliance test limits.

Expected / Observable Results

The tJITper(RE) measurement value must be within the conformance limits as specified in the ONFI specification.

tJITcc(RE)

This test is applicable to the Rising Edge Measurement. The cycle-to-cycle jitter (tJITcc) is the amount the clock period can deviate from one cycle to the next. The purpose of this test is to measure the difference in the clock period between two consecutive clock cycles. The tJIT(cc) Rising Edge Measurement measures the clock period from the rising edge of a clock cycle to the next rising edge.

Signals of Interest

Based on the test definition (Read or Write):

- RE

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ
- RE

Test Definition Notes from the Specification

Table 107 Timing Mode specific values for Cycle-to-Cycle Jitter

NV-DDR2/NV-DDR3 Jitter values for tJITcc(RE)			
Timing Mode #	Data Rate in MT/s	Minimum tJITcc(RE) in ns	Maximum tJITcc(RE) in ns
Mode 0	~ 66	–	3.6
Mode 1	80	–	3.0
Mode 2	~ 132	–	1.8
Mode 3	~ 166	–	1.5
Mode 4	200	–	1.2
Mode 5	~ 266	–	0.90
Mode 6	~ 332	–	0.72
Mode 7	400	–	0.60
Mode 8	~ 534	–	0.45
Mode 9	~ 666	–	0.36
Mode 10	800	–	0.3
Mode 11	~1066	–	0.188
Mode 12	1200	–	0.167
Mode 13	~1334	–	0.156
Mode 14	~1466	–	0.150
Mode 15	1600	–	0.140

Test References

See *Table 92* in *Section 4.18.3* of the *Open NAND Flash Interface Specification Revision 4.2.*

Measurement Algorithm

As an example, consider the input test signal with a frequency of 1KHz and 202 cycles acquired.

1 Measure the difference between every adjacent pair of periods.
2 Generate 201 measurement results.
3 Check the results for the smallest and largest worst case values.
4 Compare the test results against the compliance test limits.

Expected / Observable Results

The tJITcc(RE) measurement value must be within the conformance limits as specified in the ONFI specification.

8 NVDDR2/NVDDR3 Eye-Diagram Tests

Setting up the ONFI Test Application to run tests / 192
Read Cycle Tests / 193
Write Cycle Tests / 194

This section provides the Methods of Implementation (MOIs) for Eye-Diagram tests using a Keysight Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the Keysight D9010ONFC ONFI Test Application.

NOTE The test methodology described below for each test is applicable for both NVDDR2 and NVDDR3 data interface types. The NV-DDR3 data interface includes all NV-DDR2 features; however, NVDDR2 operates at VccQ=1.8V whereas NVDDR3 operates at VccQ=1.2V.

KEYSIGHT TECHNOLOGIES

Setting up the ONFI Test Application to run tests

1 Launch the ONFI Test Application as described in "Starting the ONFI Test Application" on page 21.
2 Connect the differential solder-in probe head to the PUTs on the ONFI device.
3 Connect the Oscilloscope probes to any Channels of the Oscilloscope.
4 On the **Set Up** tab of the ONFI Test Application:
   a Select the required **Data Interface** type.
   b Select or type a data rate value from the drop-down options in the **Speed Grade** area. The Test Application displays the corresponding **Timing Mode** number automatically.
   c In the **Input Signal Setup** area, **Live** is selected by default. Select **Offline** to load one or more waveform files located on your machine.
   d Type in or select the **Device Identifier** as well as **User Description** from the drop-down list. Enter your comments in the **Comments** text box.
5 Click the **Select Tests** tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.
6 Start running the selected tests. When performing the Electrical tests for Strobe and Data Signals, the ONFI Test Application will prompt you to make the proper connections. The **Connect** tab in the ONFI Test Application displays the exact number of probe connections. You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the **Configure** tab of the ONFI Test Application.

NOTE

The values for sampling rate and sampling point configuration options in the **Configure** tab differ for Digital Storage Oscilloscopes and UXR Oscilloscopes.

Sampling Rate (in GSa/s) options in DSOs are 10, 20, 40, 80 and MAX (default); whereas in UXRs, sampling rate (in GSa/s) options are 8, 16, 32, 64 (default), 128 and MAX.

The default option for **Sampling Points (Pts) for Eye Diagram Tests Only in DSOs** is 2MPts; whereas in UXRs, the default option is 4MPts.

For more information about the functionality of various tabs and running tests using the ONFI Test Application's user interface, refer to the *Keysight D9010ONFC ONFI Test Application Online Help*.

Read Cycle Tests

Refer to "Understanding ONFI Concepts for Measurements" on page 27 to read about the conceptual information associated with each test.

Eye Diagram for Read DQ

The purpose of this test is to automate all the required setup procedures in order to generate an eye diagram for the ONFI data's READ cycle. This feature allows you to perform evaluation and debugging on the created eye diagram. This test is considered for Information-Only purpose.

Signals of Interest

Based on the test definition (Read cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test References

There is no available test specification on eye testing in ONFI specification.

Measurement Algorithm

1 Calculate the initial value of time scale based on the selected ONFI Test Application speed grade option.

2 Set or view the configuration parameter **Sampling Points (Pts) for Eye Diagram Tests Only** in the **Configure** tab of the ONFI Test Application:

- For Digital Storage Oscilloscopes, default configuration is 2MPts.
- For UXR Oscilloscopes, default configuration is 4MPts.

3 Based on the sampling points obtained in step 2, acquire the exact number of sampling points for eye folding.

4 Check for valid DQS input test signals by verifying its frequency and amplitude values.

5 Set up the Oscilloscope to generate an eye diagram.

   a Use the timing/electrical engine to separate READ burst and return the filtered DQS signals as recovered clock for eye folding later.

   b Set up measurement threshold values for the DQx channel and the DQSx channel input.

   c Set up fix vertical scale values for DQx channel and DQSx channel input.

   d Set the Color Grade Display option to ON.

   e Set up Clock Recovery settings on SDA.
   : Explicit Clock, Source = DQS, Rise/Fall Edge

   f Set Real Time Eye on SDA to ON.

6 Process only one acquisition.

7 The generated Eye Diagram for the READ cycle is considered for Information-Only purposes.

Expected / Observable Results

Generation of an eye diagram for the ONFI data's READ cycle.

Write Cycle Tests

Refer to "Understanding ONFI Concepts for Measurements" on page 27 to read about the conceptual information associated with each test.

Eye Diagram for Write DQ

The purpose of this test is to automate all the required setup procedures in order to generate an eye diagram for the ONFI data's WRITE cycle, which can be used to perform evaluation (and debugging, if needed) on the created eye diagram. This test is considered for Information-Only purpose.

Signals of Interest

Based on the test definition (Write cycle only):

- DQ

Signals required to perform the test on the Oscilloscope:

- DQS
- DQ

Test References

There is no available test specification on eye testing in ONFI specification.

Measurement Algorithm

1. Calculate the initial value of time scale based on the selected ONFI Test Application speed grade option.
2. Set or view the configuration parameter **Sampling Points (Pts) for Eye Diagram Tests Only** in the **Configure** tab of the ONFI Test Application:
   - For Digital Storage Oscilloscopes, default configuration is 2MPts.
   - For UXR Oscilloscopes, default configuration is 4MPts.
3. Based on the sampling points obtained in step 2, acquire the exact number of sampling points for eye folding.
4. Check for valid DQS input test signals by verifying its frequency and amplitude values.
5. Set up the oscilloscope to generate an eye diagram.
   a Use the timing/electrical engine to separate WRITE burst and return the filtered DQS signals as recovered clock for eye folding later.
   b Set up measurement threshold values for the DQx channel and the DQSx channel input.
   c Set up fix vertical scale values for DQx channel and DQSx channel input.
   d Set the Color Grade Display option to ON.
   e Set up Clock Recovery settings on SDA.
   : Explicit clock, Source = DQS, Rise/Fall Edge
   f Set Real Time Eye on SDA to ON.
6. Process only one acquisition.
7. The generated Eye Diagram for the WRITE cycle is considered for Information-Only purposes.

Expected / Observable Results

Generation of an eye diagram for the ONFI data's WRITE cycle.

KEYSIGHT
TECHNOLOGIES

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