Keysight Technologies B1505A Power Device Analyzer/Curve Tracer

Step by Step Measurement Handbook for Power MOSFET

KEYSIGHT TECHNOLOGIES

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Introduction

Agilent B1505A Power Device Analyzer/Curve Tracer is a powerful tool for measuring and characterizing power devices.

This power MOS-FET measurement handbook covers how to measure the typical power MOS-FET parameters found in power MOS-FET specifications or data sheet as shown in table 1. Each test is covered with step by step instructions of cable connection to the power MOS-FET and the parameter setting of the test, you can easily setup the test and execute it by just following the guide.

The step by step measurement handbook covers:

- A cable connection from the instrument to the device terminal,
- A test setup of the measurement parameters and the data extraction scheme,
- A test execution and analysis on EasyEXPERT software which is resident in B1505A and provides all the control of the B1505A.

A customized Application Test Library is created for testing the specifications introduced in this measurement handbook. They can be downloaded from the Agilent web site and you can use them by importing to your B1505A. They include the Application Test library and the test definitions, and you can start measurements right away.

Measuring power devices sometimes requires special knowledge of both the device and the measuring instruments.
For example, the high voltage breakdown test sometimes requires a series resistor connected between the High voltage SMU (HVSMU) and the drain of power MOS-FET to protect from a damage of the device from an unusual device breakdown.

Another example: a pulsed measurement required in high current measurements for eliminating a self-heating of the device sometimes results in a totally incorrect measurement result due to the slow rise up of measurement pulse signal caused by a large stray capacitance of the power MOS-FET.

The measurement basics and measurement tips are covered in appendix section for covering wider applications and assisting your troubleshooting with more in-depth knowledge of the B1505A. You are able to understand the reason of the test approaches taken in the measurement examples introduced in this measurement handbook. Knowing the right way and limiting any impeding factors obtained from the measurement tips when characterizing the power MOS-FET by using the B1505A should reduce a lot of Engineer's time.

Table 1. Typical DC and Capacitance parameters of power MOS-FET and the compatibility of the B1505A.

Typical power MOSFET Parameter	Symbol	Unit	Measurement *1	Measure by B1505A	Measurable by B1505A
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V	Id-Vd	YES	-3,000 V to 3,000 V (Minimum 200 μV resolution) *2
Gate-to-Source Voltage	V_{GSS}	V	Ig-Vg	YES	-200 V to 200 V (Minimum 2 μV resolution) *3
Drain Current (DC)	I_D	A	Id-Vd	YES	-2 A to 2 A (Minimum 10 pA resolution) *4
Drain Current (Pulse)	I_{DP}, I_{DM}	A	Id-Vd	YES	-40 A to 40 A (Minimum 10 pA resolution) *4
Drain-to-Source Leakage Current	I_{DSS}	A	Id-Vd	YES	-8 mA to 8 mA (Minimum 10 fA resoluion, ≤ 1,500 V) *5
Gate-to-Source Leakage Current	I_{GSS}	A	Ig-Vg	YES	-1 A to 1 A (Minimum 10 fA resolution) *3
Gate threshold Voltage, or Cutoff Voltage	$V_{GS(th)}$ $V_{GS(off)}$	V	Id-Vg	YES	-200 V to 200 V (Minimum 2 μV resolution) *3
Forward Transfer Admittance, or Forward Transconductance	|yfs| Gfs	S	Vd-Id @Vds	YES	1 mS ~ 1000 S *6
Static Drain-to-Source On-State Resist	$R_{DS(on)}$	ohm	Vd-Vg @Id	YES	Better than 100 μohm *7
Diode Forward Voltage	V_{SD}	V	Is-Vs	YES	-40 A to 40 A (Minimum 10 pA resolution) *4
Reverse Drain Current	I_{SD}	A	Is-Vs	YES	-40 A to 40 A (Minimum 10 pA resolution) *4
Input Capacitance	Ciss	pF	C-V	YES	Better than 1% at C<10 nF *8
Output Capacitance	Coss	pF	C-V	YES	Better than 1% at C<10 nF *8
Reverse Transfer Capacitance	Crss	pF	C-V	YES	Better than 1% at C<10 nF *8

Note:

*1: Measurement used for extracting the parameter.

*2: HVSMU

*3: HPSMU

*4: With two HCSMUs and requires Dual HCSMU Combination Adapter.

*5: Maximum 4 mA at 3,000 V.

*6: Rule of thumb (Example: 1mA/1V ~ 1A/1mV)

*7: Rule of thumb (Example: 1 mV/10 A)

*8: Max. 3,000V DC bias with High-voltage Bias T adapter.

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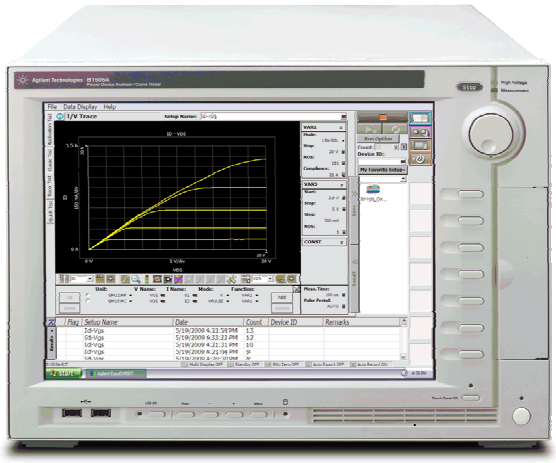
Chapter 1: Basic Knowledge of the B1505A



This chapter provides basic B1505A related information that is better to know before you proceed this material.

1.1 Agilent B1505A Power Device Analyzer/ Curve Tracer

Agilent B1505A Power Device Analyzer / Curve Tracer is designed for measuring present power devices. B1505A uses the EasyEXPERT software, a specially-designed Microsoft Windows® application program.

The B1505A can measure wide range of power devices from 10 fA to 40 A and 2 μV to 3,000 V with 3,000 V CV measurement features.

The EasyEXPERT software, which is resident on the B1505A, provides an intuitive and flexible data management and analysis environment.

- B1505A has 10 module slots, which support the following modules
- B1510A High Power SMU (HPSMU) 10 fA~1 A/2 μV~200 V
- B1512A High Current SMU (HCSMU) 10 pA~1 A/200 nV~40V (DC) or 10 pA~20 A/200 nV~20 V (Pulse)
- B1513A High Voltage SMU (HVSMU) 10 fA~4 mA/200 μV~3000 V or 10 fA~8 mA/200 μV~1500 V
- B1520A Multi Frequency CMU (MFCMU) 1 fF~10 nF @ 1 MHz for power MOS FET parameters with 0~3000 V DC bias by using High Voltage Bias-Tee adapter.

Output and measurement range of each module are visually shown in figure 1-1.

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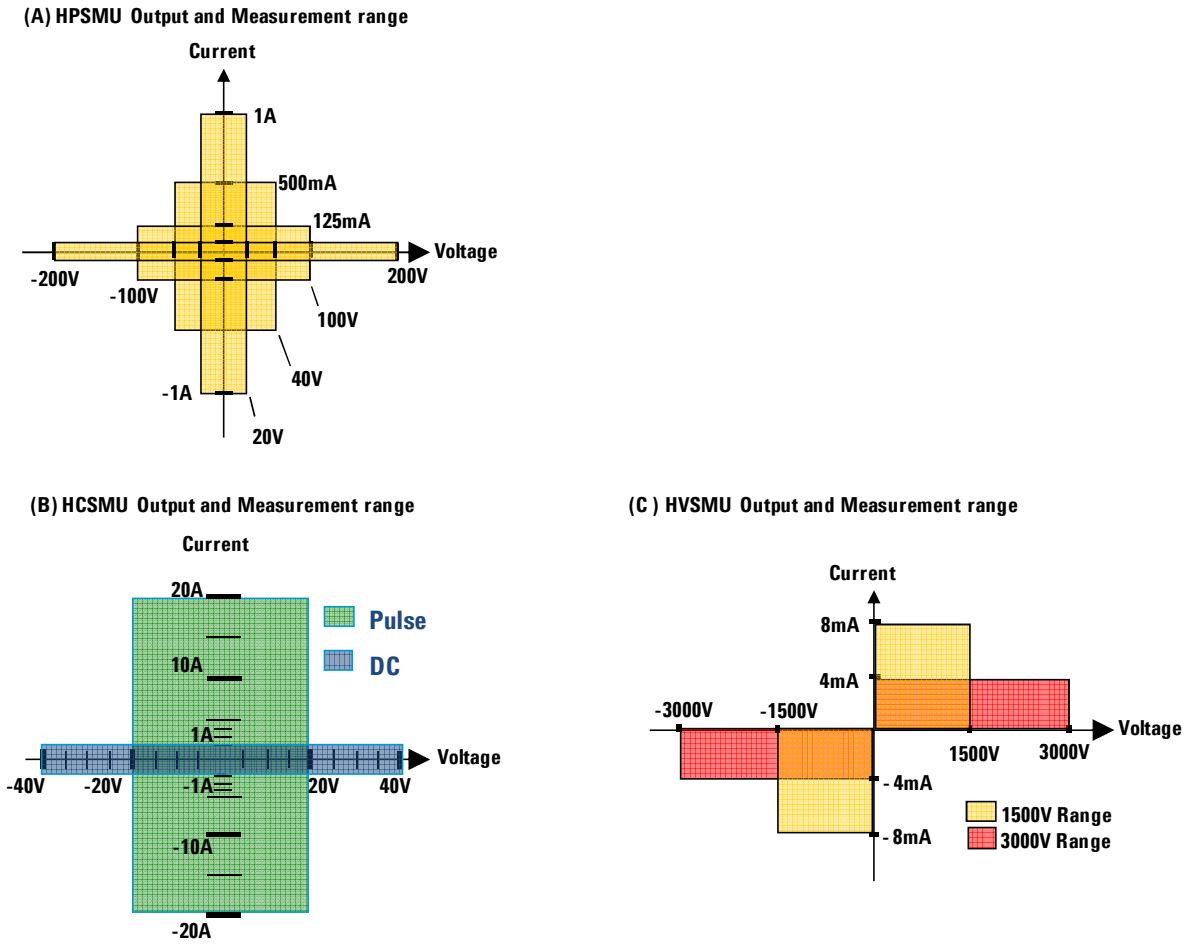


Figure 1-1. Output and measurement range

Figures 1-2. Agilent N1259A Test Fixture

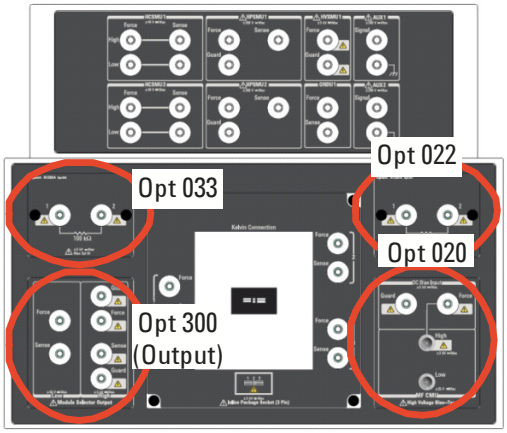


Figure 1-3. N1259A Opt 020, 022, 033 and 300

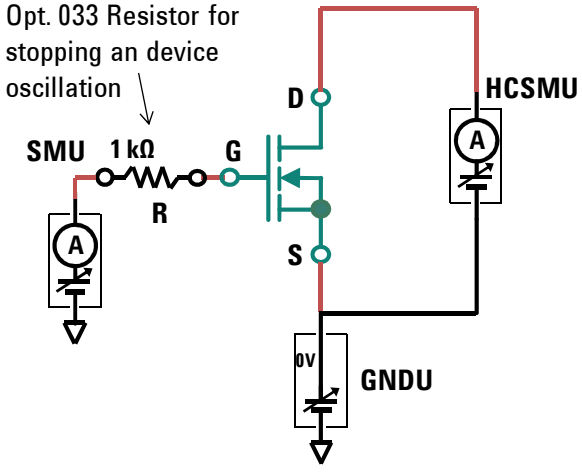


Figure 1-4: Option 033 Series R inserted between gate SMU and the gate

1.2 Agilent N1259A Power Device Fixture

Agilent N1259A Power Device Fixture shown in figure 1-2 is used for measuring packaged power devices, It can basically covers the B1505A`s maximum output range; 40 A and 3 kV.

We use N1259A with options 033 1 kΩ resistor, option 020 High Voltage Bias-Tee and option 022 100 k Ω resistor (optional) shown in figure 1-3. The module selector option 300 is handled in appendix section.

1 kΩ resistor is used for eliminating the device oriented oscillation in high gm operation region of power MOS FET. It is inserted between the gate SMU and the gate terminal of the power MOS FET as shown in Figure 1-4. There are no side-effects by inserting a 1 kΩ resistor except it becomes harder for using a narrower pulse, but a much more stable measurement by using a resistor cancels out the drawback, and this resister is always used in the following measurement examples.

Option 020 High Voltage Bias-Tee is required if you perform a CV measurement with more than 25 V DC bias, and it expands the DC bias range up to 3 kV with HVSMU. You can perform the CV measurement without Option 020 if the requirement of maximum bias voltage is less than 25 V which can be output from MFCMU-self.

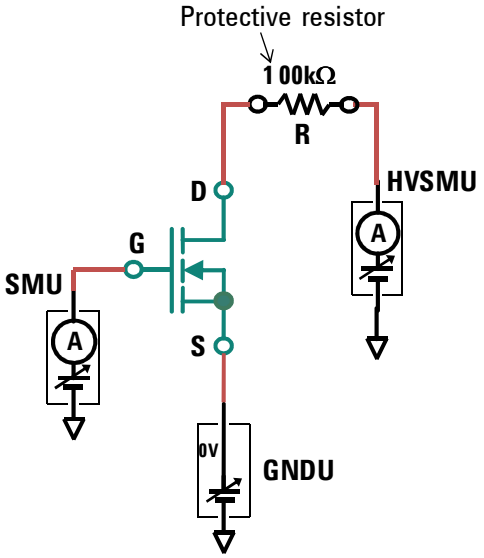


Figure 1-5. Option 022 Series R inserted between the drain and drain HVSMU.

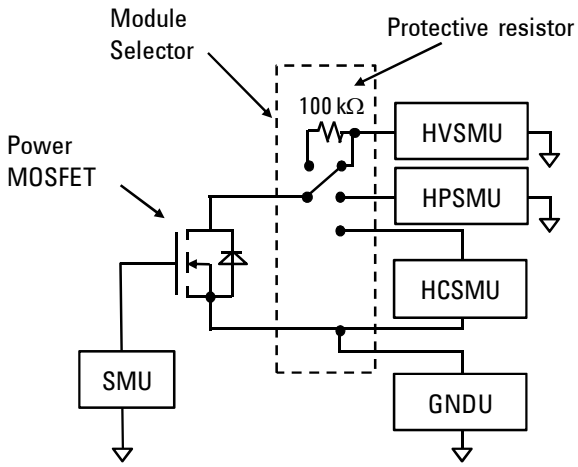


Figure 1-6. Simplified connection diagram using N1259A Option 300 Module Selector

Option 022 100 kΩ resistor is basically used by inserting 100 kΩ resistor in series between the HVSMU and the drain of the power MOS-FET as shown in Figure 1-5.

Note:

We are not using Option 300 Module Selector which is convenient for automatically switching the measurement resources between the HVSMU, HCSMU and HPSMU without manually re-connecting the cables between the power MOS-FET and each SMUs. Figure 1-6 shows a simplified image of Module Selector connected to the drain of the power MOS-FET.

We can simplify the test setup in the example by not using Option 300 and it becomes more versatile for many users. If you have option 300 installed in the N1259A, then you can simply use this option by properly interpreting the step by step instruction for the drain connection.

However the instructions for using the module selector are covered in the appendix section.

1.3 EasyEXPERT Software

The Easy EXPEERT software as a graphical user interface (GUI) of the B1505A has three types of TEST mode, Application Test, Classic Test and Tracer Test. Each TEST mode has its unique features and using an appropriate TEST mode that fits to your test requirement is important for getting a better result sooner. Following describes briefly about the B1505A`s TEST mode.

Application Test mode

The Application Test mode shown in figure 1-7 is a pre-defined test library coming with the B1505A and it includes a basic and frequently used test, for example, Id-Vd measurements. The user can start measurements by just typing in the measurement parameters and the test results with a proper data which is automatically extracted by the measurement is coming out by just pressing the Measure button.

We use improved Application Test definitions which are slightly modified version from the original version included in the B1505A. You can find the instruction for installing these files used in the handbook in the next section

It is simple and very easy for adding modifications like the example. You can refer to the application note B1500A-4 “Customizing Agilent B1500A EasyEXPERT Application Tests”, Agilent P/N: 5989-5167EN.

As a conclusion, Application Test is the best choice if it satisfies your requirement. If not, there are two choices; one is to modify the existing Application Test definition, and the other is going to Classic Test mode.

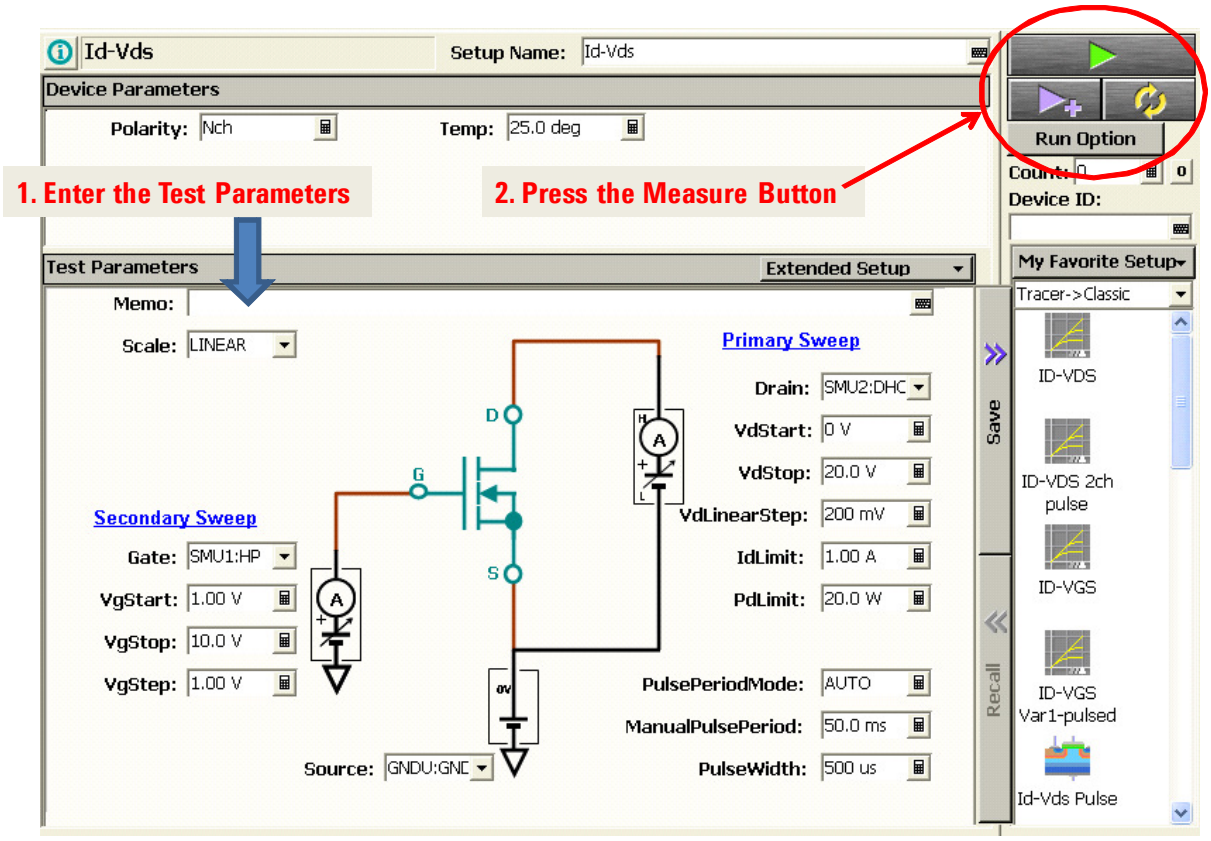


Figure 1-7. Application Test GUI

Classic Test mode

Classic Test is used inside of the Application Test definition as a main measurement engine for defining and executing a test. Classic Test can be used itself as a stand-alone test engine and it can define a unique test. The user interface of the Classic Test mode adopts the same concept of the Agilent Semiconductor Parameter Analyzers and anyone can get used to handle this interface easily. Any application that is not covered in the Application Test library can be covered by using the Classic Test mode.

Figure 1-8 shows an example Classic test setup window where 1. Channel Setup page, 2. Measurement Setup page and 3. optional SMU parameter setup sub-panels and 4. Display setup page that is minimum pages you have to fill in before starting measurements.

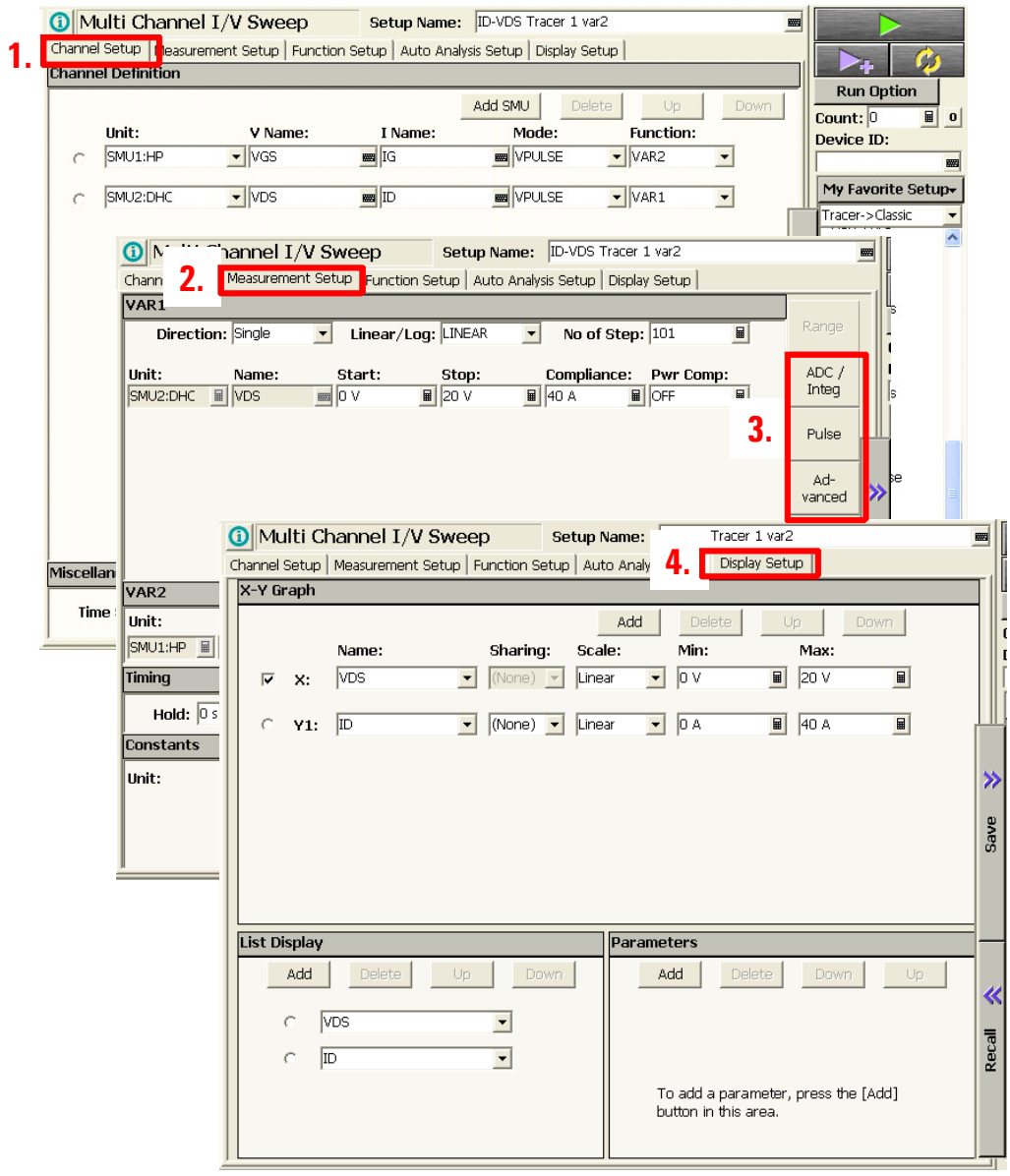


Figure 1-8. Example Classic Test measurement parameter setup panels.

Setting up a new Classic Test definition requires more knowledge as like the connection between the device and SMUs of the B1505A and the function setup of the SMUs as shown in figure 1-8 compared to the pre-defined Application Test. Generally speaking, the user can interact more directly to the SMU control in the case of Classic Test compared to the Application Test which is somewhat black box to the user until knowing the inside setup by sneaking in the Application Test definitions.

After you create a new Classic Test definition, you may have two choices; one is continuously using that Classic Test definition or the other is converting the Classic Test definition to a new Application Test definition. Creating a new Application Test is effective if the new test definition is used by many people for relatively long period because you can add more information to the user or operator through the Application Test GUI and it can be considered as a simple record of the test definition.

Note: The Classic Test example setups used in the example application Test definitions are included in the same example file set of the Application Test.

You can modify the measurement details such as user function, auto-analysis and display items by using the example setups

Tracer Test mode

Tracer Test mode shown as an example in figure 1-9 provides a real time feedback in controlling the measurements like a curve tracer and it is useful as a debugging tool for characterizing or quick check of a new or unknown devices. In the Tracer Test mode, you can change the measurement parameters while the test is repeatedly executed, for example, the drain voltage of the Id-Vd sweep can be manually changed by rotating a knob of the B1505A like rotating a voltage dial of the curve tracer.

Figure 1-9 shows an interactive dual polarity sweep which sweeps to both positive and negative direction for drain voltage for characterizing the on characteristics of power MOS-FET.

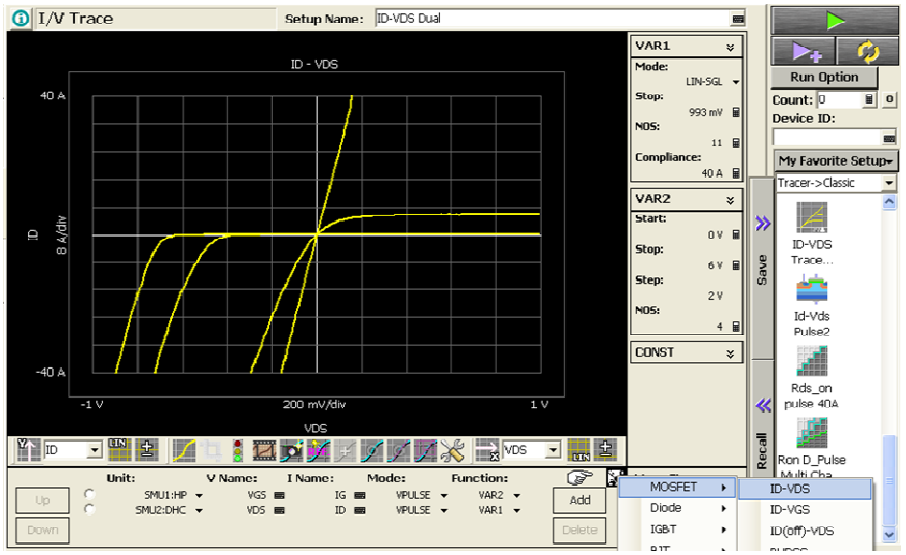


Figure 1-9. Example Tracer Test mode GUI.

There are other ways for using the Tracer Test mode. Since the Tracer Test setup can be easily converted to a Classic Test setup, you can use Tracer Test mode as an easy test setup and test debugging tool by using the sample setup features which will automatically set complicated setup and the interactive measurement control features. Then, you can convert the completed setup to a Classic test for repeated use with fixed measurement parameters or adding extra display traces and analysis functionalities such as automatic markers or lines.

Note: Dual polarity example setup is included in the example setup files.

These three test modes are used in the test setup examples in this handbook for measuring the parameters found in the specification or data sheet of power MOS-FET.

2-1. Before using B1505A

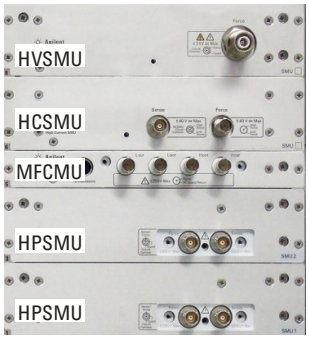
WARNING **There are potentially hazardous voltages (3000 V for HVSMU, and 200 V for HPSMU) present at the Force, Sense, and Guard terminals of Agilent B1505A. To prevent electrical shock, the following safety precautions must be observed during the use of B1505A.**

- Use a three-conductor AC power cable to connect the cabinet (if used) and B1505A to an electrical ground (safety ground).
- You must connect an interlock cable between B1505A and the test fixture.
- Confirm periodically that the interlock function is functional.
- Do not modify the interlock circuit.
- Do not use extension cables for connecting the DUT the outside of the test fixture.
- Before touching the connections on the Force, Guard, and Sense terminals, turn the B1505A off and discharge any capacitors. If you do not wish to turn the B1505A off, complete all of the following items, regardless of the B1505A settings.
    - Press the Stop key to turn the module output off.
    - Confirm that the High Voltage indicator is not lit.
    - Open the shielding box access door.
    - Discharge any capacitors connected to an SMU.

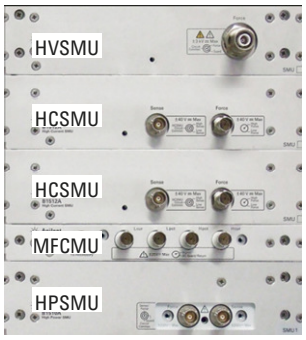
2-2. Instruments and Accessories used in the measurement examples

We use the following two B1505A configurations in the measurement example, one is 20 A configurations that uses two HPSMUs and one HCSMU (figure 2-1(A)) and
the other is 40 A configuration that uses one HPSMU and two HCSMUs (figure 2-1 (B).

You can use the same sample example files by just replacing the corresponding SMU names.



(A) Two HPSMU configuration.



(B) Two HCSMU configuration.

Figure 2-1. B1505A configuration used in the example.

Agilent B1505A Power Device Analyzer/Curve Tracer

20 A configuration:

- 1 X HVSMU (B1513A) High Voltage SMU
- 1 X HCSMU (B1512A) High Current SMU
- 2 X HPSMU (B1510A) High Power SMU (Note: only one HPSMU is used in the example)
- 1 X MFCMU (B1520A) Multi-Frequency CMU

40 A configuration:

- 1 X HVSMU (B1513A) High Voltage SMU
- 2 X HCSMU (B1512A) High Current SMU
- 1 X HPSMU (B1510A) High Power SMU
- 1 X MFCMU (B1520A) Multi-Frequency CMU

Figures 2-2. Agilent N1259A Test Fixture

Following shows the N1259A test fixture configuration and cables used for connecting between B1505A and the N1259A.

Agilent N1259A High Power Test Fixture

- Opt 020 High Voltage Bias Tee
- Opt 300 Module Selector (Optional: Check appendix section for using the Module Selector)
- Opt 010 Inline package socket module (3 pin)
- Opt 022 100 kΩ R-Box (Optional)
- Opt 033 1 kΩ R-Box
- (10 X Test leads, 2 X SHV cables and SHV-Banana adapters are including in the N1259A)

Cables

(40A configuration is noted in parenthesis for each items)

- 1 X 16493S HCSMU Cable (2 X for 40 A config.)
- 1 X 16493T HV Triax Cable
- 4 X 16494A Triax Cable (2 X for 40 A config.)
- 1 X 16493L GNDU Cable
- 1 X N1300A CMU Cable
- 1 X 16493J Interlock Cable

16493T HV Triax

16494A Triax Cable

N1300A CMU Cable

16493T HCSMU Cable

16493J Interlock Cable

Figure 2-3. Cables used for connecting between the B1505A and the N1259A

The following adapter and the cable are required for configuring the 40 A solution by using two HCSMU modules.

Optional accessories (for 40A configuration only):

- 1 X 16493S Opt 021 Dual HCSMU Combination Adapter
- 1 X 16493S Opt 021 cable

16493S Opt 021
(40 A option)

16493S Opt 021 Cable
(40 A option)

Figures 2-4. Cables used for 40 A configuration

Note:

Digital I/O cable shown in figure 2-5 is used for controlling the N1259A Option 300 Module Selector.
Since the Module Selector is not used in this section, there is no need for connecting this cable at the moment.

However Module Selector is handled in appendix section where the N1259A Option 300 Module Selector is used for automatically switching between HCSMU and HVSMU.

16493G Digital I/O Cable
(Optional for N1259A Opt 300)

Figure 2-5. Digital I/O Cable

2-3. Devices used in the measurement examples

The following two devices are used in the measurement examples of this handbook.

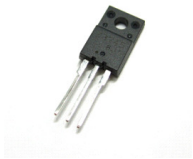
2SK2745LS is a high-voltage power MOS-FET and this transistor is used in the high voltage measurement examples. The maximum current of this transistor is limited by two amperes and it is not good for high current measurement examples.

We use IRFP2907 for measuring high current parameter extractions in the following examples. These two power MOS-FETs used in the example in the next chapter are suitable for showing the full capabilities of the B1505A`s performance in wide range of applications.

The test setup of the B1505A is not being affected by which power MOS-FET is used, and the user can just enter an appropriate parameters depending on the specification of the power MOS-FET used.

Power MOS-FET specifications

2SK3745LS – High voltage applications



2SK3745LS

- BVdss: > 1500 V (ID=1 mA, Vgs=0 V)
- Vgss: < +-20 V (Absolute Maximum)
- Idss: < 100 μA (Vds=1200 V, Vgs=0 V)
- Igss: < +-10 μA (Vgs=+-10 V, Vds=0 V)
- Idp < 4 A (Absolute Maximum)
- PD 35 W (Tc=25 degC)
- Vgs(off): 2.5-3.5 V (Vds=10 V, Id=1 mA)
- |yfs|: > 0.7 S, typ. 1.4 S (Vds=20 V, Id=1 A)
- Rds(on): < 12 Ω, typ. 10 Ω (Id=1A, Vgs=10V)
- Vsd: <1.2 V (Id=2 A, Vgs=0 V)
- Ciss: typ. 380 pF (Vds=30 V, f=1 MHz)
- Coss: typ. 70 pF (Vds=30 V, f=1 MHz)
- Crss: typ. 40 pF (Vds=30 V, f=1 MHz)

IRFP2907 – High current for automotive applications

IRFP2907

- BVdss: > 75 V (ID=250 μA, Vgs=0 V)
- Vgss: < +-20 V (Absolute Maximum)
- Idss: < 200 nA (Vds=75 V, Vgs=0 V)
- Igss: < +-200 nA (Vgs=+-20 V, Vds=0 V)
- Idp < 840 A (Absolute Maximum)
- PD 470 W (Tc=25 degC)
- Vgs(th): 2.0 V-4.0 V (Vds=10 V, Id=250 μA)
- |gfs|: > 130 S (Vds=25 V, Id=125 A)
- Rds(on): < 4.5 mΩ, typ. 3.6 mΩ (Id=125 A, Vgs=10V)
- Vsd: <1.3 V (Id=125 A, Vgs=0 V)
- Ciss: typ. 13,000 pF (Vds=25 V, f=1 MHz)
- Coss: typ. 2100 pF (Vds=25 V, f=1 MHz)
- Crss: typ. 500 pF (Vds=25 V, f=1 MHz)

2-4. Cable Connection between the B1505A and the N1259A Test Fixture

Before starting the measurements, connect the cables between the B1505A and the N1259A depending on which configurations to use, 20 A or 40 A. These connections are used for all the measurement examples, and there is no need for changing this configuration.

2-4-1. 20 A configuration

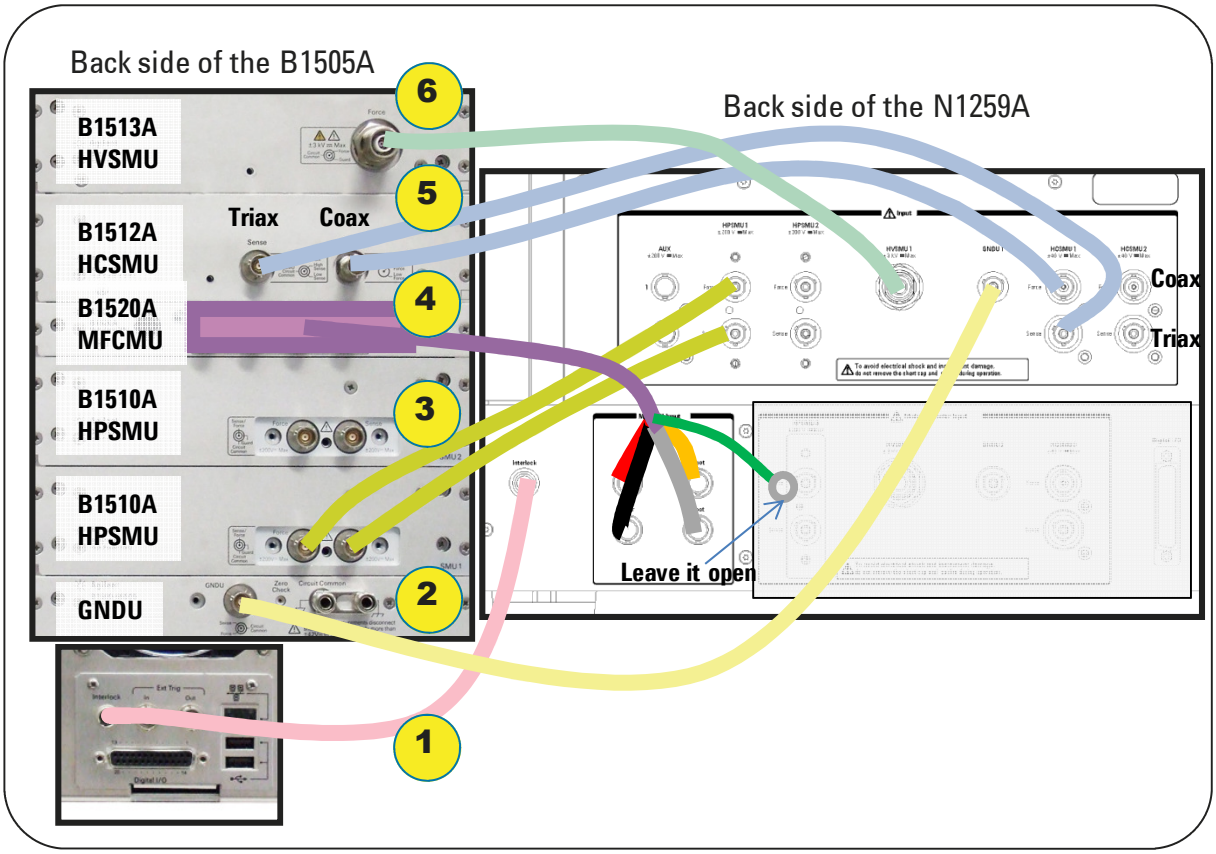


Figure 2-6. Connections for 2x HPSMU and 1x HCSMU 20 A Configuration.

20A configuration is used when only one HCSMU is installed in the B1505A.

Connect the cables between the B1505A and the N1259A as shown in figure 2-6 by following the step number 1 to 6.
The breakdown of each steps with cable figures and the connector locations are shown in figure 2-7.

Step number 1:

Using a 16493J Interlock Cable, connect the Interlock on the B1505A and the Interlock on the N1259A

Tips:

For connecting the interlock cable, hold the black plastic part and then turn the connector by pressing toward the interlock connector in the instrument side as shown in figure 2-8.

For disconnecting the interlock cable, hold the metal part and turn pull by turning the connector.

Step 1

Step 2

Step 3

Step 4

Step 5

Step 6

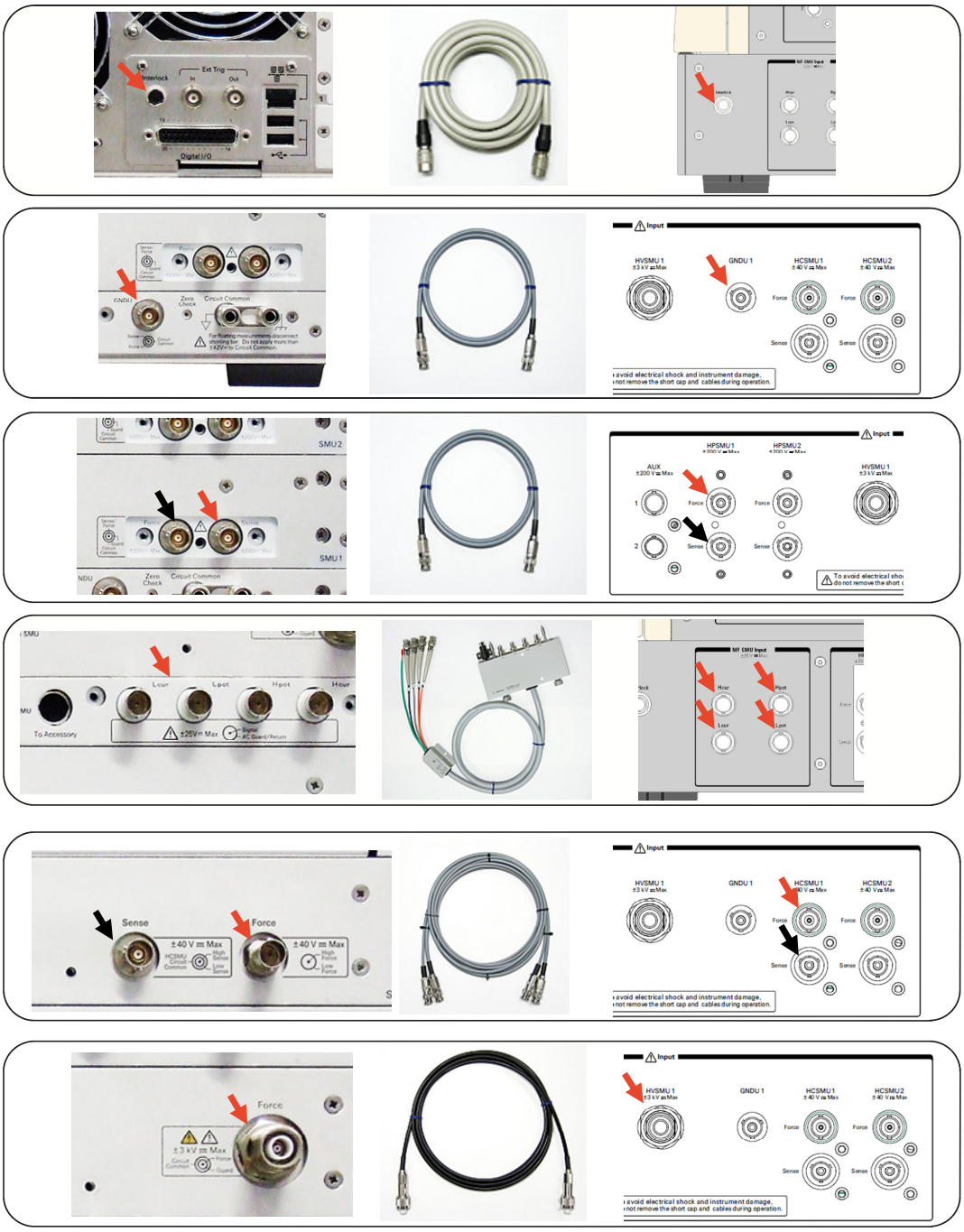


Figure 2-7. Breakdown of the cable connection for 20 A configuration.

For connecting:

Pressing and turn

For disconnecting:

Pulling and turn

Figure 2-8. Interlock connection.

Step number 2:

Using a 16493L GNDU Cable, connect the GNDU on the B1505A to the GNDU1 Input on the N1259A.

Step number 3:

Using a 16494A Triax Cable, connect the Force and Sense connectors on the lower B1510A HPSMU (SMU1) to the respective connectors on the HPSMU1 input of the N1259A.

Note: HPSMU uses a pair of two triax cables. HCSMU cables look similar as HPSMU cables, but HCSMU cables are a pair of a coax cable and a triax cable. It is a good practice for distinguishing these two cables.

Step number 4:

Using a N1300A CMU Cable, connect the B1520A CMU to the respective connectors of MF CMU Input (Hcur, Hpot, Lcur, Lpot) on the N1259A.

Note: Leave the green cable with a round terminal as it is.

Step number 5:

Using a 16493S HCSMU Cable, connect the Force and Sense connectors on the B1512A HCSMU to the respective connectors of HCSMU1 Input on the N1259A.

Note: HCSMU cables are a pair of a coax cable and a triax cable. In case of HPSMU, it uses a pair of two triax cables. It is a good practice for distinguishing these two cables.

Step number 6:

Using a 16493T HV Triax Cable, connect the Force connector on the B1513A HVSMU to the HVSMU1 input of the N1259A

2-4-2. 40 A configuration

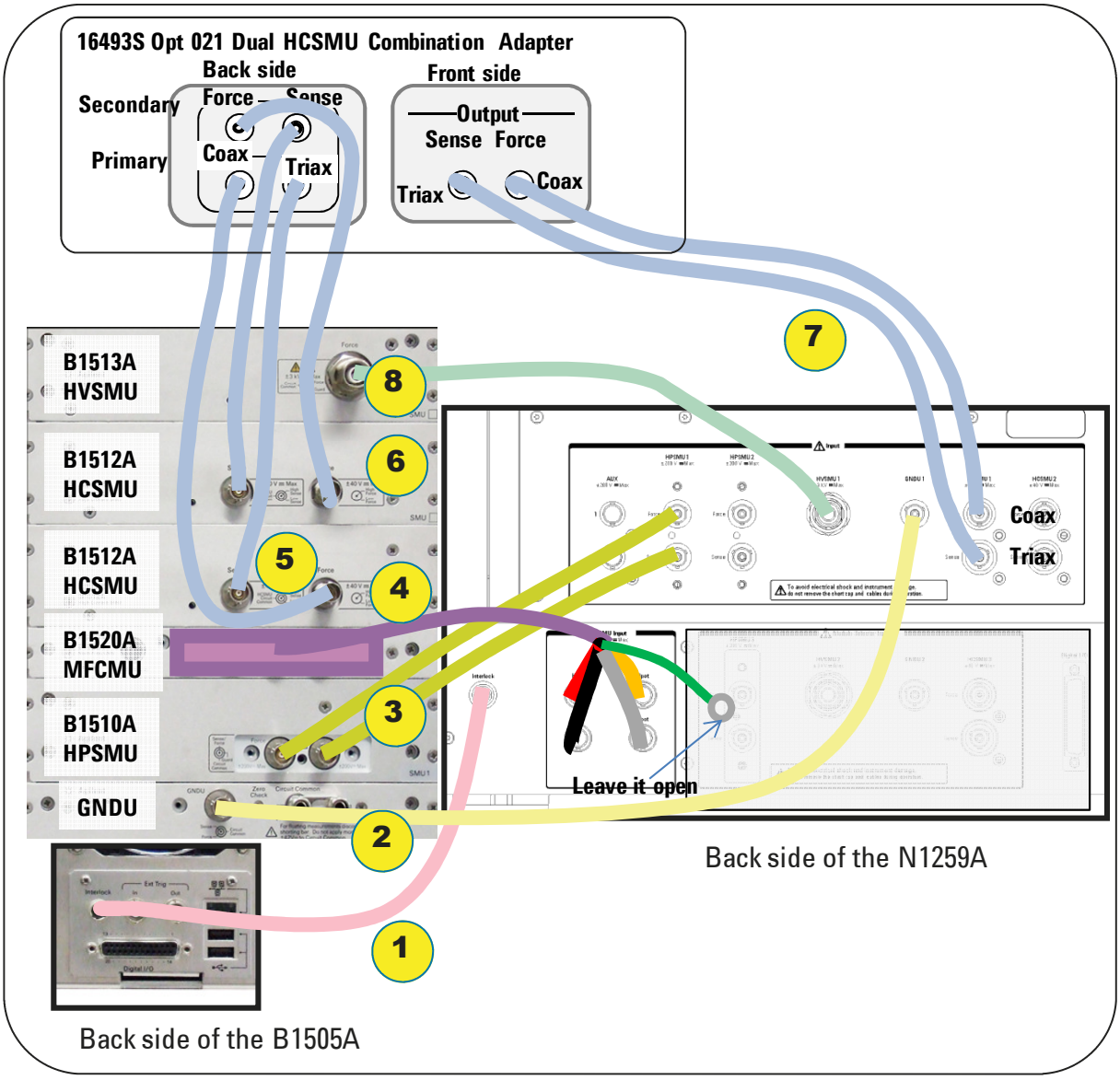


Figure 2-9. Connections for 1x HPSMU and 2x HCSMU 40 A Configuration.

40 A configuration is possible only when two HCSMUs are installed in the B1505A. Use this configuration if your device requires more than 20 A current.

Connect the cables between the B1505A and the N1259A as shown in figure 2-9 by following the step number 1 to 7.
The breakdown of each steps with cable figures and the connector locations are shown in figure 2-10.

Step number 1 to 4:

The step number from 1 to 4 is the same as the 20 A configuration, and follow the steps of the 20 A configuration.

Step number 5: (See figure 2-10)

Using a 16493S HCSMU Cable, connect the Force and Sense connectors on the lower side B1512A HCSMU to the respective connectors of Primary input (lower side) of 16493S Opt 021 Dual HCSMU Combination Adapter.

Note: HCSMU cables are a pair of a coax cable and a triax cable. In case of HPSMU, it uses a pair of two triax cables. It is a good practice for distinguishing these two cables.

Step number 6:

Using a 16493S HCSMU Cable, connect the Force and Sense connectors on the upper side B1512A HCSMU to the respective connectors of Secondary input (upper side) of 16493S Opt 021 Dual HCSMU Combination Adapter.

Step number 7:

Using a 16493S Opt 021 30 cm HCSMU Cable, connect the Force and Sense output connectors on the 16493S Dual HCSMU Combination Adapter (Output side) to the respective connectors of the HCSMU1 input of the N1259A

Step number 8:

Using a 16493T HV Triax Cable, connect the Force connector on the B1513A HVSMU to the HVSMU1 input of the N1259A

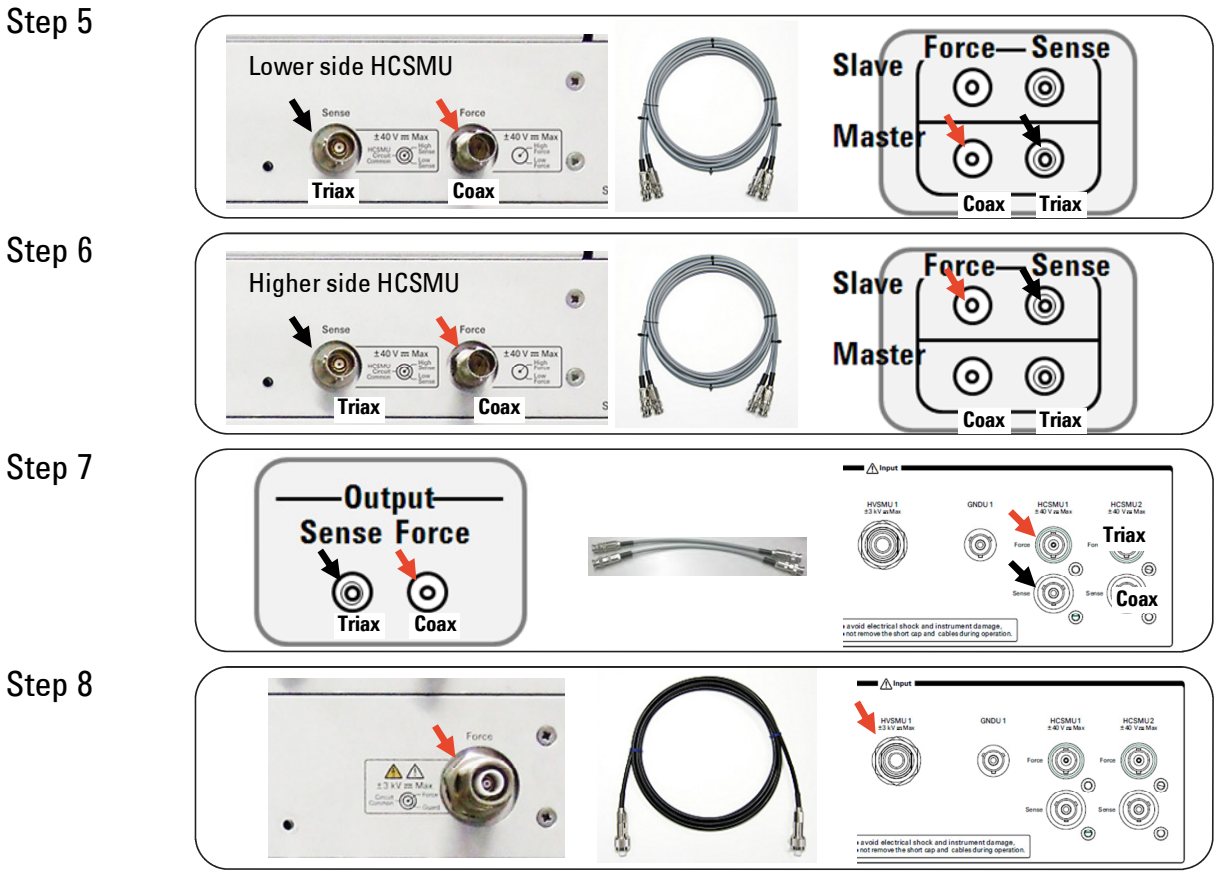


Figure 2-10. Breakdown of the cable connection for 40 A configuration .

2-4-3. Power cable, Keyboard and mouse

Be sure connecting power cable, keyboard and a mouse before starting the B1505A.

Key Board

Mouse

Power Cable

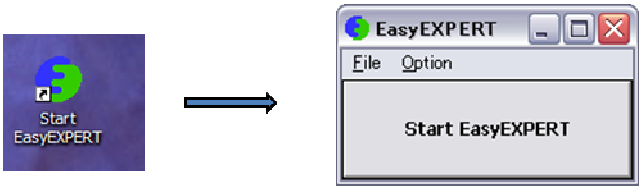
Figure 2-11. Key Board, Mouse and Power Cable.

2-5 Starting the B1505A

2-5-1 Starting the B1505A

After connecting the cables, power on the B1505A.

After Windows® starts up, click "Start EasyEXPERT" icon and then start the EasyEXPERT software by pressing the "Start EasyEXPERT" button.



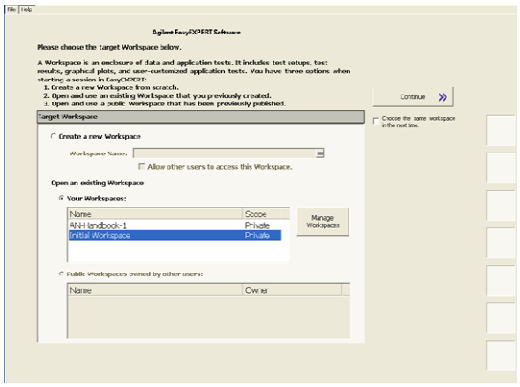


Figure 2-12. Workspace management page.

Then Workspace management page, "Agilent EasyEXPERT Software" page opens as shown in figure 2-12.

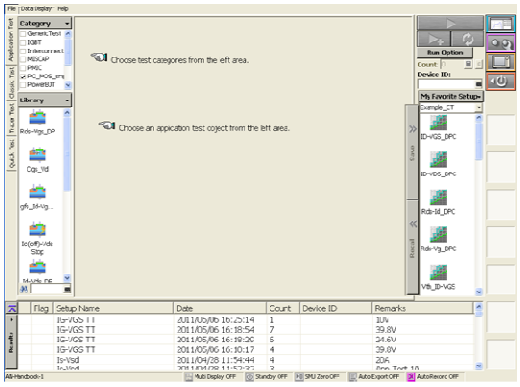


Figure 2-13. EasyEXPERT workspace.

If your B1505A directly opens one of your EasyEXPERT workspaces as shown in figure 2-13, then follow the steps shown in "How to return to Workspace Management page." in the appendix section.

If you have any other problems, please refer to the manuals (B1505A User's Guide, EasyEXPERT Software User's Guide, EasyEXPERT Application Library Reference, etc.) for more details on the EasyEXPERT software.

2-5-1-1 Creating a new workspace

Creating a new workspace is recommended for practicing the new Application Test Libraries created for this measurement handbook.

This measurement handbook includes many Application Library Test setups, Classic Test definitions, Tracer Test definitions and sample measurement data example. In the later section, the procedure for installing these setups and data files in to your B1505A is coming on.

Tips:

By creating a new workspace, you can manage your EasyEXPERT easily.
For example, if this is Agilent demo system, you can delete the new workspace when you return the system, and all of your trace including a measurement data can be deleted by a single operation.

If this operation is on your B1505A, you can practice without contaminating your existing workspace by adding unnecessary measurement setup and data.

Instruction for creating a new Workspace:

Follow the next steps for creating a new workspace:

Step 1. Open the Workspace management window as shown in the figure 2-14.

Step 2. Check "Create a new Workspace"

Step 3. Enter appropriate Workspace name. Say "AN-Handbook".

Step 4. Pressing "Continue" opens a new Workspace.

Step 5. New Workspace name appears in the lower-left corner of the current EasyEXPERT workspace.

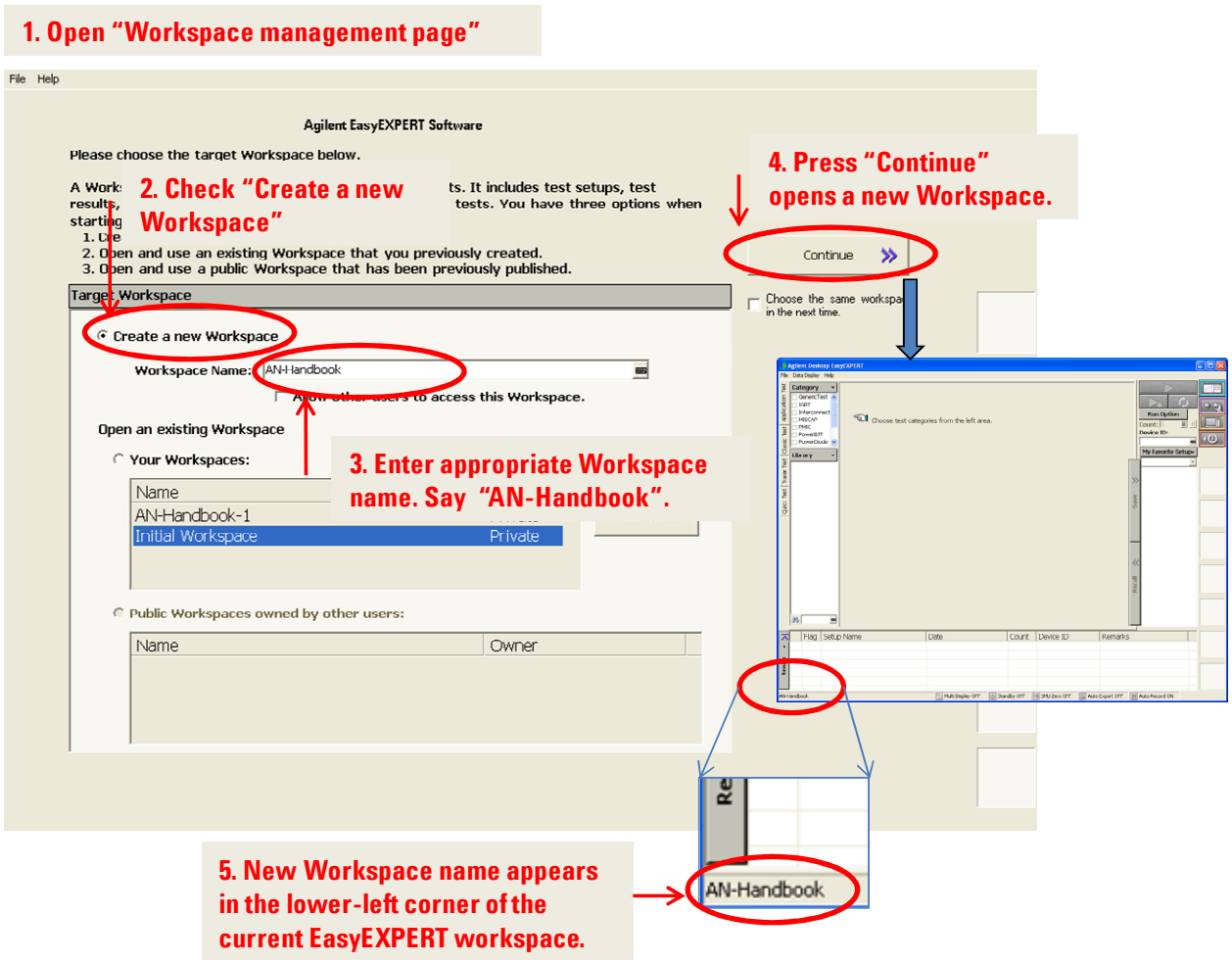


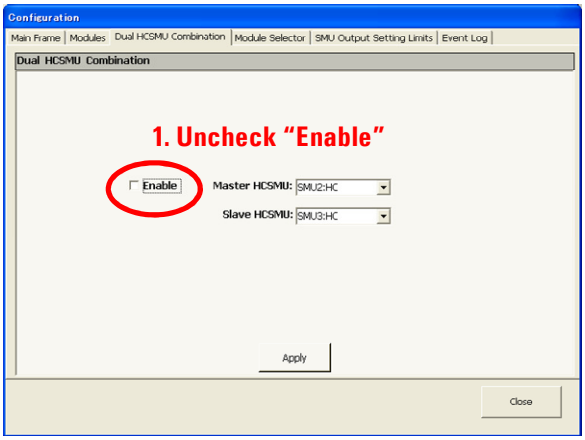
figure 2-14. Creating a new workspace

2-5-1-2 EasyEXPERT configuration before starting a measurement

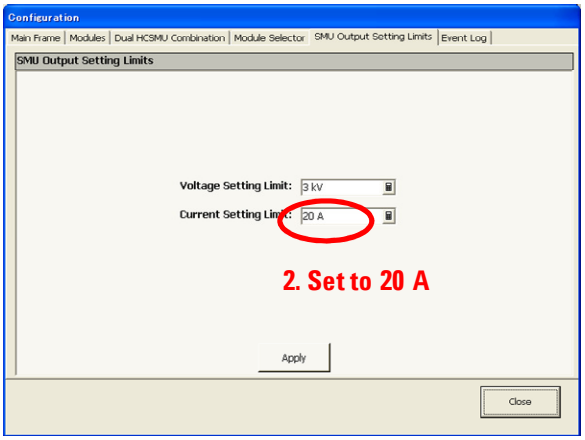
IMPORTANT

Before starting a measurement, check the configuration for HCSMU and the module selector. You can view and change the configuration as follows.

1. Click the configuration button  on the right side of the screen.
2. Select the "Dual HCSMU Combination" tab.
   Set the HCSMU Combination depending on your 20 A or 40 A hardware setting as shown in figure 2-15 and figure 2-16.
   20 A Configuration: figure 2-15 (A)
   40 A Configuration: figure 2-16 (A)
3. Select the "SMU Output Limit Setting" tab.
   Set the Current Setting Limit depending on your 20 A or 40 A hardware setting as shown in figure 2-15 and figure 2-16.
   20 A Configuration: figure 2-15 (B)
   40 A Configuration: figure 2-16 (B)
4. Select the "Module selector" tab.
   Make sure that Module selector is disabled as shown in figure 2-17.

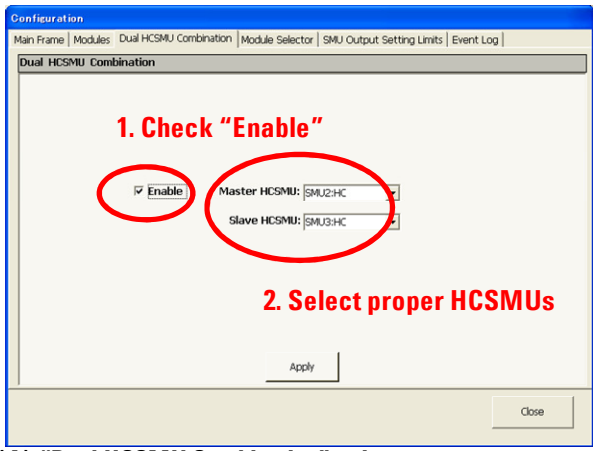


(A) "Dual HCSMU Combination" tab

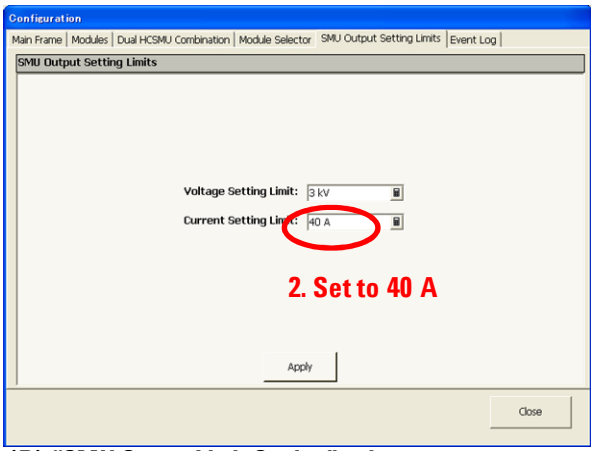


(B) "SMU Output Limit Setting" tab

Figure 2-15. 20 A Configuration setting



(A) "Dual HCSMU Combination" tab



(B) "SMU Output Limit Setting" tab

Figure 2-16. 40 A Configuration setting.

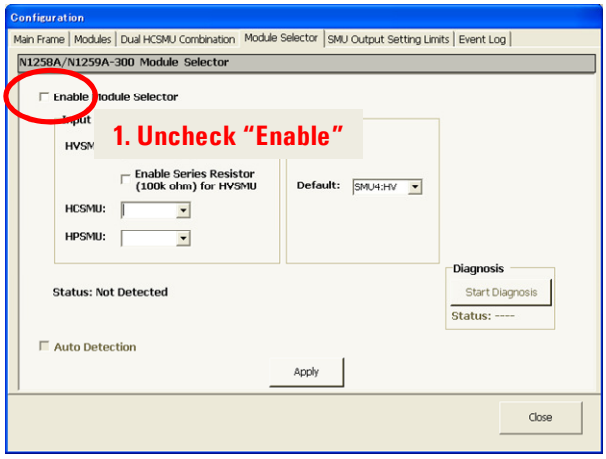


Figure 2-17. Module Selector setting.

2-5-2 Setup the example file-set to the EasyEXPERT software

Before starting the specific measurements, we are installing an example application test library, test setups and the example measurement data used in this measurement handbook.

Please follow the instruction below in order.

2-5-2-1 Download the example file-set from the Agilent web site

To get the example file set to the B1505AI, please visit Agilent web site and download the example file-set.

Please refer to Appendix 1 about the instructions for downloading the example file-set.
After the download, you can copy file via CD or USB memory.

Copying the example file-set

- Copy Downloaded "B1505A_ AN_HB1_Library.zip" file to a proper folder of the B1505A`s folder, say D:/tmp or desktop.

2-5-2-2 Extracting from zip compressed file:

The downloaded "B1505A_ AN_HB1_Library.zip" file has to be extracted to the regular Windows® file format for reading from EasyEXPERT.

Follow the steps shown in figure 2-18 for extracting files from the downloaded zip file.

Step 1: Right click the B1505A_ AN_HB1_Library.zip file.

Step 2: Select "Extract All ..." menu from the pop up window.

Step 3:Extraction Window opens, and click "Next".

Step 4: Select a proper existing folder for extracting from the downloaded zip file. Then click "Next".

All the file is extracted under the "B1505A_ AN_HB1_Library" parent folder.

Please remember this folder name for the later use for importing files to EasyEXPERT software.

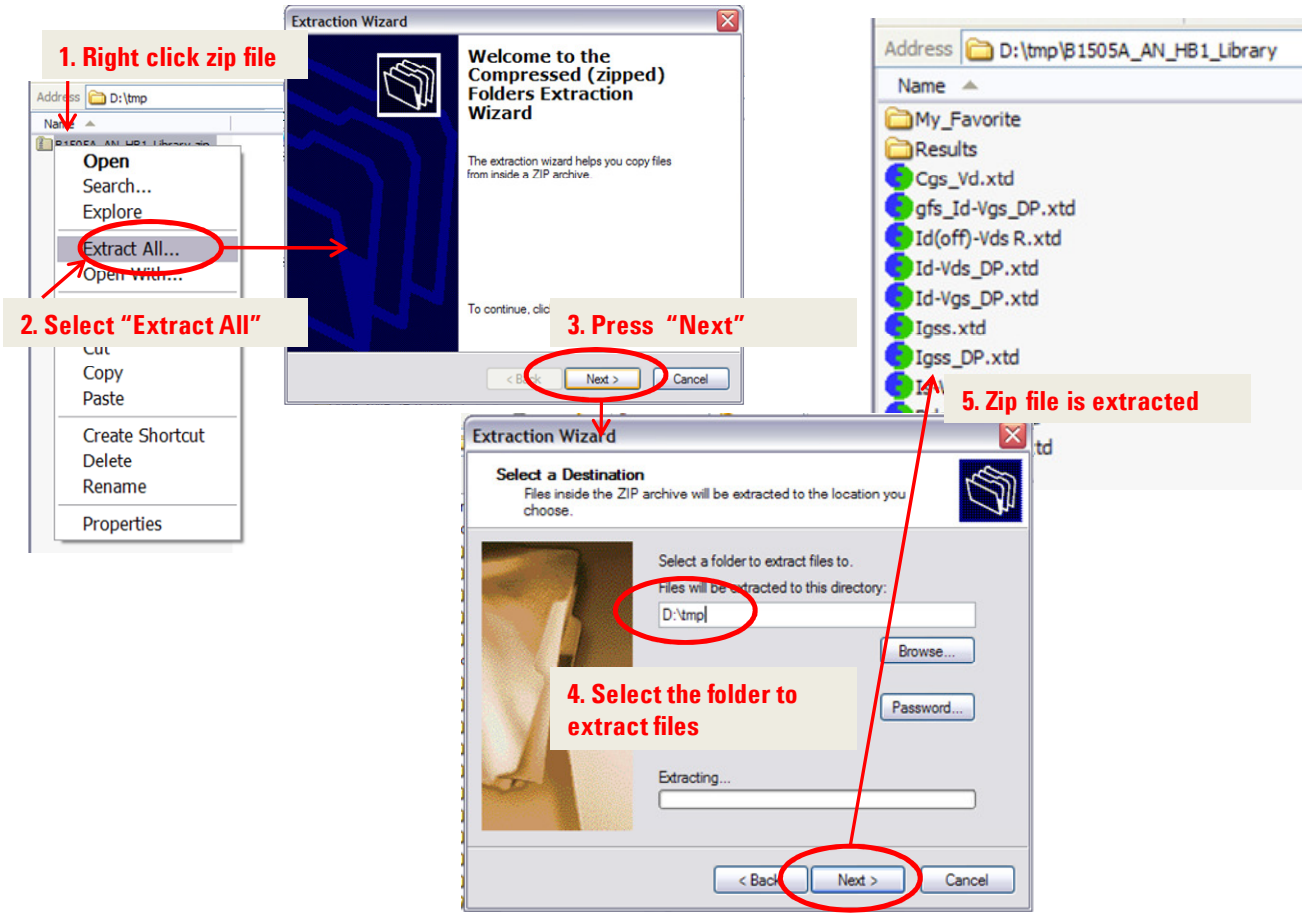


Figure 2-18. Extracting the downloaded zip file.

Extracting the compressed file produces the following three types of file set.

1. New Application Test definitions:

- Cgs_Vd. xtd : Cgs versus Vd measurement (max 100 kHz)
- gfs_Id-Vgs_DP.xtd : Gfs or yfs measurement using a dual pulse for both the gate and the drain
- Id(off)-Vds R.xtd: Id off and Vbd measurement where Vd sweep stops at the detection of Vbd
- Id-Vds_DP.xtd: Id versus Vd measurement using a dual pulse for both the gate and the drain
- Id-Vgs_DP.xtd: Id versus Vgs measurement using a dual pulse for both the gate and the drain
- Igss.xtd: Ig versus Vg measurement
- Igss_DP.xtd: Ig versus Vg measurements for both the positive and the negative dual polarity
- Is_Vsd.xtd: Diode Forward Voltage measurement
- Rds-Id_DP.xtd: Rds versus Id characteristics by using Id-Vg dual pulse test
- Rds-Vgs_DP.xtd: Rds versus Vgs characteristics by using Id-Vg dual pulse test

These new test definitions added to the existing library are all customized for properly measuring the data sheet specifications of power MOS-FETs. The new application definitions with _DP (dual pulse) extension are effective for measuring high Gm and high current power MOS-FETs. The other type of new application test definitions are just an supplementary application tests which were not included in the B1505A.

2. Application Test, Classic Test or Tracer Test setup files:

- Example_AT.xpg
  The Application Test setups used in this handbook are included in this file, and they can be imported in your EasyEXPERT as a Preset Group.
- Example_CT.xpg
  The Classic Test or Tracer Test setups used in this handbook are included in this file, and they can be imported in your EasyEXPERT as a Preset Group.

All the test setups introduced as the measurement samples in this measurement handbook can be accessed from the preset group of My Favorite Setup , and you can work on these files by just changing the measurement parameters or adding necessary modifications to the EasyEXPERT measurement functions,

3. EasyEXPERT example data files

- EE_example.ztr
  This file is in a format of compressed test result and it includes the sample measurement data used in the test example.

2-5-2-3 Importing the example files to the EasyEXPERT software

There is an installing order for the imported files to EasyEXPERT. Please import the example application test library at first before importing the test setup or example measurement data.

1. Importing the example application test library

The example test library is installed both in new Po_MOS_smpl application test category and the existing PowerMOSFET application category. “Po_MOS_smpl” category is created in the category section of your EasyEXPERT.

After the installation of the example application test library, the following nine application tests appear in the Library section.

Cgs_Vd, gfs_Id-Vgs_DP, Id(off)-Vds Stop, Id-Vds_DP, Id-Vgs_DP, Igss, Igss_DP, Rds-Id_DP, Rds-Vgs DP,

[PROCEDURE] – See figure 2-19

Step 1: Press “Library” bar of EasyEXPERT.

Library menu opens

Step 2: Select “Import Test Definition” from the Library menu.

Windows® Explorer opens.

Step 3: Find the folder where you extract the example file set.

Step 4: Select all the Application Test definitions as shown in Step 4 in the figure.

Step 5: Press “Open” of the Windows Explorer button.

All the Application Test definitions are imported in to the EasyEXPERT Library.

PO_MOS_smpl (Power MOS-FET sample) category is created.

All the new Application Test definitions are included to the PO_MOS_smpl and the PowerMOSFET category.

Step 6: Check “PO_MOS_smpl” in the Category window.

Step 7: The new Application Test definitions appear in the Library window.

Check if all the Application Test definition exist by scrolling the menu bar

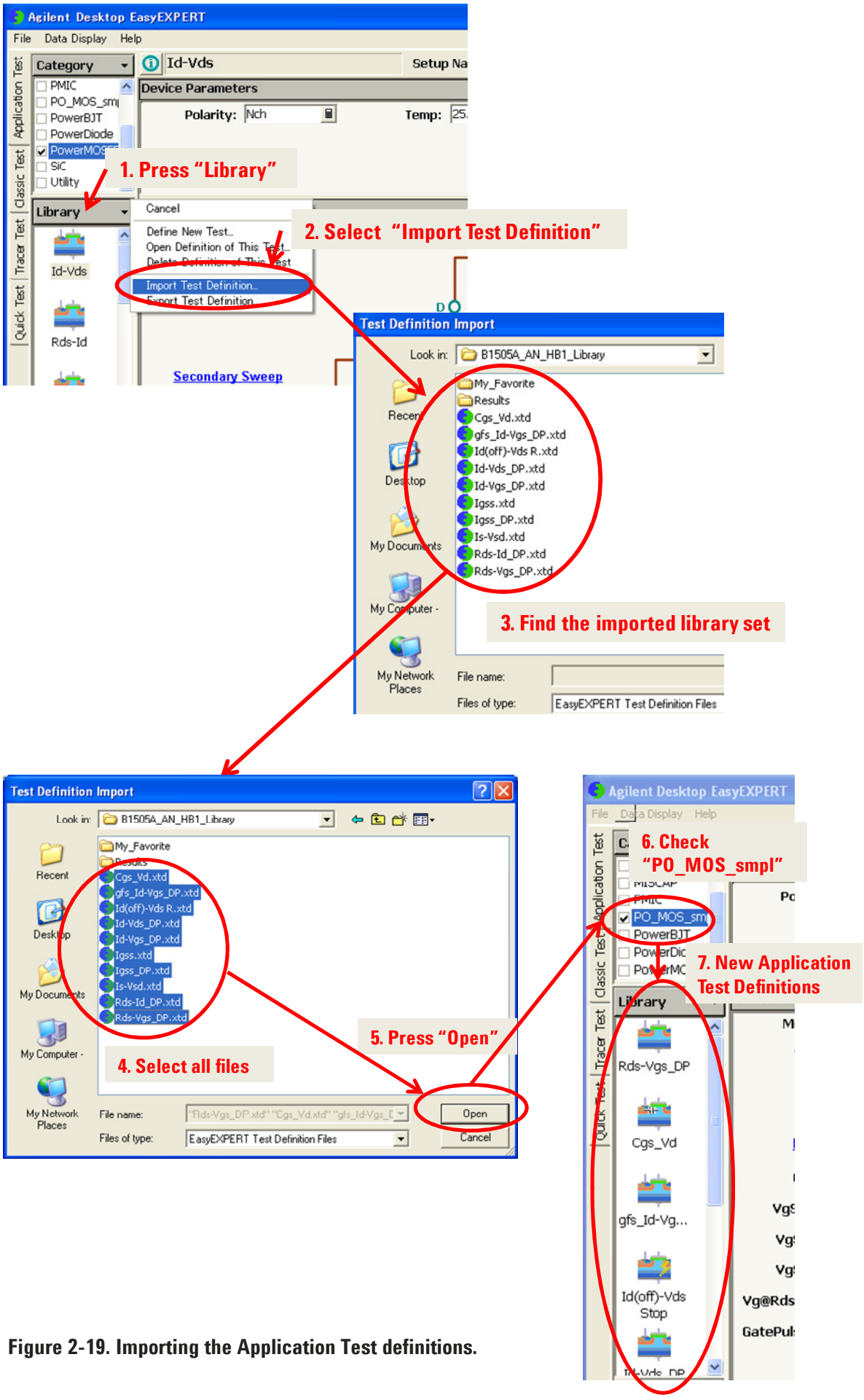


Figure 2-19. Importing the Application Test definitions.

2-5-2-4 Importing example test setup files

The example file set includes the test setups used in the example and the test setup files are imported to a preset group of My Favorite Setup.

Example test setup files include two types of setup data.

One is test setup of the Application Test definitions for each corresponding data sheet specifications used in the example. They are imported to “Example-AT” i.e. example-application test, preset group.

The other test setups are the Classic Test definitions of the corresponding application test setups. The classic test definitions provide exactly the same data as the application test setup and it is not necessary for using this setup. However these setup files are useful when you want to change some of the test functions in the example application test library, and they are provided for this purpose.

They are imported to “Example-CT” i.e. example-classic test, preset group.

[PROCEDURE] – See figure 2-20

Step 1: 1. Press “My Favorite Setup”

“My Favorite Setup menu” opens

Step 2. Select “Preset Group” from the menu list

“Preset Group menu” opens

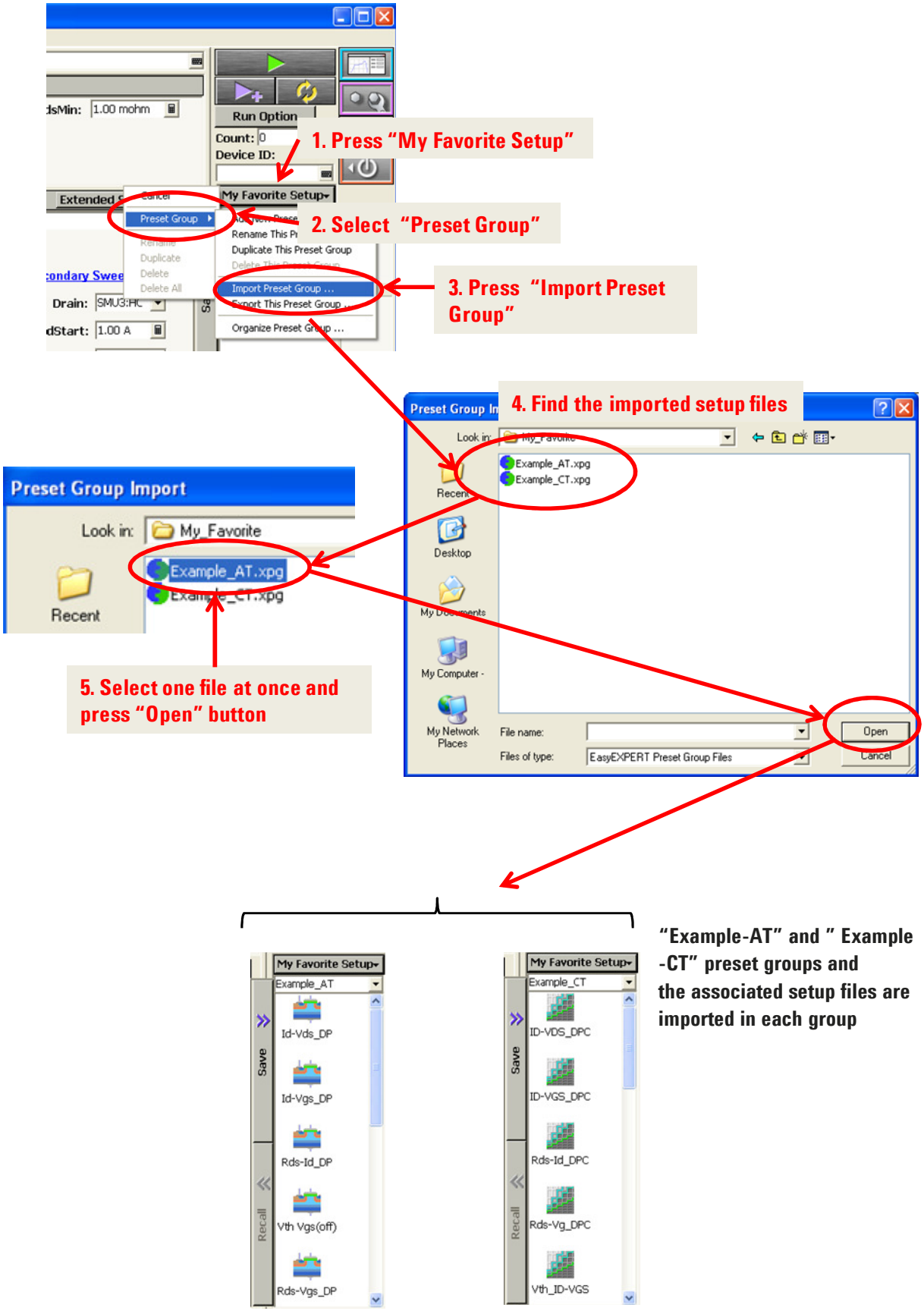
Step 3. Press “Import Preset Group” from the menu list

Windows Explorer opens.

Step 4. Find the imported setup files using the Explorer

Step 5. Select one file at once and press “Open” button

“Example-AT” and ” Example-CT” preset groups and the associated setup files are imported in each group



"Example-AT" and " Example -CT" preset groups and the associated setup files are imported in each group

Figure 2-20. Importing the My Favorite Setup files.

2-5-2-5 Importing example measurement data

Measurement data used in the examples in the handbook are included in the example file set.

If you import the data to the Results windows of EasyEXPERT, you can easily explore the EasyEXPERT functionality with a real measurement data.

[PROCEDURE] – See figure 2-21

Step 1. Press "Results".

"Results" menu opens.

Step 2. Select "Transport Data".

"Transport Data" menu opens.

Step 3. Press "Import . . ."

Windows® Explorer opens.

Step 4. Find the imported Test result file by using the Explorer.

Step 5. Select the imported file and press "Open" button.

Example data set are imported to the result area.

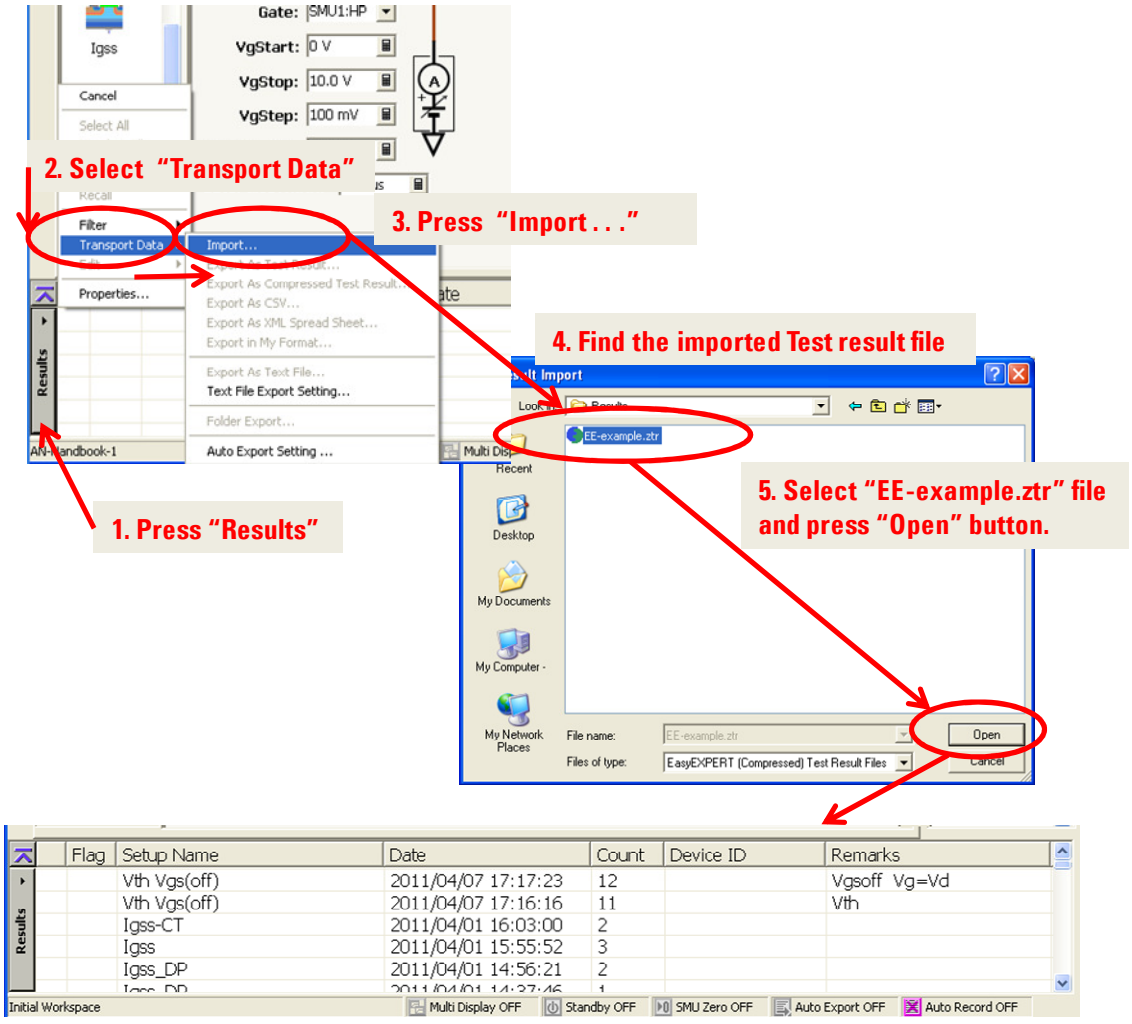


Figure 2-21. Importing the example Results data files.

Chapter 3. Measurements of Data Sheet Specifications of Power MOS-FETs

This chapter demonstrates how the B1505A measures the power MOS-FET parameters in the data sheet specifications.

The test parameters included in this measurement handbook are listed next categorized in four measurement groups.

Each measurement group uses basically the same hardware setup and the device connection. This measurement handbook introduces the measurement example by following this order in the group and the list.

1. Id-Vgs Measurement group:

- Id - Vgs curve General Id-Vg characteristics
- VGS(th), VGS(off) Gate threshold Voltage, or Cutoff Voltage
- RDS(on) Static Drain-to-Source On-State Resistance
- |yfs| , Gfs Forward Transfer Admittance, or Forward Trans conductance
- IGSS Gate-to-Source Leakage Current
- VGSS Gate-to-Source Voltage

2. Id-Vds Measurement group 1: High current

- ID - Vds curve General Id-Vds characteristics
- VSD Diode Forward Voltage
- ISD Reverse Drain Current

3. Id-Vds Measurement group 2: High voltage

- V(BR)DSS Drain-to-Source Breakdown Voltage
- IDSS Drain-to-Source Leakage Current

4. Capacitance Measurement group:

- Ciss Input Capacitance
- Coss Output Capacitance
- Crss Reverse Transfer Capacitance

General Idea of measurement using the EasyEXPERT software

Figure 3-1 shows the general idea of measurement using the EasyEXPERT Application Test Library.

The idea is straight forward and easy to use;

Step 1. Choose device type or application category from the Category field.

Or, just from step 1` where your unique setup has been saved in My Favorite Setup field, and you can just start from here by just selecting a setup icon and skip step 2 and go to step 3 Measure.

Step 2. Select Application Test definition from the Library field.

Step 3. Measurement buttons for Single measure, Append measure and Repeat measure.

Then measurement data pops up and the data can be saved in Results area automatically.

Chapter 3 uses the full features of these easy to use EasyEXPERT test environments.

EasyEXPERT has many default applications for basic measurements. You can measure the device easily, by simply selecting the desired application. With an illustrative user interface, you can intuitively modify the parameters to suit your DUT.

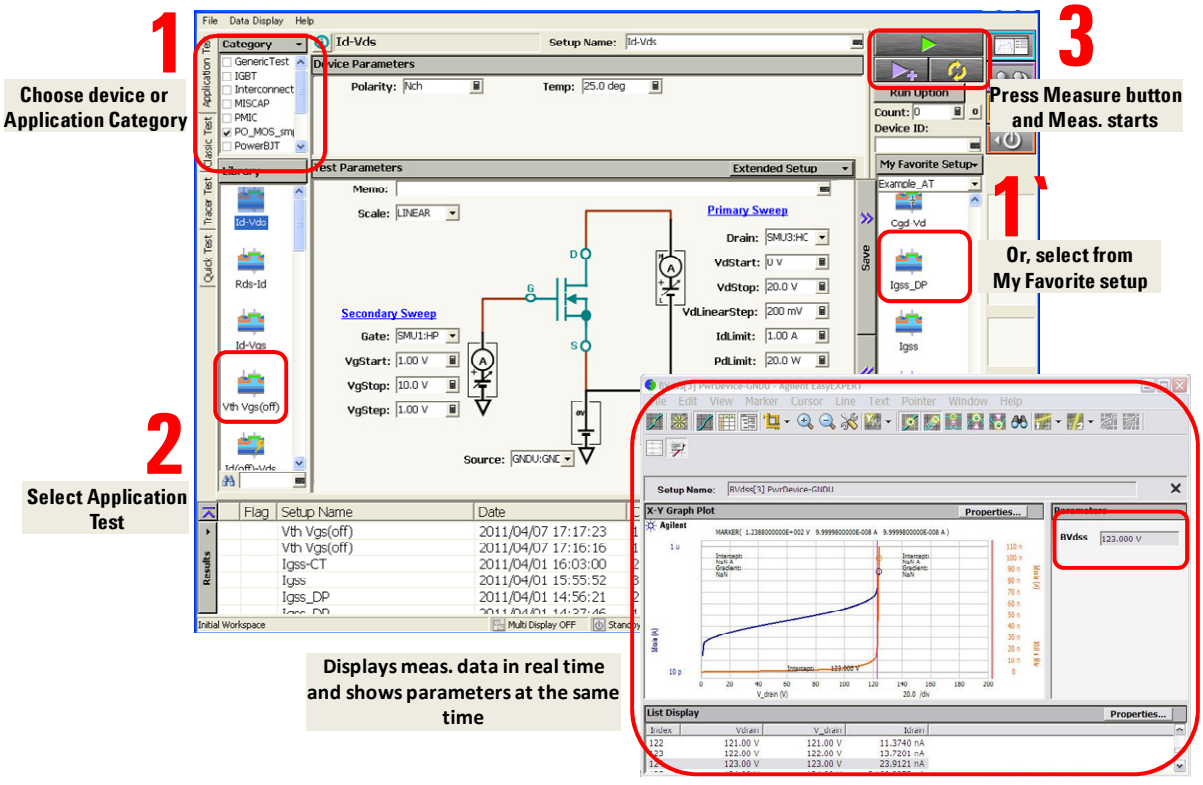


Figure 3-1. General Idea of measurement using the EasyEXPERT software.

3-1. Id-Vgs Measurement group:

This chapter, the Id-Vgs measurement group demonstrates the following measurements.

- VGS(th), VGS(off) Gate threshold Voltage, or Cutoff Voltage
- RDS(on) Static Drain-to-Source On-State Resistance
- |yfs| , Gfs Forward Transfer Admittance, or Forward Trans conductance
- IGSS Gate-to-Source Leakage Current
- VGSS Gate-to-Source Voltage

The Id-Vgs measurement group basically sweeps the gate voltage as a primary sweep source while the drain voltage stays as a constant voltage while the gate is swept as shown in Figure 3-2. Some Application Test setup can step the drain voltage as a secondary parameter which increases the drain voltage after the end of each gate primary sweep.

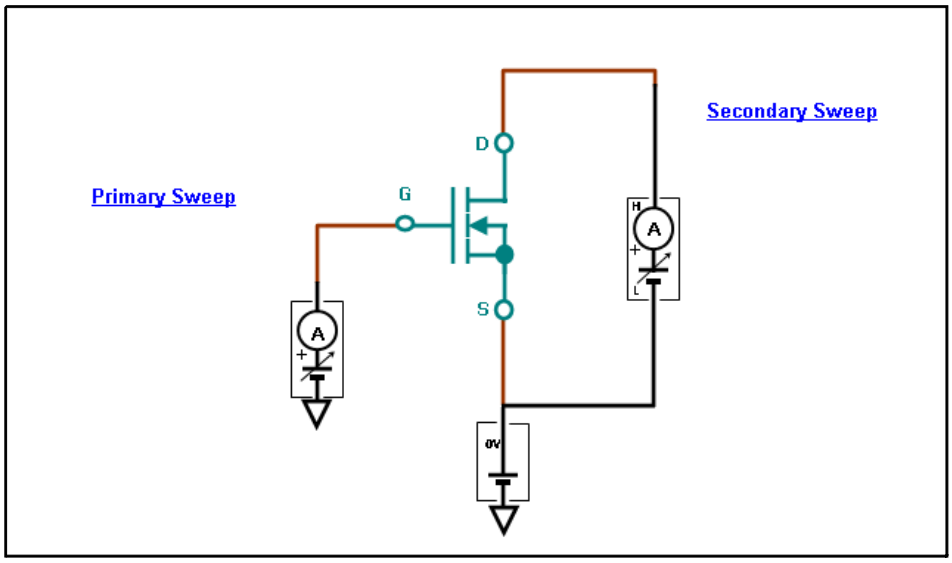


Figure 3-2. Basic configuration of Id-Vgs group measurement

Connection inside the N1259A Test Fixture

Open the N1259A test fixture cover, and connect the test leads shown in figure 3-3 by following the step numbers as shown in figure 3-4.

Figure 3-3. Test Lead for the N1259A Test Fixture

Note: The available colors of the leads are black and red only. The lead color used in figure 3-4 is for reference only.

The numbers of the procedure steps correspond to the numbers on the drawing for connecting the test leads.

[PROCEDURE]

Step 1. Insert the power MOS-FET (example: IRFP2907 or 2SK3745LS) into the socket on the N1259A. Make sure the device pin name matches the socket numbers shown in figure 3-4.

Step 2. Connect the HPSMU1 Force to the terminal 1 on the 1 kΩ resistor.

Step 3. Connect the HPSMU1 Sense to the terminal 1 on the 1 kΩ resistor.

Step 4. Connect the terminal 2 on the 1 kW resistor to the terminal 1 Force (Gate) on the Inline Package Socket.

Step 5. Connect the High-Force of the HCSMU1 to the terminal 2 Force (Drain) on the Inline Package Socket.

Step 6. Connect the High-Sense of the HCSMU1 to the terminal 2 Sense (Drain) on the Inline Package Socket.

Step 7. Connect the Low-Force of the HCSMU1 to the terminal 3 Force (Source) on the Inline Package Socket.

Step 8. Connect the Low-Sense of the HCSMU1 to the terminal 3 Sense (Source) on the Inline Package Socket.

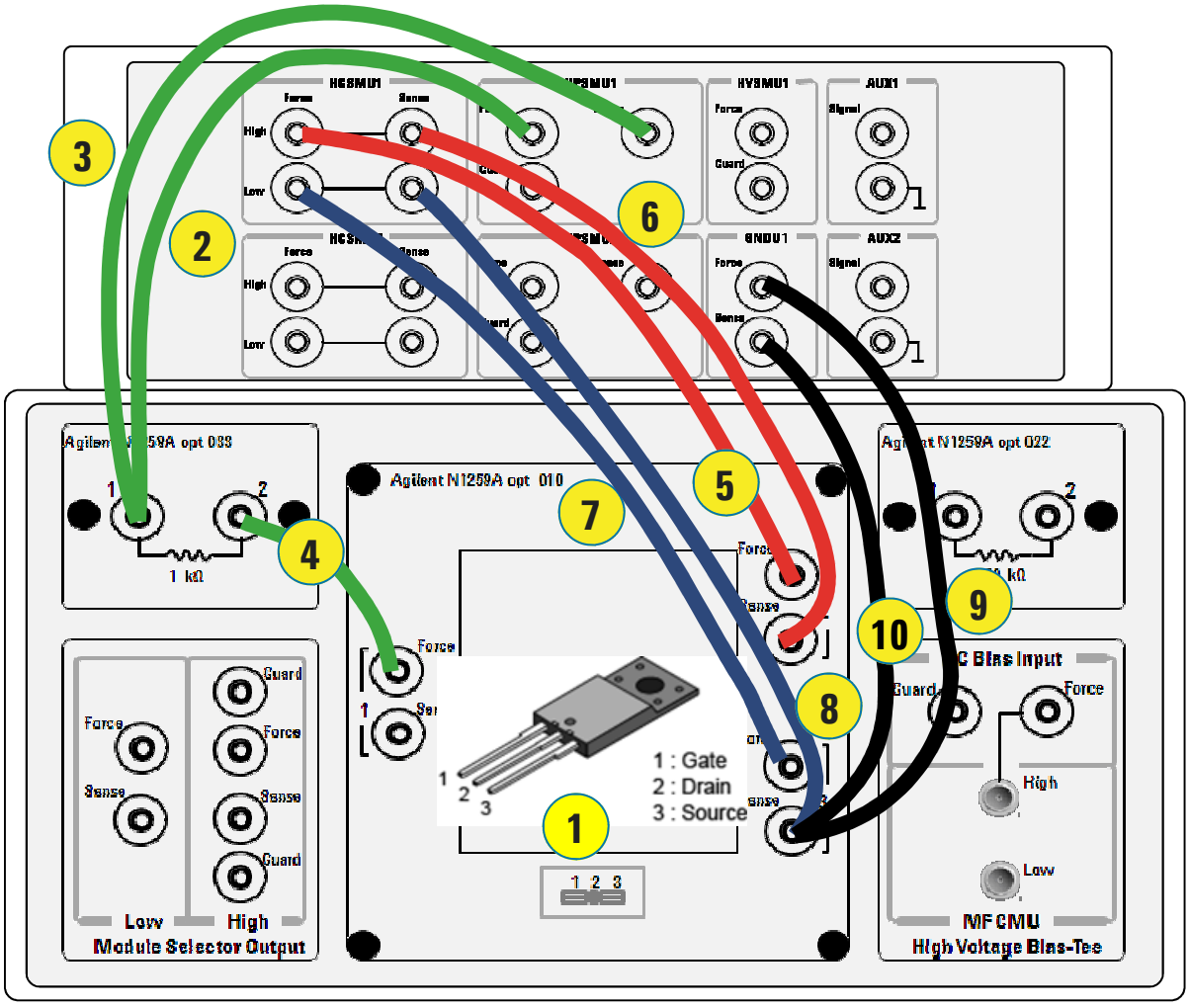


Figure 3-4. Connection between the SMUs and the power MOS-FET fixture

Step 9. Connect the GNDU1 Force to the terminal 3 Sense (Source) on the Inline Package Socket.

Step 10. Connect the GNDU1 Sense to the terminal 3 Sense (Source) on the Inline Package Socket.

Close the N1259A fixture cover.

NOTE: If Measurement is made with Opt.300 Module Selector, use the process shown in appendix A2-3-1.

Tips on connection inside the N1259A

Tips 1:

Inserting 1 kΩ resister in series near the gate terminal as in step 2 is almost must condition in measuring high gm power MOS-FETs. This register reduces the possibility of the power MOS-FET oscillation very much as explained in the appendix section.

Tips 2:

High gm and high current power MOS-FET is very sensitive in the parasitic components especially the series inductance. Sometimes the test leads layout from the HCSMU and the power MOS-FET inside the N1259A test fixture disturbs the measurements as shown in figure 3-5.

It is a good practice for lowering the wiring inductance by twisting connection ca-

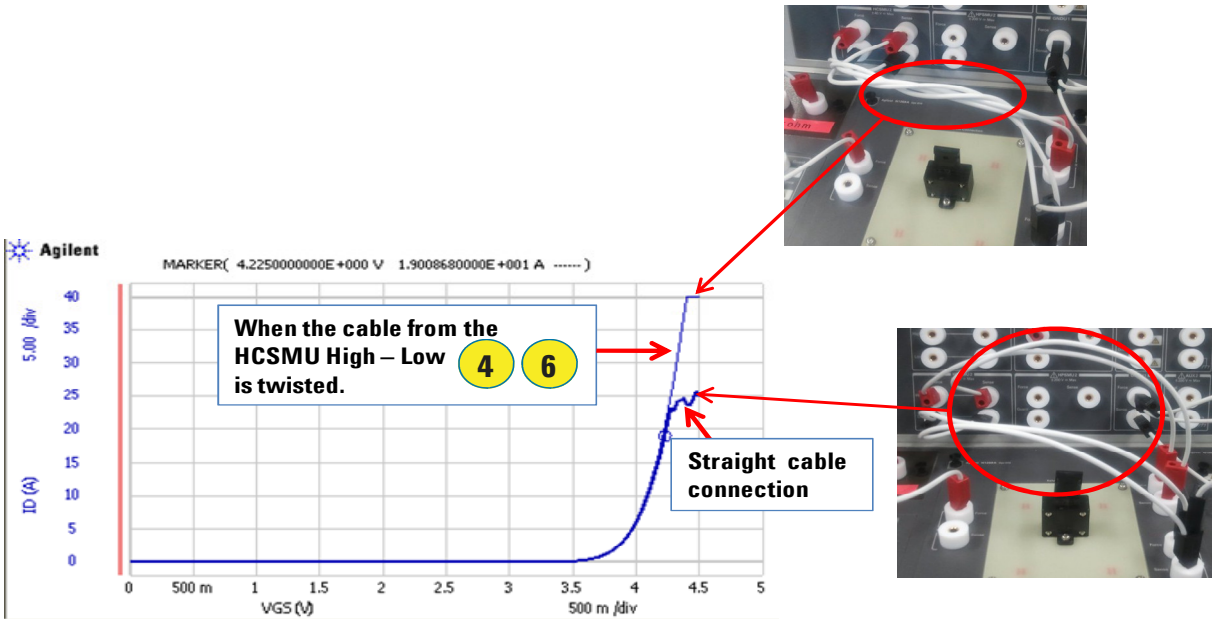


Figure 3-5. Example of the difference by the cable routing.

3-1-1. Id - Vgs measurement

Measurement Parameters: General Id-Vgs characteristics, gfs max

Application Test name: Id-Vgs_DP (Id-Vgs characteristics, SMU Dual Pulse)

Application Test setup name (My Favorite Setup -> Example_AT): Id-Vgs_DP

Classic Test setup name (My Favorite Setup -> Example_CT): ID-VGS_DPC

Device used in the example: IRFP2907

Application description:

If the characteristics of a power MOS-FET are unknown, a good practice as a general idea is starting the measurement from the Id-Vg characteristics and then maybe checking more detail from the Id-Vd measurements. These two measurements provide an overview of the power MOS-FET characteristics in the beginning of the test. Then you can proceed to more detailed measurements for other parameters like Vth, breakdown characteristics, on resistance and so on.

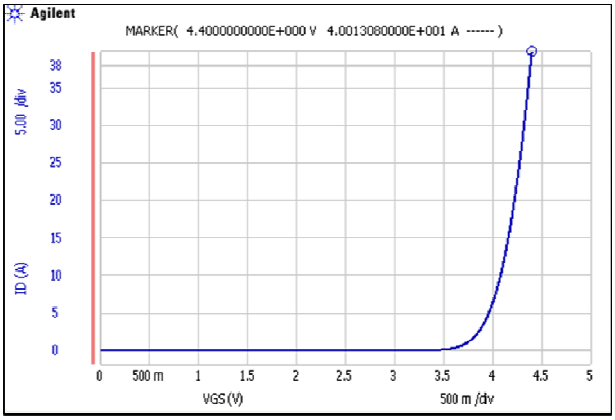


Figure 3-6. Id-Vg test example.

Typical data sheet specification starts from the general Id-Vg measurement curve shown in figure 3-6. This measurement provides important parameters in the beginning when characterizing the power MOS-FETs. Figure 3-7 shows an example setup of this test using Dual HCSMU (DHC) for expanding the maximum drain current to 40 A and Vg is swept as a primary sweep source from zero volts to a little bit above the threshold voltage for viewing the full drain swing capability while the drain voltage is fixed to 10 volts though it can be step to another voltage as a secondary sweep source. If you do sweep the drain voltage as secondary sweep source, the output graph is a bit crammed and may not be easy to distinguish from the one to the other.

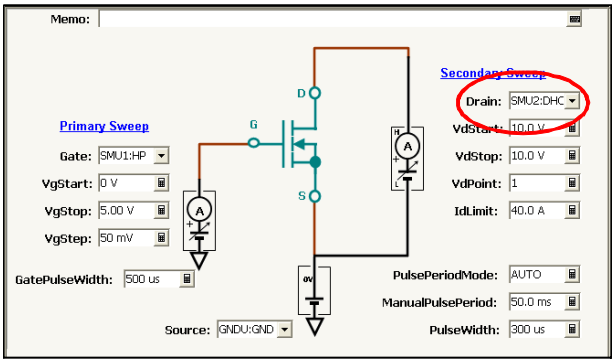


Figure 3-7. Id-Vg_DP Application Test setup using Dual HCSMU configuration.

Id-Vgs_DP Application Test definition applies pulse to both the gate and the drain for assuring a stable measurement for high current and high gm power MOS-FETs. Refer to "Improved two pulse source I/V" section in the appendix if you want to know more details about this measurement.

This test finds the Vth at the crossing of Vgs X axis coordinate of the line drawn at gm maximum point on Id-Vgs curve as shown in figure 3-9.

Since this test uses pulse in the measurement, all the SMU range is fixed to its current compliance range and the measurement range is limited to maximum six digits. In case for measuring 100 μA range of Vth, using " Vth, Vgs(off)" Application Test described next section 3-1-2.

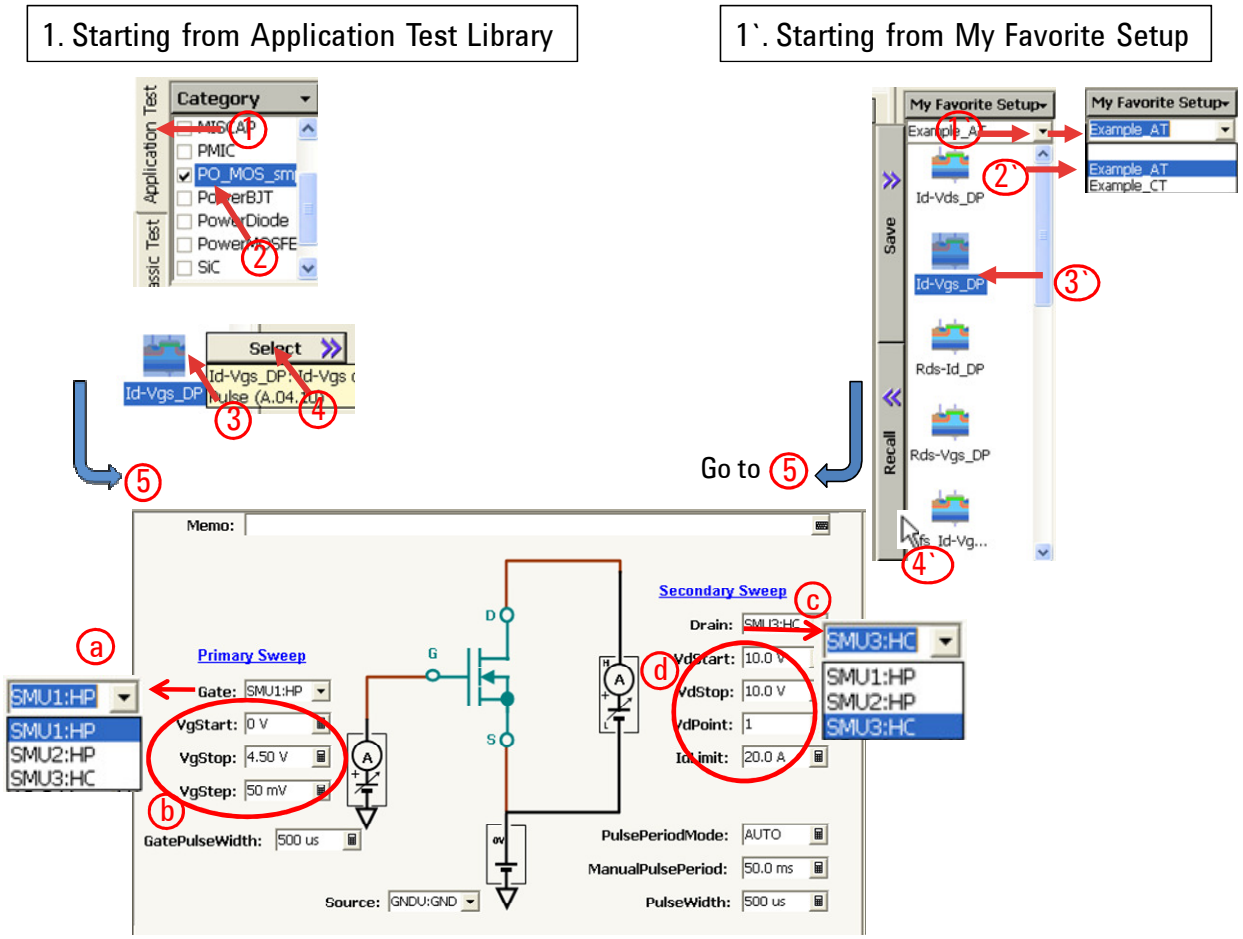


Figure 3-8. Id-VGS_DP Application Test setup.

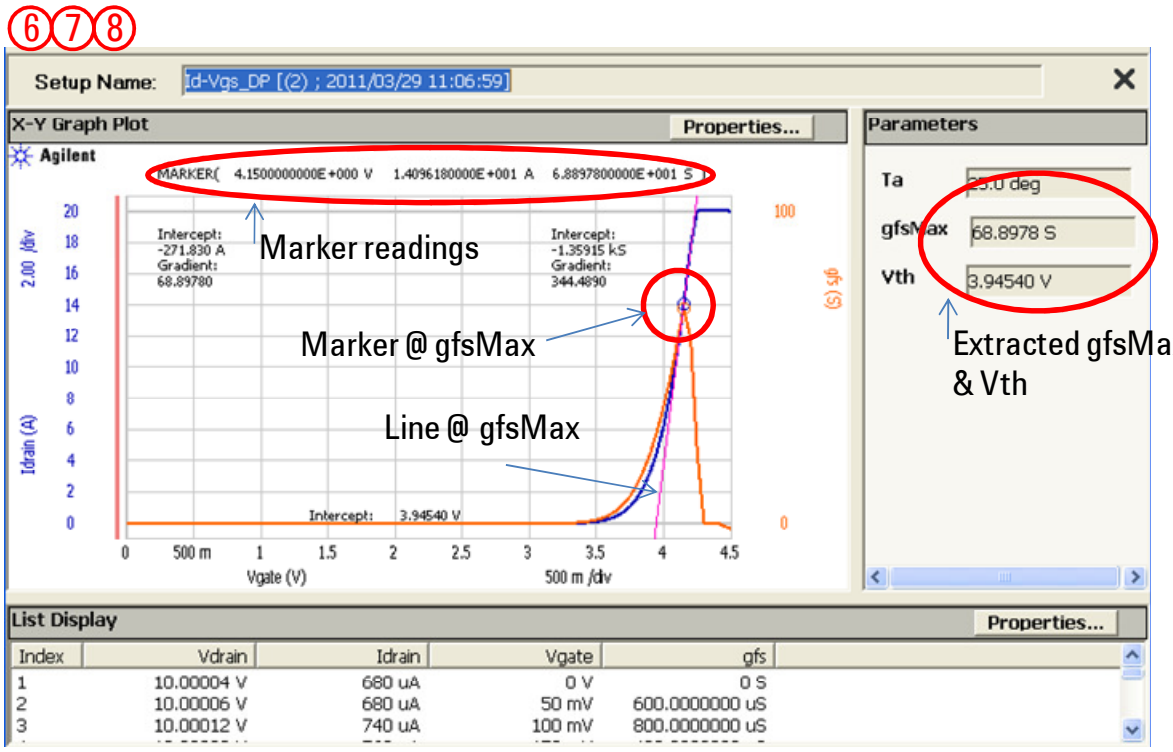


Figure 3-9. Id-VGS_DP test display.

A. Measurement Procedure: Id-Vgs_DP Application Test,

- Starting from Application Test Library

This test approach starts measurements by using an Application Test Library which starts from the default setup parameters and you have to customize the measurement parameters depending on your requirements.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-8.

Step 1. Click the Application Test tab.

Step 2. Check the PO_MOS_smpl category.

Step 3,4. Select Id-Vgs_DP (Click the Id-Vgs_DP then click Select 

)

Step 5. Set the test parameters shown in figure 3-8 to an appropriate one depending on your B1505A configuration and your test device.
The important check points are;
a. Gate SMU setup
b. Set Vg sweep parameters
c. Drain SMU setup
d. Set Vd test condition

Step 6. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

Step 7. The graph window pops up and the measurement starts.

Step 8. You can see the Id-Vgs curve and gfs (Y2 axis) graph in figure 3-9.

Figure 3-9 plots drain current Iv in Y1 axis and gfs in Y2 axis versus gate voltage Vgs in X axis. Marker is automatically located to the maximum gfs point and a tangent line is drawn on Y1 axis. The X coordinate of the cross point of the line is defined as the Vth. Maximum gfs and Vth appears on Parameter display as shown in marked by circles on the figure.

Review:

Though the measurement is limited to 20 A, the curve agrees to the data-sheet information. The gfs data may not be accurate because the Vg step is relatively large compared to the steep rise up of Id-Vg curve. Smaller Vg step voltage and 40A configuration may result in different gfs results.

A`. Measurement Procedure: Id-Vgs_DP Application Test,

- Starting from pre-defined test setup of My favorite Setup

This test approach starts measurements by using a pre-defined test setup saved in My favorite Setup instead of starting from a scratch by using an Application Test Library.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1`. Starting from Application Test Library" side of figure 3-8.

Step 1`. Click the Preset group of My Favorite Setup.

Step 2`. Select Example_AT preset group.

Step 3`. Select Id-Vgs_DP (Click the Id-Vgs_DP)

Step 4`. Click "Recall" button.

Next step: Go to step 5 of "Starting from Application Test Library" above, and continue by following the test step numbers.

B. Measurement Procedure: ID-VGS_DPC Classic Test

Refer to figure 3-10 for the following Step 1 to Step 16.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_CT preset group.

Step 3. Select ID-VGS_DPC (ID-VGS Dual Pulse).

Step 4. Press Recall button.

Step 5. Pre-defined example ID-VGS_DPC classic test setup – Channel Definition page opens.

Channel Definition page setups the SMUs and its measurement function.

Step 6. Set Unit field appropriately depending on your B1505A and connection setups.

The connection between the SMU definitions and the power MOS_FET pins must be matched to each other.

Step 7. Press Measurement Setup tab.

You can change measurement parameters in this page.

Step 8. VAR1 or primary sweep parameters: VGS can be set.

Step 9. VDS constant voltage can be set.

Step 10. Hold and Delay time can be set.

Step 11. Pressing “Pulse" button opens "Pulse Setup" sub-window.

Step 12. Integration time in pulsed measurement can be set. Make sure the integration time is less than 1 ms considering the maximum pulse width for

HCSMU is 1 ms. We require more than 50 us typical until the pulse is settled in higher current region, say more than 10 or 20 A, the integration time are to be less than pulse width - 50 us.

Step 13. Pulse width can be set. Since the minimum pulse width of HPSMU is 500 us and the maximum pulse width of HCSMU is 1 ms in 20A range, the possible range for pulse width id between 500 us to 1ms for HPSMU. HCSMU can be set less than 500 us, and it is effective for reducing the power dissipation of the power MOS-FET. Note that the minimum pulse width for the HCSMU is 50 us that is explained in step 12 plus the integration time. Refer to the appendix section if you want to know more about the pulsed measurements.

Step 14. Press Display Setup tab.

You can set the X-Y Graph, List Display and the Parameters of the measurement results in this page.

Step 15. The X, Y1, Y2 and so on to maximum Y8 axis can be defined as X-Y graph display.
Log or Linear scale and the Min. and the Max. scale parameters are set.

Step 16. List Display sets the measurement parameters that are shown in the List area of Display Graph window.

Step 17. Parameters field set the display of extracted parameters.
In the example setup, gfsMax and Vth are defined in the Auto Analysis and Function Setup tabs.

Step 18. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.

Start the measurement. (Click the Single button )

Step 19. The graph window pops up and the measurement starts.

Step 20. You can see the Id-Vgs curve and gfs (Y2 axis) graph that is the same as figure 3-9.

Note: Step 19 and 20 are the same as the step 7 and 8 of figure 3-9.

Tips:

As we see, Classic Test requires more setup steps compared to the Application Test, but Classic Test has more freedom in changing the test setups such as the measurement functions, measurement parameters and display parameters and format by the expense of a little bit complicated setup steps and no fancy user interface GUI.

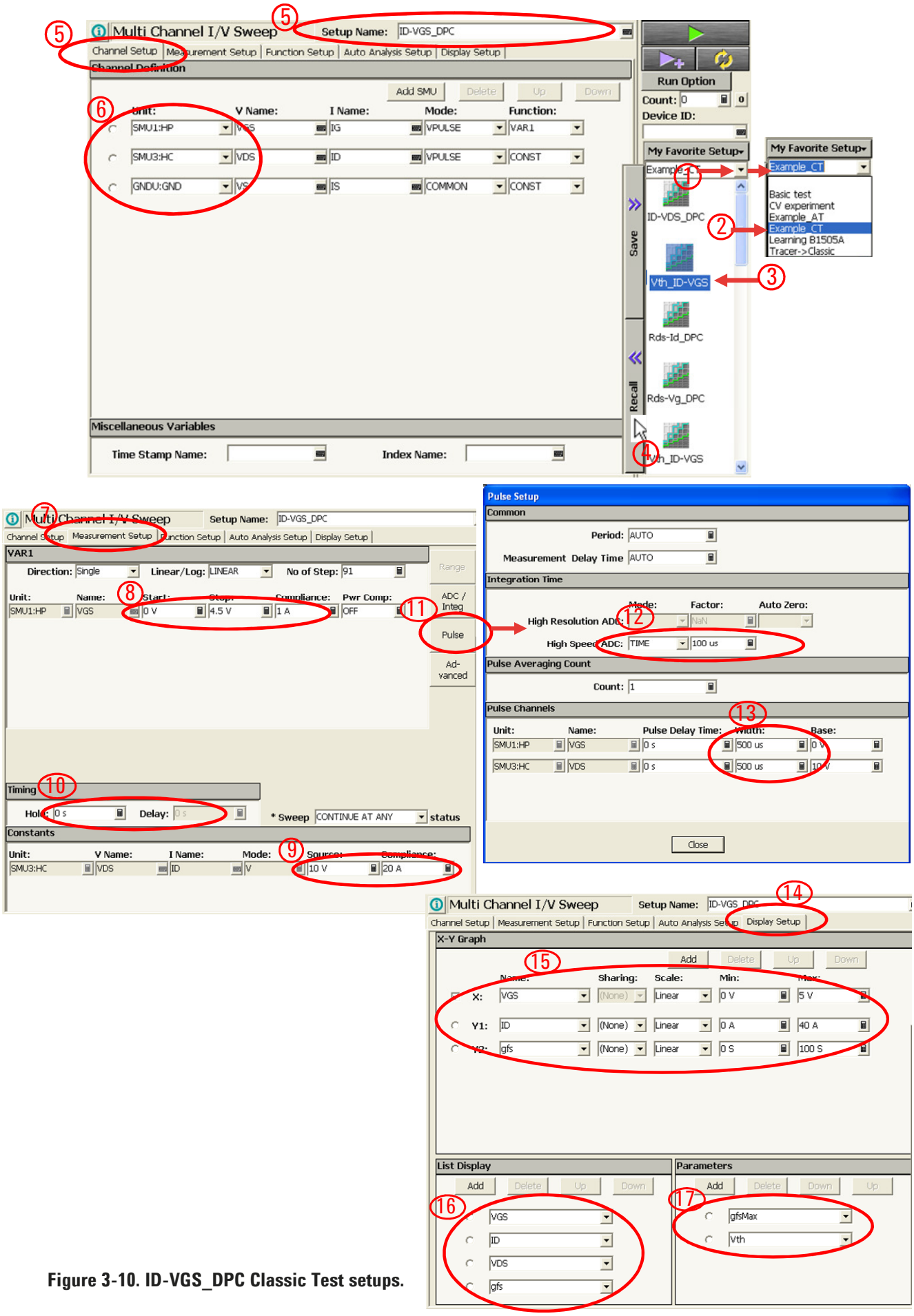


Figure 3-10. ID-VGS_DPC Classic Test setups.

3-1-2 Vth, Vgs(off) Gate threshold Voltage or Cutoff Voltage measurement

Measurement Parameters: Vth, Vgs(off) Gate threshold or Cutoff Voltage

Application Test name: Vth, Vgs(off) Figure 3-11

Application Test setup name (My Favorite Setup -> Example_AT):
Vth Vgs(off) - Vth, Vth Vgs(off) - Vgsoff

Classic Test setup name (My Favorite Setup -> Example_CT):
Vth_ID-VGS, Vgsoff_ID-VGS

Device used in the example: IRFP2907

Application description:

VGS(th), VGS(off) Application Test measures Vth or Vg(off) gate voltage at specified drain current (Id@Vth_Vgsoff). DC (not a pulse) is used in the test for supporting wide dynamic range of the drain current measurement by using an auto-ranging mode.

This Application Test supports two measurement modes by "Vth" and "Vgsoff" in the MeasMode parameter as shown in figure 3-11.

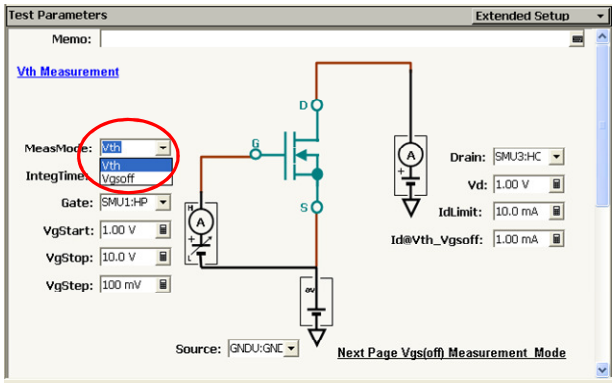


Figure 3-11. "Vth Vgs(off)" Application Test GUI.

Vth measurement method sweeps the gate voltage while the drain voltage is set as a constant voltage and extracts the gate voltage at the specified drain current..

Vgsoff measurement method sweeps the gate and the drain with the same synchronized voltage (Refer to figure 3-12) and extracts the gate voltage at the specified drain current.

Vth method seems the de-facto standard measurement method, but Vgsoff method is used in the traditional curve tracer application because the traditional analog curve tracer does not have an independent sweep source to the gate and the gate voltage sweep is substituted by connecting the gate and the drain together.

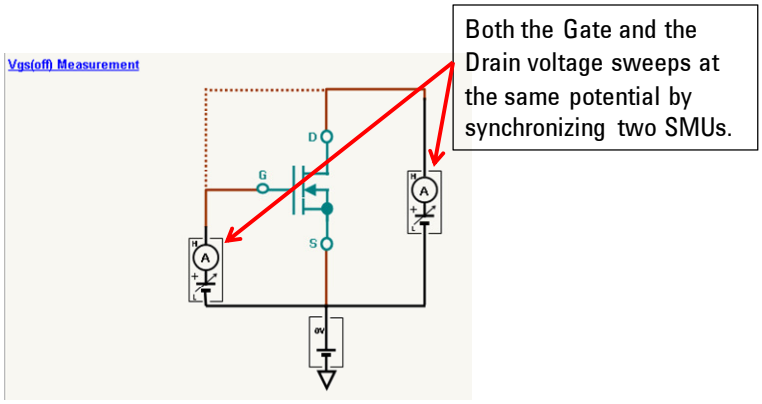


Figure 3-12. "Vgs(off)" Application Test measurement: Emulating the traditional curve tracer measurements.

A. Measurement Procedure: Vth Application Test,

-Starting from Application Test Library

This test approach starts measurements by using an Application Test Library which starts from the default setup parameters and you have to customize the measurement parameters depending on your requirements.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-13

Step 1. Click the Application Test tab.

Step 2. Check the PowerMOSFET category.

Step 3,4. Select Vth, Vgs(off) (Click the Vth, Vgs(off) then click Select 

)

Step 5. Set the test parameters shown in figure 3-13 to an appropriate one depending on your B1505A configuration and your test device.

The important check points are;
a. MeasMode = Vth
b. Gate SMU setup
c. Vg sweep parameters

Note: By narrowing the gate sweep voltage span, you can measure the Id-Vgs measurement faster. Checking the data sheet specification is a good practice. Since the drain current is limited by IdLimit parameter, you can just use wider gate sweep span without any worry for adding extra stress to the power MOS-FET in general case.

d. Drain SMU setup
e. Vg extraction conditions

Id@Vth_Vgoff is a set parameter for automatically extracting the Vth value and especially important.

Step 6. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.

Start the measurement. (Click the Single button )

Step 7. The graph window pops up and the measurement starts.

Step 8. You can see the Id-Vgs curve and gfs (Y2 axis) graph as shown in figure 3-14.

Figure 3-14 plots drain current Idrain in Y1 linear axis and Y2 log axis versus gate voltage Vgs in X axis. Marker is automatically located to the specified Id @Vth_Vgsoff point. The Vth parameter appears in the Parameter Display field as shown in the figure.

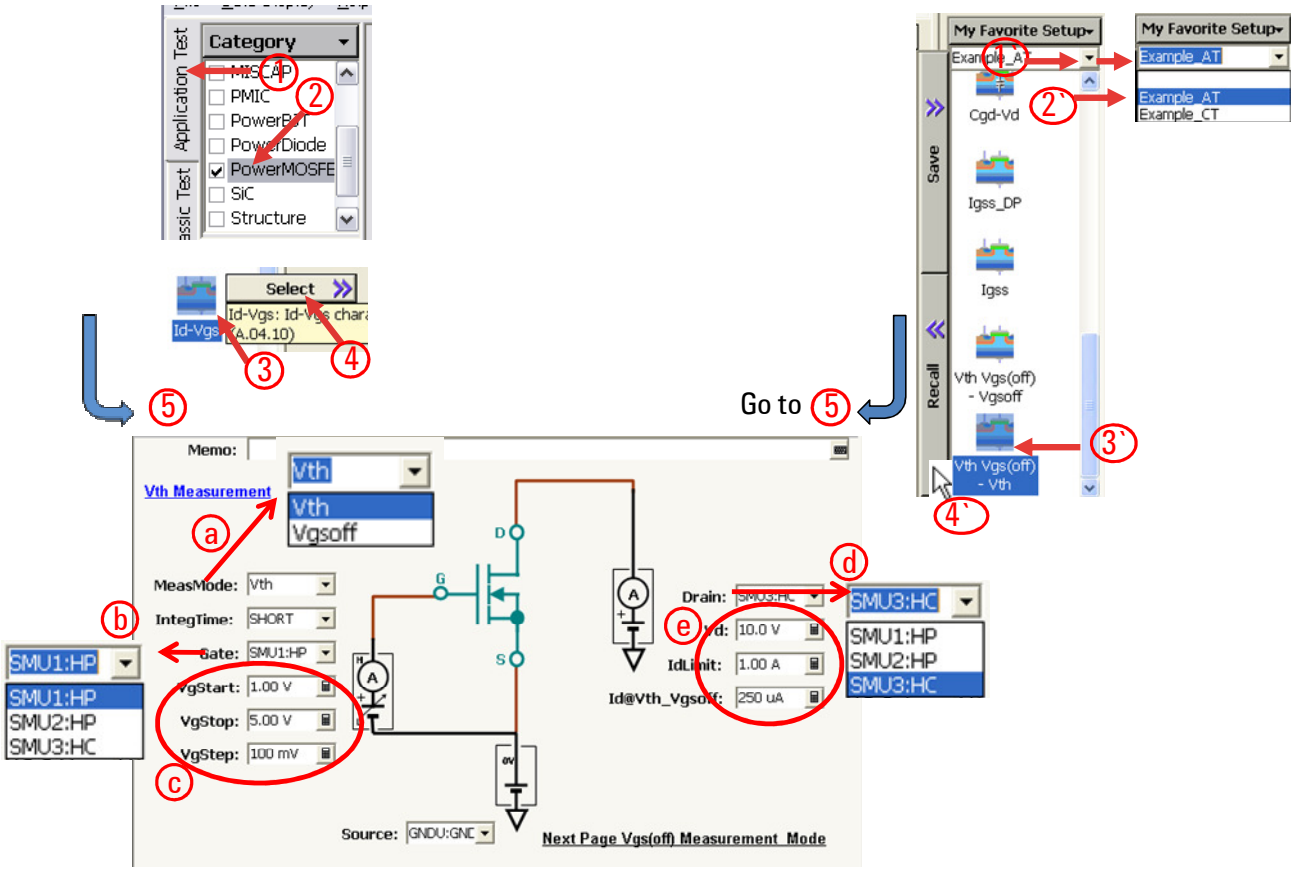


Figure 3-13. Vth test setup of "Vth, Vgs(off)" Application Test.

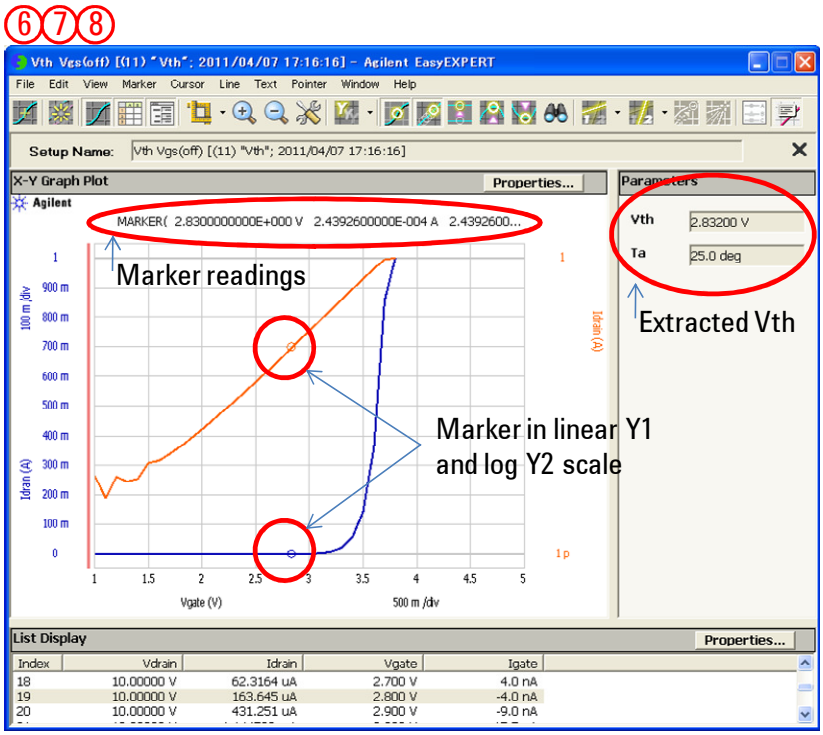


Figure 3-14. Vth test data example

Review:
The Vth specification of IRFP2907 used in the example is 2 - 4 V @Id=250 μA. The extracted Vth of the example shows 2.83 V, and it is a good agreement.
DC measurement is essential for measuring a lower current in wide dynamic range of Id characteristics as well as using a log Id scale for monitoring low current characteristics as shown in the measurement.

A`. Measurement Procedure: Vth Application Test,

- **Starting from pre-defined test setup of My favorite Setup**

This test approach starts measurements by using a pre-defined test setup saved in My favorite Setup instead of starting from a scratch by using an Application Test Library.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1`. Starting from Application Test Library" side of figure 3-13.

Step 1`. Click the Preset group of My Favorite Setup.

Step 2`. Select Example_AT preset group.

Step 3`. Select " Vth Vgs(off) - Vth" (Click the Vth Vgs(off) - Vth)

Step 4`. Click "Recall" button.

Then go to step 5 of "Starting from Application Test Library" above, and continue by following the test step numbers.

B. Measurement Procedure: Vth_ID-VGS Classic Test

Refer to figure 3-15 for the following Step 1 to Step 16.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_CT preset group.

Step 3. Select Vth_ID-VGS.

Step 4. Press Recall button.

Step 5. Pre-defined example Vth_ID-VGS classic test setup – Channel Definition page opens.

Channel Definition page setups the SMUs and its measurement function.

Step 6. Set Unit field appropriately depending on your B1505A and connection setups.

The connection between the SMU definitions and the power MOS_FET pins must be matched to each other.

Step 7. Press Measurement Setup tab.

You can change measurement parameters in this page.

Step 8. VAR1 or primary sweep parameters: Vgs can be set.

Step 9. Vds constant voltage can be set.

Step 10. Hold and Delay time can be set.

Step 11. Pressing “ADC/Integ" button opens "A/D Converter & Integration Time Setup" sub-window.

Step 12. Integration time can be set.

Step 13. Press Display Setup tab.

You can set the X-Y Graph, List Display and the Parameters of the measurement results in this page.

Step 14. The X, Y1, Y2 and so on to maximum Y8 axis can be defined as X-Y graph display.
Log or Linear scale and the Min. and the Max. scale parameters are set.

Step 15. List Display sets the measurement parameters that are shown in the List area of Display Graph window.

Step 16. Parameters field set the display of extracted parameters.
In this example classic test setup, Vth parameter is defined in Auto Analysis and Function Setup tabs.

Step 17. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

Step 18. The graph window pops up and the measurement starts.

Step 19. You can see the Vth (Id-Vg) graph in figure 3-16.

Note:

Id definition for extracting Vth parameter is made in Auto Analysis Setup page by specifying the automatic marker position as shown in figure 3-17.

The result is the same as the Application Test result.

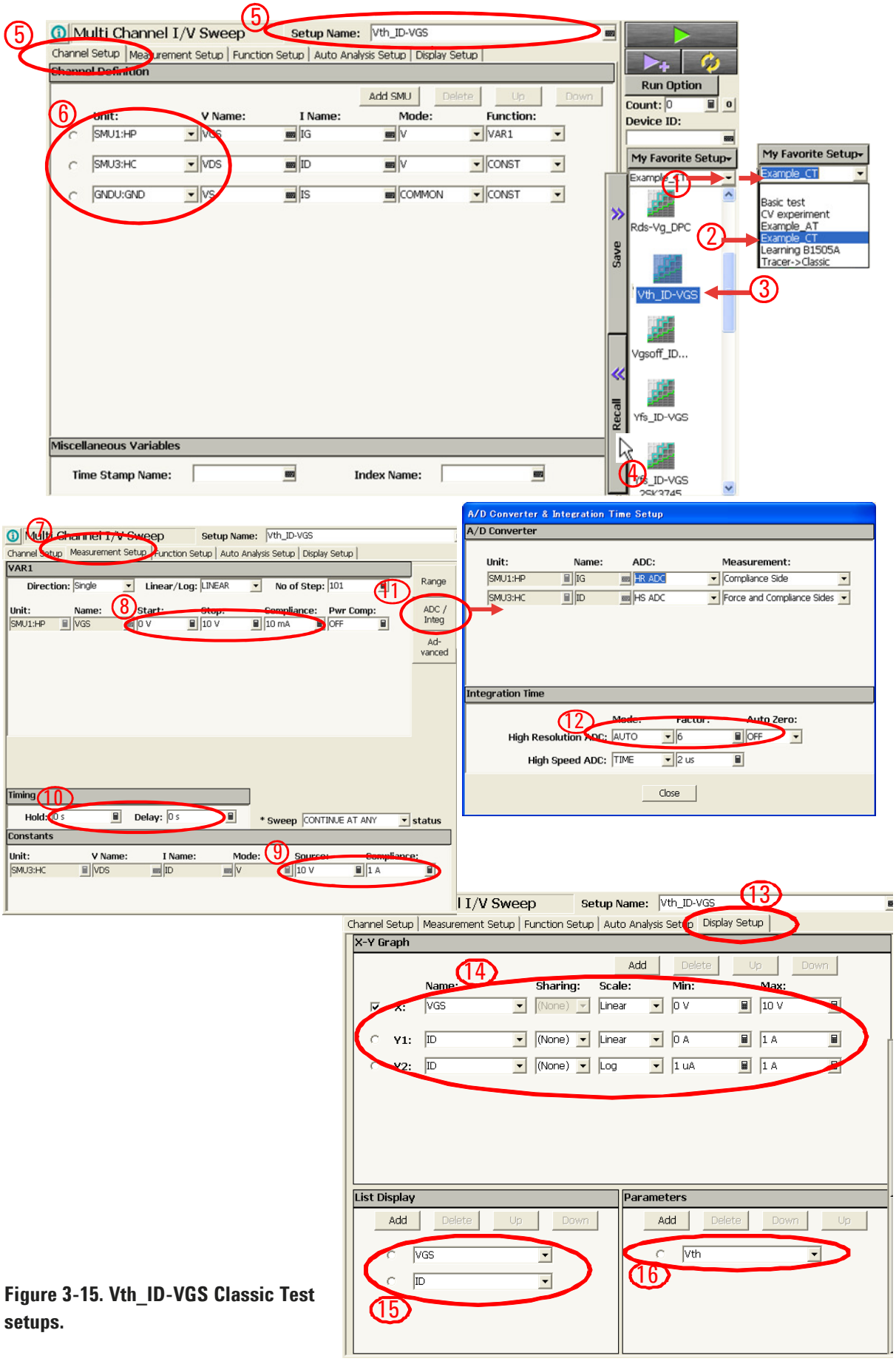


Figure 3-15. Vth_ID-VGS Classic Test setups.

18 19

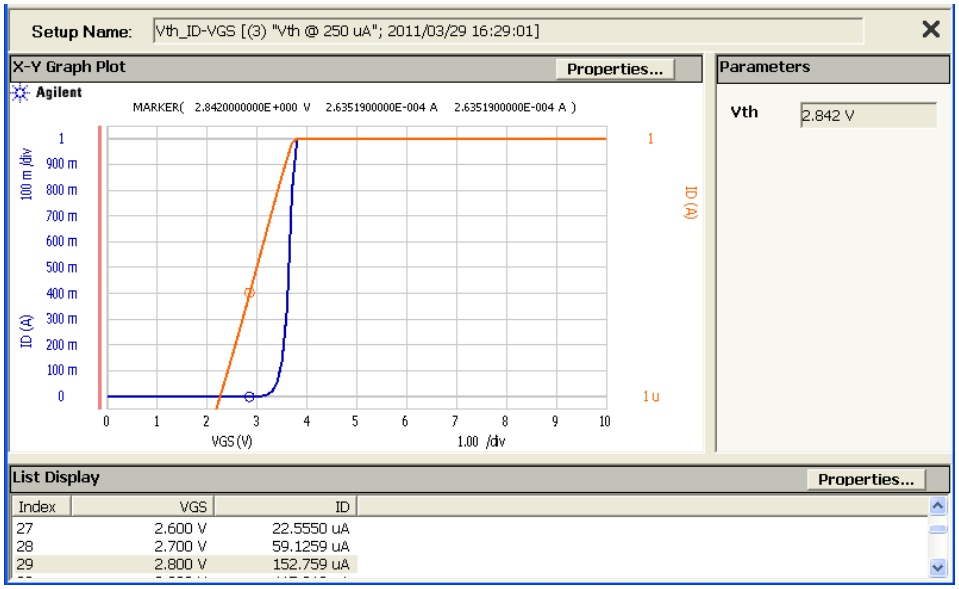
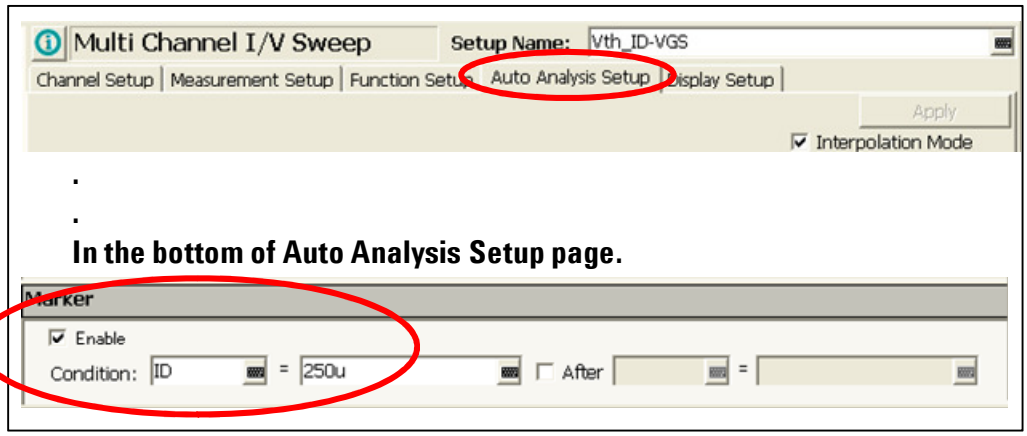


Figure 3-16. Vth_ID-VDS Classic Test data example.



.

.

In the bottom of Auto Analysis Setup page.

Figure 3-17. Marker position defining in Auto Analysis Setup.

C. Measurement Procedure: Vgsoff_ID-VGS

There are three ways as described for Vth parameter measurements for starting from the Application Test Library, Application Test definition of My favorite Setup and Classic Test definition of My Favorite Setup.

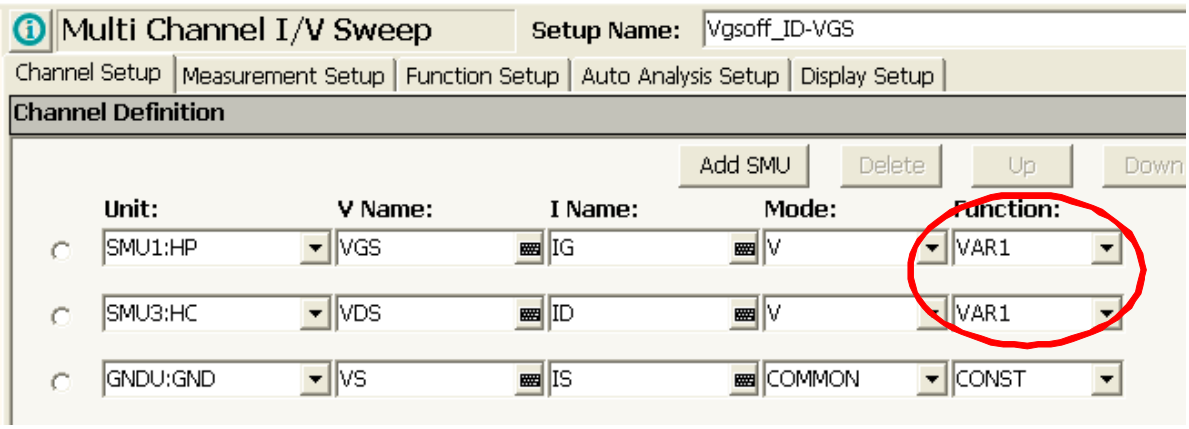
The Application Test is basically the same except selecting "Vgsoff" in the "MeasMode" parameter.

The Classic Test setup is basically the same as previous Vth_ID-VGS Classic Test definition except that this test sweeps the drain as shown in figure 3-18 (A). The sweep parameter for drain and the gate is the same as shown in Figure 3-18 (B).

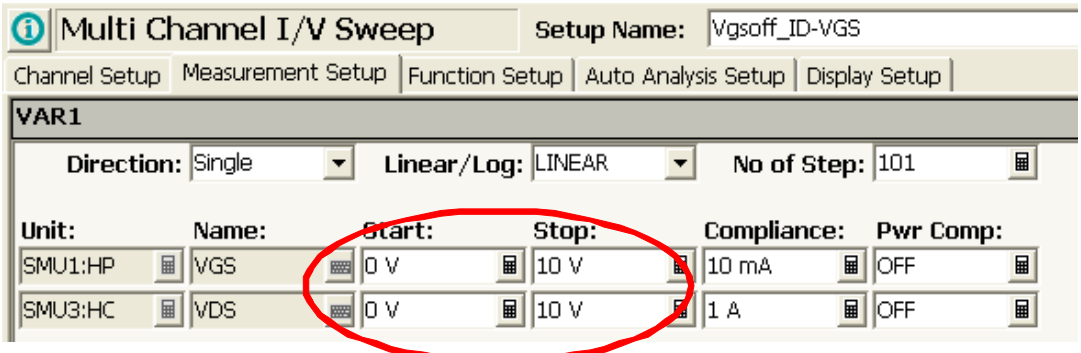
The other steps for using this Classic Test setup are the same as previous section B.

Review:

There is a example data in the Result area for Vgsoff_ID-VGS classic test, but the result is the same as Vth test. This is because the drain characteristic is very similar in both cases above Vth in the drain voltage due to the very flat Id-Vd characteristics of IRFP2907 power MOS-FET.



(A) Vgoff-ID-GGS Classic Test sweeps both Vgs and Vds as VAR1.



(B) The Gate and the Dran set the same start and stop sweep voltage in Vgoff-ID-GGS Classic Test.

Figure 3-18. Difference of Vgoff-ID-VGS and Vth_ID-VGS Classic Test.

3-1-3 RDS(on) Static Drain-to-Source On-State Resistance measurement

Measurement Parameters: RDS(on), Rds-Id or Rds-Vg
Static Drain-to-Source On-State Resistance

Application Test name: Rds-Id_DP, Rds-Vgs_DP

Application Test setup name (My Favorite Setup -> Example_AT):
Rds-Id_DP, Rds-Vgs_DP

Classic Test setup name (My Favorite Setup -> Example_CT):
Rds-Id_DPC, Rds-Vg_DPC

Device used in the example: IRFP2907

Application description:

Measures Drain current vs. Gate voltage characteristics and extracts Rds-Id or Rds-Vgs characteristics. SMU pulse is used for both the Drain-Source current and the Gate-Source voltage output.

A. Measurement Procedure: Rds-Vg_DP Application Test

-Starting from Application Test Library

This test approach starts measurements by using an Application Test Library which starts from the default setup parameters and you have to customize the measurement parameters depending on your requirements.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-19.

Step 1. Click the Application Test tab.

Step 2. Check the PO_MOS_smpl category.

Step 3,4. Select Rds-Vgs_DP (Click the Rds-Vgs_DP then click Select 

)

Step 5. Set the test parameters shown in figure 3-19 to an appropriate one depending on your B1505A configuration and your test device.

The important check points are;
a. Gate SMU setup
b. Set Vg sweep parameters
c. Drain SMU setup
d. Set Id and Vd test condition:

Id can be step as a secondary sweep, but the example set one bias current, 10 A. Maximum drain voltage is set to 2 V.
e. Linear or Log Rds display scale in the output graph can be select. The min. and max. Rds plot scale can be set in the Device Parameters field.

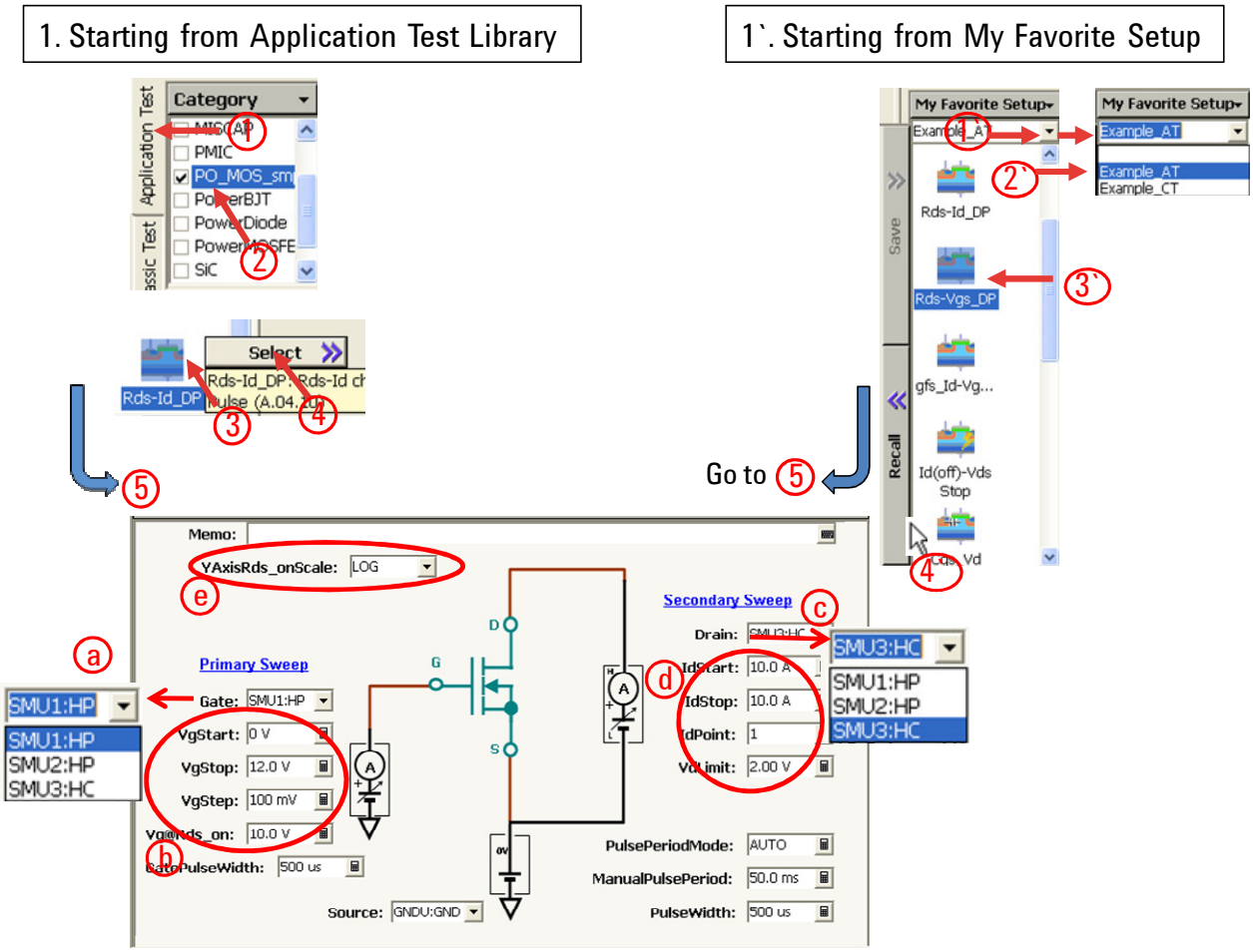


Figure 3-19. Rds-Vgs_DP Application Test setup.

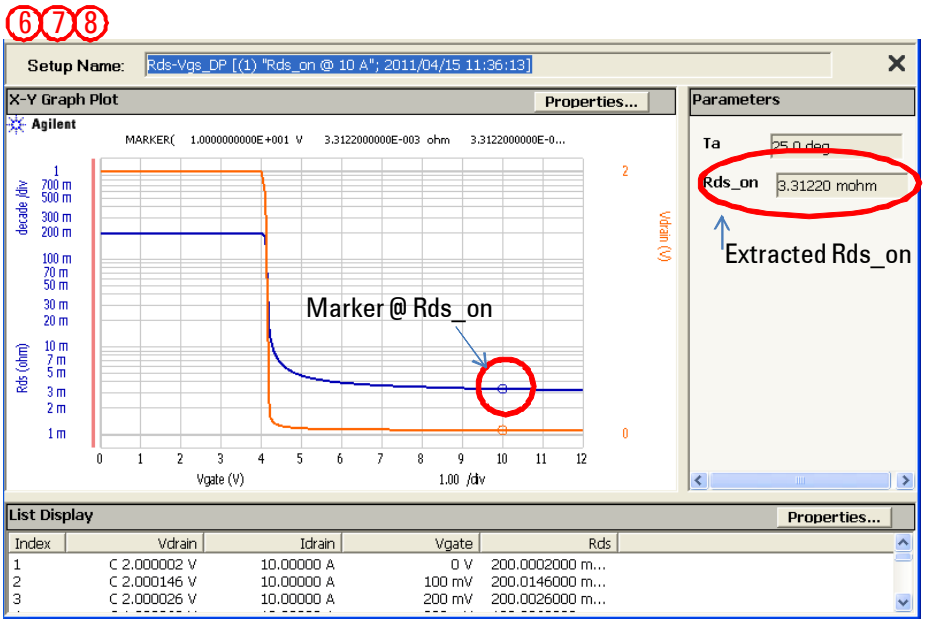


Figure 3-20. Rds-Vgs_DP test results.

Step 6. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.

Start the measurement. (Click the Single button )

Step 7. The graph window pops up and the measurement starts.

Step 8. You can see the Rds-Vgs_DP graph in figure 3-20.

> Figure 3-20 plots drain to source resistance Rds in log scale in Y1 axis and drain voltage in Y2 axis versus gate to source voltage in X axis. Marker is automatically located to the specified gate voltage Vg@Rds_on and automatically extracted Rds_on parameter is shown in the Parameters display field as shown in marked by circles on the figure.

Review:

Measured Rds on is about 3.3 mΩ at Id=20 A and Vg=10 V.
The specification of IRFP2907 is 3.6 mΩ at Id=125 A. Though the measurement condition of drain current is limited in B1505A (Id=20 A in the example), the measured Rds on value agrees to the data sheet specification.

It can be also noted that the measurement and data extraction is made just by one click of the measure button.

A`. Measurement Procedure: Rds-Vgs_DP Application Test,

- Starting from pre-defined test setup of My favorite Setup

This test approach starts measurements by using a pre-defined test setup saved in My favorite Setup instead of starting from a scratch by using an Application Test Library.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1`. Starting from Application Test Library" side of figure 3-19.

Step 1`.Click the Preset group of My Favorite Setup.

Step 2`. Select Example_AT preset group.

Step 3`.Select Rds-Vgs_DP (Click the Rds-Vgs_DP then click Select 

)

Then go to step 5 of "Starting from Application Test Library" above, and continue by following the test step numbers.

B. Measurement Procedure: Rds-Vg_DPC Classic Test

Refer to figure 3-21 for the following Step 1 to Step 16.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_CT preset group.

Step 3. Select Rds-Vg_DPC (Rds-Vg Dual Pulse).

Step 4. Press Recall button.

Step 5. Pre-defined example Rds-Vg_DPC classic test setup – Channel Definition page opens.

Channel Definition page setups the SMUs and its measurement function.

Step 6. Set Unit field appropriately depending on your B1505A and connection set-ups.

The connection between the SMU definitions and the power MOS_FET pins must be matched to each other.

Step 7. Press Measurement Setup tab.

You can change measurement parameters in this page.

Step 8. VAR1 or primary sweep parameters: Vg can be set.

Step 9. Vd constant voltage can be set.

Step 10. Hold and Delay time can be set.

Step 11. Pressing “Pulse" button opens "Pulse Setup" sub-window.

Step 12. Integration time in pulsed measurement can be set. Make sure the integration time is less than 1 ms considering the maximum pulse width for HCSMU is 1 ms. We require more than 50 us typical until the pulse is settled in higher current region, say more than 10 or 20 A, the integration time are to be less than pulse width - 50 us.

Step 13. Pulse width can be set. Since the minimum pulse width of HPSMU is 500 us and the maximum pulse width of HCSMU is 1 ms in 20A range, the possible range for pulse width id between 500 us to 1ms for HPSMU. HCSMU can be set less than 500 us, and it is effective for reducing the power dissipation of the power MOS-FET. Note that the minimum pulse width for the HCSMU is 50 us that is explained in step 12 plus the integration time. Refer to the appendix section if you want to know more about the pulsed measurements.

Step 14. Press Display Setup tab.

You can set the X-Y Graph, List Display and the Parameters of the measurement results in this page.

Step 15. The X, Y1, Y2 and so on to maximum Y8 axis can be defined as X-Y graph display.
Log or Linear scale and the Min. and the Max. scale parameters are set.

Step 16. List Display sets the measurement parameters that are shown in the List area of Display Graph window.

Step 17. Parameters field set the display of extracted parameters.
In the example setup, Rds_on is defined in the Auto Analysis and Function Setup tabs.

Step 18. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.

Start the measurement. (Click the Single button )

Step 19. The graph window pops up and the measurement starts.

Step 20. You can see the Id-Vgs curve and gfs (Y2 axis) graph that is the same as figure 3-20.

Note: Step 19 and 20 are the same as the step 7 and 8 of figure 3-20.

Tips:

As we see, Classic Test requires more setup steps compared to the Application Test, but Classic Test has more freedom in changing the test setups such as the measurement functions, measurement parameters and display parameters and format by the expense of a little bit complicated setup steps and no fancy user interface GUI.

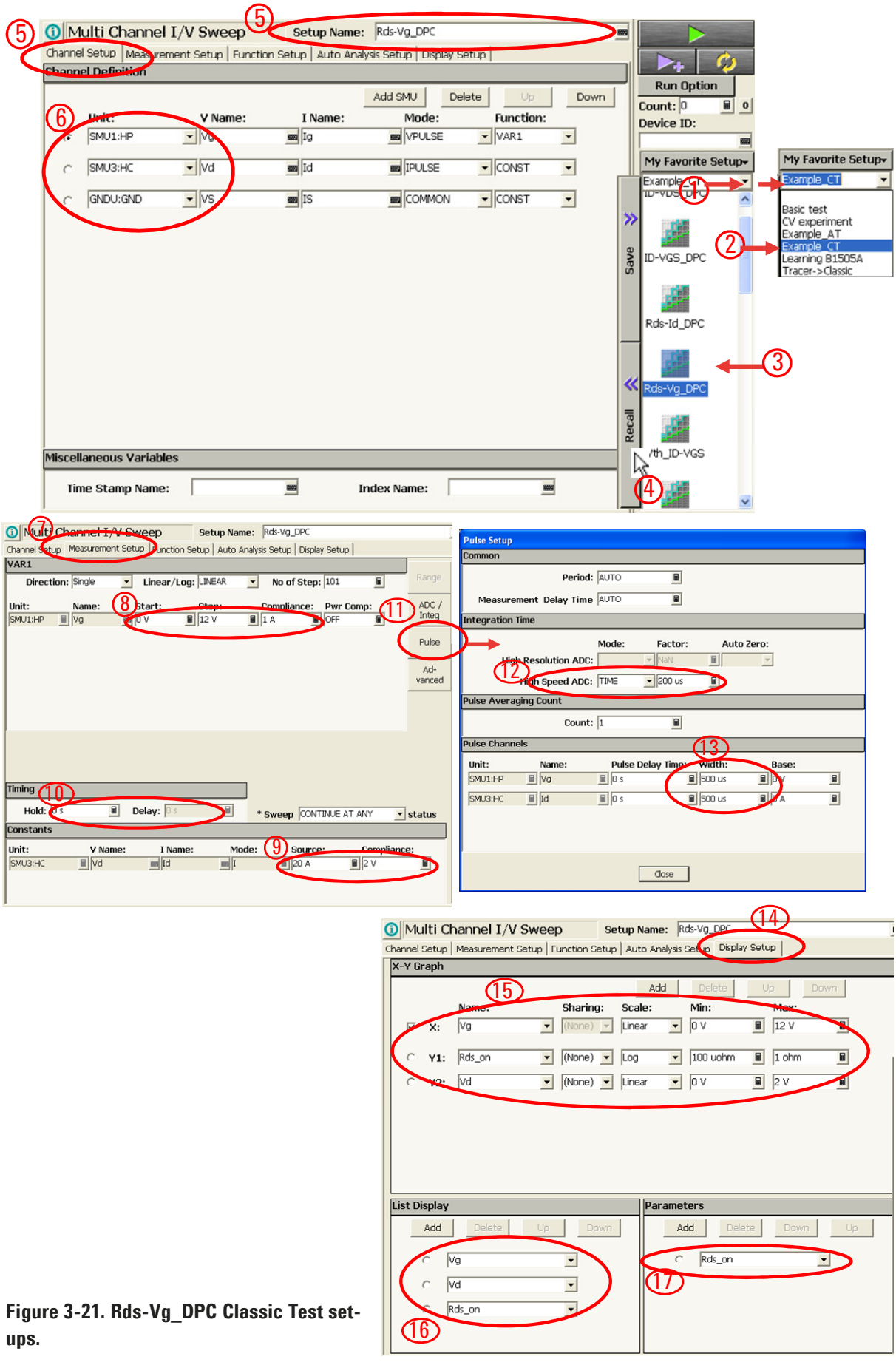


Figure 3-21. Rds-Vg_DPC Classic Test set-ups.

C. Measurement Procedure: Rds-Id_DP , Rds-Id_DPC

There are two ways for describing Rds, one is Rds versus Vgs (Rds-Vg) measurements as described and the other method is Rds versus Id (Rds-Id) measurements.

The difference between these two measurements are Rds-Vg measurement sweeps gate voltage Vg with constant drain current while Rds-Id measurement sweeps the drain current Id as a primary sweep and Vg is stepped for each Id sweep.

Figure 3-22 shows the user interface of Rds-Id_DP Application Test. The items with red circle indicate the main difference of these two measurement methods.

Scale parameter defines linear or log sweep. If log sweep is selected, the Rds X axis and the Id Y axis are both plotted in log scale.

Figure 3-23 shows an example of log scale output of Rds-Id_DP Application Test result.

The Classic Test definition Rds-Id_DPC measurement process is exactly the same as we experimented through Rds-Vg_DPC Classic Test measurements.

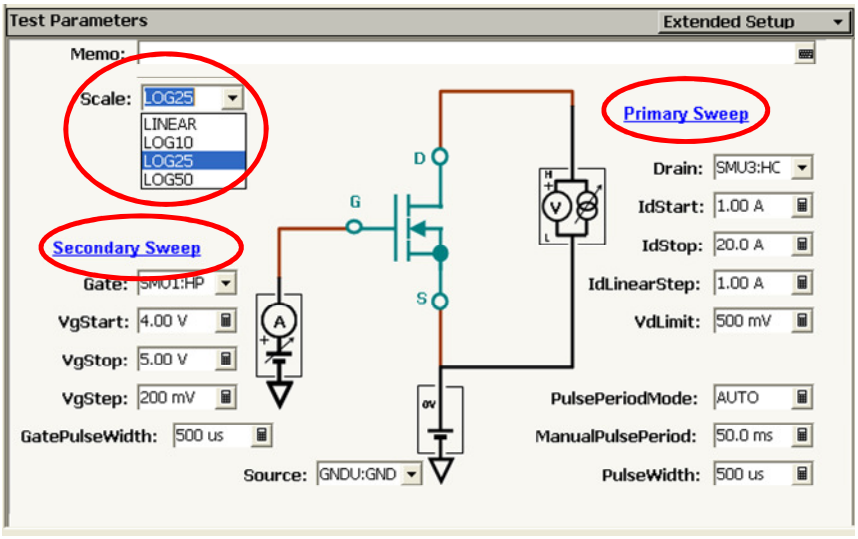


Figure 3-22. Difference of Rds-Id_DP Application setups.

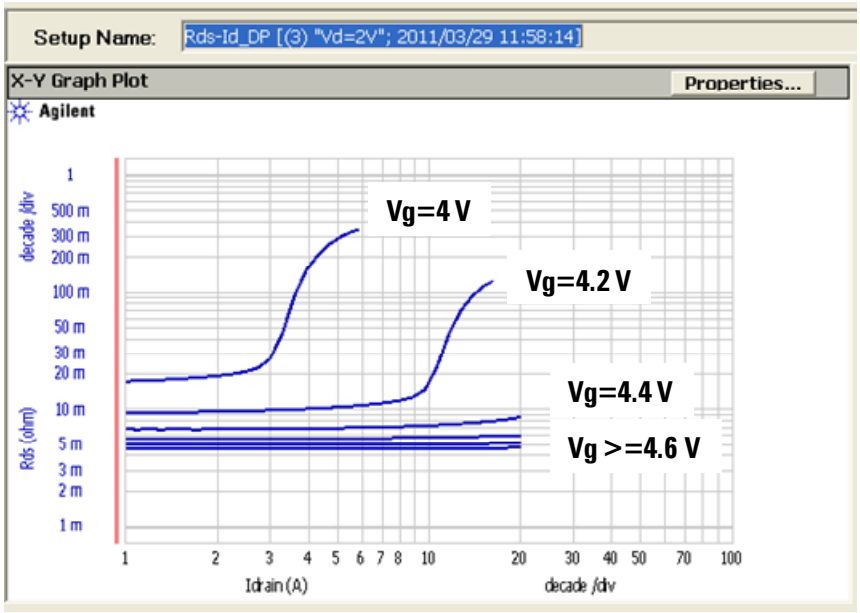


Figure 3-23. Log scale test example of Rds-Id_DP Application Test.

3-1-4 |yfs| , Gfs Forward Transfer Admittance, or Forward Trans conductance measurement

Measurement Parameters: |yfs| , Gfs Forward Transfer Admittance, or Forward Trans conductance

Application Test name: gfs_Id-Vgs_DP

Application Test setup name: (My Favorite Setup -> Example_AT): gfs_Id-Vgs_DP

Classic Test setup name: (My Favorite Setup -> Example_CT): Yfs_ID-VGS

Device used in the example: 2SK3745LS (Application Test), IRFP2907 (Classic Test)

Application description:

Measures Drain current vs. Gate voltage characteristics and extracts gfs - Idrain characteristics. SMU dual pulse is used for both the Drain-Source and the Gate-Source voltage output.

A. Measurement Procedure: gfs_Id-Vgs_DP Application Test

-Starting from Application Test Library

This test approach starts measurements by using an Application Test Library which starts from the default setup parameters and you have to customize the measurement parameters depending on your requirements.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-24.

Step 1. Click the Application Test tab.

Step 2. Check the PO_MOS_smpl category.

Step 3,4. Select gfs_Id-Vgs_DP (Click the gfs_Id-Vgs_DP then click Select 

)

Step 5. Set the test parameters shown in figure 3-24 to an appropriate one depending on your B1505A configuration and your test device.

The important check points are;
a. Gate SMU setup
b. Set Vg sweep parameters
c. Drain SMU setup
d. Set Vd test condition:

Vd can be step as a secondary sweep, but the example set one bias voltage, 10 V. Maximum drain current is set to 1 A.

e. Linear or Log gfs Y1 axis display scale in the output graph can be select. The min. and max. gfs plot scale can be set in the Device Parameters field.

Step 6. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.

Start the measurement. (Click the Single button )

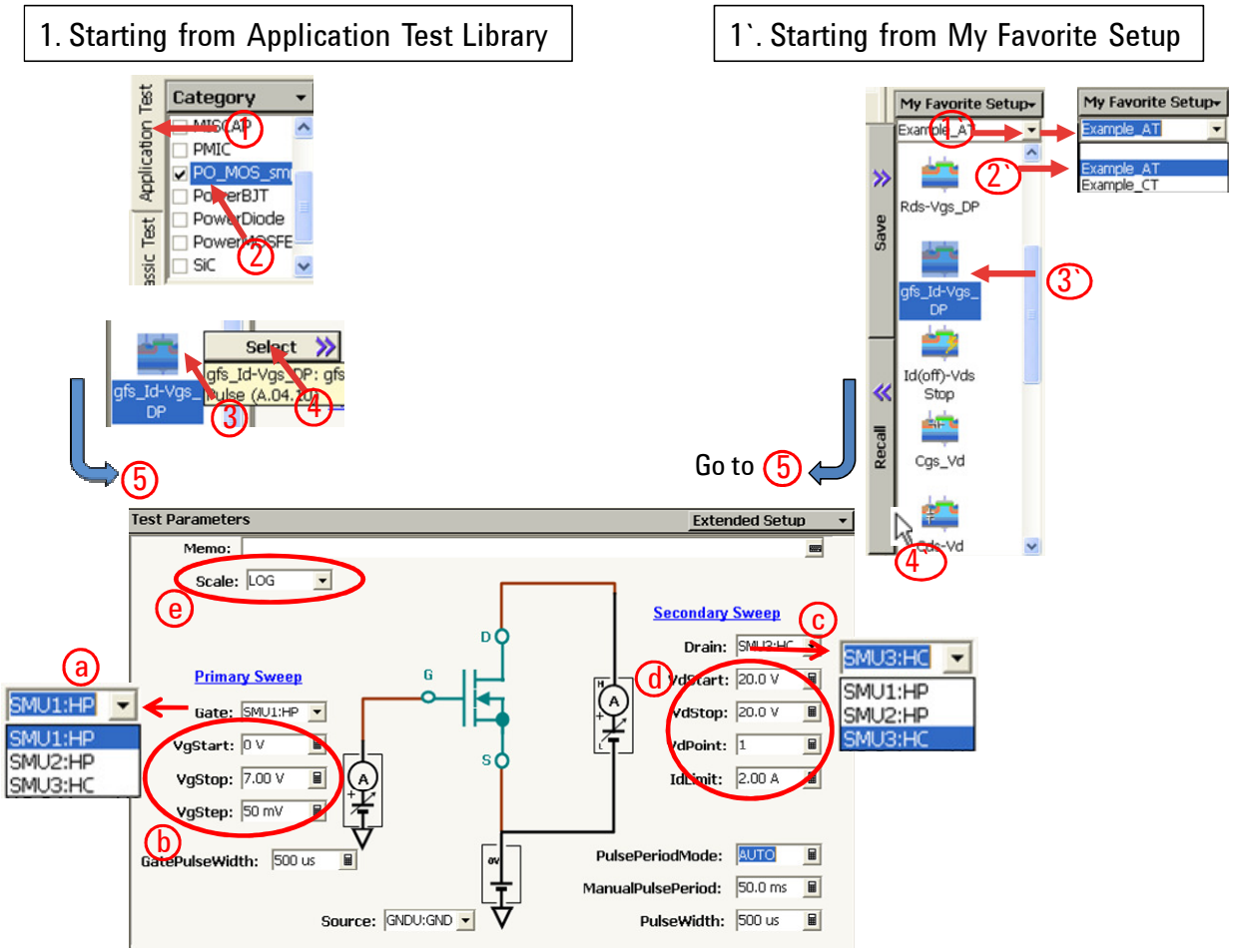


Figure 3-24. gfs_Id-Vgs_DP Application Test setup.

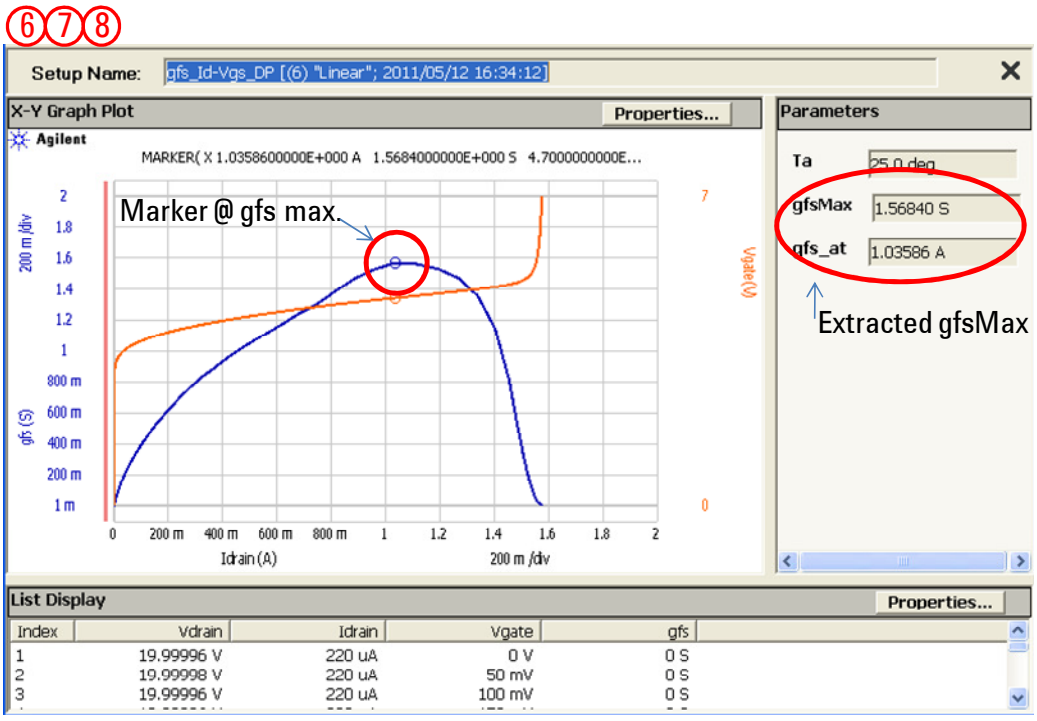


Figure 3-25. gfs_Id-Vgs_DP test results

Step 7. The graph window pops up and the measurement starts.

Step 8. You can see the gfs_Id-Vgs_DP graph in figure 3-25.

Figure 3-25 plots gfs forward transfer conductance of drain to source in log scale in Y1 axis and corresponding gate voltage in Y2 axis versus drain current in X axis. Marker is automatically located to the maximum gfs point as shown in marked by circles on the figure. Extracted gfs and its drain current are shown as gfsMax in the Parameters display field.

Review:

The measured gfs is maximum about 1.5 S around Id=1 A as automatically extracted and shown in Parameters field. The yfs (=gfs) specification of 2SK3745LS is 1.4 S typical at Vd=20 V and Id=1 A. The example gfs measured agrees to the specification data.

Y axis can select both for linear or log scale.

A`. Measurement Procedure: gfs_Id-Vgs_DP Application Test,

- Starting from pre-defined test setup of My favorite Setup

This test approach starts measurements by using a pre-defined test setup saved in My favorite Setup instead of starting from a scratch by using an Application Test Library.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1`. Starting from Application Test Library" side of figure 3-24.

Step 1`. Click the Preset group of My Favorite Setup.

Step 2`. Select Example_AT preset group.

Step 3`. Select R gfs_Id-Vgs_DP (Click the gfs_Id-Vgs_DP)

Step 4`. Click "Recall" button.

Then go to step 5 of "Starting from Application Test Library" above, and continue by following the test step numbers.

B. Measurement Procedure: Yfs_ID-VGS Classic Test

Refer to figure 3-26 for the following Step 1 to Step 16.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_CT preset group.

Step 3. Select Yfs_ID-VGS (Yfs_ID-VGS Dual Pulse).

Step 4. Press Recall button.

Step 5. Pre-defined example Yfs_ID-VGS classic test setup – Channel Definition page opens.

Channel Definition page setups the SMUs and its measurement function.

Step 6. Set Unit field appropriately depending on your B1505A and connection set-ups.

The connection between the SMU definitions and the power MOS_FET pins must be matched to each other.

Step 7. Press Measurement Setup tab.

You can change measurement parameters in this page.

Step 8. VAR1 or primary sweep parameters: VGS can be set.

Step 9. VDS constant voltage and current compliance can be set.

Note that the current range is fixed by the compliance range and the minimum resolution available in the test is limited. The dynamic range of HCSMU is six digits, and the minimum drain current resolution in the example setup is 20 μA.

Step 10. Hold and Delay time can be set.

Step 11. Pressing “Pulse" button opens "Pulse Setup" sub-window.

Step 12. Integration time in pulsed measurement can be set. Make sure the integration time is less than 1 ms considering the maximum pulse width for HCSMU is 1 ms. We require more than 50 us typical until the pulse is settled in higher current region, say more than 10 or 20 A, the integration time are to be less than pulse width - 50 μs.

Step 13. Pulse width can be set. Since the minimum pulse width of HPSMU is 500 us and the maximum pulse width of HCSMU is 1 ms in 20 A range, the possible range for pulse width is between 500 us to 1ms for HPSMU. HCSMU can be set less than 500 us, and it is effective for reducing the power dissipation of the power MOS-FET.
Note that the minimum pulse width for the HCSMU is 50 us, which is explained in the step 12, plus the integration time. Refer to the appendix section if you want to know more about the pulsed measurements.

Step 14. Press Display Setup tab.

You can set the X-Y Graph, List Display and the Parameters of the measurement results in this page.

Step 15. The X, Y1, Y2 and so on to maximum Y8 axis can be defined as X-Y graph display.
Log or Linear scale and the Min. and the Max. scale parameters are set.

Step 16. List Display sets the measurement parameters that are shown in the List area of Display Graph window.

Step 17. Parameters field set the display of extracted parameters.
In the example setup, Yfs is defined in the Auto Analysis and Function Setup tabs.

Step 18. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.

Start the measurement. (Click the Single button )

Step 19. The graph window pops up and the measurement starts.

Step 20. You can see the yfs-ID curve and VGS (Y2 axis) graph in figure 3-27.
Marker is automatically positioned to the Id specified in the Marker function of Auto Analysis Setup, and the corresponding Yfs and the drain current is displayed on the Parameter field.

The marker position in the Auto Analysis can be set in the Marker field of Auto Analysis Setup tab as shown in figure 3-28.

Tips:

As we see, Classic Test requires more setup steps compared to the Application Test, but Classic Test has more freedom in changing the test setups such as the measurement functions, measurement parameters and display parameters and format by the expense of a little bit complicated setup steps and no fancy user interface GUI.

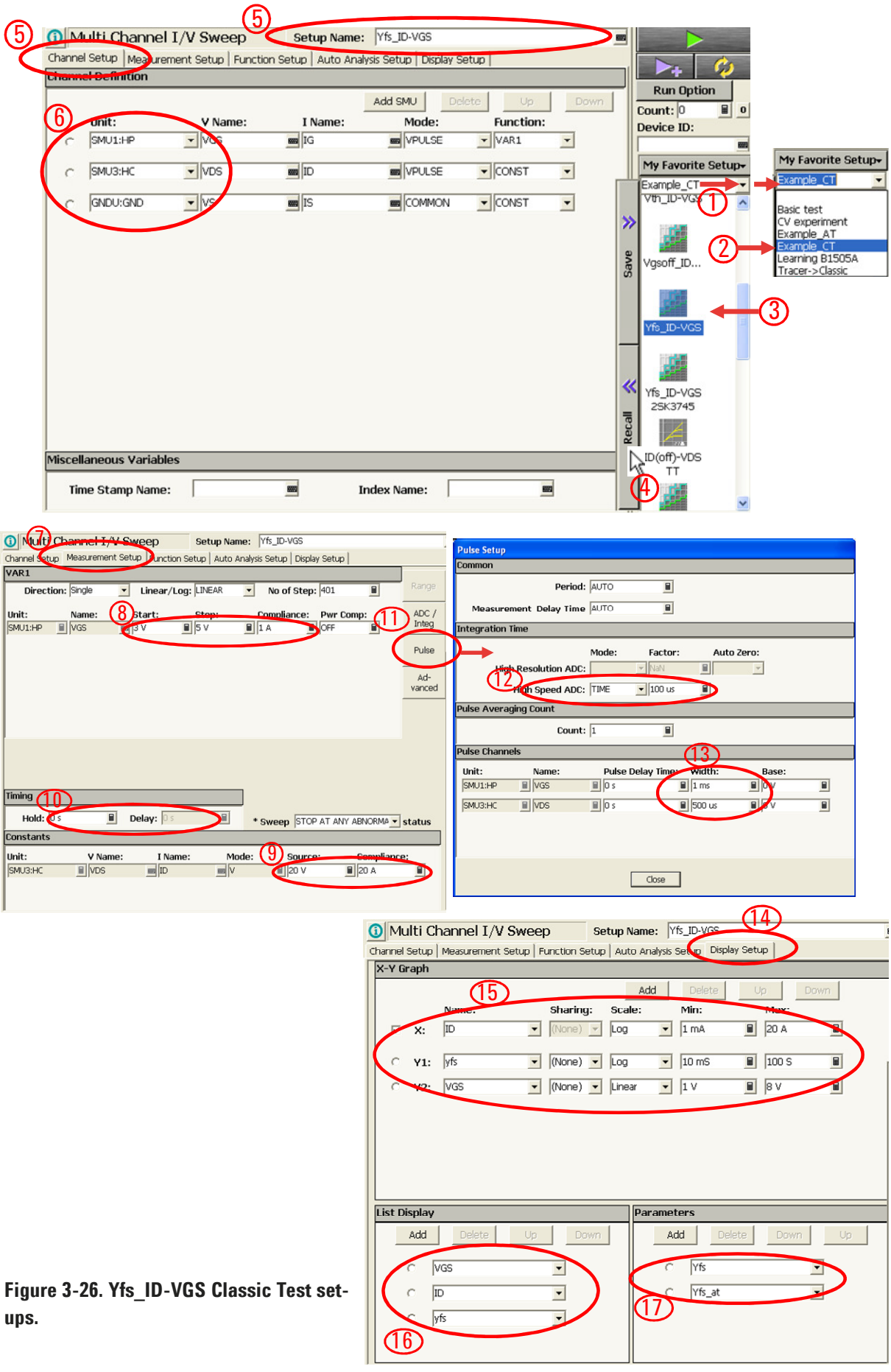


Figure 3-26. Yfs_ID-VGS Classic Test set-ups.

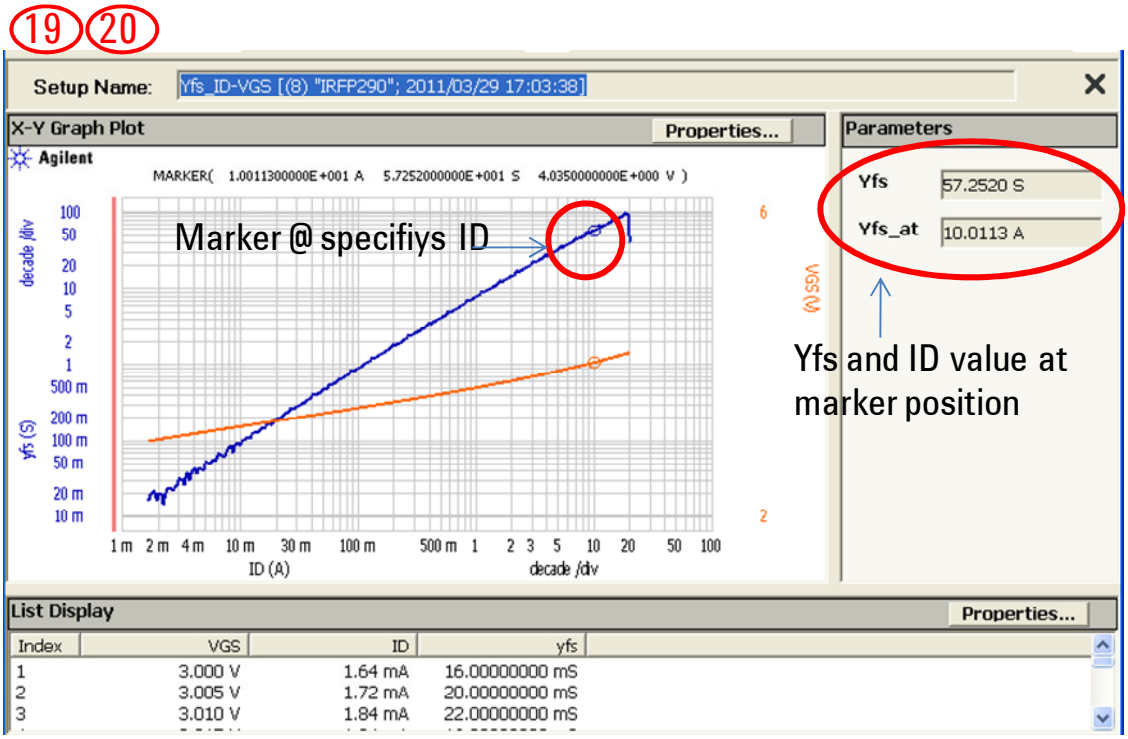


Figure 3-27. Yfs_ID-VGS Classic Test example for IRFP2907.

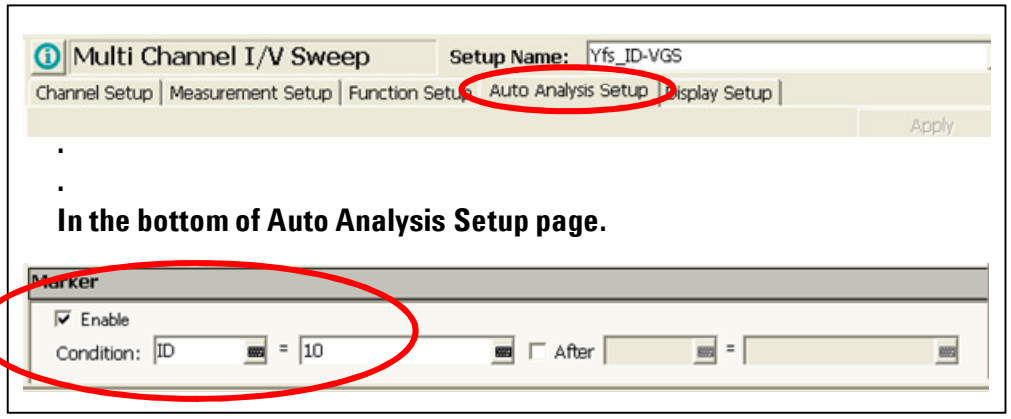


Figure 3-28. Marker position defining in Auto Analysis Setup.

3-1-5 IGSS Gate-to-Source Leakage Current measurement

Measurement Parameters: IGSS Gate-to-Source Leakage Current

Application Test name: Igss, Igss_DP (dual polarity)

Application Test setup name: (My Favorite Setup -> Example_AT): Igss, Igss_DP

Classic Test setup name: (My Favorite Setup -> Example_CT): Igss-CT

Device used in the example: 2SK3745LS

Application description:

Measures Gate current vs. Gate-Source voltage characteristics and extracts the Igss at specified gate voltage (Vg@Igss).

A. Measurement Procedure: Igss Application Test

Application description:

Measures Gate current vs Gate-Source voltage characteristics and extracts the Igss at specified gate voltage (Vg@Igss).
Two measurements are necessary for measuring both positive and negative gate leakage current.

-Starting from Application Test Library

This test approach starts measurements by using an Application Test Library which starts from the default setup parameters and you have to customize the measurement parameters depending on your requirements.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-29.

Step 1. Click the Application Test tab.

Step 2. Check the PO_MOS_smpl category.

Step 3,4. Select Igss (Click the Igss then click Select 

)

Step 5. Set the test parameters shown in figure 3-29 to an appropriate one depending on your B1505A configuration and your test device.

The important check points are;
a. Gate SMU setup
b. Set Vg sweep parameters

This test is acquiring gate current Igss at the specified gate voltage Vg@Idss, the start voltage can be set closer to the Vg@Idss for speeding the test.

c. Drain SMU setup
d. Set Vd test condition:
Vd voltage is typically zero volts.

e. Set the gate voltage to extract the Igss.
f. Changing Hold Time and Delay Time in Extended Setup would be effective if the gate start voltage is close to the Vg@Igss value.

Step 6. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.

Start the measurement. (Click the Single button )

Step 7. The graph window pops up and the measurement starts.

Step 8. You can see the Igss graph in figure 3-30.

Figure 3-30 plots Igss gate-to-source leakage current versus gate voltage. Marker is automatically located to the specified Vg@Igss point as shown in marked by circles on the figure. Extracted Igss and the gate voltage are shown in the Parameters display field.

Review:

Igss measures the gate leakage current and it is very low in MOS-FETs. The specification of 2SK3745LS is maximum 10 μA at Vgs=16V, Vds+0 V. The measured Igss is 26 nA which is much lower compared to the specification, but it is natural. We sweep the gate voltage with the initial 100 ms hold time for waiting the first measurement and then 20 ms delay time for each gate sweep step voltage (this value is set in Extended Setup). Please note that the leakage current measurement is affected by these wait time settings.

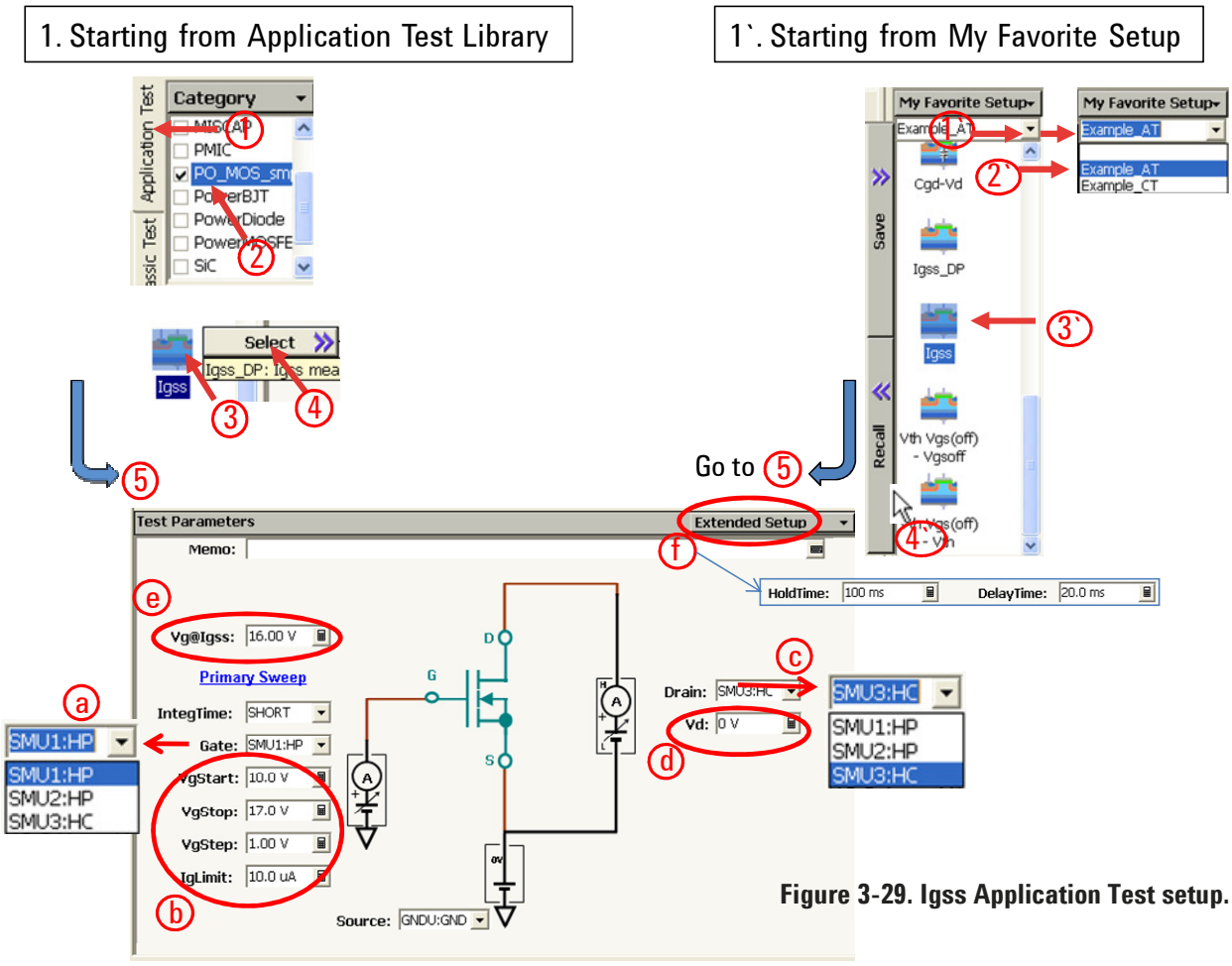


Figure 3-29. Igss Application Test setup.

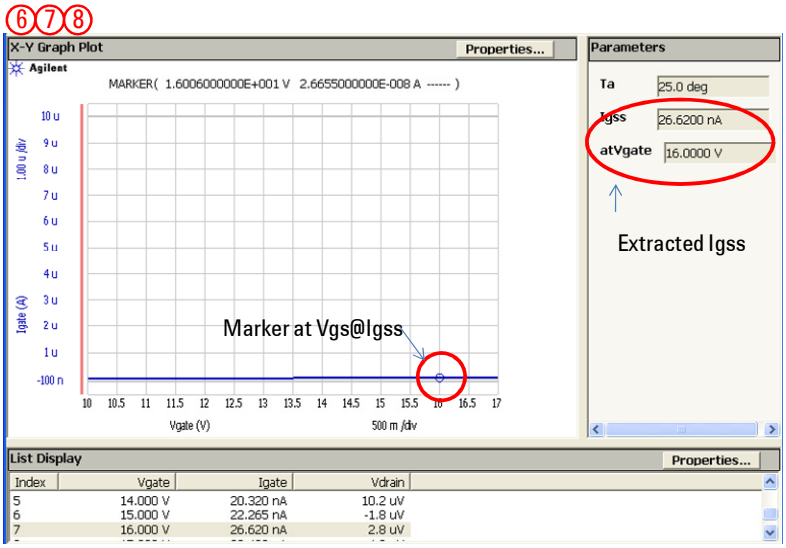


Figure 3-30. Example of Igss Application Test results.

A`. Measurement Procedure: Igss Application Test,

- Starting from pre-defined test setup of My favorite Setup

This test approach starts measurements by using a pre-defined test setup saved in My favorite Setup instead of starting from a scratch by using an Application Test Library.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1`. Starting from Application Test Library" side of figure 3-29.

Step 1`. Click the Preset group of My Favorite Setup.

Step 2`. Select Example_AT preset group.

Step 3`. Select Igss (Click the Igss)

Step 4`. Click "Recall" button.

Then go to step 5 of "Starting from Application Test Library" above, and continue by following the test step numbers.

B. Measurement Procedure: Igss_DP (Igss dual polarity) Application Test

Application description:

Measures Gate current vs. Gate-Source voltage characteristics and extracts the Igss at specified gate voltage (Vg@Igss). Second measurements are made by inverting the gate voltage and both polarity Igss parameters are extracted in the final List window.
This test does not require two independent measurements.

-Starting from Application Test Library

This test approach starts measurements by using an Application Test Library which starts from the default setup parameters and you have to customize the measurement parameters depending on your requirements.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-31.

Step 1. Click the Application Test tab.

Step 2. Check the PO_MOS_smpl category.

Step 3,4. Select Igss_DP (Click the Igss_DP then click Select 

)

Step 5. Set the test parameters shown in figure 3-24 to an appropriate one depending on your B1505A configuration and your test device.
The important check points are;
a. Gate SMU setup
b. Set Vg sweep parameters
This test is acquiring gate current Igss at the specified gate voltage Vg@Idss, the start voltage can be set closer to the Vg@Idss for speeding the test.

c. Drain SMU setup
d. Set Vd test condition:
Vd voltage is typically zero volts.
e. Set the gate voltage to extract the Igss.
f. Changing Hold Time and Delay Time in Extended Setup would be effective if the gate start voltage is close to the Vg@Igss value.

Step 6. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.

Start the measurement. (Click the Single button )

Step 7. The graph window pops up and the first measurement starts, and extracts the positive Igss.

Step 8. Second measurement for negative Vgs starts, and extracts the second Igss.

Step 9. Finally the extracted Igss for both polarity are displayed in the third windows as you can in figure 3-32.

Note that the measurement graph in figure 3-32 appears when the measurements are executed, but only the final result data is saved in Result field.

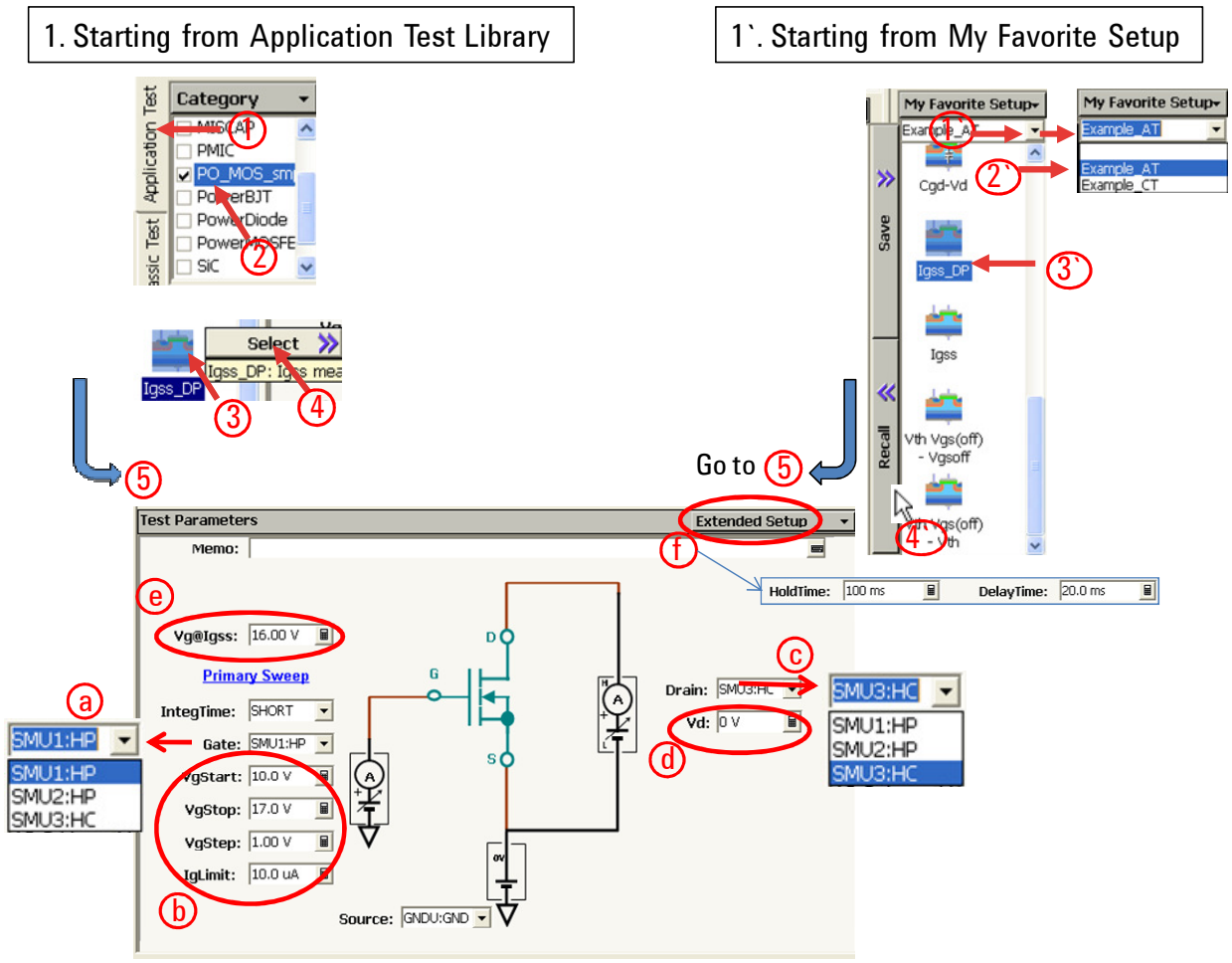


Figure 3-31. Igss_DP Application Test setup.

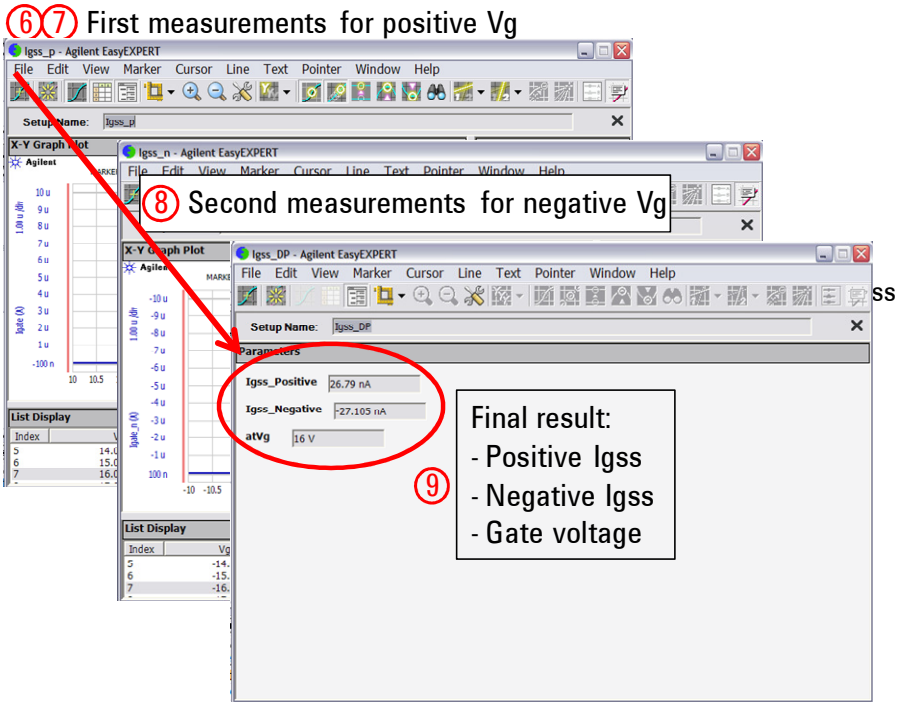


Figure 3-32. Example of Igss_DP Application Test results.

Review:

As previously noted, Igss is measuring gate leakage and it is specified for both plus and minus polarity. This Application Test executes plus and minus sweep sequentially and then extracts the leakage current at specified voltage. The measurement curve itself does not include much information, and therefore this test saves just the final value only. The Igss measured is almost the same in both polarity and the previous test.

If you need to save the graph, a good idea is using a Quick Test that runs two tests in one execution.

B`. Measurement Procedure: Igss_DP Application Test,

- Starting from pre-defined test setup of My favorite Setup

This test approach starts measurements by using a pre-defined test setup saved in My favorite Setup instead of starting from a scratch by using an Application Test Library.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1`. Starting from Application Test Library" side of figure 3-31.

Step 1`. Click the Preset group of My Favorite Setup.

Step 2`. Select Example_AT preset group.

Step 3`. Select Igss_DP (Click the Igss_DP)

Step 4`. Click "Recall" button.

Then go to step 5 of "Starting from Application Test Library" above, and continue by following the test step numbers.

C. Measurement Procedure: Igss-CT Classic Test

Refer to figure 3-33 for the following Step 1 to Step 18.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_CT preset group.

Step 3. Select Igss-CT (Igss Classic Test).

Step 4. Press Recall button.

Step 5. Pre-defined example Igss-CT classic test setup – Channel Definition page opens.

Channel Definition page setups the SMUs and its measurement function.

Step 6. Set Unit field appropriately depending on your B1505A and connection set-ups.

The connection between the SMU definitions and the power MOS_FET pins must be matched to each other.

Step 7. Press Measurement Setup tab.

You can change measurement parameters in this page.

Step 8. VAR1 or primary sweep parameters: Set Start, Stop and Step of Vgate sweep parameter.

Step 9. Vdrain constant voltage and current compliance can be set.

Step 10. Hold and Delay time can be set.

Step 11. Pressing “ADC/Integ" button opens "A/D Converter & Integration Time Setup" sub-window.

Step 12. Integration time can be set.

Step 13. Press Auto Analysis Setup tab.

Step 14. Set gate voltage where the gate leakage current is measured.

Step 15. Press Display Setup tab.

You can set the X-Y Graph, List Display and the Parameters of the measurement results in this page.

Step 16. The X, Y1, Y2 and so on to maximum Y8 axis can be defined as X-Y graph display.
Log or Linear scale and the Min. and the Max. scale parameters are set.

Step 17. List Display sets the measurement parameters that are shown in the List

area of Display Graph window.

Step 18. Parameters field set the display of extracted parameters.
In the example setup, Igss and the gate voltage defined in the Auto Analysis and Function Setup tabs are set.

Step 19. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

Step 20. The graph window pops up and the measurement starts.

Step 21. You can see the Igate versus Vgate curve in figure 3-34.
Marker is automatically positioned to the Id specified in the Marker function of Auto Analysis Setup, and the corresponding Yfs and the drain current is displayed on the Parameter field.

The marker position in the Auto Analysis can be set in the Marker field of Auto Analysis Setup tab as shown in figure 3-33 step 14.

The negative Igss has to be measured by changing the test setup for Vg sweep in Measurement Setup page and the Vgate marker value in Auto Analysis Setup page.

Tips:

You can use Quick Test for running both positive Igss and negative Igss measurement at once.

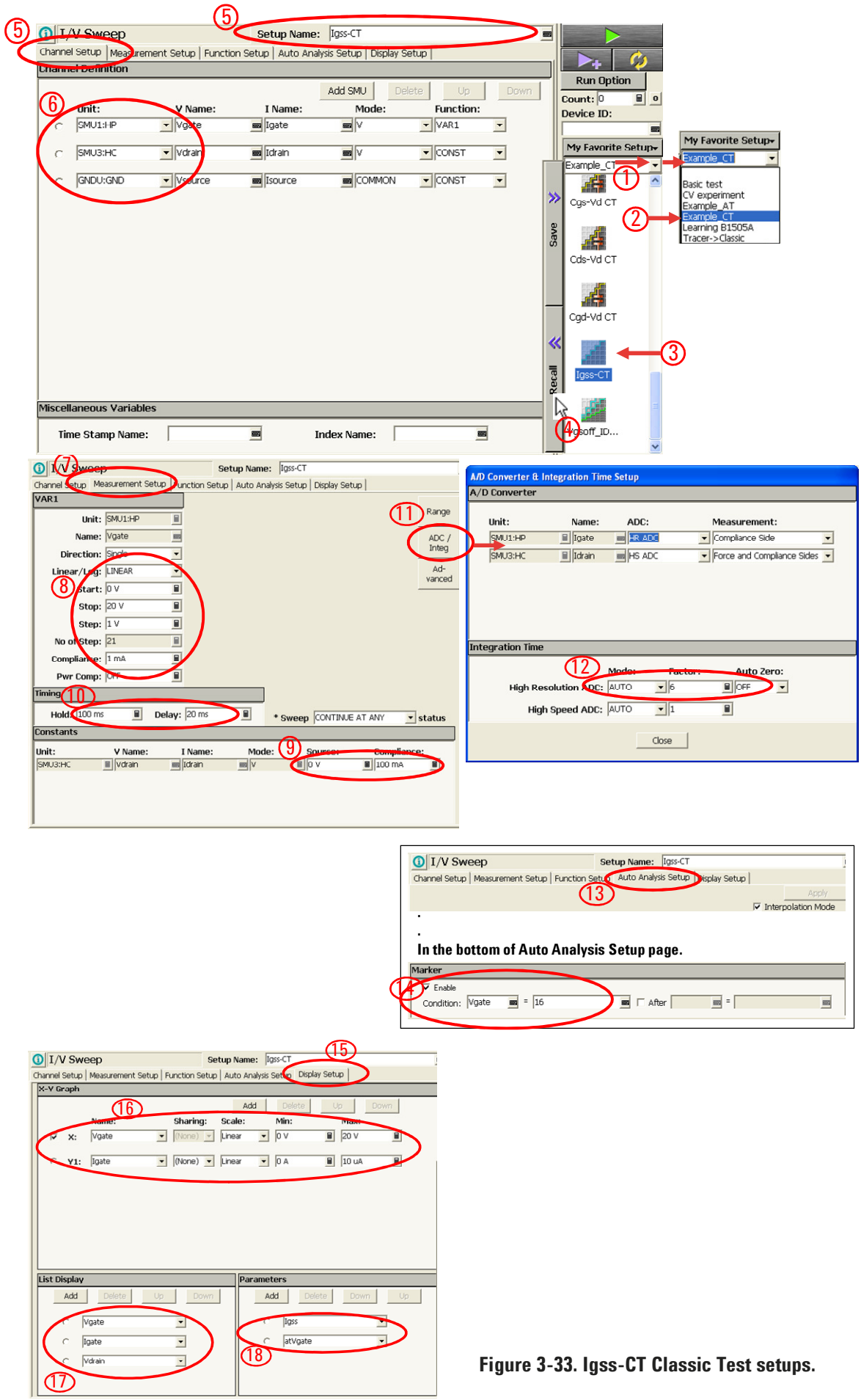


Figure 3-33. Igss-CT Classic Test setups.

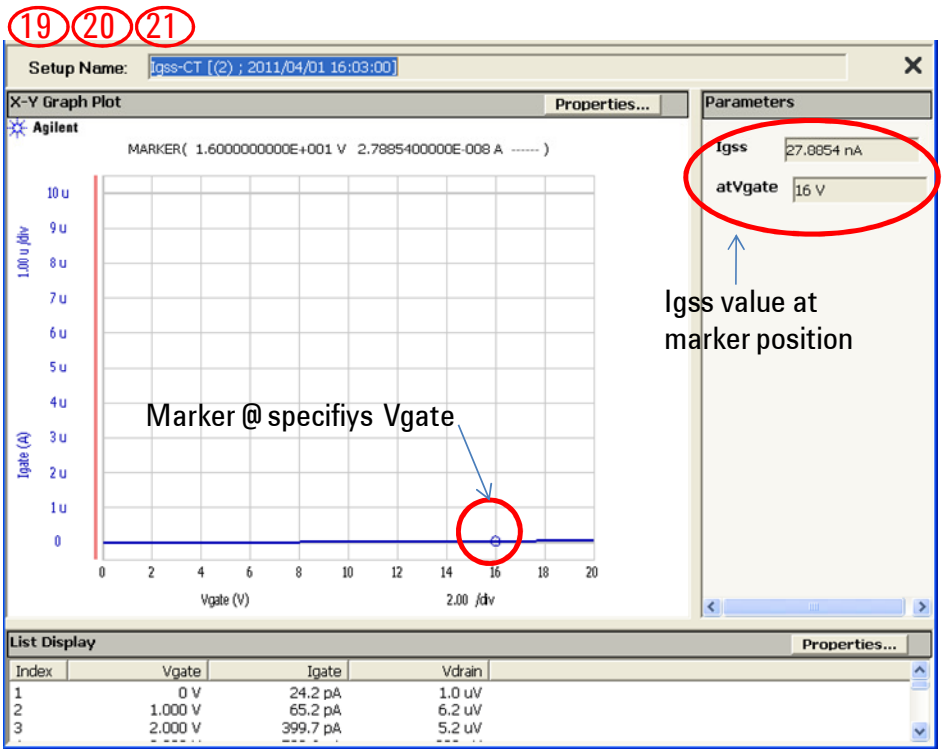


Figure 3-34. Igss-CT Classic Test example.

3-1-6 VGSS Gate-to-Source Voltage measurement

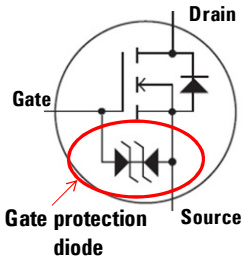
Measurement Parameters: VGSS, Vgs Gate-to-Source Voltage

Tracer Test setup name: (My Favorite Setup -> Example_CT): IG-VGS TT

Device used in the example: 2SK3745LS

Application description:

Vgss or Vgs (Gate to Source voltage) is categorized in absolute maximum ratings of power MOS-FET specification. This parameter is not necessarily measured as like the Vdss drain to source voltage which is an important parameter in designing the circuit block.



Typically there is a protection diode included between the gate and the source of power MOS-FET, and the actual measurement for Vgss performance check is to measure the breakdown characteristics of this protection diode.

This measurement handbook tries to measure the gate breakdown characteristics by using a dual polarity interactive sweep of Tracer Test mode.

Note: This test can be performed by using the 3-1-5 procedure by just increasing the Vg stop voltage for Application Test and the Classic Test setup.

A. Measurement Procedure: IG-VGS TT Tracer Test

Measurement Procedure: IG-VGS TT Tracer Test

One of the features of Tracer Test is a Dual Polarity sweep functionality. It can do from zero to both the positive and negative direction voltage or current sweep with one click of measure button or by continuously changing the maximum sweep value by using the rotary knob.

Vgss test can be a suitable example for trying to use the dual polarity sweep capability.

Step 1. Click Tracer Test from the EasyEXPERT Test menu on the left-upper side of the display as shown figure 3-35.

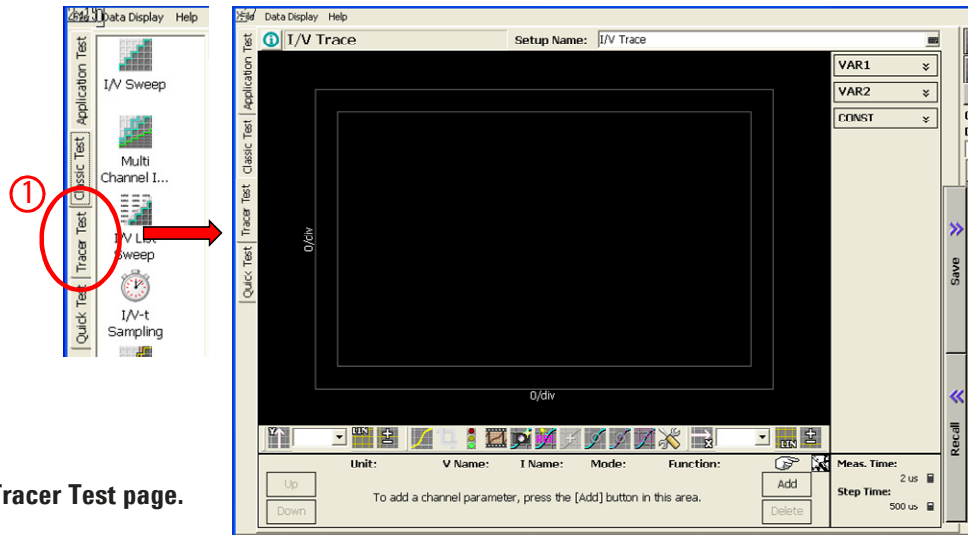


Figure 3-35.
To open the Tracer Test page.

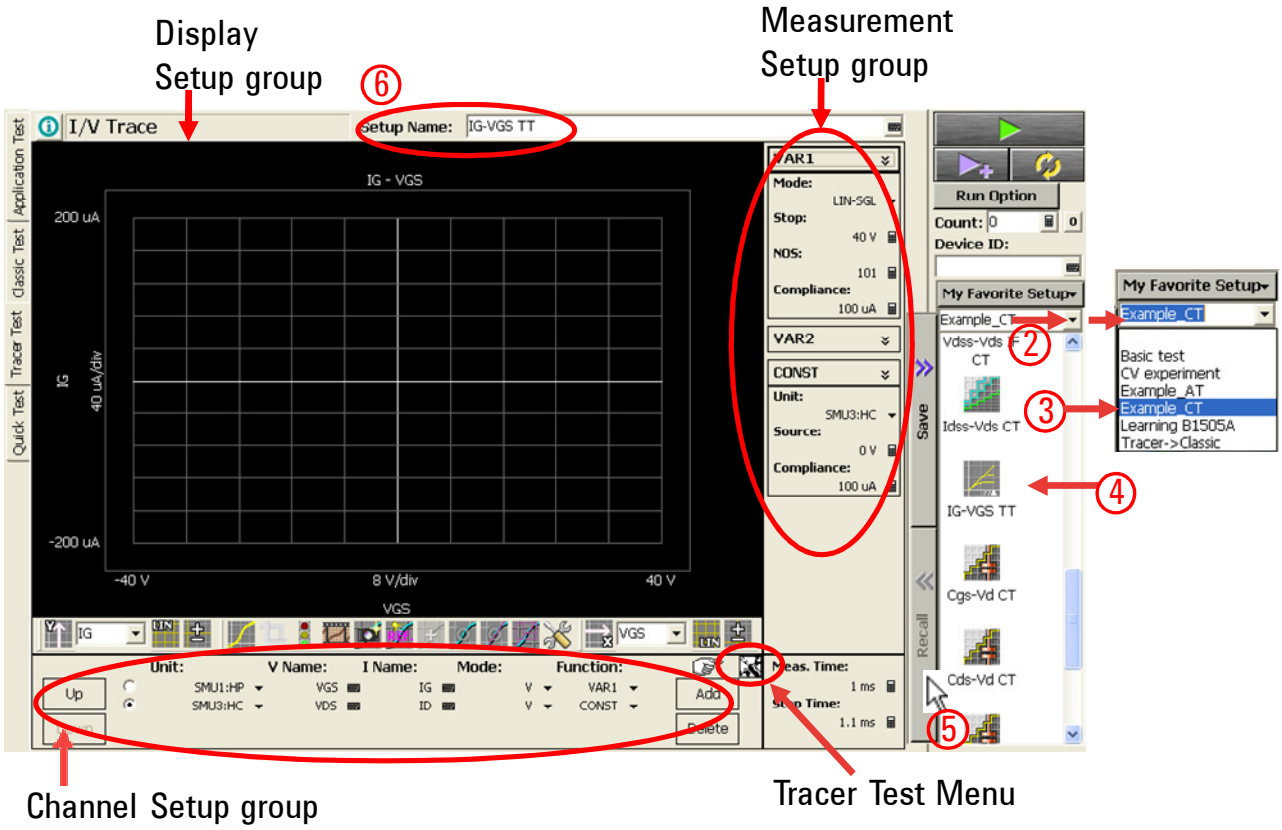


Figure 3-36. IG-VGS Tracer Test setup.

Tips: To open the Tracer Test setups, you have to open the Tracer Test page first.

Refer to figure 3-36 for the following Step 2 to Step 6.

Step 2. Click the Preset group of My Favorite Setup.

Step 3. Select Example_CT preset group.

Step 4. Select IG-VGS TT (IG-VGS Tracer Test).

Step 5. Press Recall button.

Step 6. Pre-defined example IG-VGS TT Tracer Test setup opens.

Note:

Tracer Test uses one page concept for all the setups and the display of the test results. The test setup functionalities are grouped in four separate areas of the display; Channel setup, Measurement setup, Display setup and Tracer Test Menu as shown in the figure.

These functions are roughly introduced by following the test setup steps.

Step 7. Set the test parameters shown in figure 3-37 to an appropriate one depending on your B1505A configuration and your test device.

The important check points are;

a. Gate and Drain SMU setup
By clicking the target Unit area, Channel definition area is activated and you can set the SMUs selection by clicking  button. The voltage and current name can be changed by just typing in to each field.

b. Set Vg sweep parameters in VAR1 field.
VAR1 parameter area can be expanded by clicking  of the VAR1 field. Set the VAR1 parameters by referring to the figure.

You can scroll the menu bar by dragging the VAR1 area where no input field is set. Input field is marked by  on the right side of the measurement parameters and you can drag any field by avoiding the lines marked by these indicators.

c. There is no VAR2 in the setup. If you set VAR2 in step a, then you can change parameters. Expansion of the input field can be done in the same manners as shown in step b.

d. Set Vd test condition in CONST field:
Vd voltage is typically zero volts.

e. Set the Y axis display parameter.
f. Set the Y axis display parameter.

g,h,i,j: Set the Y and X axis maximum and minimum value. The pop-up window opens by clicking each scales maximum or minimum number displayed on the screen. Please carefully target the mouse pointer enactory on the number field, else the pop-up window won`t open.

k. Tips:

By clicking the  icon, you can open the Tracer Test menu, and start from a predefined setup. This is an easy way for creating a Tracer Test setup. This is especially effective for creating a complicated test setup such as like including a pulse source.
Later, you can convert this setting to a Classic Test setup where no preset test definitions are available.

Step 8. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.

Start the measurement. (Click the Single button )

Step 9. The measurement starts and the graph appears as shown in figure 3-38.

You can activate Marker to read a specific data by clicking  mark in the lower side bar of the graph display.

Step 10. You can activate Marker to read a specific data by clicking  mark in the lower side bar of the graph display.

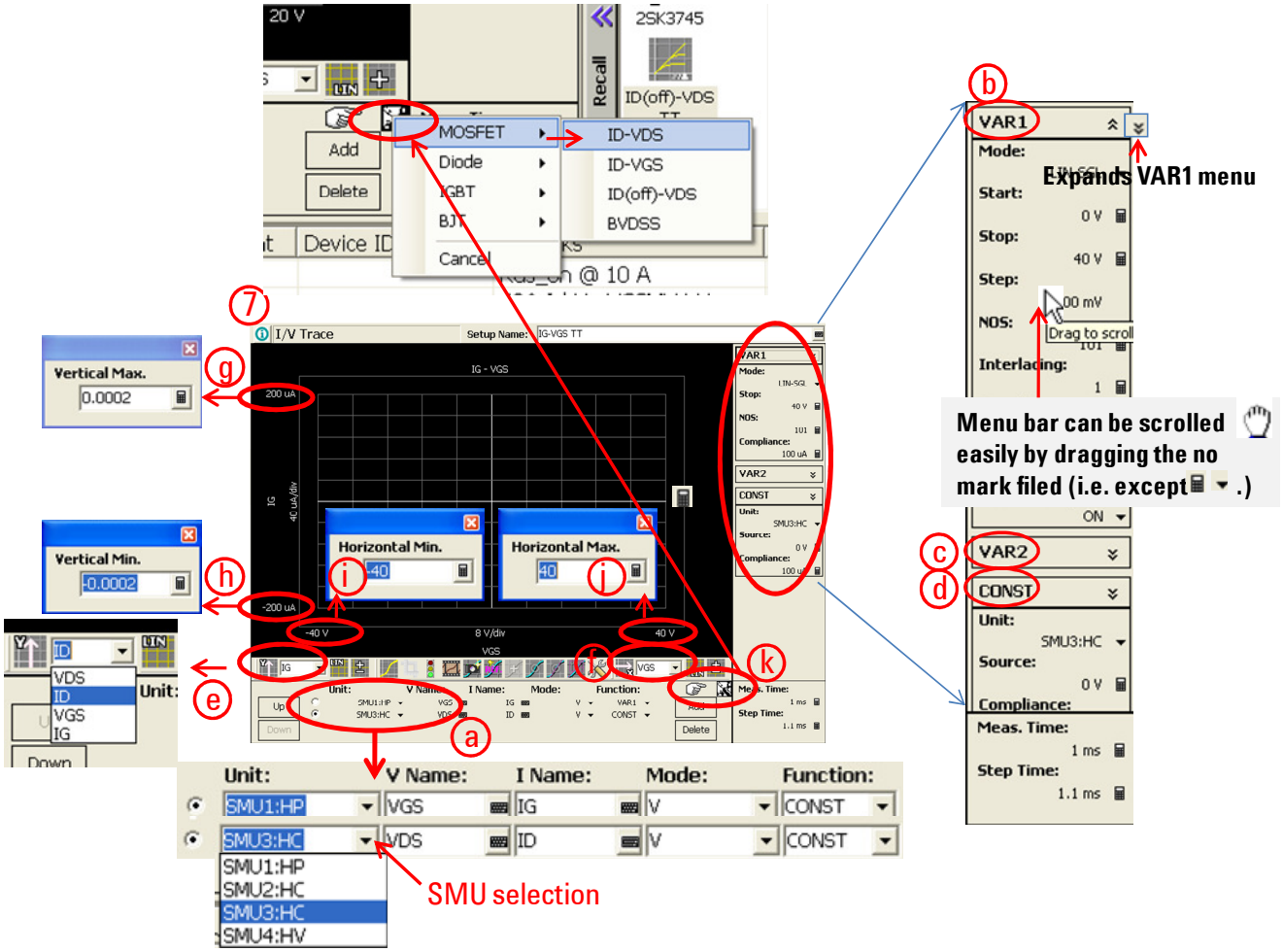


Figure 3-37. IG-VGS Tracer Test parameter setup.

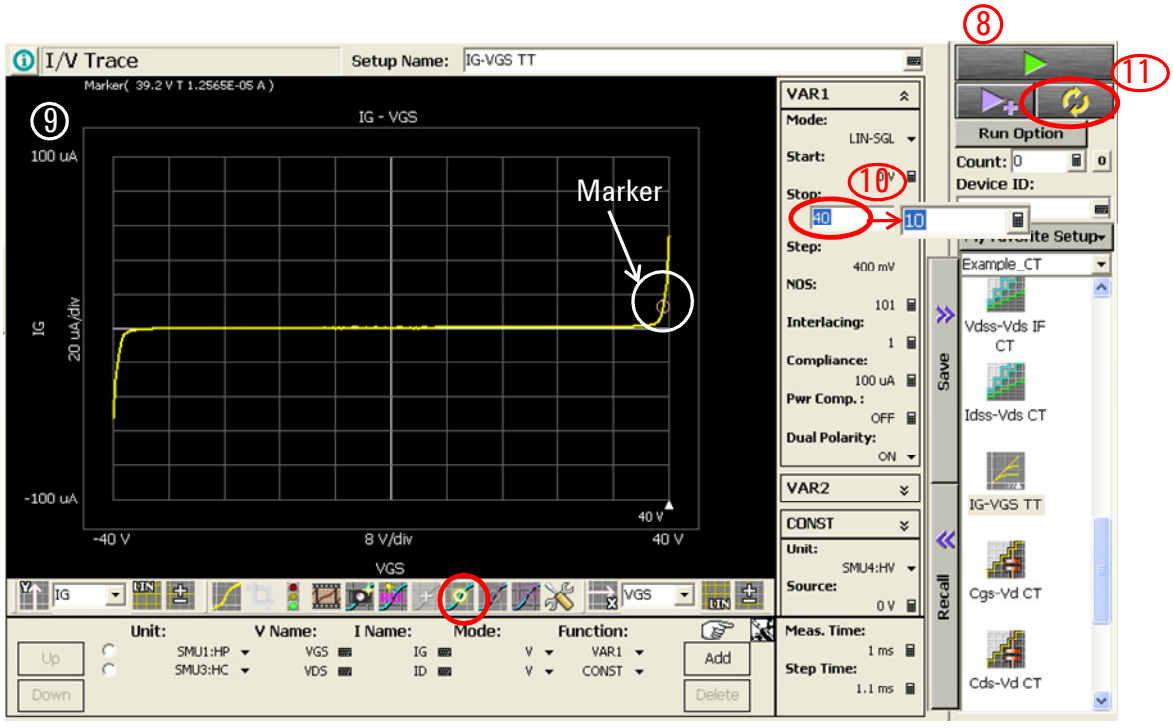


Figure 3-38. IG-VGS TT Tracer Test example.

Interactive sweep control:

You can control the sweep by manually by following the following steps; (See figure 3-39)

Step 11. Activate Stop voltage of VAR1, and set the voltage to a lower safe voltage, say 10 V.

Step 12. Start repeat measurement by pressing Repeat Measure  button.

Step 13. The graph sweeps to +-10 V marked "step 13" in figure 3-39 (top left) is shown.

Step 14. Activate Stop voltage of VAR1.

Now, you can control the maximum sweep voltage by rotating a rotary knob in real time manner.

Step 15. Rotate the knob clock wise.

The sweep end points increases as shown marked "step 15" (bottom left) in the figure.

Then the sweep finished at VGS=39.8 V in the example.

Tips:

There is typically a lot of margin between the Vgss absolute maximum rating and the breakdown voltage of gate protection diode. Therefore testing for showing the breakdown of the protection diode is not performed. When performing this test, set the gate SMU current compliance to a small value to prevent damaging the device. Slowly increasing the gate voltage by monitoring the breakdown characteristics as shown would be also effective.

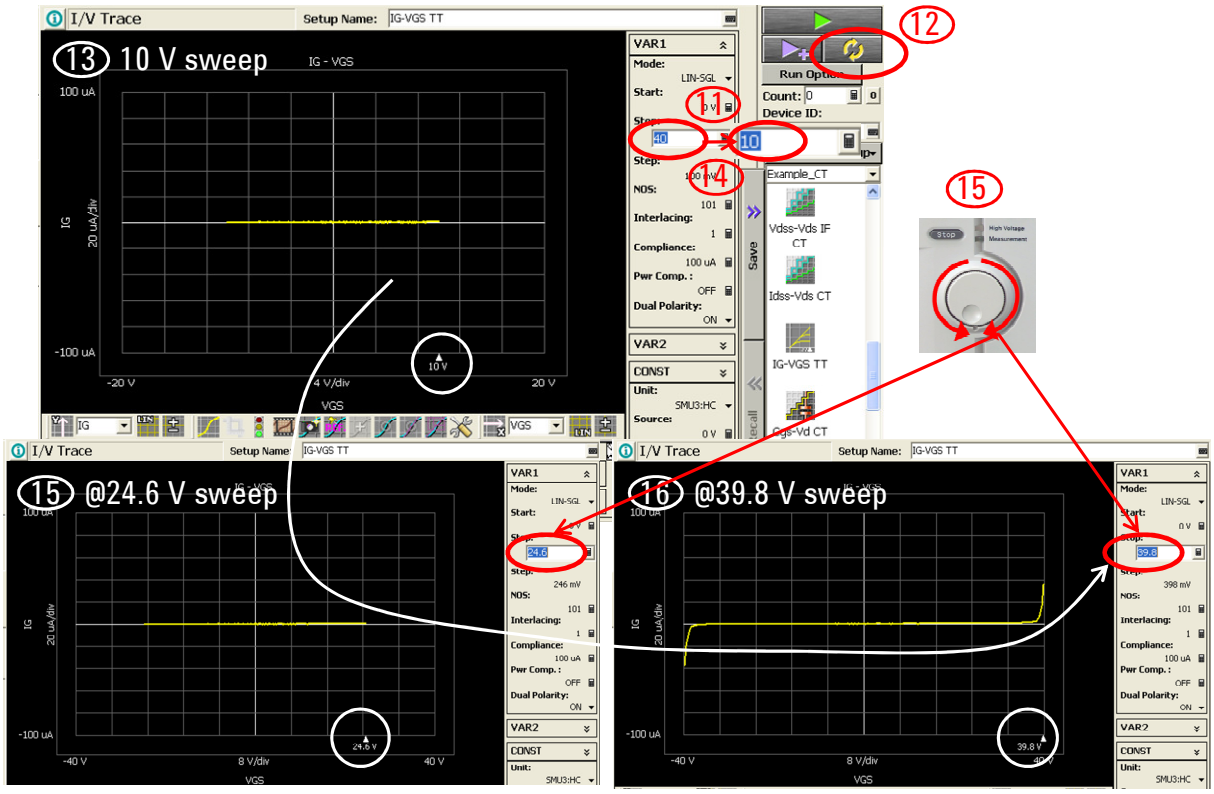


Figure 3-39. IG-VGS TT Tracer Test: Interactive sweep control.

3-2. Id-Vds Measurement group 1: High current

This section, the Id-Vds measurement group demonstrates the following measurements.

Id - Vds curve General Id-Vds characteristics, ID & IDP

ISD-VSD Reverse Drain Current and Diode Forward Voltage measurement

The Id-Vds measurement group basically sweeps the drain voltage as a primary sweep source while the gate voltage steps as a secondary sweep voltage source while the drain is swept as shown in Figure 3-40.

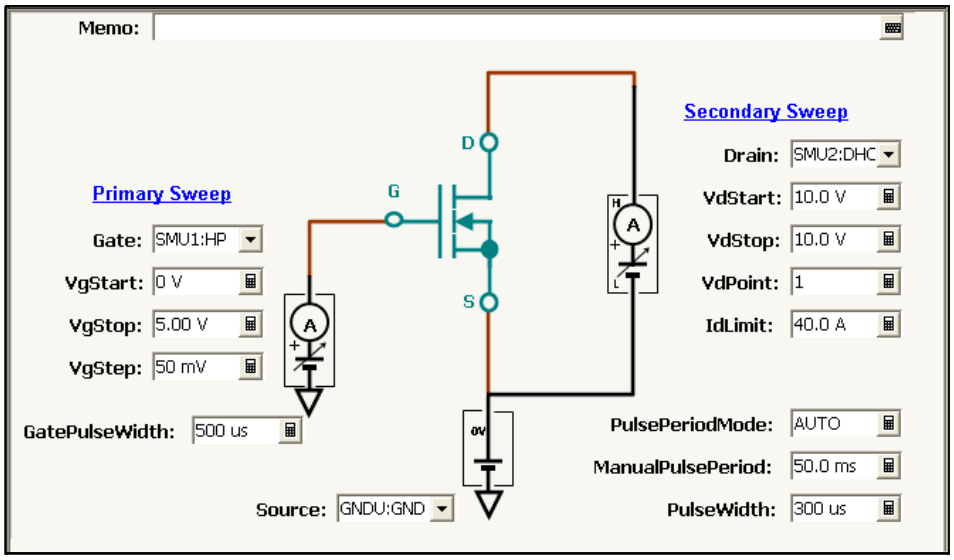


Figure 3-40. Id-Vg Application Test setup.

If the characteristics of a power MOS-FETs are unknown, starting the measurement from the Id-Vg characteristics and then maybe checking more detail from the Id-Vd measurements would be a good practice as a general idea. These two measurements provide an overview of the power MOS-FET characteristics in the beginning of the test.

Typical data sheet specification starts from the general Id-Vds measurement curve shown in figure 3-41 and the Id-Vgs curve which is already described in section 3-1-1.

Once the range of the gate voltage of the operation region of the power MOS-FET is found by the Id-Vg measurement as described, Id-Vd measurements can be made efficiently by eliminating sweeps with extra gate steps where the drain voltage is almost zero or already exceeding the measurement limit. This approach is more effective in pulsed Id-Vd measurements that take relatively longer measurement time compared to a DC test.

Id-Vd measurements provide a wide variety of information of the power MOS-FET for interfacing to the outside power circuit.

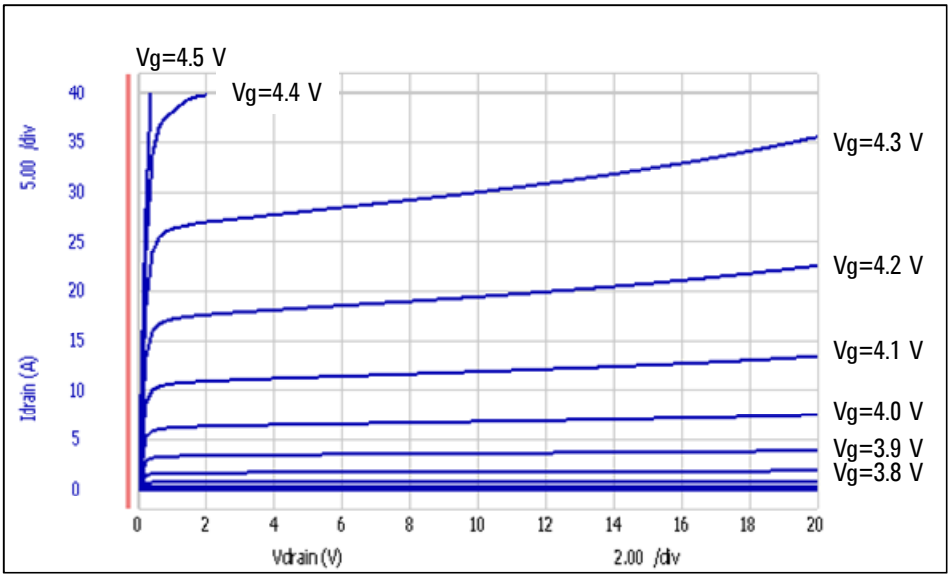


Figure 3-41. Typical Id-Vd measurement example.

Connection inside the N1259A Test Fixture

Connection inside the N1259A Test Fixture is the same as section 3-1 Id-Vgs measurement group.

Follow section 3-1 and figures from 3-3 to 3-5 for making a connection inside the N1259A Test Fixture.

NOTE: If Measurement is made with Opt.300 Module Selector, use the process shown in appendix A2-3-1.

3-2-1. Id - Vds measurement

Measurement parameters: General Id-Vds characteristics, ID & IDP

Application Test name: Id-Vds_DP (Id-Vds characteristics, SMU Dual Pulse)

Application Test setup name (My Favorite Setup -> Example_AT): Id-Vds_DP

Classic Test setup name (My Favorite Setup -> Example_CT): ID-VDS_DPC

Device used in the example: IRFP2907

Application description:

Measures Drain current vs. Drain voltage characteristics. SMU pulse is used for both the Drain-Source and the Gate-Source voltage output.

Following parameter (typically included in Absolute maximum rating) can be evaluated;
ID Drain Current (DC)
IDP, IDM Drain Current (Pulse)

A. Measurement Procedure: Id-Vgs_DP Application Test,

-Starting from Application Test Library

This test approach starts measurements by using an Application Test Library which starts from the default setup parameters and you have to customize the measurement parameters depending on your requirements.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-42.

Step 1. Click the Application Test tab.

Step 2. Check the PO_MOS_smpl category.

Step 3, 4. Select Id-Vds_DP (Click the Id-Vds_DP then click Select 

)

Step 5. Set the test parameters shown in figure 3-42 to an appropriate one depending on your B1505A configuration and your test device.

The important check points are;
a. Gate SMU setup
b. Set Vg secondary sweep parameters
c. Drain SMU setup
d. Set Vds primary sweep parameters
e. Drain voltage sweep can be set linear or log sweep.
Log scale provides more detail in lower drain voltage range.

Step 6. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

Step 7. The graph window pops up and the measurement starts.

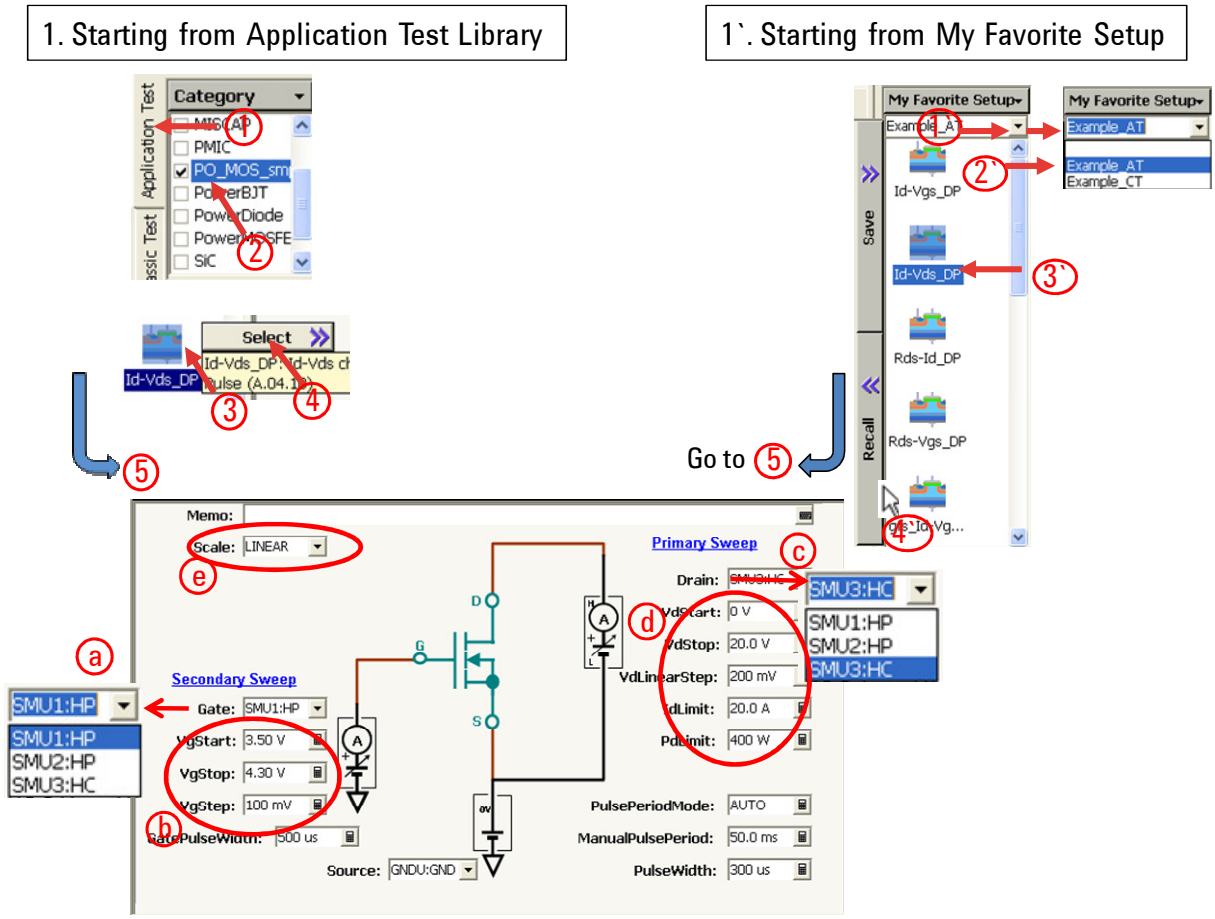


Figure 3-42. Id-Vds_DP Application Test setup.

Step 8. You can see the Id-Vds curve graph as shown in figure 3-43.

Figure 3-43 plots drain current Iv in Y axis versus drain voltage Vgs in X axis.

Tips:
Marker can be used for reading each drain current and voltage by rotating the rotary knob. You can read between the two measurement points by activating Interpolation mode to ON status.
Marker position can be stepped to next secondary sweep (Var2) step by pressing the rotary knob.

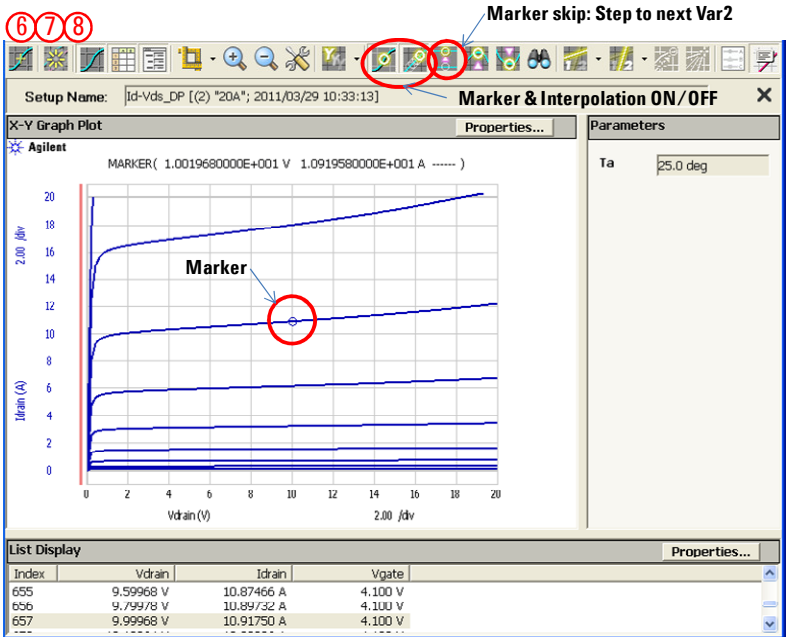


Figure 3-43. Id-Vds_DP Application Test Display.

A`. Measurement Procedure: Id-Vds_DP Application Test,

- Starting from pre-defined test setup of My favorite Setup

This test approach starts measurements by using a pre-defined test setup saved in My favorite Setup instead of starting from a scratch by using an Application Test Library.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1`. Starting from Application Test Library" side of figure 3-42.

Step 1`. Click the Preset group of My Favorite Setup.

Step 2`. Select Example_AT preset group.

Step 3`. Select Id-Vds_DP (Click the Id-Vgs_DP).

Step 4`. Click "Recall" button.

Then go to step 5 of "Starting from Application Test Library" above, and continue by following the test step numbers.

B. Measurement Procedure: ID-VGS_DPC Classic Test

Refer to figure 3-44 for the following Step 1 to Step 16.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_CT preset group.

Step 3. Select ID-VDS_DPC (ID-VDS Dual Pulse).

Step 4. Press Recall button.

Step 5. Pre-defined example ID-VDS_DPC classic test setup – Channel Definition page opens.

Channel Definition page setups the SMUs and its measurement function.

Step 6. Set Unit field appropriately depending on your B1505A and connection set-ups.

The connection between the SMU definitions and the power MOS_FET pins must be matched to each other.

Step 7. Press Measurement Setup tab.
You can change measurement parameters in this page.

Step 8. VAR1 or primary sweep parameters: VDS can be set.

Step 9. VAR2 or secondary sweep parameters: VGS can be set.

Step 10. Hold and Delay time can be set.

Step 11. Pressing “Pulse" button opens "Pulse Setup" sub-window.

Step 12. Integration time in pulsed measurement can be set. Make sure the integration time is less than 1 ms considering the maximum pulse width for HCSMU is 1 ms. We require more than 50 us typical time until the pulse is settled in higher current region, say more than 10 or 20 A, the integration time are to be less than pulse width - 50 us.

Step 13. Pulse width can be set. Since the minimum pulse width of HPSMU is 500 us and the maximum pulse width of HCSMU is 1 ms in 20A range, the possible range for pulse width id between 500 us to 1ms for HPSMU. HCSMU can be set less than 500 us, and it is effective for reducing the power dissipation of the power MOS-FET. Note that the minimum pulse width for the HCSMU is 50 us that is explained in step 12 plus the integration time. Refer to the appendix section if you want to know more about the pulsed measurements.

Step 14. Press Display Setup tab.

You can set the X-Y Graph, List Display and the Parameters of the measurement results in this page.

Step 15. The X, Y1, Y2 and so on to maximum Y8 axis can be defined as X-Y graph display.
Log or Linear scale and the Min. and the Max. scale parameters are set.

Step 16. List Display sets the measurement parameters that are shown in the List area of Display Graph window.

It is important for adding VGS parameter in the list because this is the only way for knowing the relation of VAR2 and the Id sweep curve.

Step 17. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

Step 18. The graph window pops up and the measurement starts.

Step 19. You can see the Id-Vgs curve and gfs (Y2 axis) graph that is the same as figure 3-43.

Note: Step 18 and 19 are the same as the step 7 and 8 of figure 3-43.

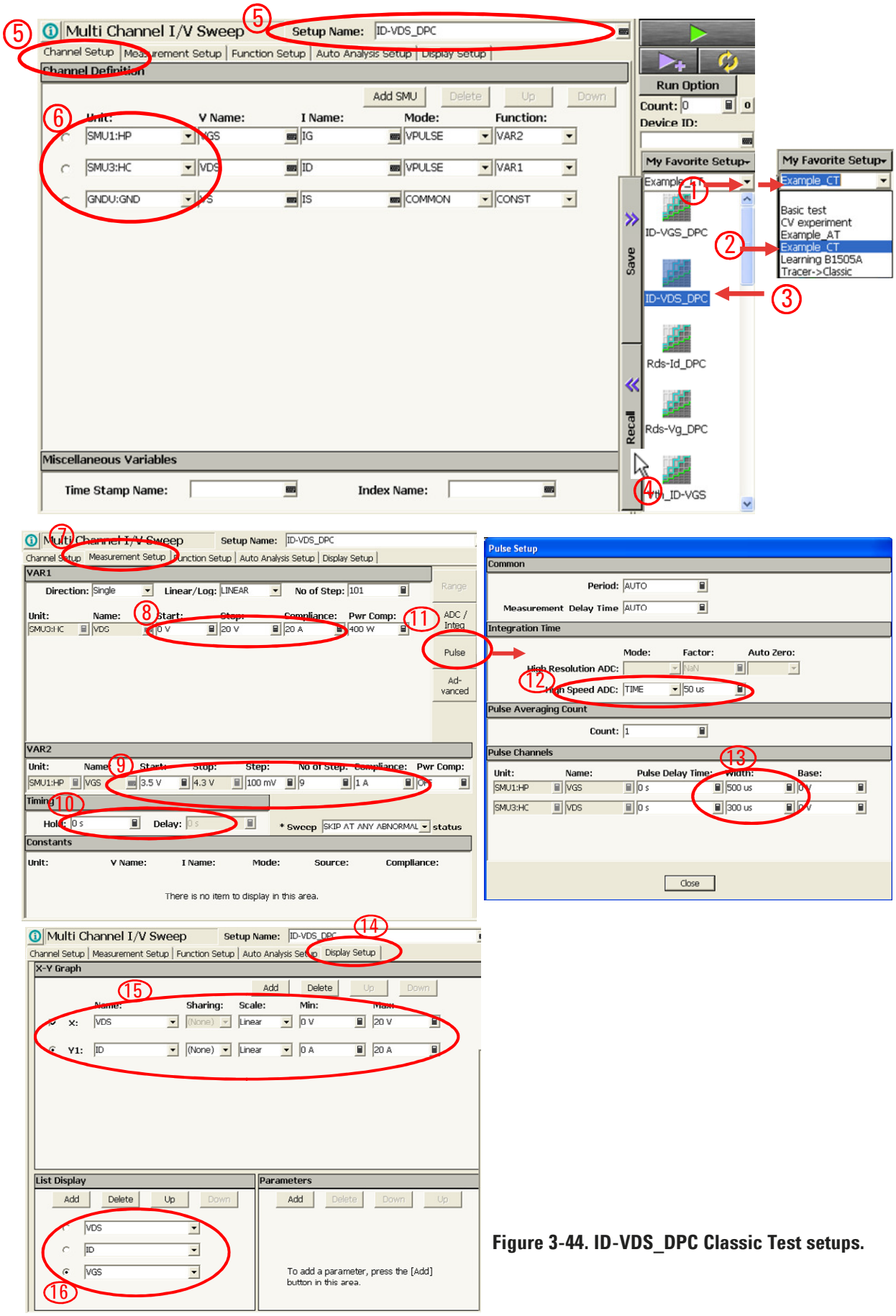


Figure 3-44. ID-VDS_DPC Classic Test setups.

Tips:

Although this example does not include any automatic analysis functions, but you can add automatic marker and lines.

Classic Test definition can change measurement parameters very easily. For example, changing the power compliance setting of the drain SMU in Measurement Setup page to 100 W generates the power limited Id-Vds graph as shown in figure 3-45.

Limiting the power compliance can emulate the similar effect of collector load line of the traditional analog curve tracer which is generated by the voltage drop of the series collector resistor in the collector supply line.
Refer appendix section for more detail about the difference and the merit of the SMU architecture of the two different system.

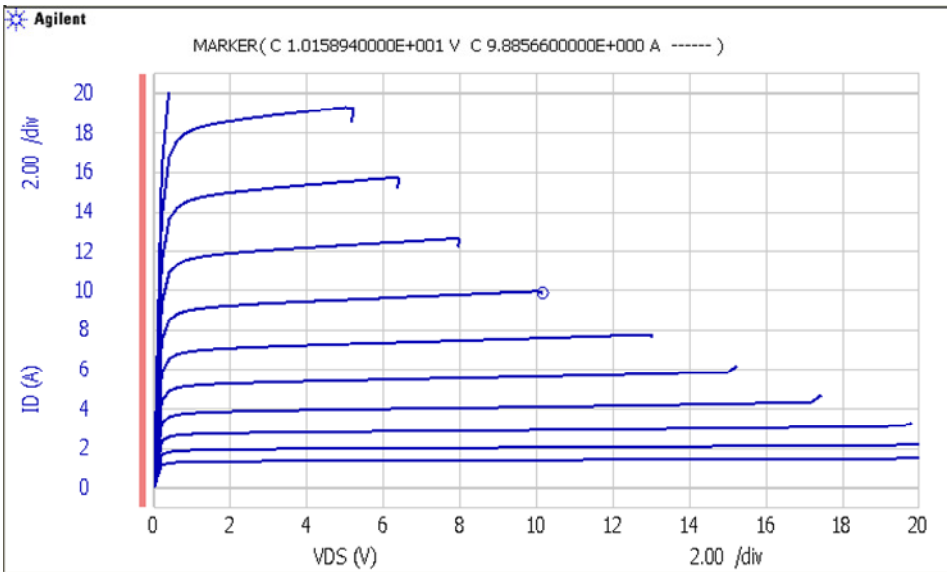


Figure 3-45. 100 W power limited ID-VDS curve.

Review:

The data sheet of high power MOS-FET sometimes shows Log Id versus log Vd characteristics for showing a wide range performance in a single shot.

You can perform this measurement very easily by using the existing definition of the Classic test. Figure 3-46 shows the locations to modify the Classic Test definition.

Step 1. Open Measurement Setup page.

Step 2. Change Var1 Linear/Log sweep to LOG10.

Step 3. Change Var1 start voltage to appropriate voltage for log sweep start voltage, say 10 mV.

Step 4. Open Display Setup page.

Step 5. Set the Y and X display scale to Log, and set minimum scale value for log display.

Start measurement to generate the log ID versus Log VDS graph as shown in figure

3-47.

Log-Log measurement is useful for checking wide range of measurement at a glance.

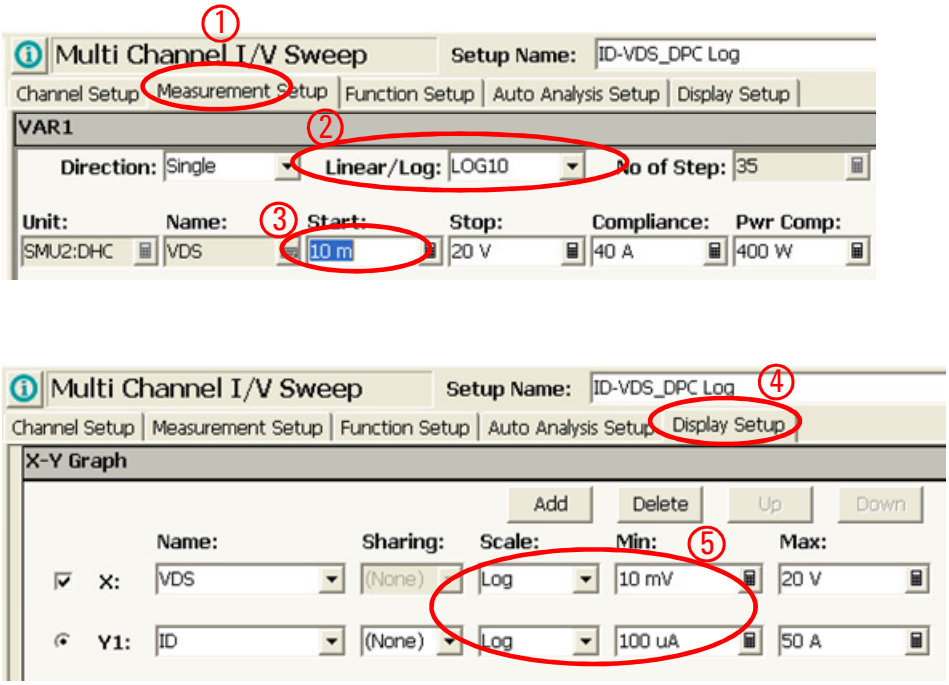


Figure 3-46. Log Id-Vd sweep and display setups.

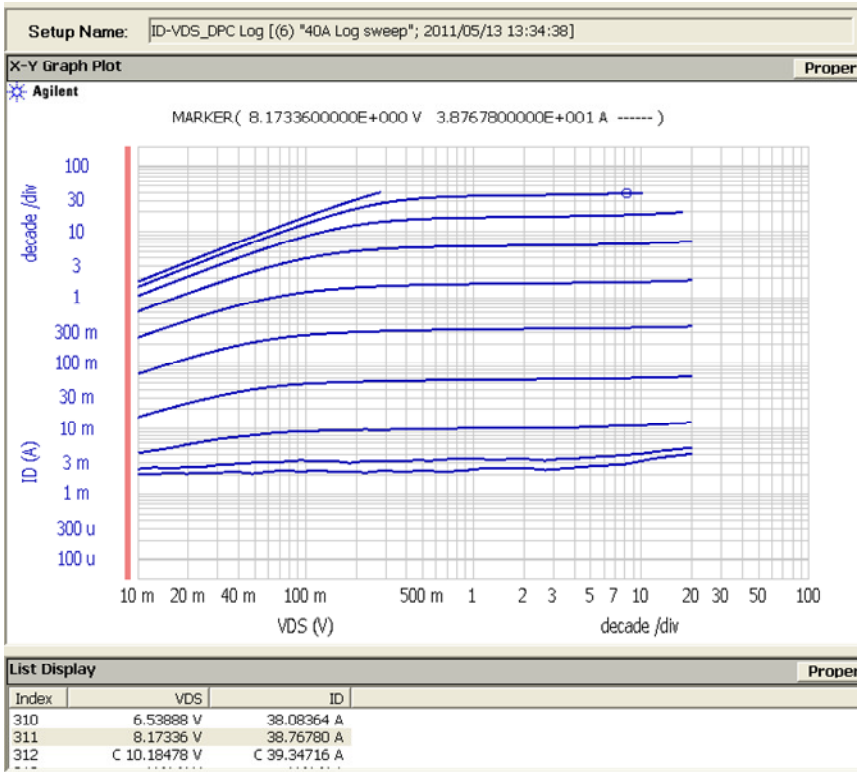


Figure 3-47. Log ID-VDS measurement example.

3-2-2. Isd - Vsd measurement

Measurement parameters: Vsd Diode Forward Voltage

Application Test name: Is-Vsd (Is-Vsd characteristics)

Application Test setup name (My Favorite Setup -> Example_AT): Is-Vsd

Classic Test setup name (My Favorite Setup -> Example_CT): ISD-VSD_CT

Device used in the example: IRFP2907

Application description:

This test measures the forward diode characteristics between the drain and the source of power MOS-FET; the Diode Forward Voltage Vs and Reverse Drain Current or Source current Is under Vgs=0 V condition. Drain SMU pulse is used for Source-Drain voltage output.

The actual test is performed by sweeping the drain for negative voltage while the source and the gate are kept in zero volts as shown in figure 3-48 EasyEXPERT GUI. The result is the same as applying positive voltage to Source while the Source and the Gate is shorted.

A. Measurement Procedure: Is-Vsd Application Test,

-Starting from Application Test Library

This test approach starts measurements by using an Application Test Library which starts from the default setup parameters and you have to customize the measurement parameters depending on your requirements.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-48.

Step 1. Click the Application Test tab.

Step 2. Check the PO_MOS_smpl category.

Step 3,4. Select Is-Vsd (Click the Is-Vsd then click Select 

)

Step 5. Set the test parameters shown in figure 3-48 to an appropriate one depending on your B1505A configuration and your test device.

The important check points are;

a. Gate SMU setup

b. Set Vg secondary sweep parameters
Usually the gate voltage is 0 V since the gate and the source voltage are the same in this measurement.
This test sweeps drain instead of sweeping Gate and Source with the same voltage.

c. Drain SMU setup

d. Set Vds primary sweep parameters
Since Source and Gate are set to zero volts, the drain is swept in negative

potential for measuring the Source-Drain diode forward characteristics.

e. Source current can be plotted in linear or log scale.
Log scale provides more detail in lower source current range and the line fit provides the quality of the diode process.

Step 6. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.

Start the measurement. (Click the Single button )

Step 7. The graph window pops up and the measurement starts.

Step 8. You can see the Is-Vsd curve graph as shown in figure 3-49.

Figure 3-49 plots source current Iv in Y1 axis versus source voltage Vsd in X axis.

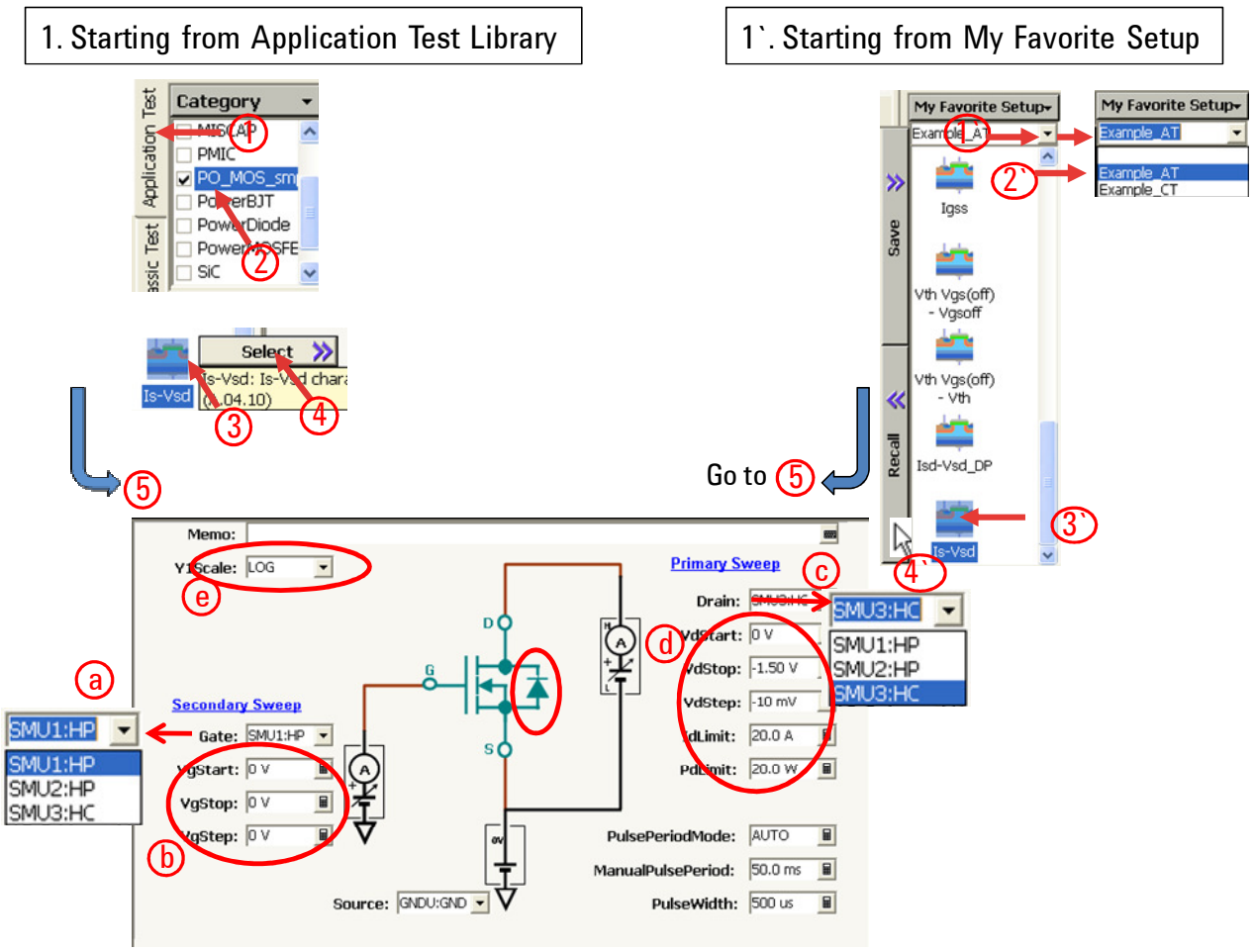


Figure 3-48. Is-Vsd Application Test setup.

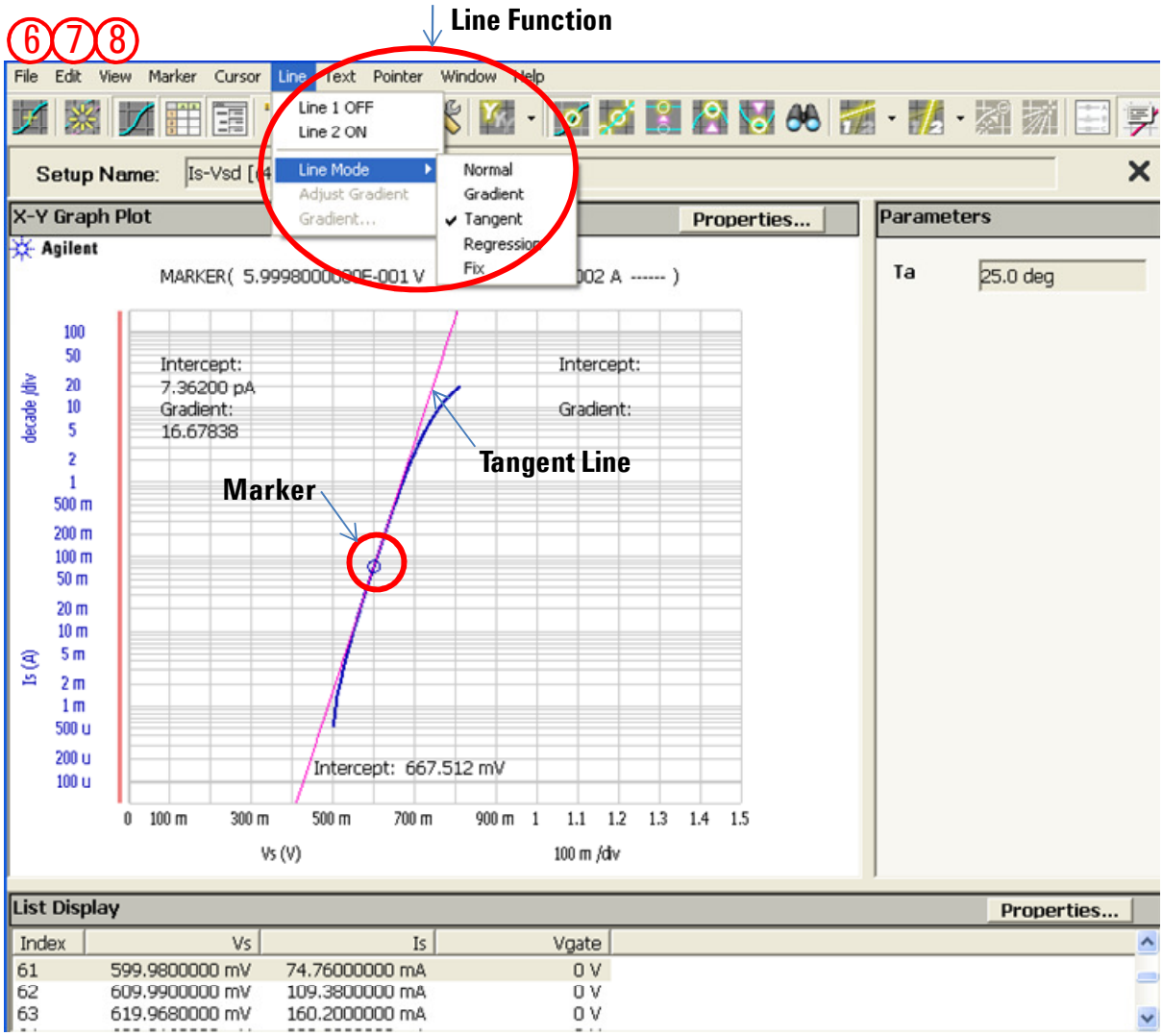


Figure 3-49. Source-Drain diode forward characteristics using the Is-Vsd Application Test.

Review:

Marker can be used for reading each source current and voltage by rotating the rotary knob. You can draw a line as shown in the figure by using the Line function; a tangent line is used in the example.

The specification of Vsd of the example IRFP2907 is maximum 1.3 V @125A. It is difficult for reading the data by extrapolating the 20 A curve, but it looks okay.

A`. Measurement Procedure: Is-Vsd Application Test,

- Starting from pre-defined test setup of My favorite Setup

This test approach starts measurements by using a pre-defined test setup saved in My favorite Setup instead of starting from a scratch by using an Application Test Library.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1`. Starting from Application Test Library" side of figure 3-48.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_AT preset group.

Step 3. Select Is-Vsd (Click the Is-Vsd).

Step 4. Click "Recall" button.

Then go to step 5 of "Starting from Application Test Library" above, and continue by following the test step numbers.

B. Measurement Procedure: ISD-VSD_CT Classic Test

Refer to figure 3-50 for the following Step 1 to Step 16.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_CT preset group.

Step 3. Select ISD-VSD_CT (ISD-VSD Classic Test).

Step 4. Press Recall button.

Step 5. Pre-defined example ISD-VSD_CT classic test setup – Channel Definition page opens.

Channel Definition page setups the SMUs and its measurement function.

Step 6. Set Unit field appropriately depending on your B1505A and connection set-ups.

The connection between the SMU definitions and the power MOS_FET pins must be matched to each other.

Step 7. Press Measurement Setup tab.

You can change measurement parameters in this page.

Step 8. VAR1 or primary sweep parameters: VDS can be set.
Note that drain is swept and the polarity is negative.

Step 9. Constant for VGS can be set. The VGS is Typically 0 V.

Step 10. Hold and Delay time can be set.

Step 11. Pressing “ADC/Integ" button opens "AD Converter & Integration Time

Setup" page.

Step 12. "Integration Time" for High Speed ADC is set.
The maximum ADC time is 1 ms when used with HCSMU`s pulse mode.

Step 13. Pressing “Pulse" button opens "Pulse Setup" sub-window.

Step 14. Pulse width of HCSMU can be set. Allowable pulse width is between 50 us to 1 ms.

Step 15. Press Function Setup tab.
You can see Is and Vs is defined in the User Function field.

Step 16. Press Display Setup tab.

You can set the X-Y Graph, List Display and the Parameters of the measurement results in this page.

Step 17. The X, Y1, Y2 and so on to maximum Y8 axis can be defined as X-Y graph display.
Log or Linear scale and the Min. and the Max. scale parameters are set.

You can set Linear/Log display scale in Y1 scale field as like the Application Test does in user GUI.

Step 18. List Display sets the measurement parameters that are shown in the List area of Display Graph window.

Step 19. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

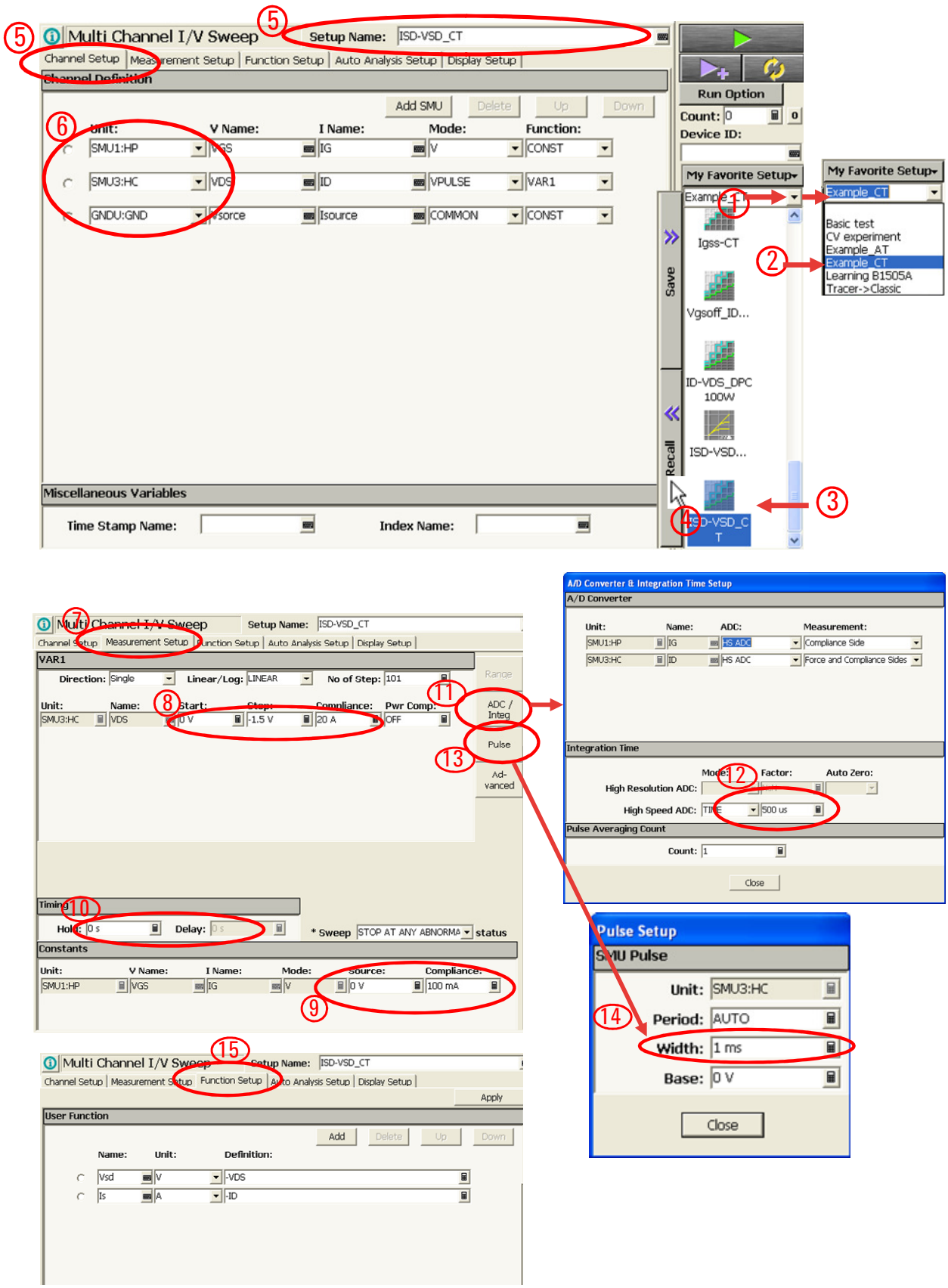
Step 20. The graph window pops up and the measurement starts.

Step 21. You can see the Id-Vgs curve and gfs (Y2 axis) graph that is the same as figure 3-49.

Note:
Step 20 and 21 are the same as the step 7 and 8 of figure 3-49. The Maker and Line function can be activated as shown in the figure 3-49.

Tips of the measurement:

This test sweeps the drain toward the negative voltage and actual output is converted to the drain voltage and the current to Source voltage and the current. The simplest way for measurement is applying the Source sweep voltage to the Source terminal, but this simple method requires HCSMU from the drain to Source. We applied the method for sweeping the drain for aiming better efficiency of the total measurement by not changing the cable connection.



Part of Figure 3-50. ISD-VSD_CT Classic Test setups. Continue to next page.

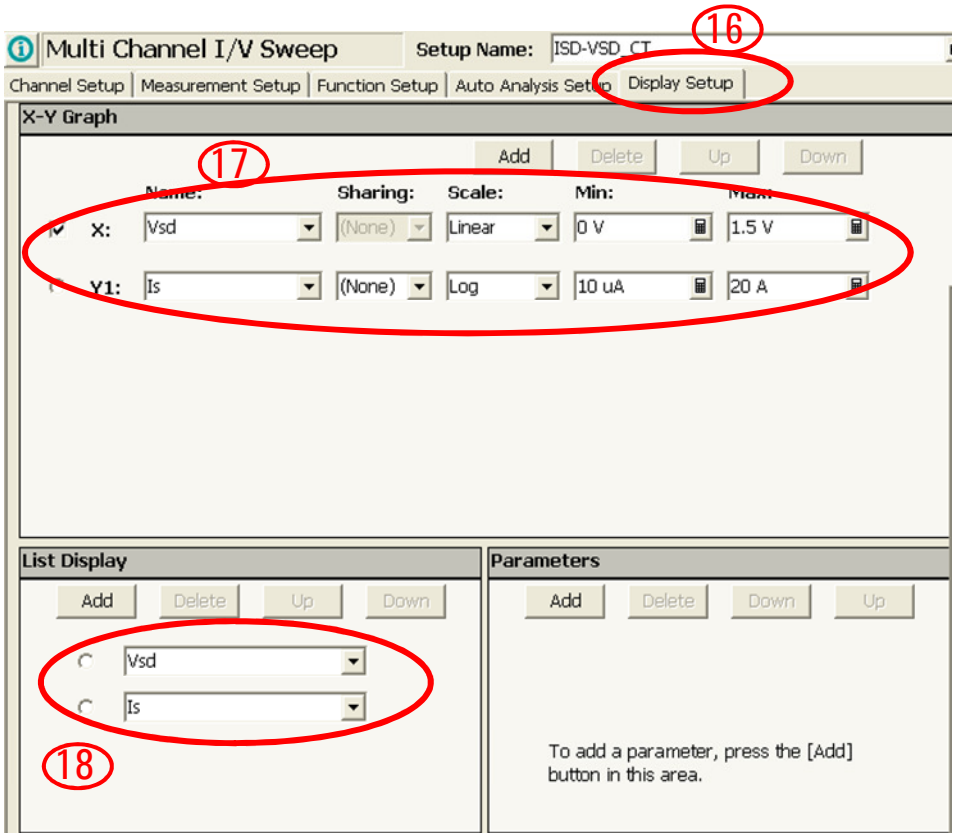


Figure 3-50. ISD-VSD_CT Classic Test setups.

3-3. Id-Vds Measurement group 2: High voltage

This section, the Id-Vds measurement group demonstrates the following measurements.

V(BR)DSS	Drain-to-Source Breakdown Voltage
IDSS	Drain-to-Source Leakage Current

The high voltage Id-Vds measurement group basically sweeps the drain voltage or current as a primary sweep source and measures current or voltage while the gate voltage is set to zero volts. Sometimes a series protection resistor is inserted between the drain SMU and the drain terminal of the power MOS-FET as shown in figure 3-51.
The voltage drop by the protective series resistor has to be compensated if the voltage drop is negligible.

Typically, Idss test measures low current at specified voltage in high resistive region and Vdss test measures voltage in low resistive region at specified current. Idss test can be performed easily by using a voltage force method and Vdss test can be performed easier by using a current force method.

In this section, we demonstrate these tests by using two different test approach in Application Test and Classical Test group.

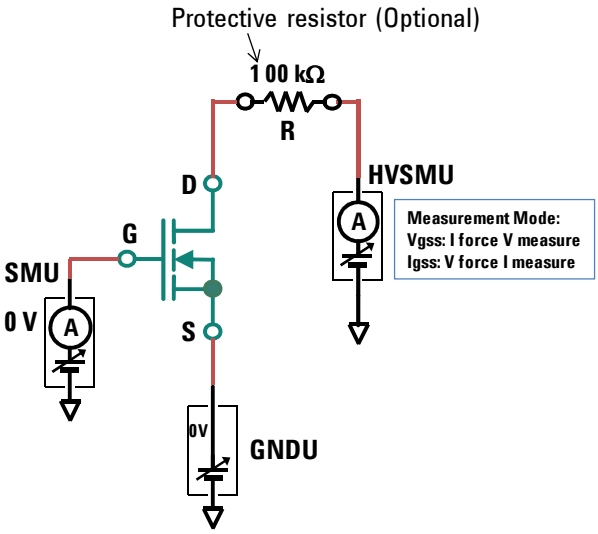


Figure 3-51: Basic configuration of Id-Vd, high voltage group measurement.

Note: Safety

This test group uses high voltage typically exceeding 1 kV and insuring safety for operating the instrument is important. The N1259A test fixture used in this handbook provides safety interlock system with the combination of B1505A mainframe.

When the output voltage from any of the B1505A SMU exceeds 42 V, there is no output voltage in the case when the fixture cover opens. i.e. the interlock system open.

When the cover is closed and more than 42V is output, then a red LED shock hazard lamp on the front side of the fixture comes on. Do not open the fixture when the shock hazard light is on.

3-3-1. V(BR)DSS and IDSS measurements using Application Test

Measurement parameters:

V(BR)DSS Drain-to-Source Breakdown Voltage

IDSS Drain-to-Source Leakage Current

Application Test name: Id(off)-Vds R (Id(off)-Vds characteristics, Protective R is supported)

Application Test setup name (My Favorite Setup -> Example_AT): Id(off)-Vds R

Classic Test setup name (My Favorite Setup -> Example_CT): None

Device used in the example: 2SK3745LS

Application description:

Measures and plots Drain current vs. Drain voltage characteristics in the cutoff region, and extracts the breakdown voltage and the cutoff current. Measurement is aborted just after the detection of the drain breakdown.

A. Measurement Procedure: Id(off)-Vds R Application Test without 100 kΩ resistor

Connection inside the N1259A Test Fixture (no 100 kΩ protective R)

Open the N1259A test fixture cover, and connect the test leads by following the step numbers as shown in figure 3-52. The numbers of the procedure steps correspond to the numbers on the drawing for connecting the test leads.

NOTE: If Measurement is made with Opt.300 Module Selector, use the process shown in appendix A2-3-1.

[PROCEDURE]

Step 1. Insert the power MOS-FET (example: 2SK3745LS) into the socket on the N1259A. Make sure the device pin name matches the socket numbers shown in figure 3-51.

Step 2. Connect the HPSMU1 Force to the terminal 1 on the 1 kΩ resistor.

Step 3. Connect the HPSMU1 Sense to the terminal 1 on the 1 kΩ resistor.

Step 4. Connect the terminal 2 on the 1 kΩ resistor to the terminal 1 Force (Gate) on the Inline Package Socket.

Step 5. Connect the GNDU1 Force to the terminal 3 Force (Source) on the Inline Package Socket.

Step 6. Connect the GNDU1 Sense to the terminal 3 Sense (Source) on the Inline Package Socket.

Step 7. Connect the Force of the HVSMU1 to the terminal 2 Force (Drain) on the Inline Package Socket.

Close the N1259A fixture cover.

Tips on connection inside the N1259A:

Inserting 1 kΩ resister in series near the gate terminal as in step 2 is not necessary in high voltage measurements. But we keep the same connection as the high current Id-Vd measurement group for reducing the re-connection of the cables.

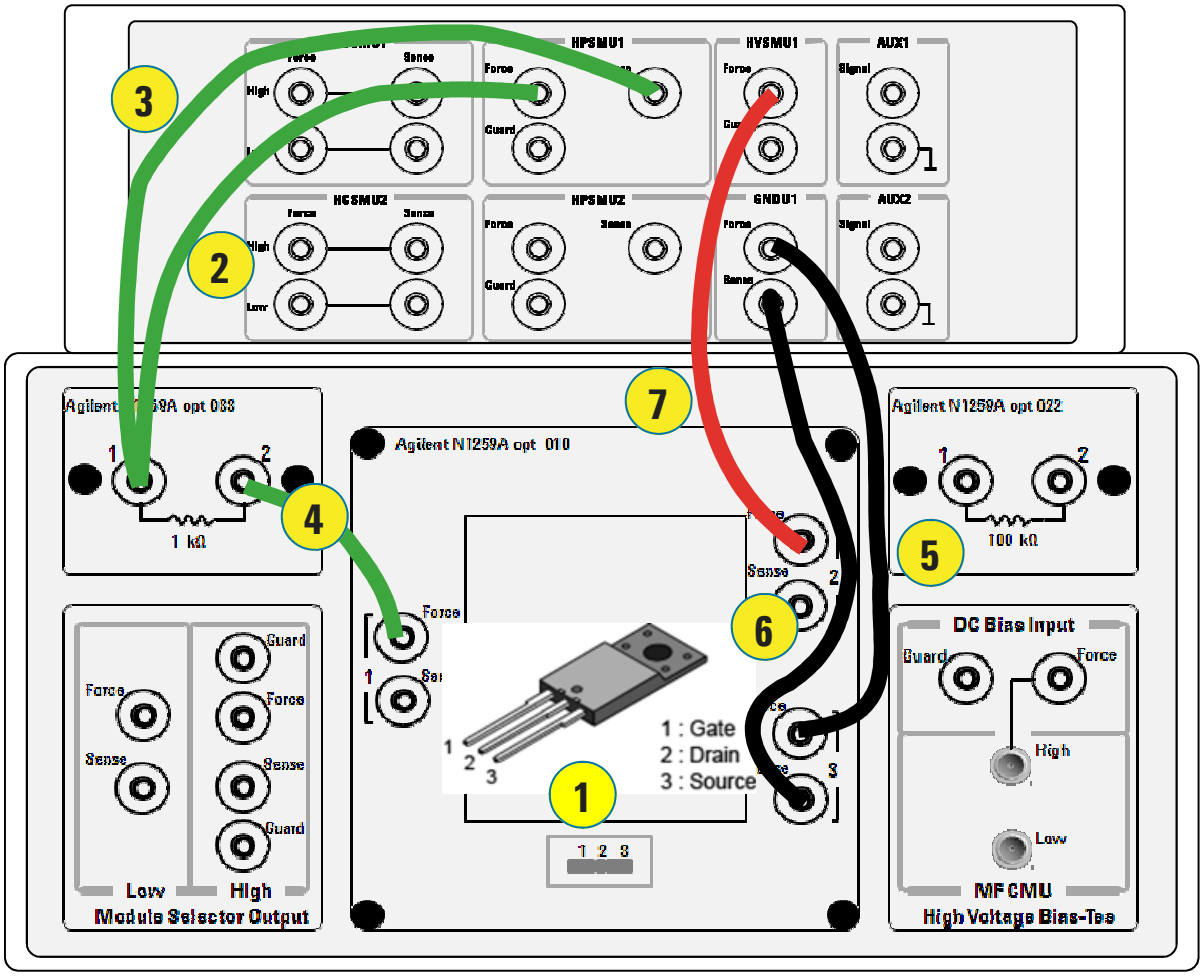


Figure 3-52. Connection between the SMUs and the power MOS-FET fixture.

-Starting from Application Test Library

This test approach starts measurements by using an Application Test Library which starts from the default setup parameters and you have to customize the measurement parameters depending on your requirements.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-53.

Step 1. Click the Application Test tab.

Step 2. Check the PO_MOS_smpl category.

Step 3,4. Select Id(off)-Vds R (Click the Id(off)-Vds R then click Select 

)

Step 5. Set the test parameters shown in figure 3-53 to an appropriate one depending on your B1505A configuration and your test device.

The important check points are;

a. Gate SMU setup
b. Set Vg constant parameter, typically 0 V.
c. Drain SMU setup. Choose HVSMU.

d. Set Vd sweep condition.
Start voltage is better to choose closer voltage of Idss specified voltage for speeding the test.
Stop voltage is chosen higher than Vdss.
Id limit is set slightly higher than the Idss specification.
The decision of Vdstep is a compromise between the sweep speed and the Vdss detection accuracy when series R for drain is not used.

e. Set the Vd@Idss that defines the drain voltage to measure Idss and Id@Vdss that defines the drain current to measure the drain breakdown voltage.
Note: If the drain step voltage is too large and the 100 kΩ series resistor is not inserted, Vdss measurement accuracy would be degraded.

f. Set Drain R value depending on your actual configuration. In the example select "0 Ω".

Step 6.Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button 
)

Step 7. The graph window pops up and the measurement starts with red Shock hazard indicator.
If interlock is not closed, i.e. the fixture cover is not closed firmly down to the fixture, then the measurement won`t start with a warning message.
In this case, make sure the interlock cable is connected and the fixture cover is closed, and repeat Step 6.

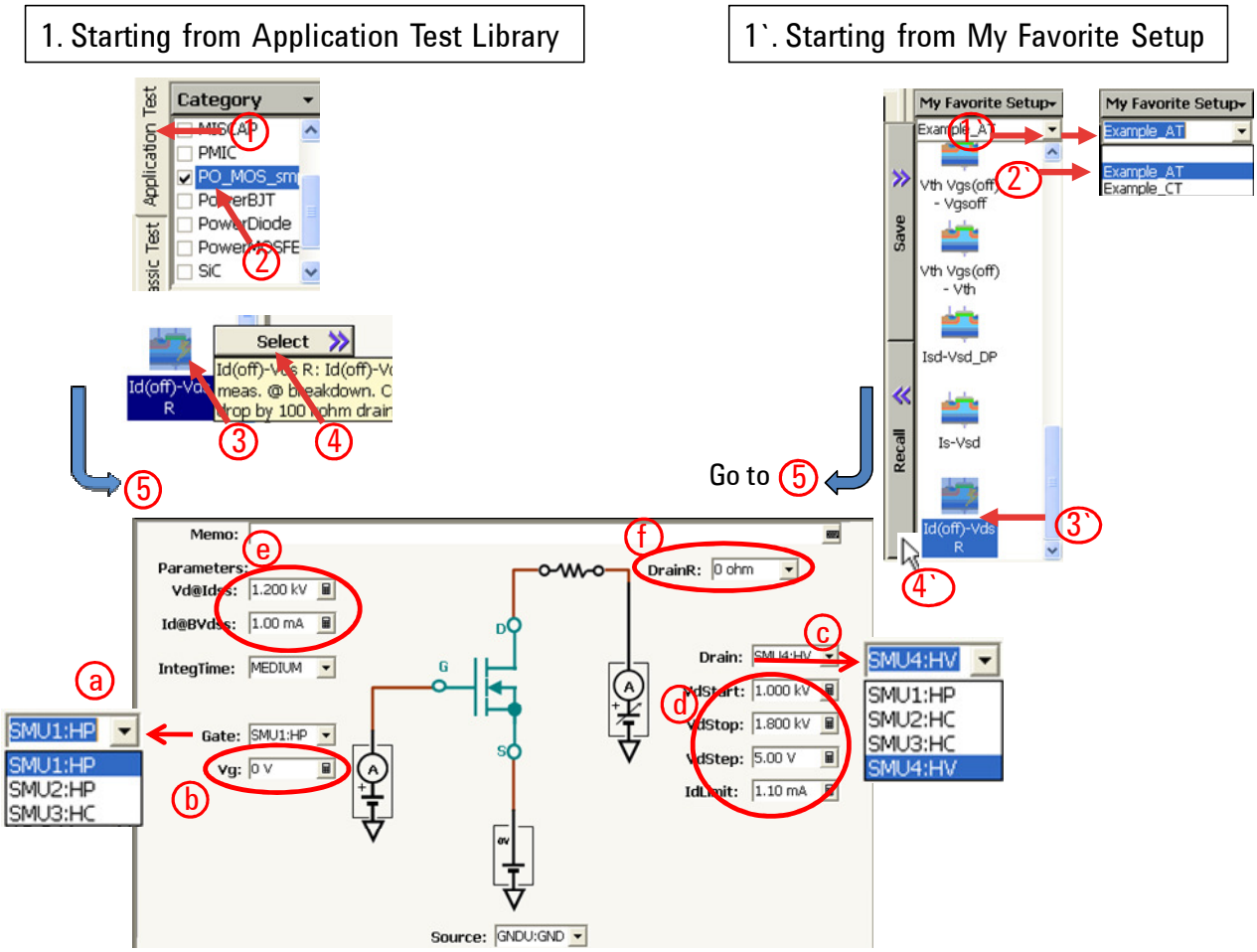


Figure 3-53. Id(off)-Vds R Application Test setup.

Step 8. You can see the Id-Vds curve with extracted Idss and BVdss in figure 3-54.

Figure 3-54 plots linear drain current Idrain in Y1 axis and log Idrain in Y2 axis versus drain voltage Vdrain in X axis. Horizontal line is drawn at Idss and Marker is automatically positioned to the BVgss point using the interpolation method.

Review:

The extracted results agree to the 2SK2745LS specification. Bvdss is 1,645 V that is larger than 1.5 kV specification and Idss is 88 nA which is much lower than the specification.

Tips:

Properly setting the HoldTime and DelayTime in Extended setup shown in figure 3-55 is important for accurate measurement of Idss. If your first Vdrain step is large, then adding an extra HoldTime for waiting the drain voltage to settle is important for accurate measurement. DelayTime is a wait time before measuring each drain voltage step, and adding a proper wait time is important.

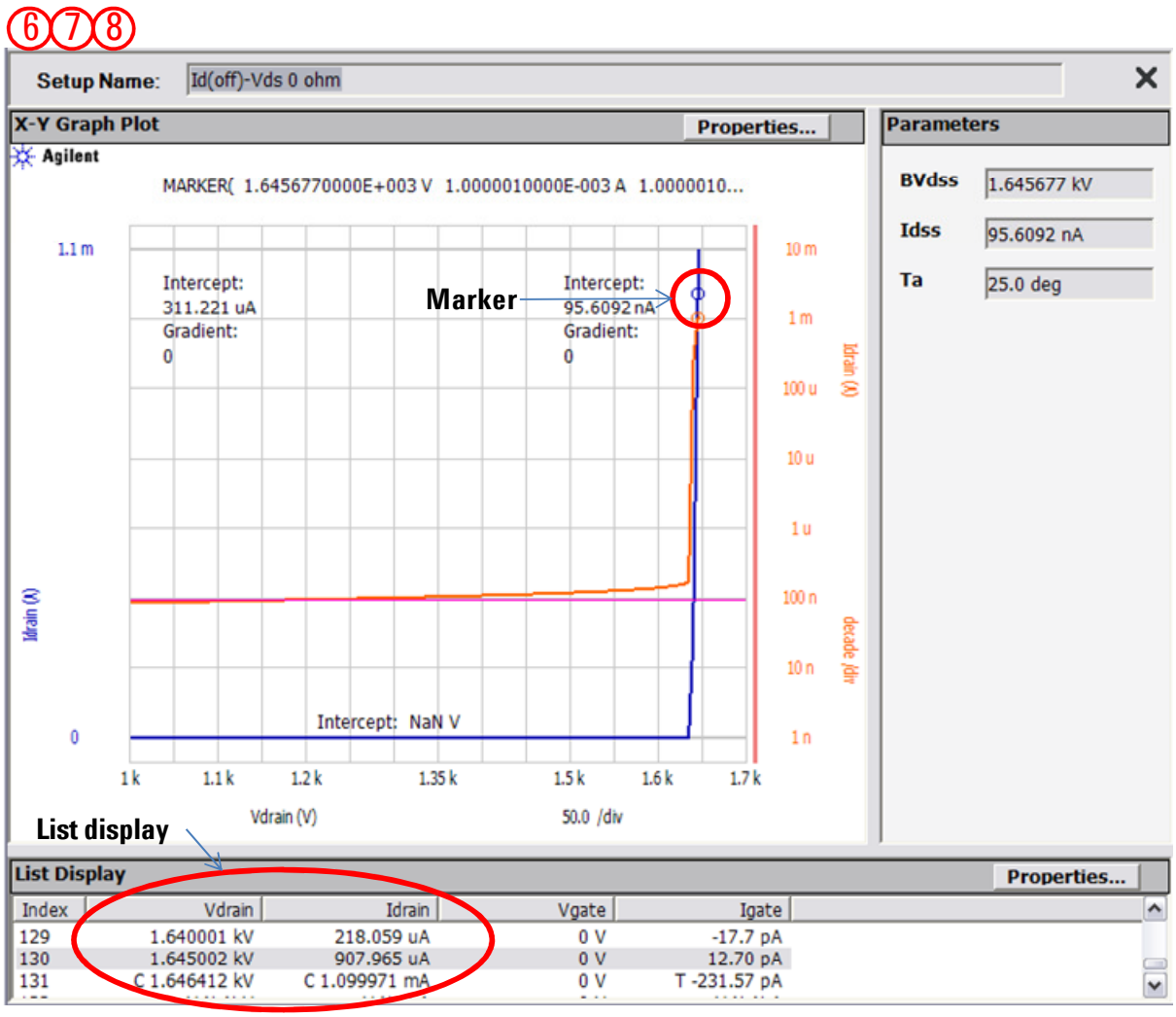


Figure 3-54. Idss and BVdss breakdown test without 100 kΩ.

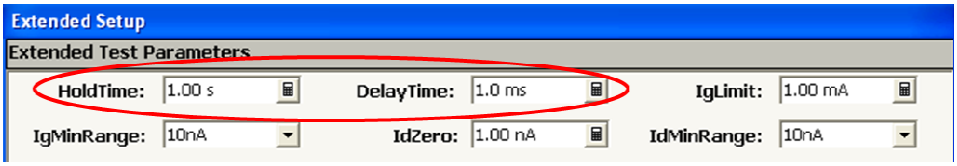


Figure 3-55. HoldTime and DelayTime setup.

A`. Measurement Procedure: Id(off)-Vds R Application Test without 100 kΩ resistor

- Starting from pre-defined test setup of My favorite Setup

This test approach starts measurements by using a pre-defined test setup saved in My favorite Setup instead of starting from a scratch by using an Application Test Library.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-53.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_AT preset group.

Step 3. Select Id(off)-Vds R (Click the Id(off)-Vds R).

Step 4. Click "Recall" button.

Next step: Go to step 5 of "Starting from Application Test Library" above, and continue by following the test step numbers.

B. Measurement Procedure: Id(off)-Vds R Application Test with 100 kΩ resistor

Connection inside the N1259A Test Fixture (with 100 kΩ protective R)

Open the N1259A test fixture cover, and connect the test leads by following the step numbers as shown in figure 3-56. The numbers of the procedure steps correspond to the numbers on the drawing for connecting the test leads.

[PROCEDURE]

Step 1 to Step 6: These steps are the same as the steps of figure 3-52 or previous section A. Please refer to these information or just change the leads in the following step 7 and 8.

Step 7. Connect the Force of the HVSMU1 to the terminal 2 of the N1279A Opt.022 (100 kΩ).

Step 8. Connect from the terminal 1 of the N1279A Opt.022 (100 kΩ) to terminal 2 Force (Drain) on the Inline Package Socket.

Close the N1259A fixture cover.

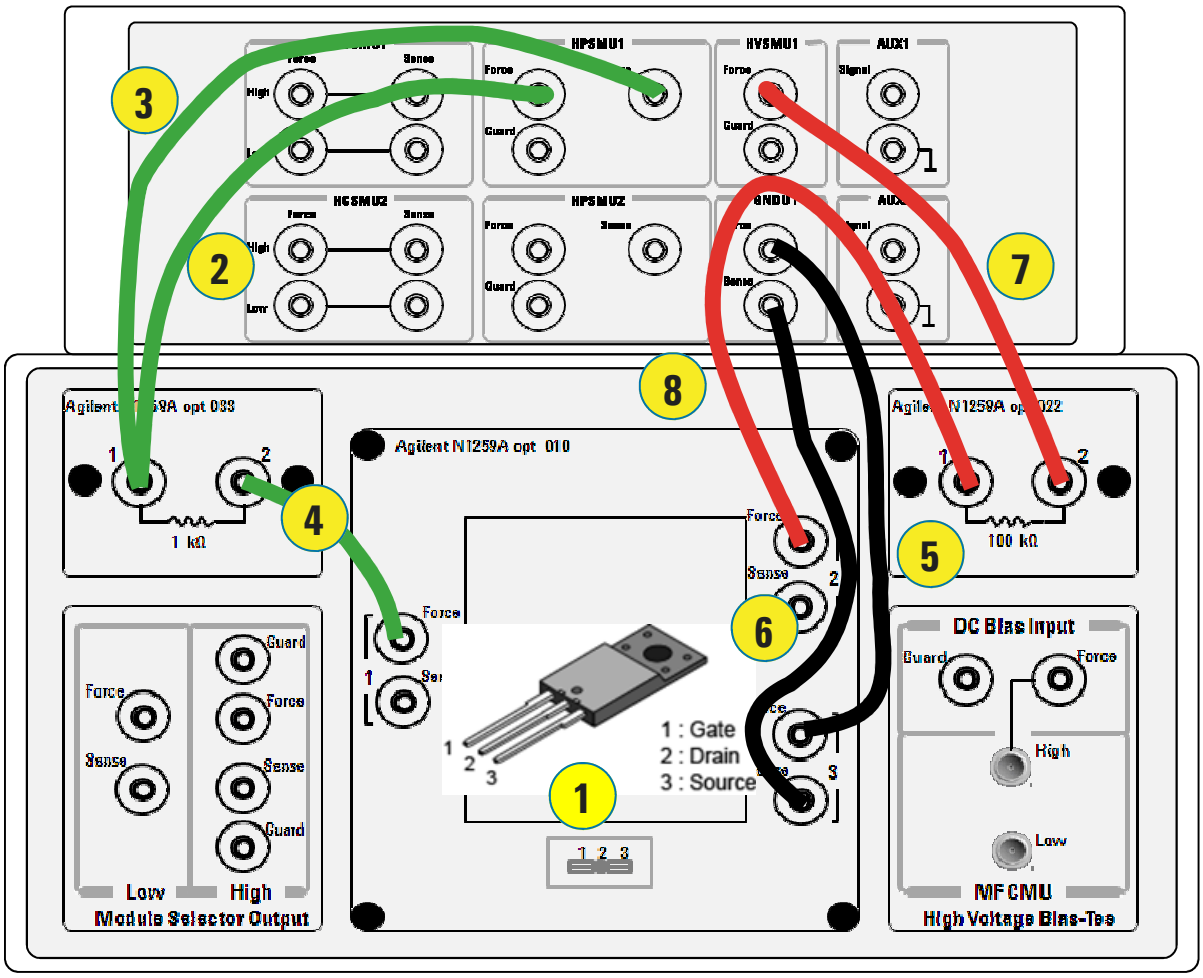


Figure 3-56. Connection between the SMUs and the power MOS-FET fixture with 100 kΩ.

NOTE: If Measurement is made with Opt.300 Module Selector, use the process shown in appendix A2-3-1.

In addition check ***"Enable Series Resistor"*** *checkbox of figure A2-5 in appendix section.*
Please make sure to ***uncheck this checkbox just after the end of this test*** *to prevent leaving the 100 kΩ resistor in the test configuration.*

-Starting from Application Test Library

This test approach starts measurements by using an Application Test Library which starts from the default setup parameters and you have to customize the measurement parameters depending on your requirements.

All the test setup steps are the same as in the previous section A or in figure 3-53 except for only one setup step 5-f as shown in figure 3-57.

Here, we start from step 5;

Step 5. Set the test parameters shown in figure 3-57 to an appropriate one depending on your B1505A configuration and your test device.

The important check points are;

a. Gate SMU setup

b. Set Vg constant parameter, typically 0 V.

c. Drain SMU setup. Choose HVSMU.

d. Set Vd sweep condition.

Start voltage is better to choose closer voltage of Idss specified voltage for speeding the test.

Stop voltage is chosen higher than Vdss.

Id limit is set slightly higher than the Idss specification.

The decision of Vdstep is a compromise between the sweep speed and the Vdss detection accuracy when series R for drain is not used.

e. Set the Vd@Idss that defines the drain voltage to measure Idss and Id@Vdss that defines the drain current to measure the drain breakdown voltage.

If the drain step voltage is too large and there is no 100 kΩ series resistor is not inserted, Vdss measurement accuracy would be degraded.

f. Set Drain R value depending on your actual configuration. In the example select "100 kΩ".

Step 6. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.

Close the lid of N1259A test fixture.

Start the measurement. (Click the Single button )

Step 7. The graph window pops up and the measurement starts with red Shock hazard indicator.

If interlock is not closed, i.e. the fixture cover is not closed firmly down to the fixture, then the measurement won`t start with a warning message.

In this case, make sure the interlock cable is connected and the fixture cover is closed, and repeat Step 6.

Step 8. You can see the Id-Vds curve with extracted Idss and BVdss in figure 3-58.

Figure 3-58 plots linear drain current Idrain in Y1 axis and log Idrain in Y2 axis versus drain voltage Vdrain in X axis. Horizontal line is drawn at Idss and Marker is automatically located to the BVgss point using the interpolation method.

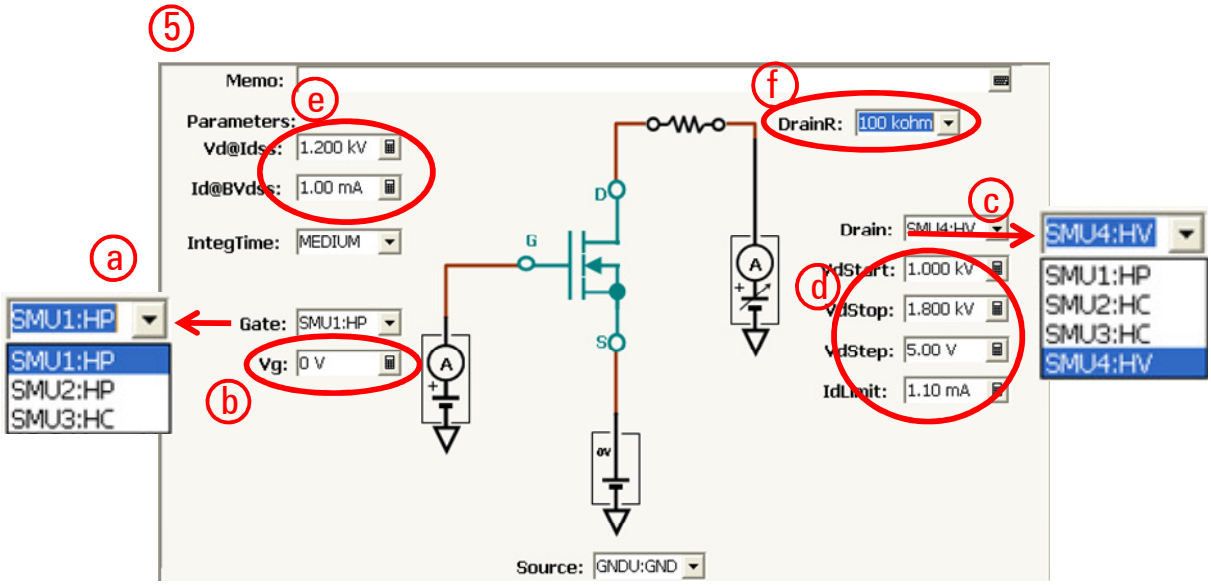


Figure 3-57. Id(off)-Vds R Application Test setup with 100 kΩ drain R.

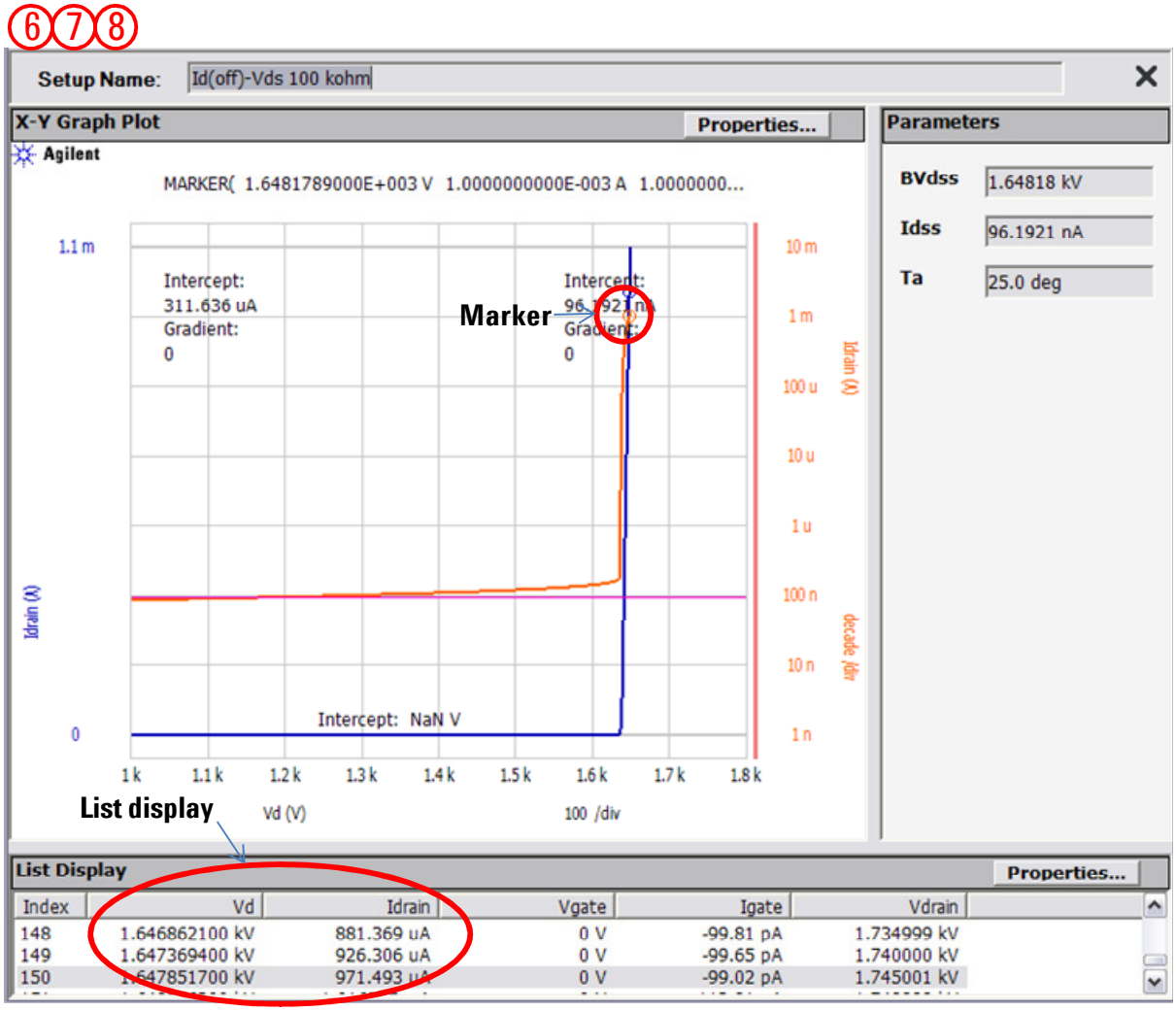


Figure 3-58. Idss and BVdss breakdown test with 100 kΩ.

Review:

The extracted results agree to the 2SK2745LS specification. Bvdss is 1,648 V that is slightly higher than the result in previous section A, though it is larger than 1.5 kV specification and Idss is 88 nA which is the same as previous section A and much lower than the specification.

Figure 3-59 shows the difference of the breakdown area by superimposing two graphs, and the difference may come from the error of the 100 kΩ resistor where about 100 V voltage drop exists at 1 mA drain current.

By inserting a 100 kΩ resistor, the number of measurement points in the breakdown area increases compared to the case without 100 kΩ resistor, but adds an additional insignificant error. If you have any concern for damaging your device by unexpected breakdown or oscillation, using a 100 kΩ resistor is not any problem.

Tips:

Properly setting the HoldTime and DelayTime in Extended setup shown in figure 3-55 is important for accurate measurement of Idss. If your first Vdrain step is large, then adding an extra HoldTime for waiting the drain voltage to settle is important for accurate measurement. DelayTime is a wait time before measuring each drain voltage step, and adding a proper wait time is important.

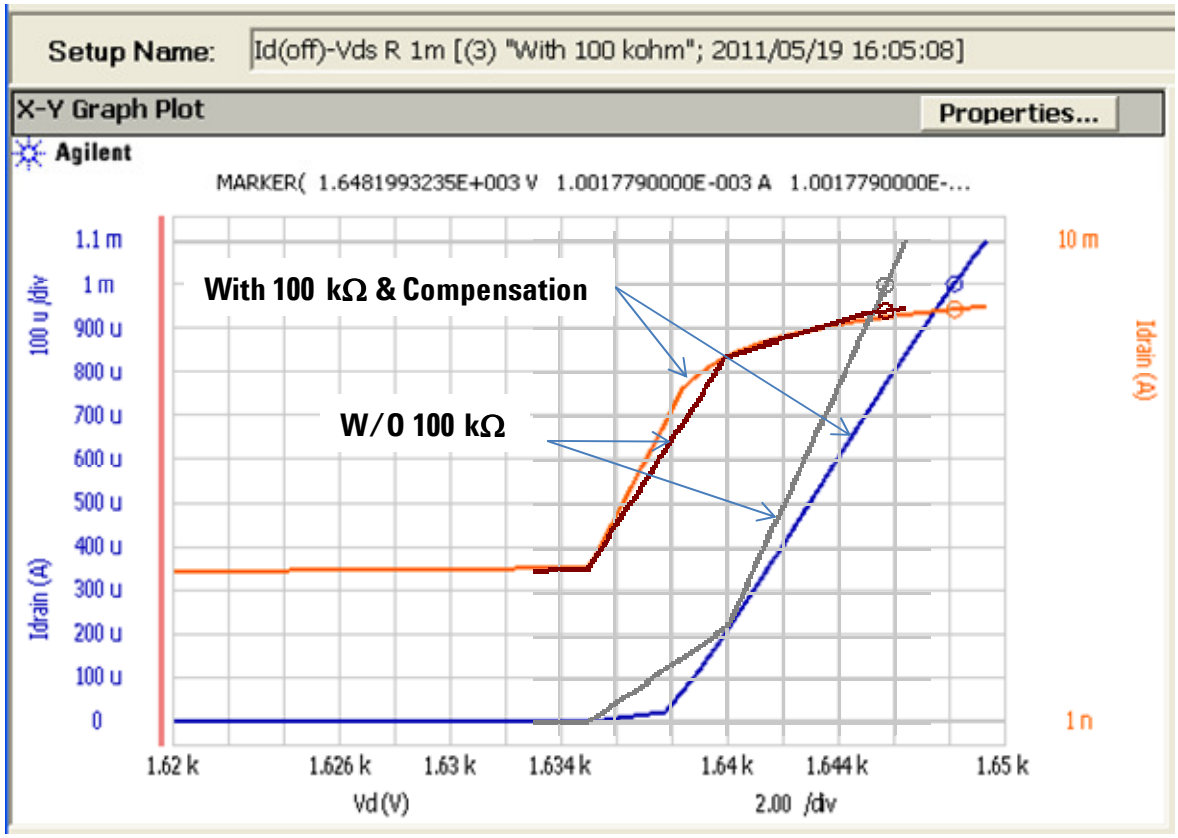


Figure 3-59. Difference of with/without 100 kΩ resistor.

3-3-2. IDSS measurements using Classic Test

Measurement parameters: IDSS Drain-to-Source Leakage Current

Classic Test setup name (My Favorite Setup -> Example_CT): Idss-Vds CT

Device used in the example: 2SK3745LS

Connection inside the N1259A Test Fixture: Use Section 3-3-1 A without 100 kΩ, Figure 3-52
NOTE: If Measurement is made with Opt.300 Module Selector, use the process shown in appendix A2-3-1.

Application description:

Measures and plots Drain current vs. Drain voltage characteristics in the cutoff region, and extracts the cutoff current, Zero-Gate voltage Drain Current - Idss.

Basically Idss and Vdss measurements require different test approach.

In Classic test approach, Idss test uses V-Force and I-Measure method that is the same as the previous Application Test.

A. Measurement Procedure: Idss-Vds CT Classic Test

This test sweeps drain current instead of drain voltage for detecting the steep drain breakdown characteristics.

Refer to figure 3-60 for the following Step 1 to Step 16.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_CT preset group.

Step 3. Select Idss-Vds CT.

Step 4. Press Recall button.

Step 5. Pre-defined example Idss-Vds CT classic test setup – Channel Definition page opens.

Channel Definition page setups the SMUs and its measurement function.

Step 6. Set Unit field appropriately depending on your B1505A and connection set-ups.

The connection between the SMU definitions and the power MOS_FET pins must be matched to each other.

Step 7. Press Measurement Setup tab.
You can change measurement parameters in this page.

Step 8. VAR1 or primary sweep parameters: VDS is set for measuring IDSS.
Enter V-start, V-stop and I-compliance value. Set V-stop larger or at least equal to the VDS for measuring Idss. Set I-compliance larger or at least equal to the IDSS maximum specification value.

Step9. No. of Step:

Note: Example is 5. Refer to Tips of this measurement.

Step 10. VGS constant voltage and current compliance can be set.

Step 11. Hold and Delay time can be set. 10 ms hold time would be enough in most cases, except if the drain capacitance is larger than 1 nF or swing voltage exceeds 2 kV.

Step 12. Pressing “ADC/Integ" button opens "A/D Converter & Integration Time Setup" sub-window.

Step 13. Integration time can be set. This test uses only High Speed ADC.

Step 14. Press Auto Analysis Setup tab.

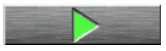
Step 15. Automatic Marker position can be set for detecting Idss. Set the drain voltage to measure Idss.

Step 16. Press Display Setup tab.

You can set the X-Y Graph, List Display and the Parameters of the measurement results in this page.

Step 17. The X, Y1, Y2 and so on to maximum Y8 axis can be defined as X-Y graph display.
Log or Linear scale and the Min. and the Max. scale parameters are set.
In the example both Linear ID and Log ID are set for displaying a wide range of current.

Step 18. List Display sets the measurement parameters that are shown in the List area of Display Graph window.

Step 19. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

Step 20. The graph window pops up and the measurement starts.

Step 21. You can see the ID-VDS curve and the extracted Idss in figure 3-61.

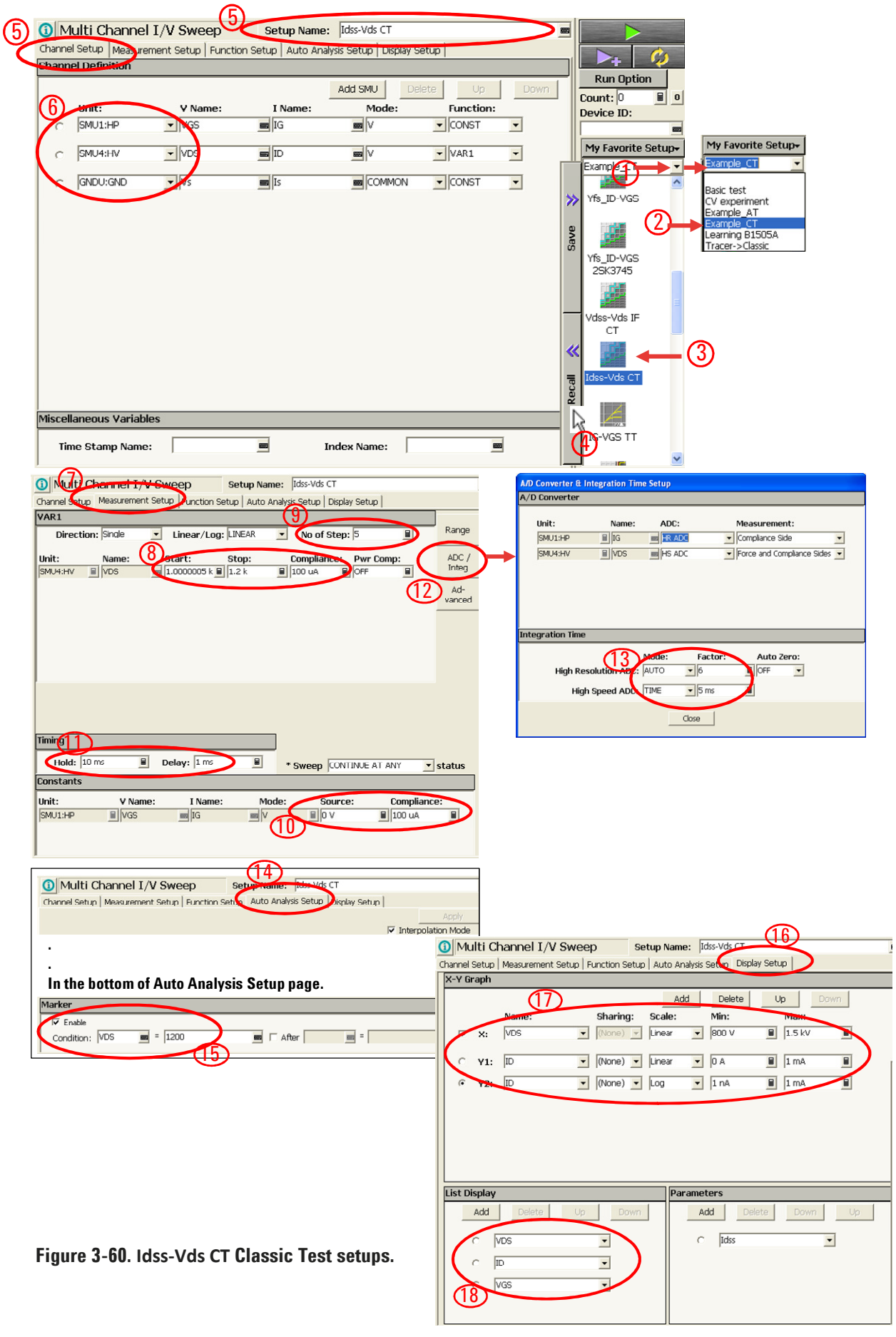


Figure 3-60. Idss-Vds CT Classic Test setups.

20 21

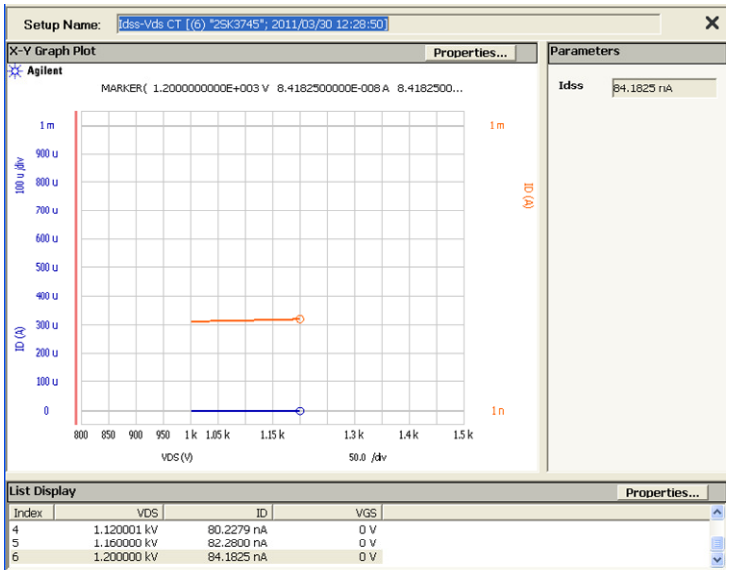


Figure 3-61. ID-VGS curve and the extracted Idss.

Review:

The measured Idss is 84 nA and it is almost same as the previous section 3-3-1 data. Data sheet specification is 100 μA, and the actual value is about 1/1000.

Tips:

In Step 9, “No of Step” is set to 5, but you can reduce the measurement points to just one point, start and stop the same value with step number as 1 since this test just measures Idss.

3-3-3. V(BR)DSS measurements using Classic Test

Measurement parameters: V(BR)DSS, VDSS Drain-to-Source Breakdown Voltage

Classic Test setup name (My Favorite Setup -> Example_CT): Vdss-Vds IF CT (Vdss -Vds I Force Classic Test)

Device used in the example: 2SK3745LS

Connection inside the N1259A Test Fixture: Use Section 3-3-1 A without 100 kΩ, Figure 3-52.

NOTE: If Measurement is made with Opt.300 Module Selector, use the process shown in appendix A2-3-1.

Application description:

Measures and plots Drain current vs. Drain voltage characteristics in breakdown region, and extracts the breakdown voltage.

This test approach is different from the previous Application Test where drain voltage is swept for the measurement.

This test forces drain current and measures drain breakdown voltage. The test method is suitable for detecting steep drain breakdown characteristics by directly forcing a few current steps. The measurement is accurate and the test speed is fast.

A. Measurement Procedure: Vdss-Vds IF (I Force) CT Classic Test

Refer to figure 3-62 for the following Step 1 to Step 16.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_CT preset group.

Step 3. Select Vdss-Vds IF CT (Vdss-Vds I Force).

Step 4. Press Recall button.

Step 5. Pre-defined example Vdss-Vds IF CT classic test setup – Channel Definition page opens.

Channel Definition page setups the SMUs and its measurement function.

Step 6. Set Unit field appropriately depending on your B1505A and connection setups.

The connection between the SMU definitions and the power MOS_FET pins must be matched to each other.

Please note that SMU4:HV is set I mode for VAR1.

Step 7. Press Measurement Setup tab.

You can change measurement parameters in this page.

Step 8. VAR1 or primary sweep parameters: ID is set for forcing start-I, Stop-I and V-compliance for measuring Vdss.

Set Stop-I to equal to or larger than the drain current specified to detect the drain breakdown. Set V-compliance larger than expected breakdown voltage.

Step 9. No of Step: Since this test just measures IDSS, you can set just two points, start and stop the same value with step number as 1 (Note: example is 5). In this case, please set enough delay time as shown in step 11.

Step 10. VGS constant voltage and current compliance can be set.

Step 11. Hold and Delay time can be set. 10 ms hold time would be enough in most of the case except the drain capacitance is larger than 1 nF or swing voltage exceeds 2 kV.

Step 12. Pressing “ADC/Integ" button opens "A/D Converter & Integration Time Setup" sub-window.

Step 13. Integration time can be set. This test uses only High Speed ADC.

Step 14. Press Auto Analysis Setup tab.

Step 15. Automatic Marker position can be set for detecting BVdss. Set the drain current specification to measure BVdss.

Step 16. Press Display Setup tab.

You can set the X-Y Graph, List Display and the Parameters of the measurement results in this page.

Step 17. The X, Y1, Y2 and so on to maximum Y8 axis can be defined as X-Y graph display.
Log or Linear scale and the Min. and the Max. scale parameters are set.
In the example both Linear ID and Log ID are set for displaying a wide range of current.

Step 18. List Display sets the measurement parameters that are shown in the List area of Display Graph window.

Step 19. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

Step 20. The graph window pops up and the measurement starts.

Step 21. You can see the ID-VDS curve and the extracted VBdss in figure 3-63.

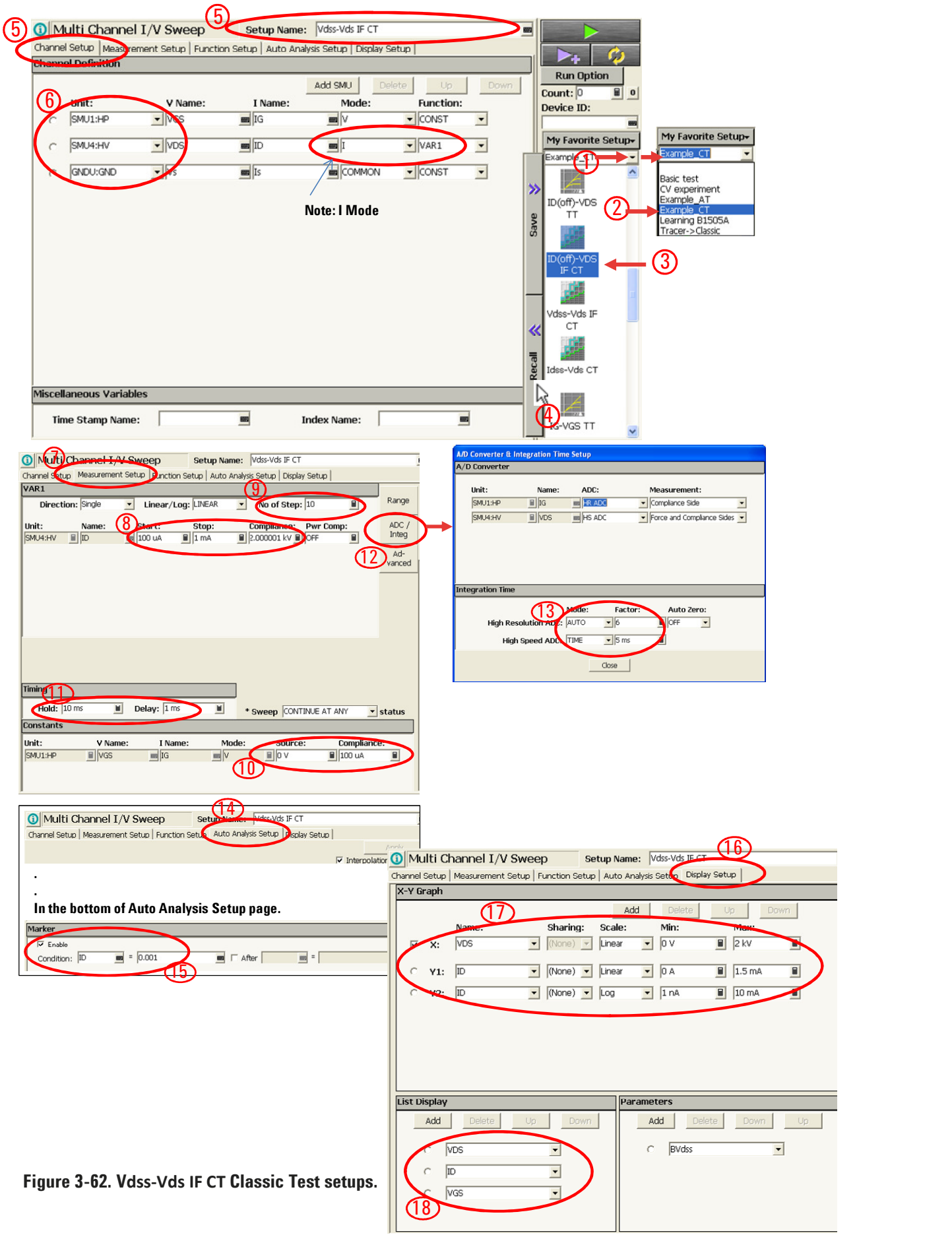


Figure 3-62. Vdss-Vds IF CT Classic Test setups.

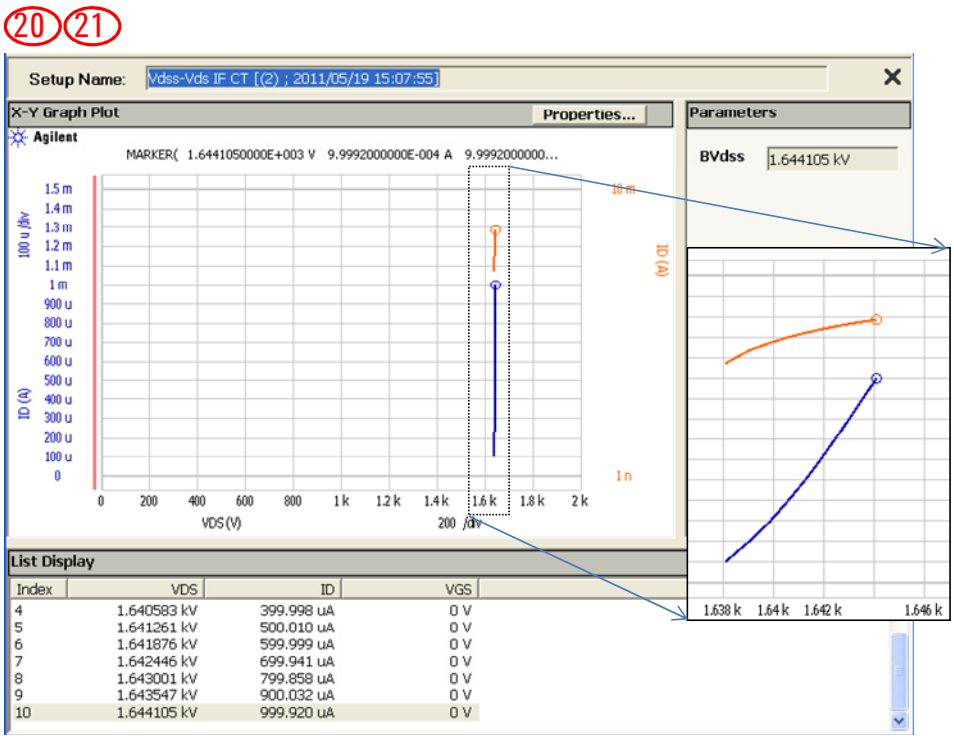


Figure 3-63. Breakdown ID-VGS curve and the extracted BVdss.

Review:

The measured BVdss is 1,644 V and it is almost the same as the previous section 3-3-1 data. Data sheet specification is minimum 1,500V at Id=1 mA, and the result agrees with the specification.

The magnified breakdown area in figure 3-63 indicates the voltage change from 100 μA to 1 mA is only 3 V. This means the Vd step voltage is necessary to sweep with at least 1 V step for detecting this breakdown behavior, and it takes a lot of time if you take the section 3-3-1 approach which sweeps drain voltage without 100 kΩ resistor. The current force approach is much easier, faster and accurate for measuring BVdss.

Tips:

1. In Step 9, Number of Step is set to 5, but you can reduce measurement points to just one point, start and stop the same value with step number as 1 since this test just measures Idss.

2. You can perform BVdss and Idss test at once by using Quick Test.

3. As we see, Classic Test requires more setup steps compared to the Application Test, but Classic Test has more freedom in changing the test setups such as the measurement functions, measurement parameters and display parameters and format by the expense of a little bit complicated setup steps and no fancy user interface GUI.

3-4. Capacitance Measurement group:

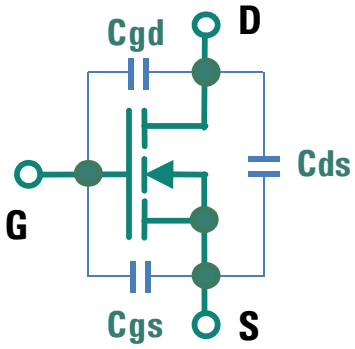
Next three capacitive components of the power MOS-FETs are typically listed in the power MOS-FET datasheet.

Crss Reverse Transfer capacitance
Coss Output capacitance
Ciss Input capacitance

Figure 3-64 shows the intrinsic capacitive components of power MOS-FET which are gate- Drain capacitor Cgd, drain-source capacitor Cds and gate-source capacitor Cgs.

Crss, Coss and Ciss capacitive components can be calculated by using Cgd, Cds and Cgs components as shown in the figure.

This section provides how to measure the intrinsic capacitive components of power MOS-FET (Cgd, Cds, and Cgs) and convert them to the datasheet expression (Crss, Coss, Ciss) or direct measurement if it can be performed easily without extra hard-ware.



MOS-FET parameters:
Coss: output capacitance
= Cds + Cgd
Ciss : input capacitance
= Cgs + Cgd
Crss : reverse transfer capacitance
= Cgd

Figure 3-64. Stray capacitances of MOS-FET and the MOS-FET parameters.

3-4-1. Cgd, Crss Capacitance measurement

Measurement parameters:
Cgd Gate-Source Capacitance
Crss Reverse Transfer Capacitance

Application Test name: Cgd

Application Test setup name (My Favorite Setup -> Example_AT): Cgd-Vd

Classic Test setup name (My Favorite Setup -> Example_CT): Cgd-Vd CT

Device used in the example: 2SK3745LS

Application description:

Measures Gate-Drain capacitance (Cgd), and plots Cgd-Vd characteristics. Cgd is the same as Crss.

Connection inside the N1259A Test Fixture

Open the N1259A test fixture cover, and connect the test leads, SHV cable and SHV-Banana Adaptor shown in figure 3-65 by following the step numbers shown in figure 3-66. The numbers of the procedure steps correspond to the numbers on the drawing for connecting the test leads and SHV cables.

Step 1. Insert the power MOS-FET (example: 2SK3745LS) into the socket on the N1259A. Make sure the device pin name matches the socket numbers shown in figure 3-66.

Step 2 Using test lead, connect the AUX2 outer shield (GND) to the terminal 3 Force (Source) of the Inline Package Socket.

Note: Connecting to GND is equivalent to connecting the MFCMU Low terminal guard (outer shield).

Step 3. Using test lead, connect the HVSMU1 Force to the DC Bias Input Force.

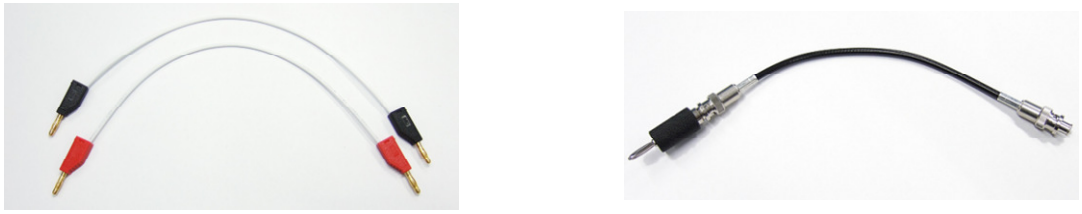
Step 4. Using test lead, connect the HVSMU1 Guard to the DC Bias Input Guard.

Step 5. Using a SHV cable and an adaptor, connect the MFCMU High output to the terminal 2 Force (Drain) of the Inline Package Socket.

Step 6. Using a SHV cable and an adaptor, connect the MFCMU Low output to the terminal 1 Force (Gate) of the Inline Package Socket.

Close the N1259A fixture cover.

NOTE: If Measurement is made with Opt.300 Module Selector, use the process shown in appendix A2-3-2, figure A2-7.



Test Lead

SHV cable and SHV-Banana Adaptor

Figure 3-65. Test Lead, SHV cable and SHV-Banana Adaptor for the N1259A Test Fixture.

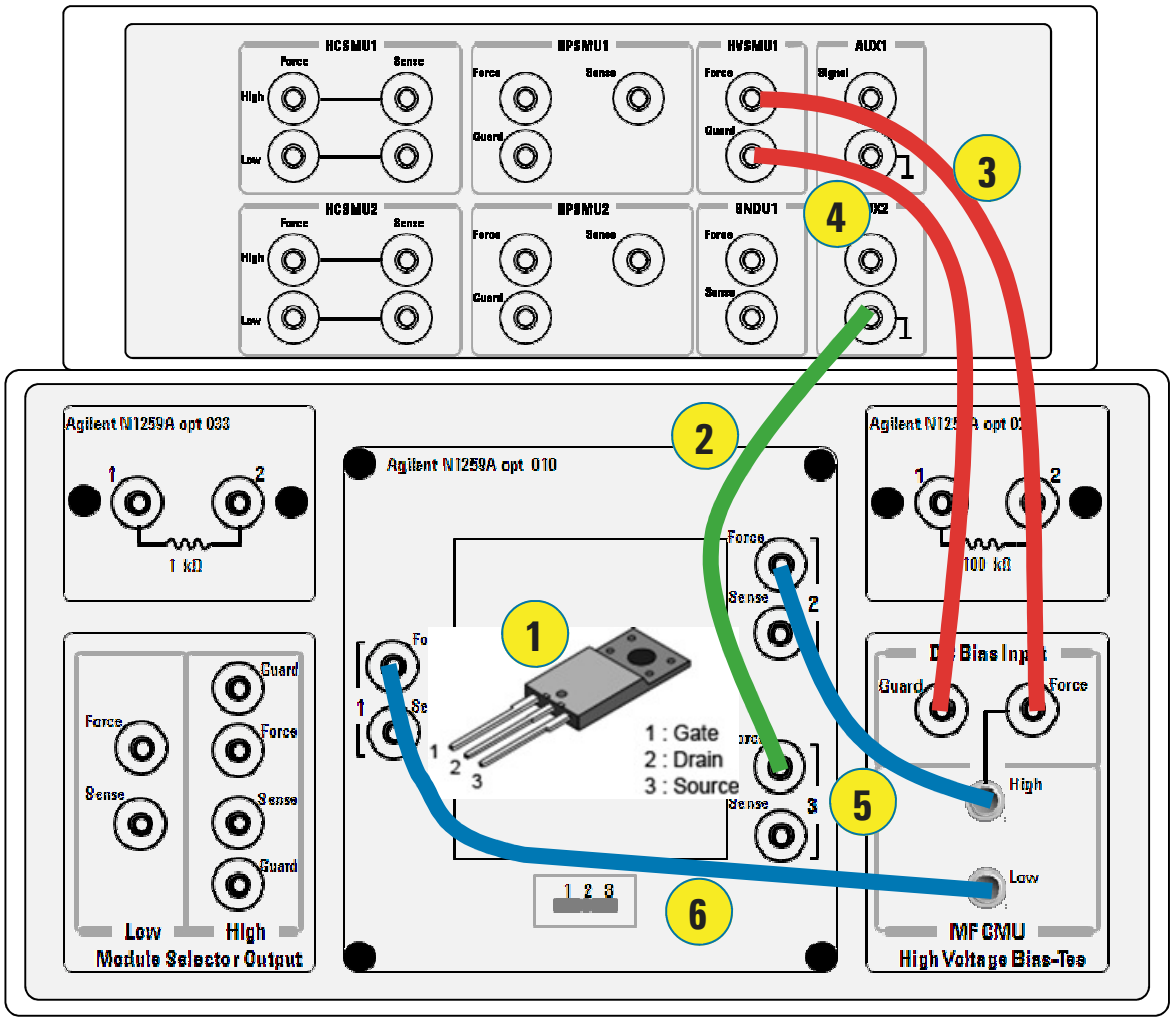


Figure 3-66. Connection for Cgd and Crss capacitance measurement.

A. Measurement Procedure: Cgd Application Test,

-Starting from Application Test Library

This test approach starts measurements by using an Application Test Library which starts from the default setup parameters and you have to customize the measurement parameters depending on your requirements.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-67.

Step 1. Click the Application Test tab.

Step 2. Check the "PowerMOSFET" application test category.

Step 3, 4. Select Cgd (Click the Cgd then click Select 

)

Step 5. Set the test parameters shown in figure 3-67 to an appropriate one depending on your B1505A configuration and your test device.

The important check points are;
a. Drain CMU setup (There should be no other selection, though!)
b. Set MFCMU DC bias HVSMU (VdBias) setup
c. Set Vd (Drain voltage) sweep parameters
d. Set MFCMU measurement parameters.
e. Set YaxisCgd minimum and maximum scale for log Cgd display.

Step 6. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

Step 7. The graph window pops up and the measurement starts.

Step 8. You can see the Cgd-Vdrain graph as shown in figure 3-68.

Figure 3-68 plots Cgd in Y axis versus drain voltage Vdrain in X axis.

Tips:
Marker can be used for reading each Cgd value and voltage by rotating the rotary knob. You can read between the two measurement points by activating Interpolation mode to ON status.

Review:

The Typical value of the Crss of 2SK3745LS is 40 pF at 30 V with 1 MHz measurement frequency.
The reading from the marker is 30.48pF. The measurement curve agrees with the datasheet measurement curve and overall measurement is okay.

1. Starting from Application Test Library

1`. Starting from My Favorite Setup

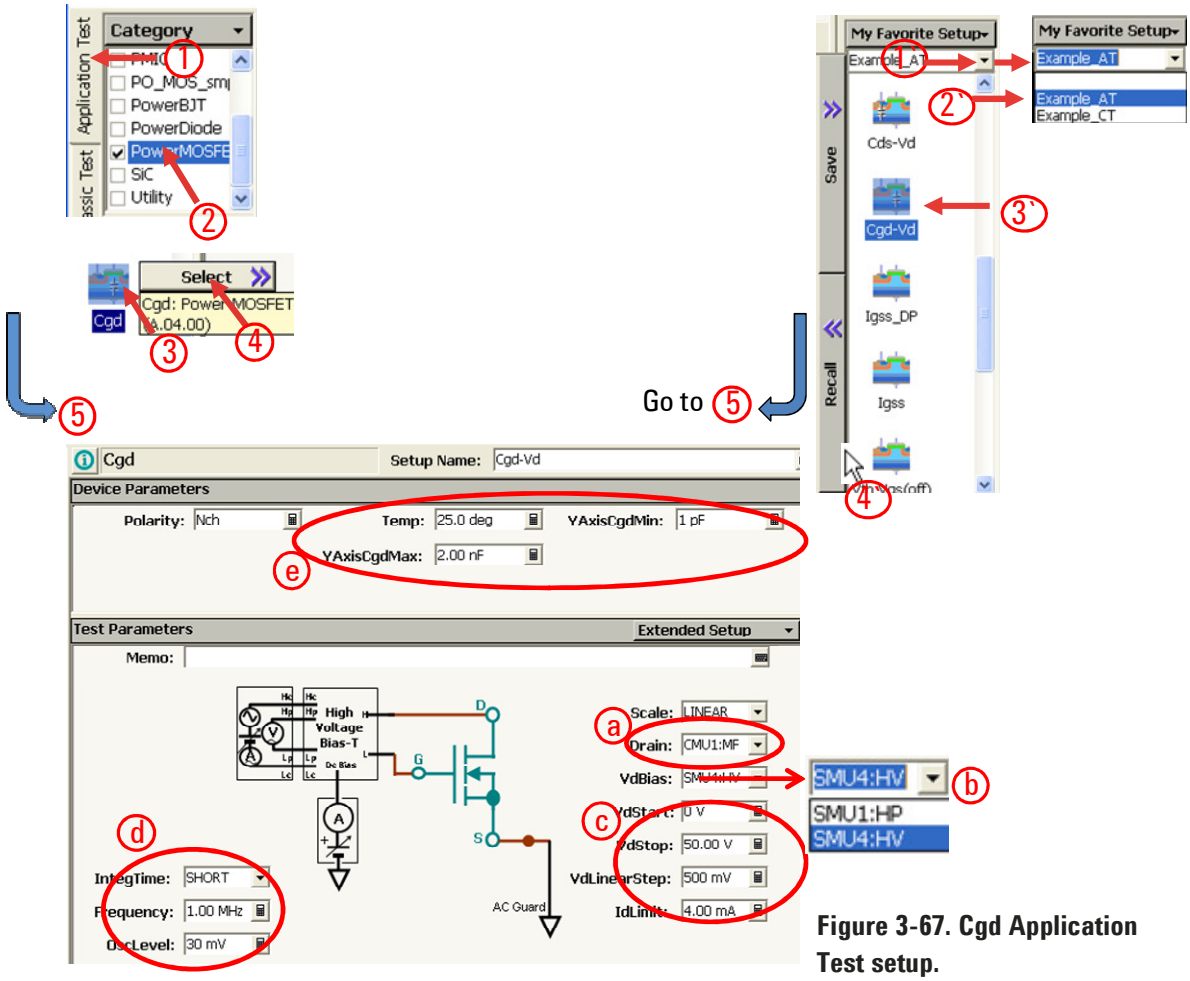


Figure 3-67. Cgd Application Test setup.

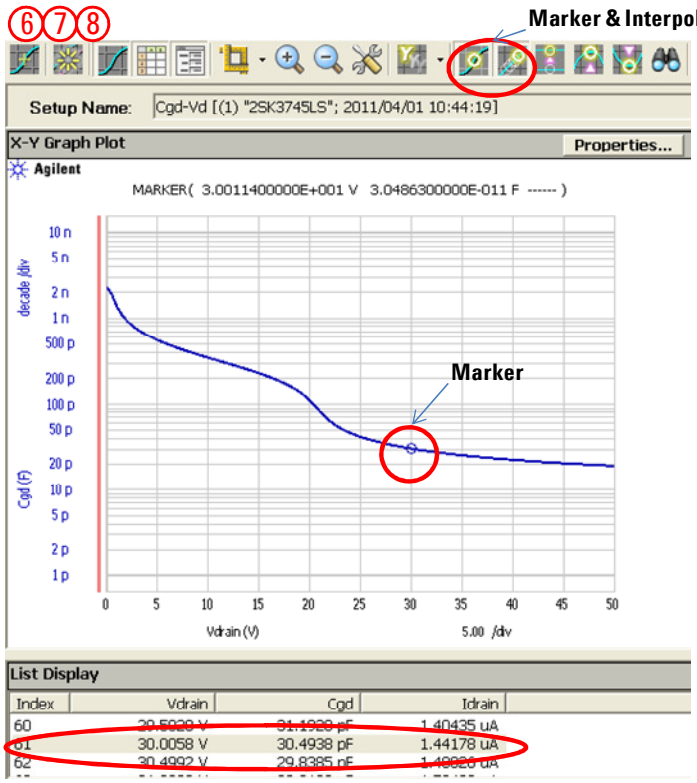


Figure 3-68. Cgd-Vds output from Cgd Application Test.

A`. Measurement Procedure: Cgd-Vd Application Test,

- Starting from pre-defined test setup of My Favorite Setup

This test approach starts measurements by using a pre-defined test setup saved in My Favorite Setup instead of starting from a scratch by using an Application Test Library.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-67.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_AT preset group.

Step 3. Select Cgd-Vd (Click Cgd-Vd).

Step 4. Click "Recall" button.

Then go to step 5 of "Starting from Application Test Library" above, and continue by following the test step numbers.

B. Measurement Procedure: Cgd-Vd CT Classic Test

Refer to figure 3-69 for the following Step 1 to Step 16.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_CT preset group.

Step 3. Select Cgd-Vd CT.

Step 4. Press Recall button.

Step 5. Pre-defined example Cgd-Vd CT classic test setup – Channel Definition page opens.

Step 6. Set Unit field appropriately depending on your B1505A and connection set-ups.

The connection between the SMU definitions and the power MOS_FET pins must be matched to each other.

Step 7. Press Measurement Setup tab.

You can change measurement parameters in this page.

Step 8. V Name field specifies the voltage source name. In this example, voltage source is the HVSMU defined in the Channel Definition.

Step 9. Set the sweep parameter.

Step 10. Set the measurement frequency of MFCMU.

Step 11. Set the AC test signal level of MFCMU.

Step 12. Hold and Delay time can be set.

Step 13. Integration time of MFCMU can be set.

Step 14. Press Display Setup tab.

You can set the X-Y Graph, List Display and the Parameters of the measurement results in this page.

Step 15. The X, Y1, Y2 and so on to maximum Y8 axis can be defined as X-Y graph display.
Log or Linear scale and the Min. and the Max. scale parameters are set.
In the CV measurement, typically log scale is used for capacitor display in Y axis.

Step 16. List Display sets the measurement parameters that are shown in the List area of Display Graph window.

Step 17. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

Step 18. The graph window pops up and the measurement starts.

Step 19. You can see the same graph shown in figure 3-68.

Note: Step 18 and 19 are the same as the step 7 and 8 of figure 3-68.

Tips:

Classic Test definition can change measurement parameters very easily.

Although this example does not include any automatic analysis functions, but you can add easily automatic marker that appears at 30 V specification point.

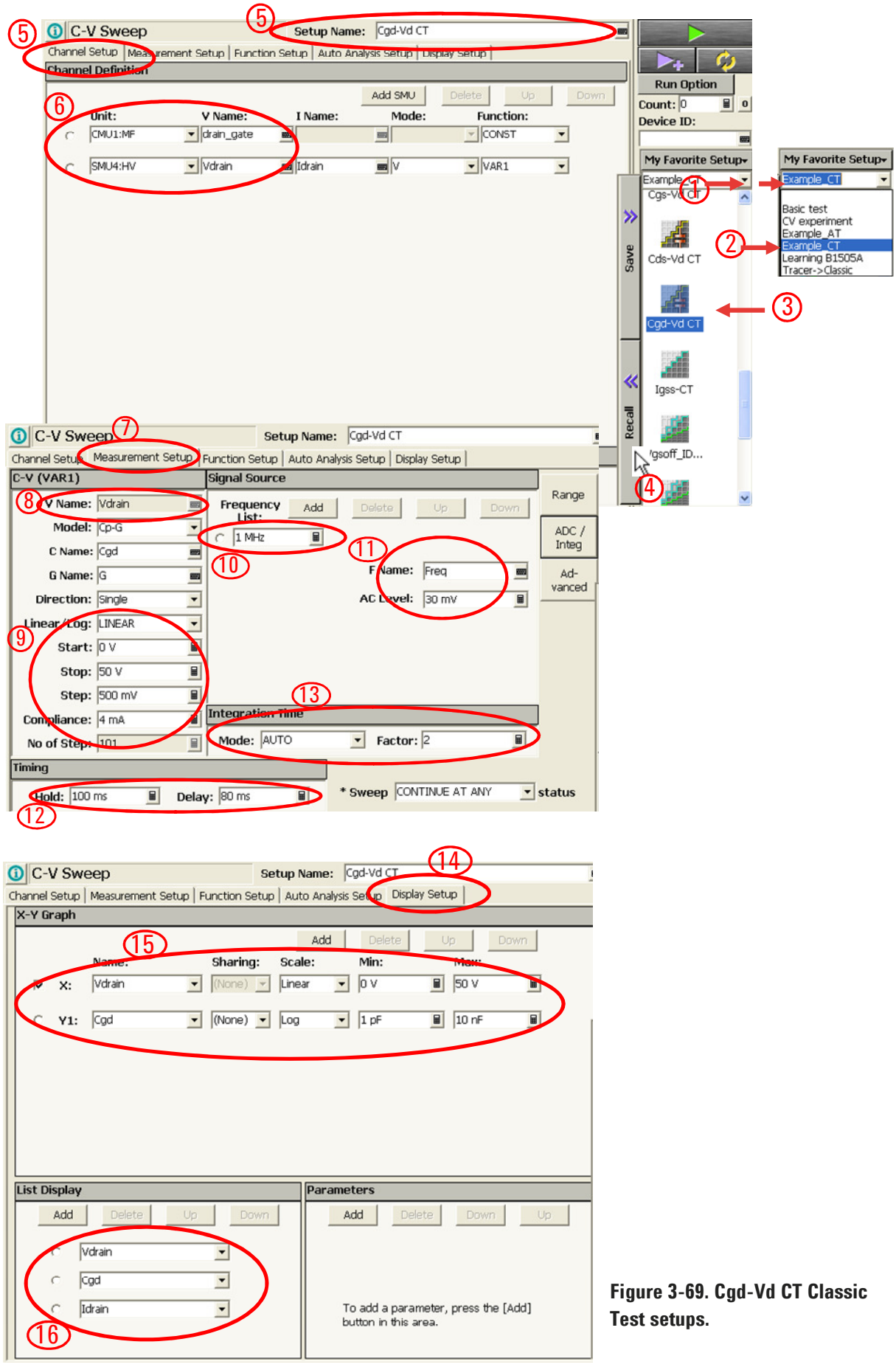


Figure 3-69. Cgd-Vd CT Classic Test setups.

3-4-2. Cds Capacitance measurement

Measurement parameters:
Cds Drain-Source Capacitance

Application Test name: Cds

Application Test setup name (My Favorite Setup -> Example_AT): Cds-Vd

Classic Test setup name (My Favorite Setup -> Example_CT): Cds-Vd CT

Device used in the example: 2SK3745LS

Application description:

Measures Drain-Source capacitance (Cds), and plots Cds-Vd characteristics.

Coss can be measured with the Cds application test by connecting both the gate and the source to MFCMU Low measurement terminal, or by adding Cds and Cgd.

Coss measurement is shown in section 3-4-3.

Connection inside the N1259A Test Fixture

Open the N1259A test fixture cover, and connect the test leads, SHV cable and SHV-Banana Adaptor shown in figure 3-65 by following the step numbers shown in figure 3-70. The numbers of the procedure steps correspond to the numbers on the drawing for connecting the test leads and SHV cables.

Step 1. Insert the power MOS-FET (example: 2SK3745LS) into the socket on the N1259A. Make sure the device pin name matches the socket numbers shown in figure 3-70.

Step 2. Using test lead, connect the AUX2 outer shield (GND) to the terminal 1 Force (gate) of the Inline Package Socket.

Note: Connecting to GND is equivalent to connecting the MFCMU Low terminal guard (outer shield).

Step 3. Using test lead, connect the HVSMU1 Force to the DC Bias Input Force.

Step 4. Using test lead, connect the HVSMU1 Guard to the DC Bias Input Guard.

Step 5. Using a SHV cable and an adaptor, connect the MFCMU High output to the terminal 2 Force (Drain) of the Inline Package Socket.

Step 6. Using a SHV cable and an adaptor, connect the MFCMU Low output to the terminal 3 Force (Source) of the Inline Package Socket.

Close the N1259A fixture cover.

NOTE: If Measurement is made with Opt.300 Module Selector, use the process shown in appendix A2-3-2, figure A2-8.

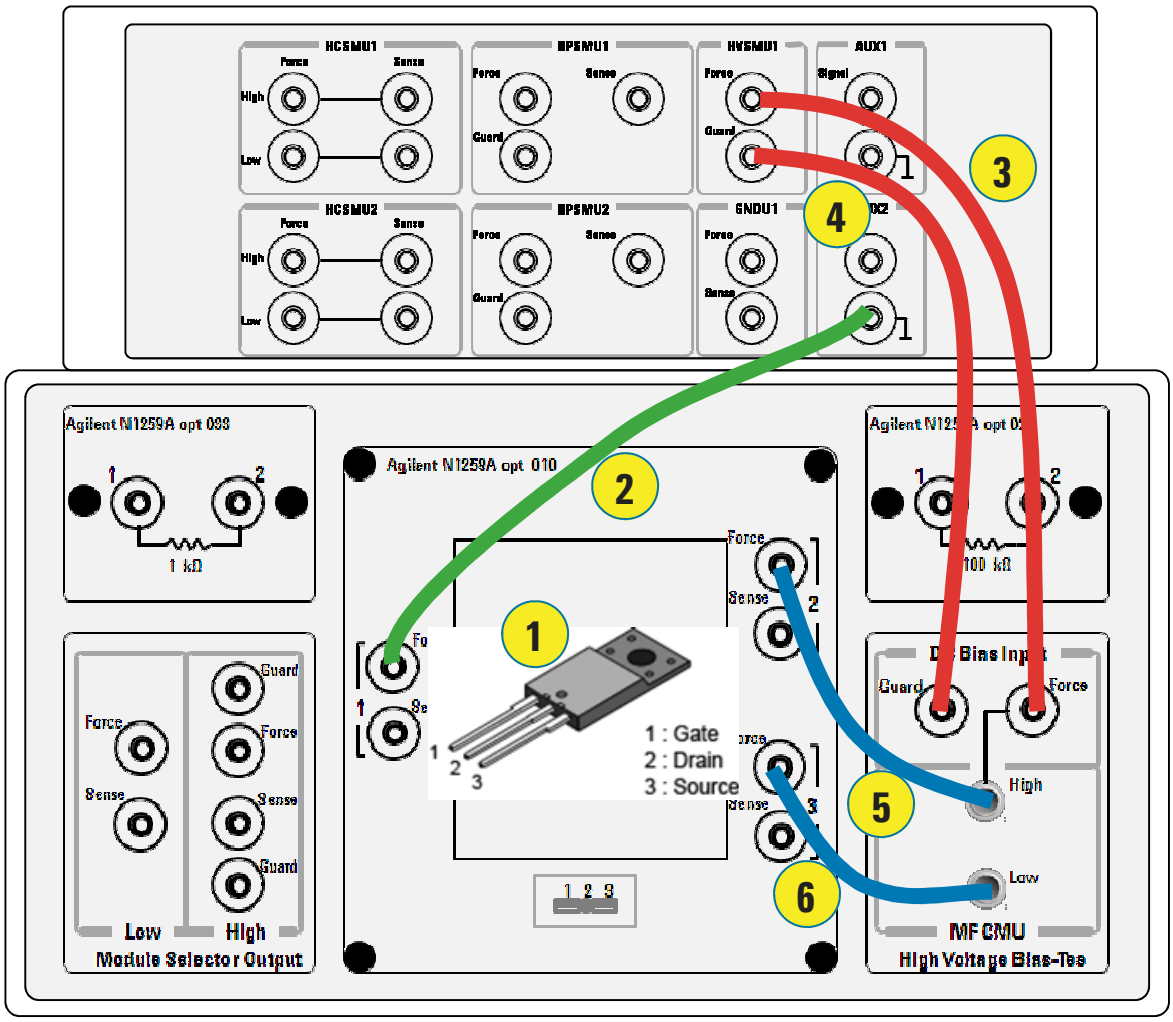


Figure 3-70. Connection for Cds capacitance measurement.

A. Measurement Procedure: Cds Application Test,

-Starting from Application Test Library

This test approach starts measurements by using an Application Test Library which starts from the default setup parameters and you have to customize the measurement parameters depending on your requirements.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-71.

Step 1. Click the Application Test tab.

Step 2. Check the "PowerMOSFET" application test category.

Step 3, 4. Select Cds (Click the Cds then click Select 

)

Step 5. Set the test parameters shown in figure 3-71 to an appropriate one depending on your B1505A configuration and your test device.
The important check points are;
a. Drain CMU setup (There should be no other selection, though!)
b. Set MFCMU DC bias HVSMU (VdBias) setup
c. Set Vd (Drain voltage) sweep parameters
d. Set MFCMU measurement parameters.
e. Set YaxisCds minimum and maximum scale for log Cds display.

Step 6. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

Step 7. The graph window pops up and the measurement starts.

Step 8. You can see the Cds-Vdrain graph as shown in figure 3-72.

Figure 3-72 plots Cds in Y axis versus drain voltage Vdrain in X axis.

Tips:
Marker can be used for reading each Cds value and voltage by rotating the rotary knob. You can read between the two measurement points by activating Interpolation mode to ON status.

Review:

There is no Cds specification in 2SK3745LS datasheet, and the Coss output capacitance has to be calculated by adding Cds and Cgd. Cds can be read 33.3 pF from the marker value or List Display of figure 3-72.
Cds + Cgs at 30 V drain bias in the example is 33.3 pF + 30.48 pF = 63.78 pF. Coss specification is 70 pF at 30 V with 1 MHz measurement frequency and it is okay.

1. Starting from Application Test Library

1`. Starting from My Favorite Setup

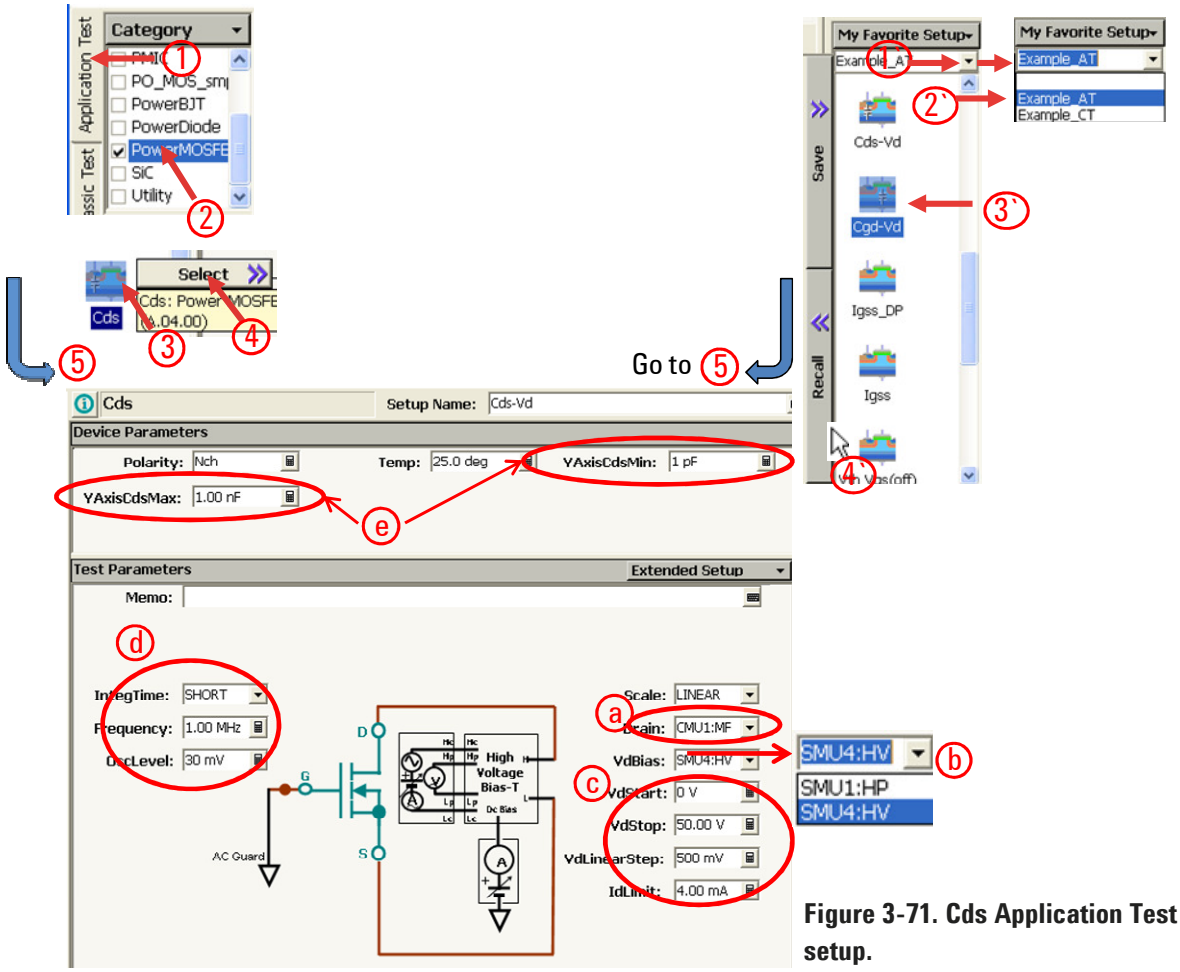


Figure 3-71. Cds Application Test setup.

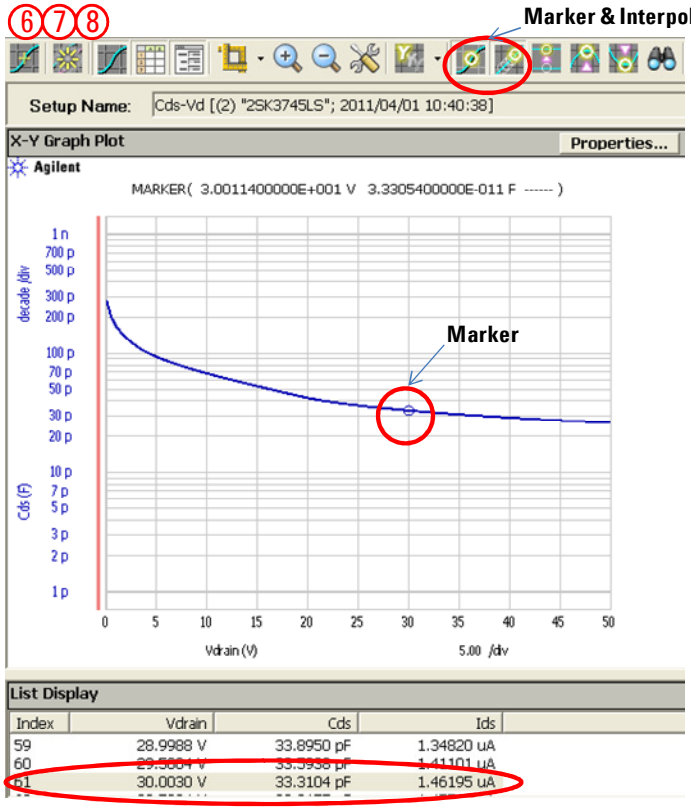


Figure 3-72. Cds-Vds output from Cds Application Test.

A`. Measurement Procedure: Cds Application Test,

- Starting from pre-defined test setup of My favorite Setup

This test approach starts measurements by using a pre-defined test setup saved in My favorite Setup instead of starting from a scratch by using an Application Test Library.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-71.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_AT preset group.

Step 3. Select Cds-Vd (Click Cds-Vd).

Step 4. Click "Recall" button.

Then go to step 5 of "Starting from Application Test Library" above, and continue by following the test step numbers.

B. Measurement Procedure: Cds-Vd CT Classic Test

Refer to figure 3-73 for the following Step 1 to Step 16.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_CT preset group.

Step 3. Select Cds-Vd CT.

Step 4. Press Recall button.

Step 5. Pre-defined example Cds-Vd CT classic test setup – Channel Definition page opens.

Step 6. Set Unit field appropriately depending on your B1505A and connection set-ups.

The connection between the SMU definitions and the power MOS_FET pins must be matched to each other.

Step 7. Press Measurement Setup tab.

You can change measurement parameters in this page.

Step 8. V Name field specifies the voltage source name. In this example, voltage source is the HVSMU defined in the Channel Definition.

Step 9. Set the sweep parameter.

Step 10. Set the measurement frequency of MFCMU.

Step 11. Set the AC test signal level of MFCMU.

Step 12. Hold and Delay time can be set.

Step 13. Integration time of MFCMU can be set.

Step 14. Press Display Setup tab.

You can set the X-Y Graph, List Display and the Parameters of the measurement results in this page.

Step 15. The X, Y1, Y2 and so on to maximum Y8 axis can be defined as X-Y graph display.
Log or Linear scale and the Min. and the Max. scale parameters are set.
In the CV measurement, typically log scale is used for capacitor display in Y axis.

Step 16. List Display sets the measurement parameters that are shown in the List area of Display Graph window.

Step 17. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

Step 18. The graph window pops up and the measurement starts.

Step 19. You can see the same graph shown in figure 3-72.

Note: Step 18 and 19 are the same as the step 7 and 8 of figure 3-72.

Tips:

Classic Test definition can change measurement parameters very easily.

Although this example does not include any automatic analysis functions, but you can add easily automatic marker that appears at 30 V specification point.

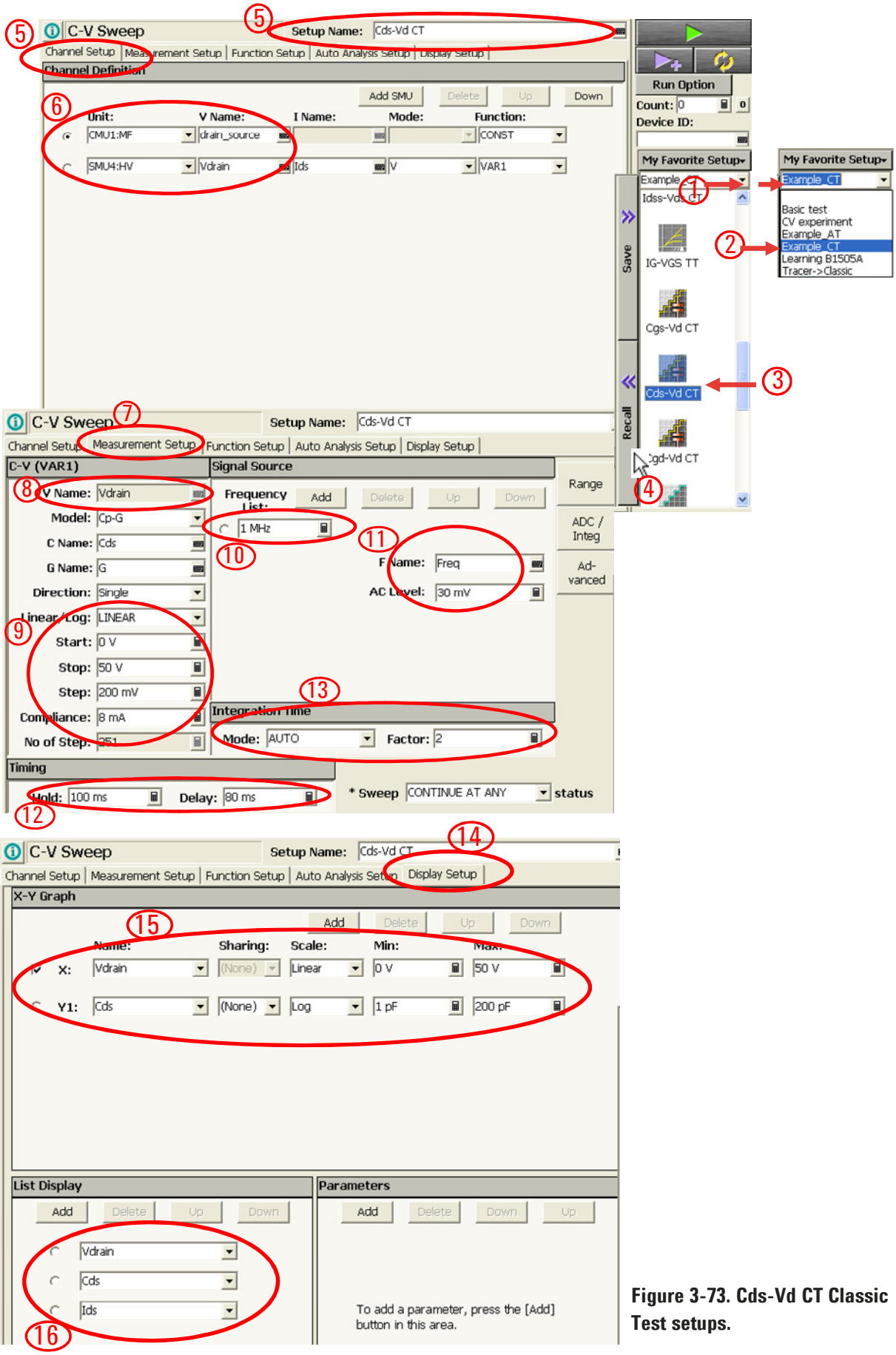


Figure 3-73. Cds-Vd CT Classic Test setups.

3-4-3. Coss Capacitance measurement

Measurement parameters:
Coss Output Capacitance

Application Test name: Cds

Application Test setup name (My Favorite Setup -> Example_AT): Coss-Vd

Classic Test setup name (My Favorite Setup -> Example_CT): Coss-Vd CT

Device used in the example: 2SK3745LS

Application description:

Measures Drain Output capacitance (Coss), and plots Coss-Vd characteristics.

Coss can be measured with the Cds application test by connecting both the gate and the source to MFCMU Low measurement terminal.
This section shows the Coss measurement example by using Coss-Vds My favorite Application test setup.

Connection inside the N1259A Test Fixture

Open the N1259A test fixture cover, and connect the test leads, SHV cable and SHV-Banana Adaptor shown in figure 3-65 by following the step numbers shown in figure 3-74. The numbers of the procedure steps correspond to the numbers on the drawing for connecting the test leads and SHV cables.

Step 1. Insert the power MOS-FET (example: 2SK3745LS) into the socket on the N1259A. Make sure the device pin name matches the socket numbers shown in figure 3-74.

Step 2. Using test lead, connect the terminal 3 Sense (Source) to the terminal 1 Force (gate) of the Inline Package Socket.

Step 3. Using test lead, connect the HVSMU1 Force to the DC Bias Input Force.

Step 4. Using test lead, connect the HVSMU1 Guard to the DC Bias Input Guard.

Step 5. Using a SHV cable and an adaptor, connect the MFCMU High output to the terminal 2 Force (Drain) of the Inline Package Socket.

Step 6. Using a SHV cable and an adaptor, connect the MFCMU Low output to the terminal 3 Force (Source) of the Inline Package Socket.

Close the N1259A fixture cover.

NOTE: If Measurement is made with Opt.300 Module Selector, use the process shown in appendix A2-3-2, figure A2-9.

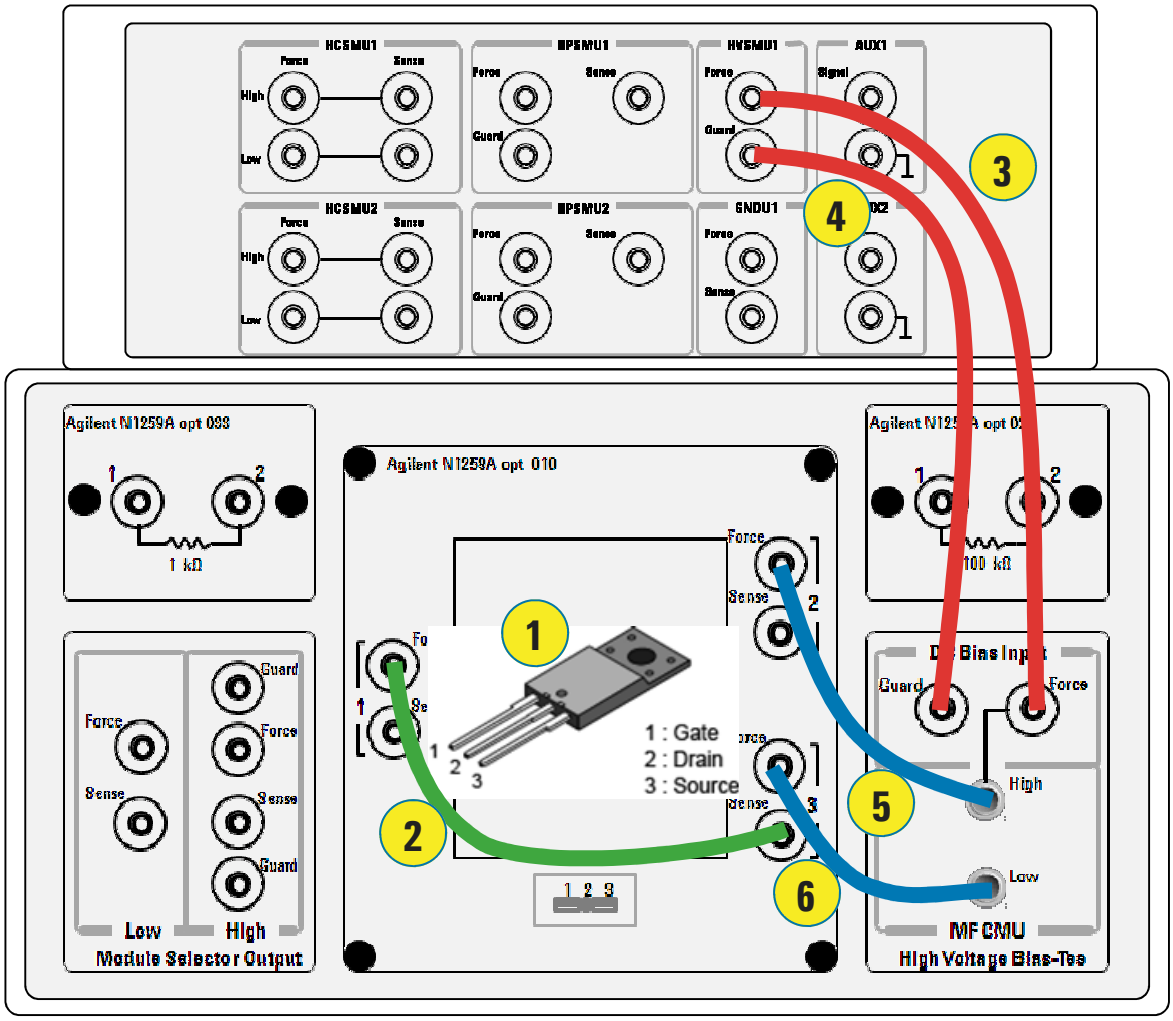


Figure 3-74. Connection for Coss capacitance measurement.

- Starting from pre-defined test setup of My favorite Setup

This test approach starts measurements by using a pre-defined test setup saved in My favorite Setup.
Note: There is no Coss Application Test Library.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-75.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_AT preset group.

Step 3. Select Coss-Vd (Click Coss-Vd).
Note that

Step 4. Click "Recall" button.
Coss setup is shown up. Please note that a memo instruction of connecting the gate to the source instead of guard is added because the graphic is different.

Step 5. Set the test parameters shown in figure 3-75 to an appropriate one depending on your B1505A configuration and your test device.
The important check points are;
a. Drain CMU setup (There should be no other selection, though!)
b. Set MFCMU DC bias HVSMU (VdBias) setup
c. Set Vd (Drain voltage) sweep parameters
d. Set MFCMU measurement parameters.
e. Set YaxisCgd minimum and maximum scale for log Cgd display.

Step 6. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

Step 7. The graph window pops up and the measurement starts.

Step 8. You can see the Coss-Vdrain graph as shown in figure 3-76.

Figure 3-76 plots Coss (Label is Cds, though) in Y axis versus drain voltage Vdrain in X axis.

Tips:

Step 9. Marker can be used for reading each drain current and voltage by rotating the rotary knob. You can read between the two measurement points by activating Interpolation mode to ON status.

Step 10. You can add Text comment to the Display X-Y Graph Plot as shown in figure 3-76.
In case of Application Test, it takes some effort and process for reflecting for minor changes as like scale name changes. In that case, Text comment is a convenient tool for leaving a memo to the result.

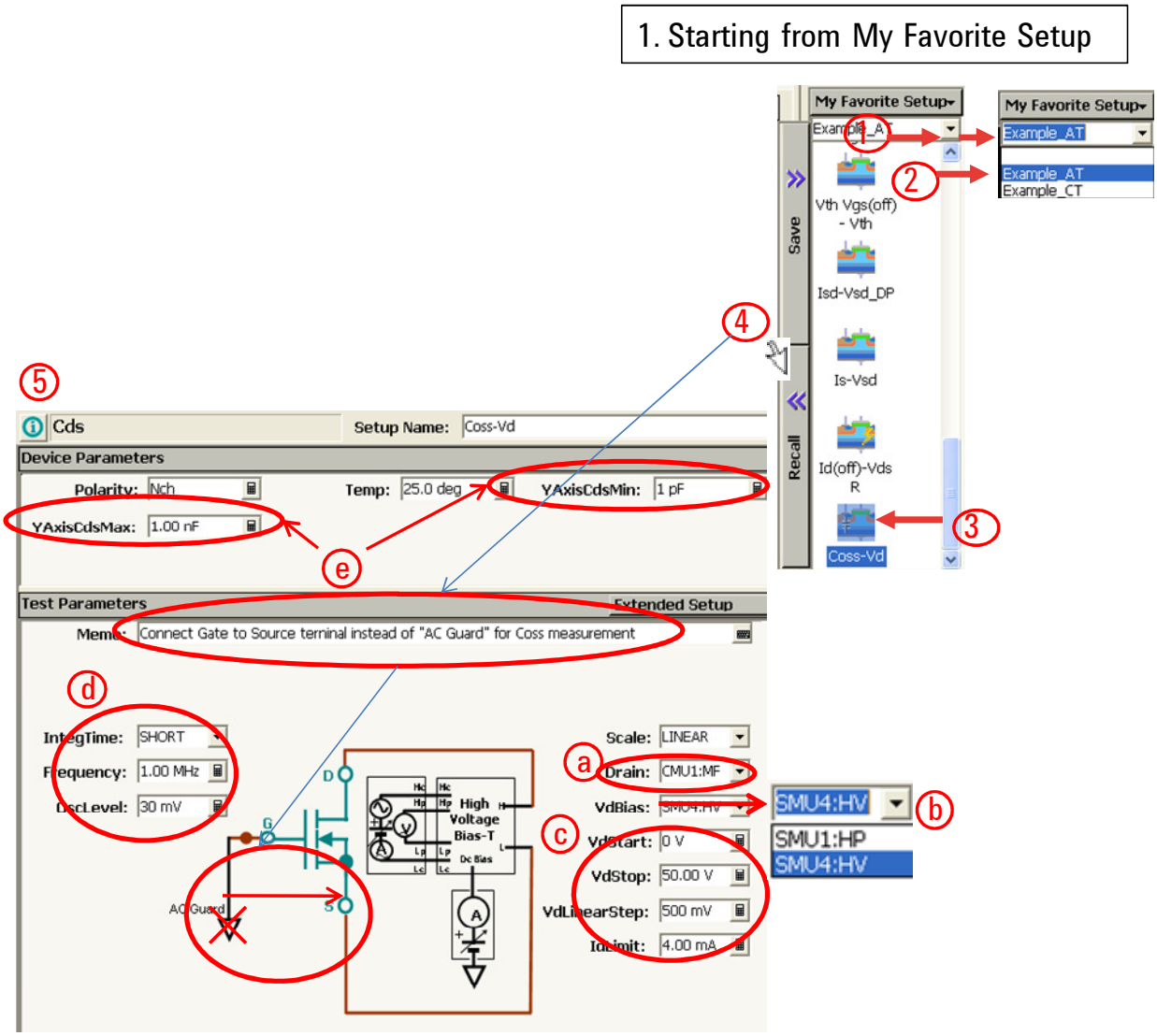


Figure 3-75. Coss-Vd Application Test setup.

Review:

Coss can be measured easily by using existing Application Test definition without modifying the original Cds Application Test definition.
The measured Coss is 63.7 pF at 30 V drain bias and 1 MHz measurement frequency.
The value is consistent with the addition of previous two test results;
Cds + Cgs at 30 V drain bias in previous measurements is 33.3 pF + 30.48 pF = 63.78 pF.

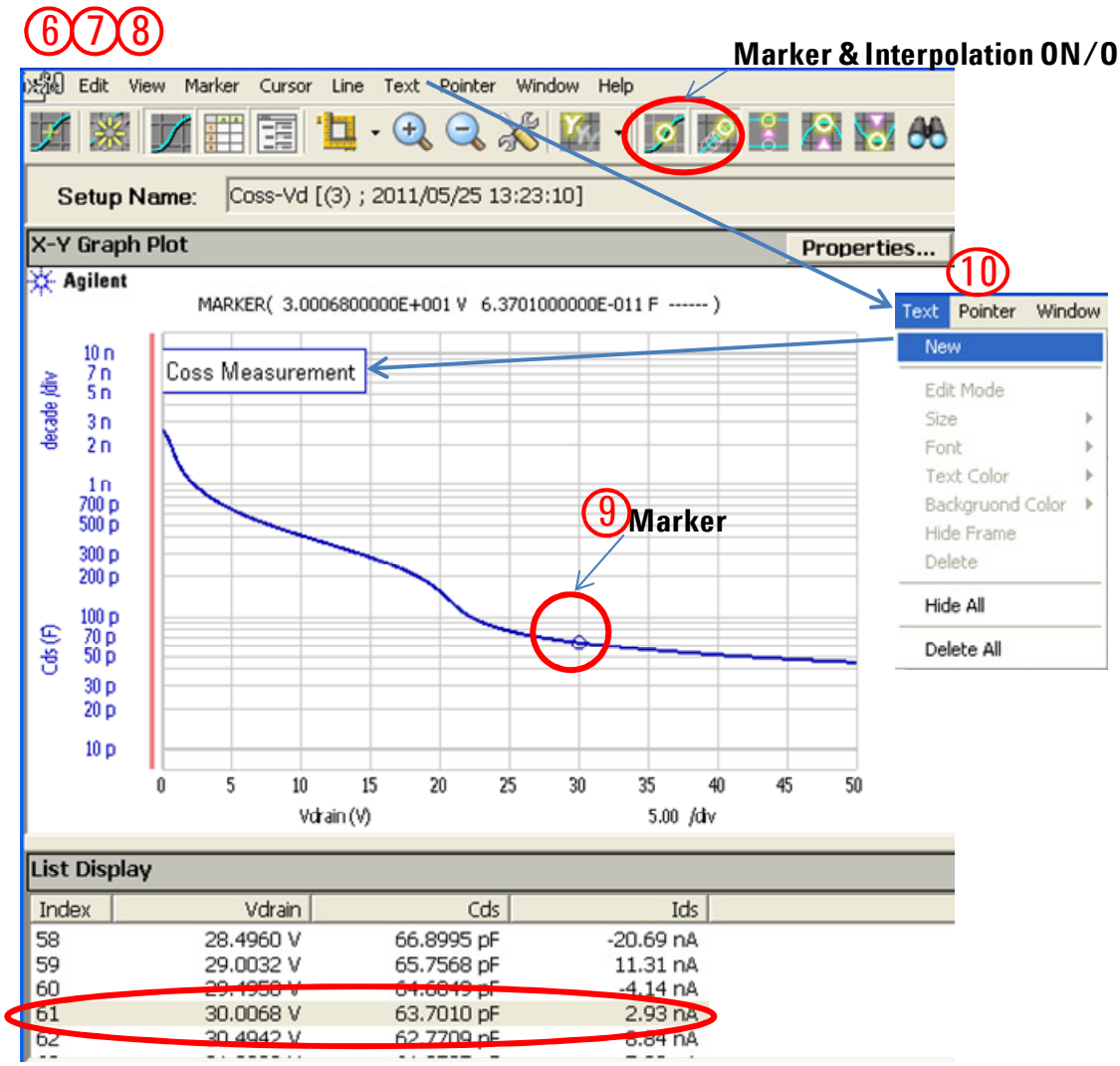


Figure 3-76. Coss-Vd output from Cds Application Test.

B. Measurement Procedure: Coss-Vd CT Classic Test

Refer to figure 3-77 for the following Step 1 to Step 17.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_CT preset group.

Step 3. Select Coss-Vd CT.

Step 4. Press Recall button.

Step 5. Pre-defined example Coss-Vd CT classic test setup – Channel Definition page opens.

Step 6. Set Unit field appropriately depending on your B1505A and connection set-ups.

The connection between the SMU definitions and the power MOS_FET pins must be matched to each other.

Step 7. Press Measurement Setup tab.

You can change measurement parameters in this page.

Step 8. V Name field specifies the voltage source name. In this example, voltage source is the HVSMU defined in the Channel Definition.

Step 9. Set the sweep parameter.

Step 10. Set the measurement frequency of MFCMU.

Step 11. Set the AC test signal level of MFCMU.

Step 12. Hold and Delay time can be set.

Step 13. Integration time of MFCMU can be set.

Step 14. Press Display Setup tab.

You can set the X-Y Graph, List Display and the Parameters of the measurement results in this page.

Step 15. The X, Y1, Y2 and so on to maximum Y8 axis can be defined as X-Y graph display.
Log or Linear scale and the Min. and the Max. scale parameters are set.
In the CV measurement, typically log scale is used for capacitor display in Y axis.

Step 16. List Display sets the measurement parameters that are shown in the List area of Display Graph window.

Step 17. Coss is available as Y1 axis at automatic marker position.

Step 18. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.

Start the measurement. (Click the Single button )

Step 19. The graph window pops up and the measurement starts.

Step 20. You can see the same graph shown in figure 3-78.

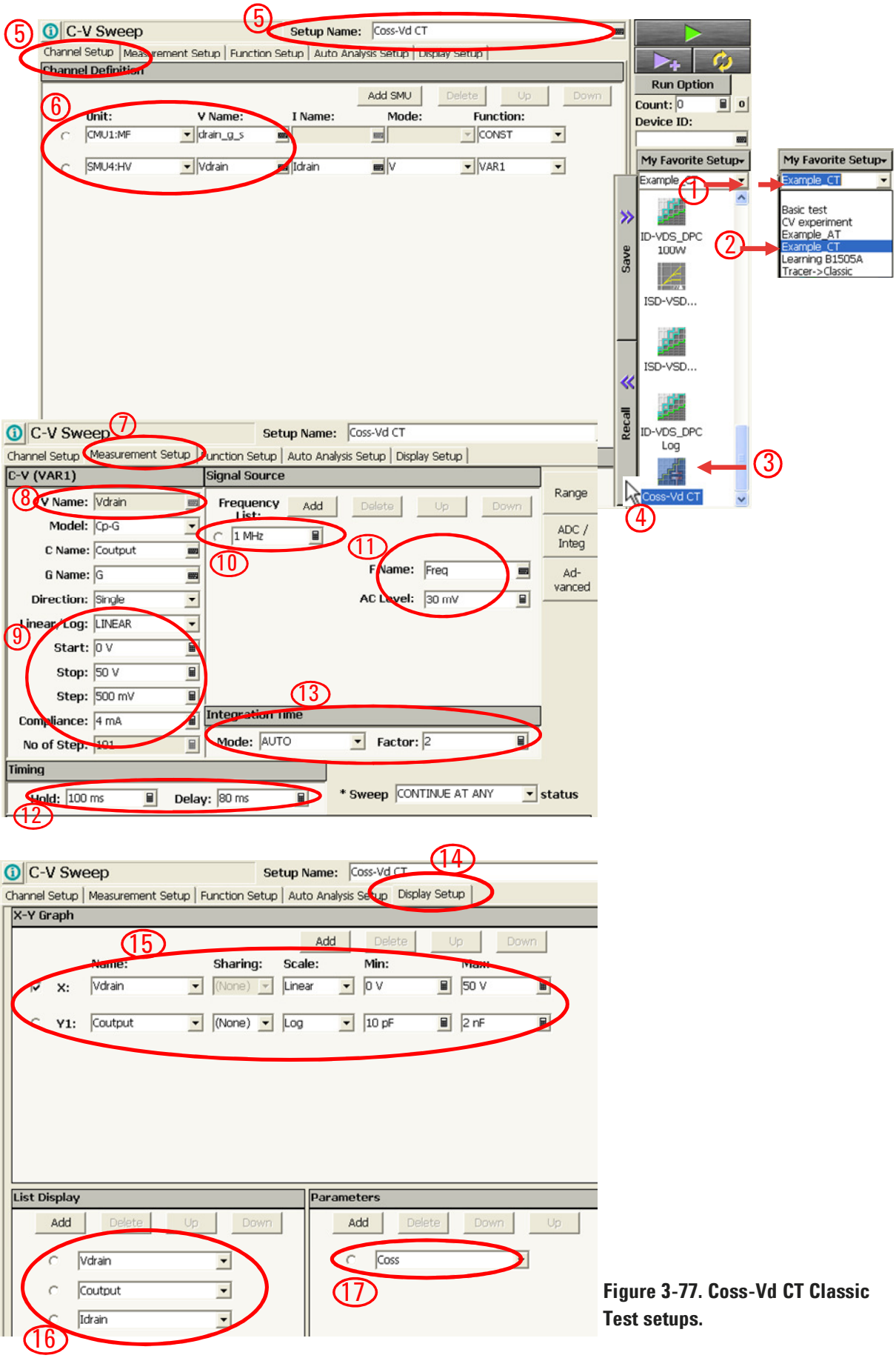


Figure 3-77. Coss-Vd CT Classic Test setups.

Review:

The definition of Classic Test can be changed very easily as in this example. This Coss-Vd Classic Test definition is modified just the name from Cds to Coutput and added automatic marker function. You can directly read Coss in the Parameters field without moving a few mouse steps.

The Coss value agrees to the Application Test results.

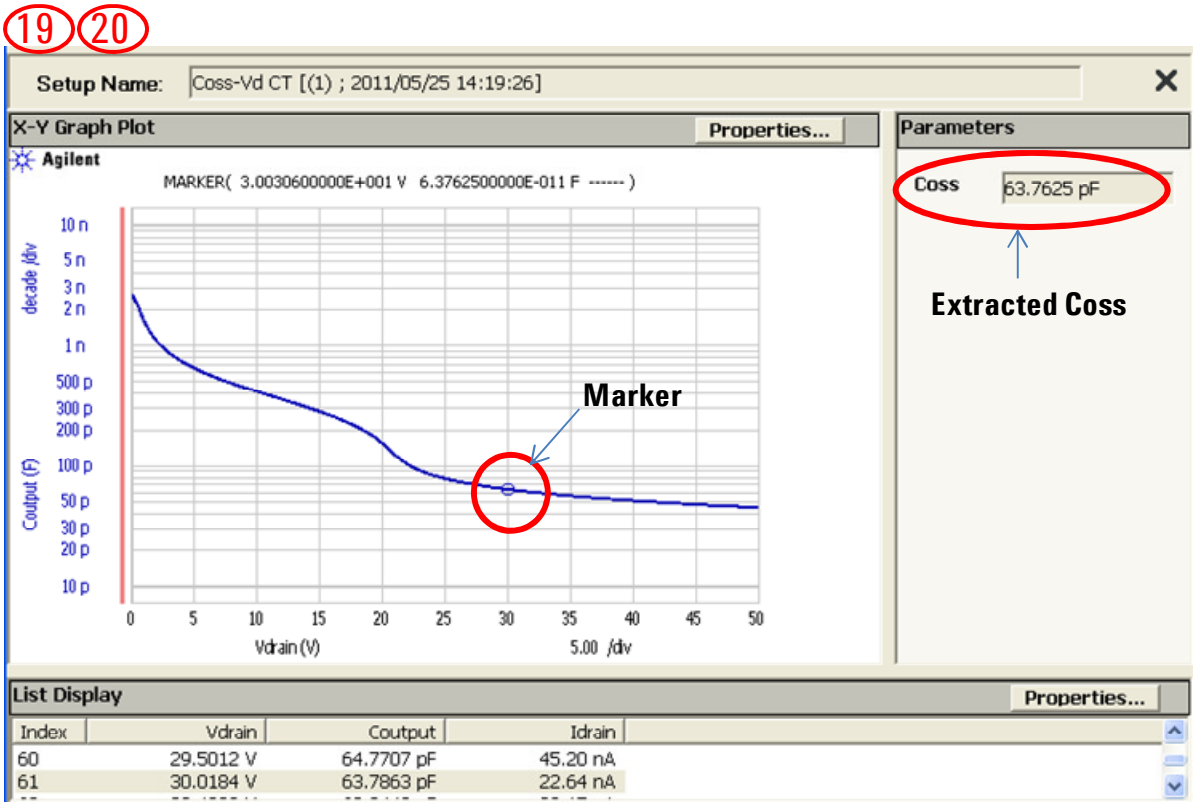


Figure 3-78. Coss-Vd CT output and extracted Coss.

3-4-4. Cgs, Ciss Capacitance measurement

Measurement parameters:
Cgs Gate- Source Capacitance

Ciss Input Capacitance

Application Test name: Cgs_Vd

Application Test setup name (My Favorite Setup -> Example_AT): Cgs_Vd

Classic Test setup name (My Favorite Setup -> Example_CT): Cgs-Vd CT

Device used in the example: 2SK3745LS

Application description:

Measures Gate-Source capacitance (Cgs), and plots Cgs-Vd characteristics. Drain SMU is used as an AC guard, and the maximum AC measurement frequency is limited to 100 kHz.

Ciss can be obtained by adding Cgs and Cgd.

The measurement frequency in this example is limited to maximum 100 kHz because it requires an external capacitor and resistor combination if to measure at 1 MHz. Refer to the Agilent application note "Accurate and Efficient Characterization of Power Devices at 3000 V/20 A", Agilent pub number 5990-3749EN, page 14.

Since there is almost no measurement frequency dependency in silicon power MOS-FET components, the stray capacitance components of power MOS-FET can be measured in better accuracy at 100 kHz rather than using 1 MHz.

Stating this, this measurement handbook introduces 100 kHz Cgs measurements methods which do not require any extra hardware.

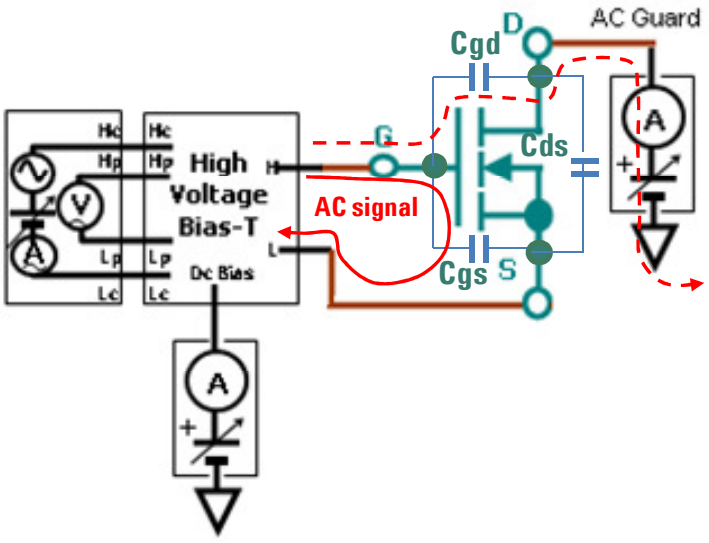


Figure 3-79 shows basic Vgs-Vds measurement block diagram where drain SMU operates as both the DC bias and the AC guard which absolves the AC test signal from the gate through Cgd capacitor, and only the AC signal from the gate to source is measured by the MFCMU. If the AC measurement signal is larger than 100 kHz, SMU cannot operate as AC guard, and the error signal that leaks through Cgd and Cds becomes a measurement error. Refer to the appendix section if more detailed information is necessary.

Figure 3-79. Basic Cgs-Vds measurement block diagram.

Connection inside the N1259A Test Fixture

Open the N1259A test fixture cover, and connect the test leads, SHV cable and SHV-Banana Adaptor shown in figure 3-65 by following the step numbers shown in figure 3-80. The numbers of the procedure steps correspond to the numbers on the drawing for connecting the test leads and SHV cables.

Step 1. Insert the power MOS-FET (example: 2SK3745LS) into the socket on the N1259A. Make sure the device pin name matches the socket numbers shown in figure 3-80.

Step 2. Using test lead, connect the HPSMU1 Force to the terminal 2 Force (Drain) of the Inline Package Socket.

Step 3. Using test lead, connect the HPSMU1 Sense to the terminal 2 Sense (Drain) of the Inline Package Socket.

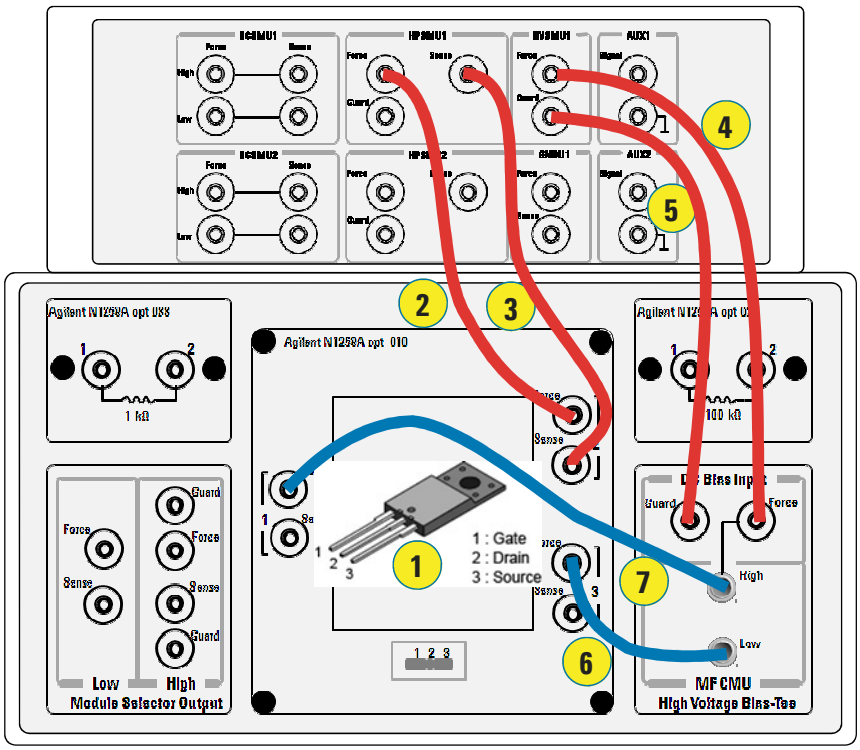
Step 4. Using test lead, connect the HVSMU1 Force to the DC Bias Input Force.

Step 5. Using test lead, connect the HVSMU1 Guard to the DC Bias Input Guard.

Step 6. Using a SHV cable and an adaptor, connect the MFCMU Low output to the terminal 3 Force (Source) of the Inline Package Socket.

Step 7. Using a SHV cable and an adaptor, connect the MFCMU High output to the terminal 1 Force (Gate) of the Inline Package Socket.

Close the N1259A fixture cover.



NOTE: If Measurement is made with Opt.300 Module Selector, use the process shown in appendix A2-3-2, figure A2-10.

Figure 3-80. Connection for Cgs capacitance measurement.

A. Measurement Procedure: Cgs Application Test,

-Starting from Application Test Library

This test approach starts measurements by using an Application Test Library which starts from the default setup parameters and you have to customize the measurement parameters depending on your requirements.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-81.

Step 1. Click the Application Test tab.

Step 2. Check the "PowerMOSFET" application test category.

Step 3, 4. Select Cgs_Vd (Click the Cgs_Vd then click Select 

)

Step 5. Set the test parameters shown in figure 3-81 to an appropriate one depending on your B1505A configuration and your test device.
The important check points are;
a. Drain SMU setup
b. Set Vd (Drain voltage) sweep parameters
c. Gate-Source CMU setup (There should be no other selection, though!)
d. Set MFCMU DC bias HVSMU (VdBias) setup
e. Set Vgate to 0 V
f. Set MFCMU measurement parameters.
g. Set YaxisCgs minimum and maximum scale for log Cgs display.

Step 6. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

Step 7. The graph window pops up and the measurement starts.

Step 8. You can see the Cgs-Vds graph as shown in figure 3-82.

Figure 3-82 plots Cgs in Y axis versus drain voltage Vds in X axis.

Tips:
Marker can be used for reading each drain current and voltage by rotating the rotary knob. You can read between the two measurement points by activating Interpolation mode to ON status.

Review:

There is no Cgs specification in 2SK3745LS datasheet, and the Ciss output capacitance has to be calculated by adding Cgs and Cgd. Cgs can be read as 311 pF from the marker value or List Display of figure 3-82.
Cgs + Cgd at 30 V drain bias in the example is 311 pF + 33.3 pF = 344.3 pF. Ciss specification is 380 pF at 30 V with 1 MHz measurement frequency and it looks okay.

1. Starting from Application Test Library

1`. Starting from My Favorite Setup

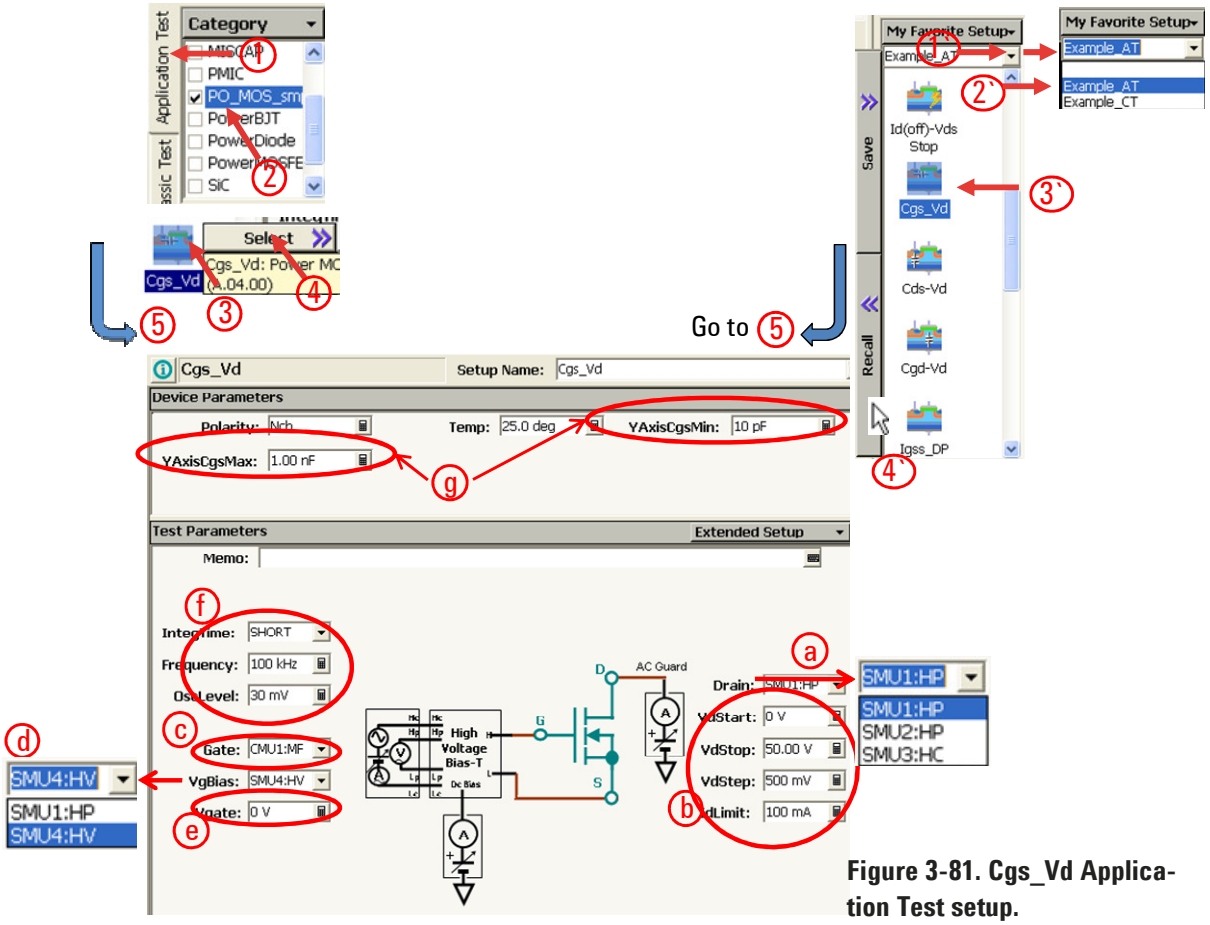


Figure 3-81. Cgs_Vd Application Test setup.

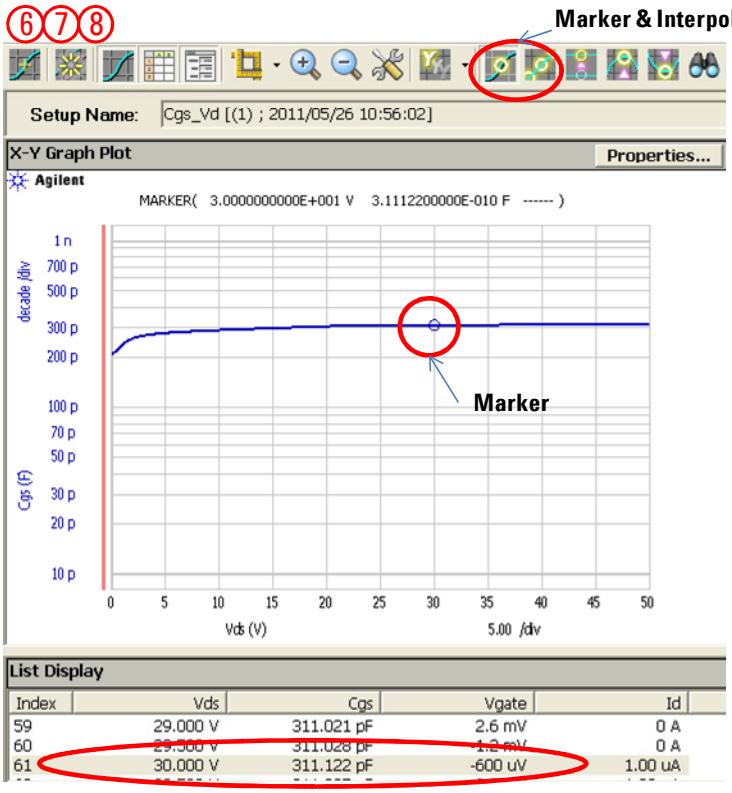


Figure 3-82. Cgs-Vds output from Cgs_Vd Application Test.

A`. Measurement Procedure: Cgs Application Test,

- Starting from pre-defined test setup of My favorite Setup

This test approach starts measurements by using a pre-defined test setup saved in My favorite Setup instead of starting from a scratch by using an Application Test Library.

Setup and execute the test by following the next steps. The same instruction steps are illustrated by the numbers on the "1. Starting from Application Test Library" side of figure 3-81.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_AT preset group.

Step 3. Select Cgs-Vd (Click the Cgs-Vd).

Step 4. Click "Recall" button.

Then go to step 5 of "Starting from Application Test Library" above, and continue by following the test step numbers.

B. Measurement Procedure: Cgs-Vd CT Classic Test

Refer to figure 3-83 for the following Step 1 to Step 16.

Step 1. Click the Preset group of My Favorite Setup.

Step 2. Select Example_CT preset group.

Step 3. Select Cgs-Vd CT.

Step 4. Press Recall button.

Step 5. Pre-defined example Cgs-Vd CT classic test setup – Channel Definition page opens.

Step 6. Set Unit field appropriately depending on your B1505A and connection set-ups.

The connection between the SMU definitions and the power MOS_FET pins must be matched to each other.

Step 7. Press Measurement Setup tab.

You can change measurement parameters in this page.

Step 8. V Name field specifies the voltage source name. In this example, voltage source is the HVSMU defined in the Channel Definition.

Step 9. Set the sweep parameter.

Step 10. Set the measurement frequency of MFCMU.

Since the drain SMU is used as AC guard, maximum frequency is limited around 100 kHz.

Step 11. Set the AC test signal level of MFCMU.

Step 12. Hold and Delay time can be set.

Step 13. Set gate bias voltage to 0 V.

Step 14. Integration time of MFCMU can be set.

Step 15. Press "Range" button. Range Setup sub-window opens.

Step 16. Set the SMU range for Drain. Since Drain SMU is used as the AC guard, minimum range would be about 1 mA.
Tips: The AC guard performance will be degraded if the minimum range is set too small, and additional leakage capacitor (error) from gate-Drain-Source path will be added to Cgs parameter.

Step 17. Press Display Setup tab.

You can set the X-Y Graph, List Display and the Parameters of the measurement results in this page.

Step 18. The X, Y1, Y2 and so on to maximum Y8 axis can be defined as X-Y graph display.
Log or Linear scale and the Min. and the Max. scale parameters are set.
In the CV measurement, typically log scale is used for capacitor display in Y axis.

Step 19. List Display sets the measurement parameters that are shown in the List area of Display Graph window.

Step 20. Make sure the device is properly selected as shown in the "Device used in the example" part or your selection.
Close the lid of N1259A test fixture.
Start the measurement. (Click the Single button )

Step 21. The graph window pops up and the measurement starts.

Step 22. You can see the same graph shown in figure 3-82.

Note: Step 21and 22 are the same as the step 7 and 8 of figure 3-82.

Tips:

Classic Test definition can change measurement parameters very easily.

Although this example does not include any automatic analysis functions, you can add easily automatic marker that appears at 30 V specification point.

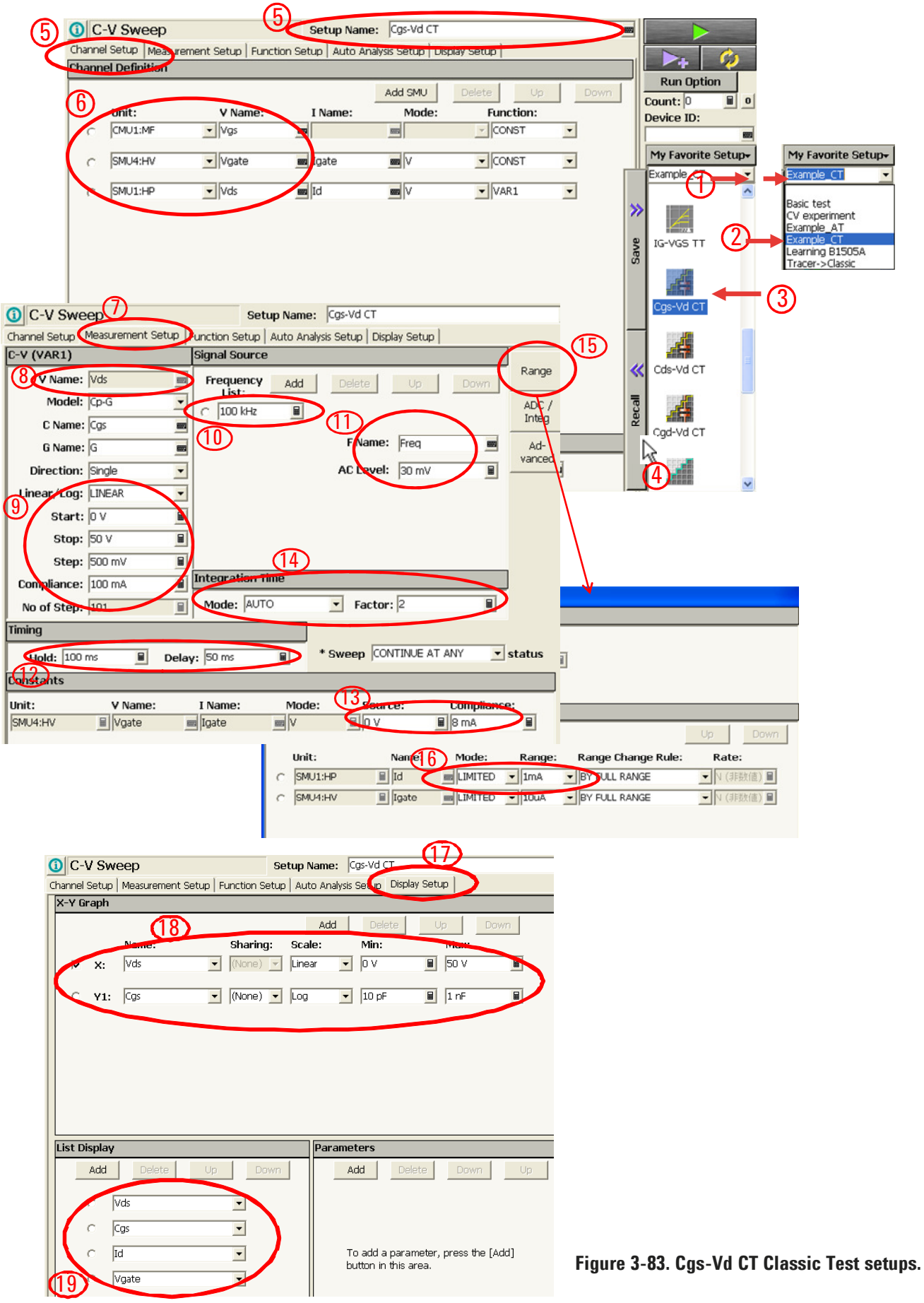
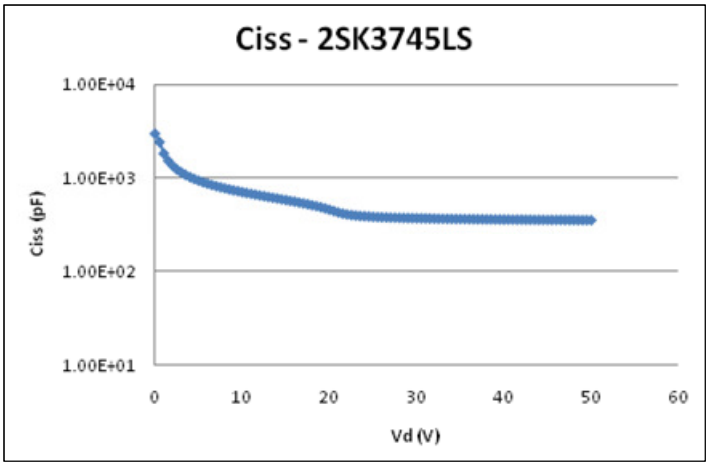


Figure 3-83. Cgs-Vd CT Classic Test setups.



Review:

Measured data can be copied to spread sheet from List Display field.

Figure 3-84 shows the Ciss calculated by using a spread sheet by adding Cgs and Cgd.

Figure 3-84. Ciss data (Ciss = Cgs + Cgd).

Tips for copying data from List data:

Before copying the List data to a clip board, the properties of List Display have to be changed as shown in figure 3-85.

Follow the steps shown in figure 3-85;

Step 1. Press "Properties..."' of List Display.

Step 2. Uncheck the "Physical Unit".

Step 3. Check "Scientific Notation".

Step 4. Press "OK".

Step 5. Press "Edit".

Step 6. Press "Copy List" from the Edit menu.

Now the list data is copied to the clip board.

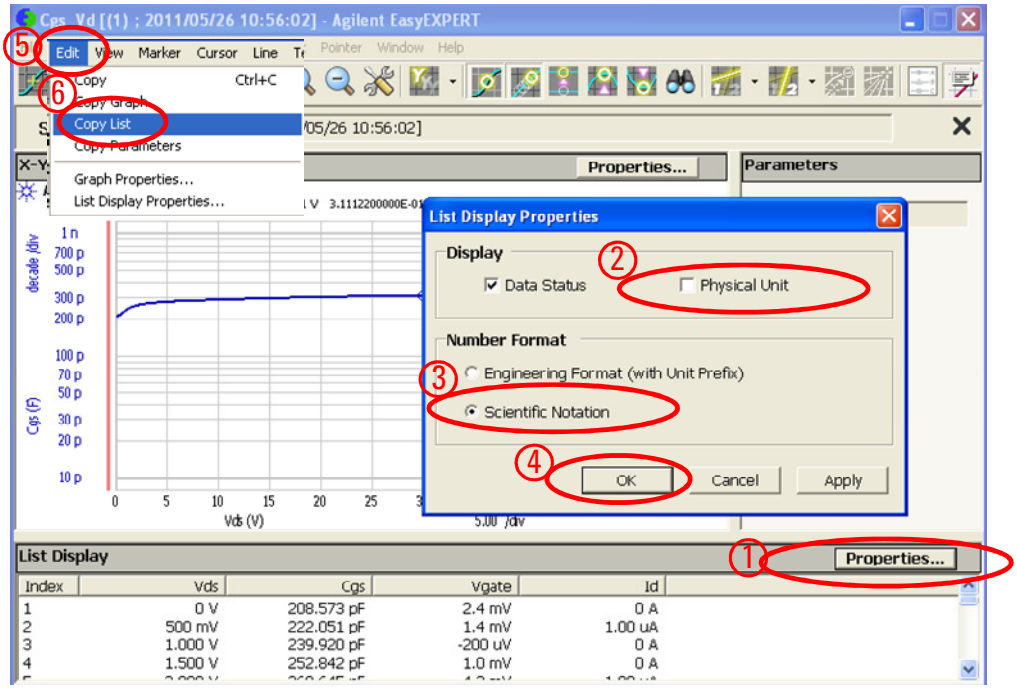


Figure 3-85. Change List Properties for copying to spreadsheet application.

Appendix

Table of Contents:

Appendix 1: Supplemental Information for Preparation

A1-1. Download the example file-set from the Agilent web site

Download the example file-set from the Agilent web site by following the next procedure.

Procedure:

- Web site:
  Visit www.agilent.com/find/b1505a and go to Technical Support area.
  Find “B1505A Step by Step Measurement Handbook for Power MOS-FET Specs” and zip file indicator.
- Download:
  By clicking the link, you can download "B1505A_AN_HB1_Library.zip" example file.
  Save it to a proper folder of the B1505A, say D:/tmp or desktop.

For installing the file-set to EasyEXPERT software, refer to the main section "2-5-2. Setup the example file-set to the EasyEXPERT software".

A1-2. How to return to Workspace management page

This section provides the information for returning to "Workspace management page" from current operating EasyEXPERT workspace like as shown in figure 2-13.
When starting the EasyEXPERT software, default setting opens Workspace management page as shown in figure 2-12.

Figure A1-1 shows how you can return to EasyEXPERT Workspace management page.
Follow the next steps for returning to Workspace Management page.

Step 1. Open file menu of EasyEXPERT software.

Step 2. Select "Close Workspace".
Ok/Cancel prompt pops up.

Step 3. Select "OK" in the Close Workspace prompt.
Then "Workspace management page" opens.

Step 4. Uncheck "Choose the same workspace in the next time" check box. (Refer to figure A1-2)
Then, next time when you start the EasyEXPERT software, you will start from selecting your operating workspace in this page.

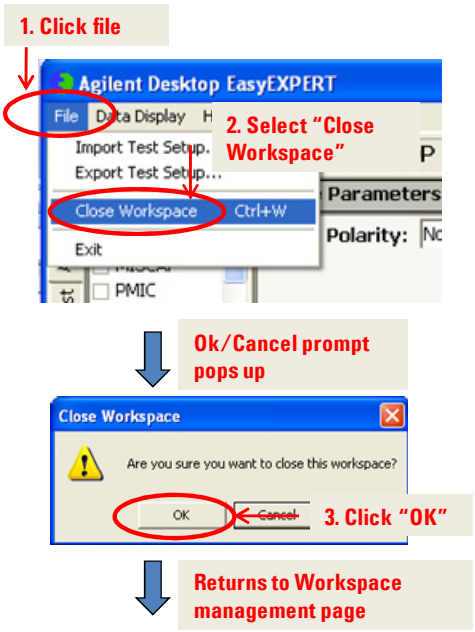


Figure A1-1. How to return to Workspace Management page.

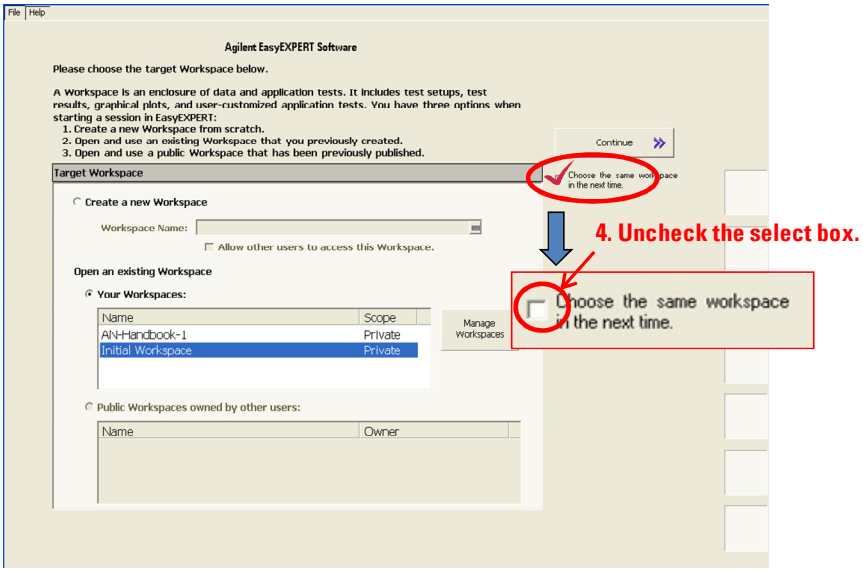


Figure A1-2. Workspace Management page.

Appendix 2. Preparation for the Measurements using the Module Selector

This section provides supplemental information for the measurements by using N1259A Option 300 Module Selector. The configuration is for 20 A solution.

A2-1. Instruments and Accessories used in the measurement examples

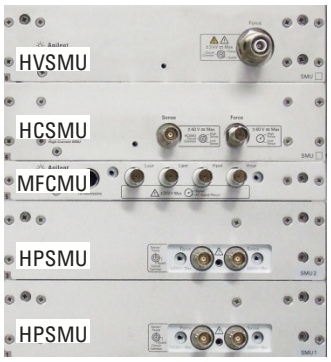


Figure A2-1. B1505A 20 A configuration used in the example.

B1505A 20 A configuration uses following modules.

Agilent B1505A Power Device Analyzer/Curve Tracer (20 A):

- 1 X HVSMU (B1513A) High Voltage SMU
- 1 X HCSMU (B1512A) High Current SMU
- 2 X HPSMU (B1510A) High Power SMU (Note: only one HPSMU is used in the example)
- 1 X MFCMU (B1520A) Multi-Frequency CMU

Following shows the N1259A test fixture configuration and cables used for connecting between B1505A and the N1259A.

Agilent N1259A High Power Test Fixture:

- Opt 020 High Voltage Bias Tee
- Opt 300 Module Selector (Optional: Check appendix section for using the Module Selector)
- Opt 010 Inline package socket module (3 pin)
- Opt 022 100 kΩ R-Box (Optional)
- Opt 033 1 kΩ R-Box
- (10 X Test leads, 2 X SHV cables and SHV-Banana adapters are including in the N1259A)

Cables:

- 1 X 16493S HCSMU Cable
- 1 X 16493T HV Triax Cable
- 4 X 16494A Triax Cable
- 1 X 16493L GNDU Cable
- 1 X N1300A CMU Cable
- 1 X 16493J Interlock Cable
- 1 X 16493G Digital I/O Cable

16493T HV Triax

16494A Triax Cable

N1300A CMU Cable

16493T HCSMU Cable

16493J Interlock Cable

16493G Digital I/O Cable
(Optional for N1259A Opt 300)

Figures A2-2. Cables used for connecting between the B1505A and the N1259A.

A2-2. Cable Connection between the B1505A and the N1259A Test Fixture

Before starting the measurements, connect the cables between the B1505A and the N1259A as shown in figure A2-3.

The breakdown of each step with cable figures and the connector locations are shown in figure A2-4.

These connections are used for all the measurement examples, and there is no need for changing this configuration.

Connections for 1x HCSMU Configuration (20 A) with Opt 300 Module selector

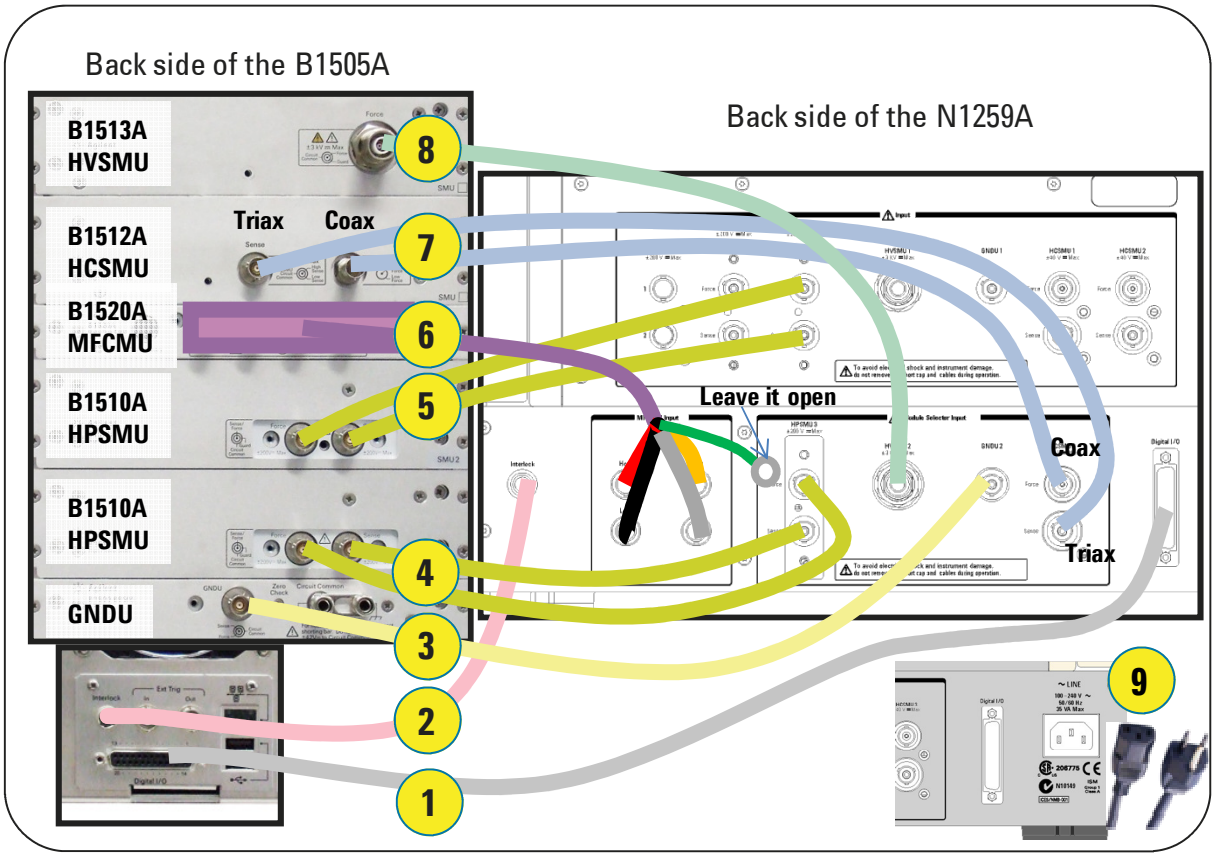


Figure A2-3. Total connection setup for the measurement with the Module Selector.

Step number1:
Using a 16493G Digital I/O Cable, connect the Digital I/O connector on the B1505A to the Digital I/O connector on the N1259A test fixture.

Step number 2:
Using a 16493J Interlock Cable, connect the Interlock on the B1505A and the Interlock on the N1259A

Tips:
For connecting the interlock cable, hold the black plastic part and then turn the connector by pressing toward the interlock connector in the instrument side as shown

in figure 2-8 (reside in main section).
For disconnecting the interlock cable, hold the metal part and turn pull by turning the connector.

Step number 3:
Using a 16493L GNDU Cable, connect the GNDU on the B1505A to the GNDU1 Input on the N1259A.

Step number 4:
Using two 16494A Triax Cables, connect the Force and Sense connectors on the lower B1510A HPSMU (SMU1) to the respective connectors on the HPSMU1 input of the N1259A.

Note:

HPSMU uses a pair of two triax cables. HCSMU cables looks similar as HPSMU cables, but HCSMU cables are a pair of a coax cable and a triax cable. It is a good practice for distinguishing these two cables.

Step number 5:
Using two 16494A Triax Cables, connect the upper B1510A HPSMU (SMU2) to the HPSMU2 on the N1259A.

Step number 6:
Using a N1300A CMU Cable, connect the B1520A CMU to the respective connectors of MF CMU Input (Hcur, Hpot, Lcur, Lpot) on the N1259A.

Note: Leave the green cable with a round terminal as it is.

Step number 7:
Using a 16493S HCSMU Cable, connect the Force and Sense connectors on the B1512A HCSMU to the respective connectors of HCSMU1 Input on the N1259A.

Note:

HCSMU cables are a pair of a coax cable and a triax cable. In case of HPSMU, it uses a pair of two triax cables. It is a good practice for distinguishing these two cables.

Step number 8:
Using a 16493T HV Triax Cable, connect the Force connector on the B1513A HVSMU to the HVSMU1 input of the N1259A

Step number 9:
Connect power cable to the fixture.

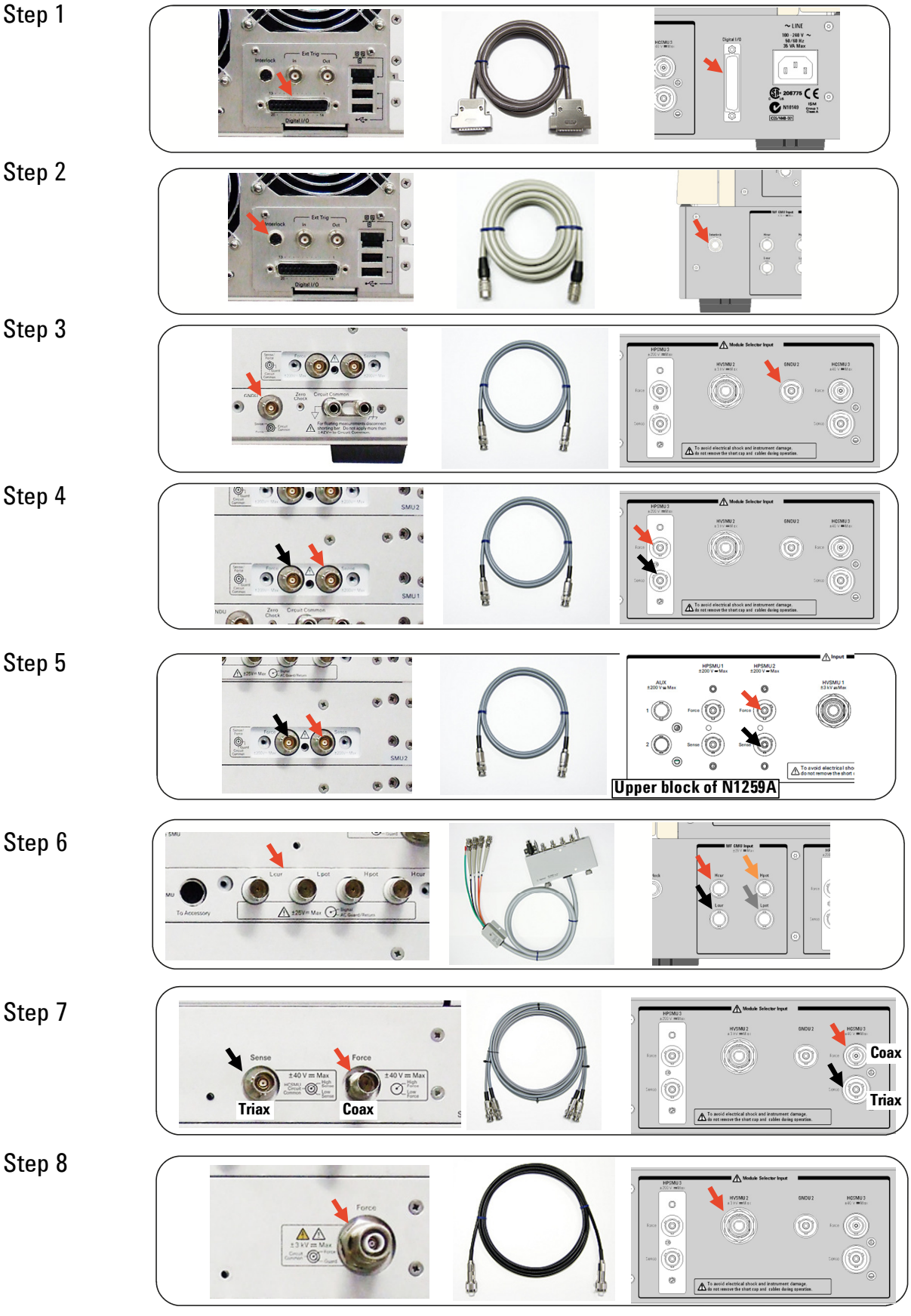


Figure A2-4. Breakdown of the cable connection for 20 A configuration.

IMPORTANT

Before starting the measurement, check the settings for the module selector. If the setting is different from the figure A2-5 setup, please change the setup as in the figure.

You can view and change the configuration of the module selector as follows.

1.Click the configuration button  on the right side of the screen.

2.Select the Module selector tab.

a. Check "Enable Module Selector"
b. Check "Auto Detection"
c. Uncheck "Enable Series Resistor"

Tips:
There is no indicator on the N1259A test fixture for showing this status. Therefore this checkbox should better be set to off just after using this function for preventing any unexpected test result in later use of B1505A.

d. Check the SMU modules
e. Press "Apply"

3. After modification, press "Apply" button.

4. Press "Close "

With this setup, the N1259A Status LED displays the current connection status.

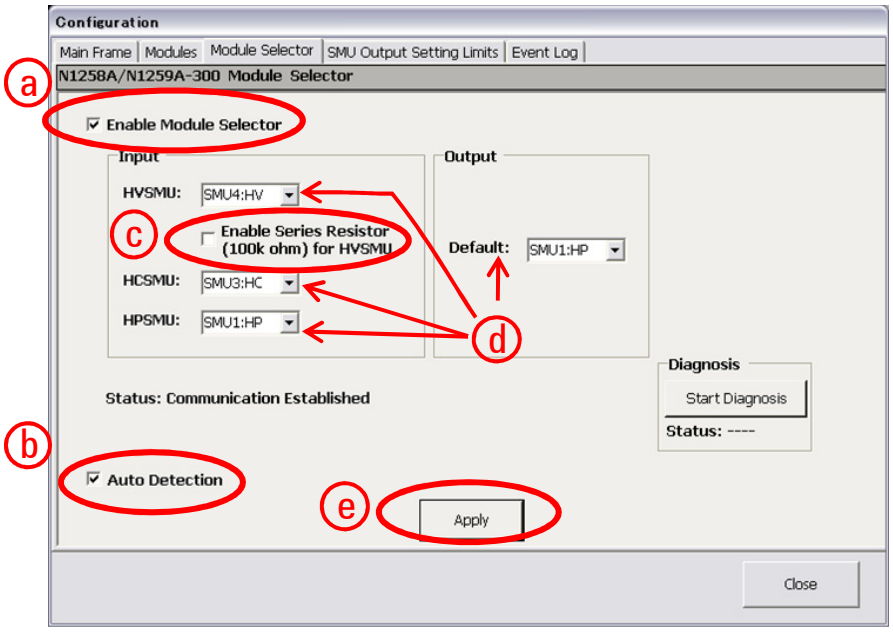


Figure A2-5. Module Selector setup for the measurement with the Module Selector.

A2-3. Connection inside the N1259A Test Fixture

A2-3-1. DC Measurement

Use figure A2-6 connection for all the DC measurement.

[PROCEDURE]

Open the N1259A test fixture cover, and connect the test leads as follows. The numbers on the drawing correspond to the procedure steps.

Step 1. Insert the device (2SK3745LS) into the socket on the N1259A.

Step 2. Connect the HPSMU2 Force to the terminal 1 on the 1 kΩ resistor.

Step 3. Connect the terminal 2 on the 1 kΩ resistor to the terminal 1 Force (Gate) on the Inline Package Socket.

Step 4. Connect the High Force of the Module Selector Output to the terminal 2 Force (Drain) on the Inline Package Socket.

Step 5. Connect the High Sense of the Module Selector Output to the terminal 2 Sense (Drain) on the Inline Package Socket.

Step 6. Connect the Low Force of the Module Selector Output to the terminal 3 Force (Source) on the Inline Package Socket.

Step 7. Connect the Low Sense of the Module Selector Output to the terminal 3 Sense (Source) on the Inline Package Socket.

Close the N1259A fixture cover.

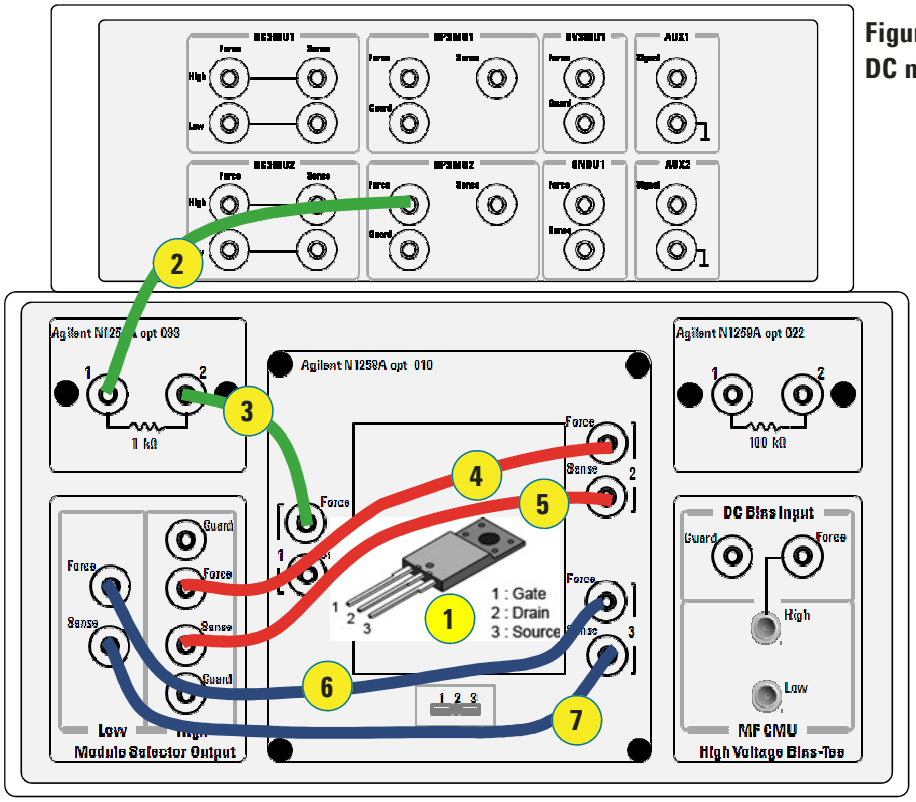


Figure A2-6. Connection for DC measurement.

A2-3-2. Capacitance Measurement

Use following connection depending on the measurement parameters.

Cgd and Crss measurement:

Open the N1259A test fixture cover, and connect the test leads and SHV cables as follows. Refer to the drawing on figure A2-7. The numbers on the drawing correspond to the procedure steps.

Step 1. Insert the device (2SK3745LS) into the socket on the N1259A.

Step 2. Using test lead, connect the AUX2 outer shield (GND) to the terminal 3 Force (Source) of the Inline Package Socket.

Step 3. Using test lead, connect the High Sense of the Module Selector Output to the DC Bias Input Force.

Step 4. Using test lead, connect the High Force of the Module Selector Output to the DC Bias Input Force.

Step 5. Using test lead, connect the High Guard of the Module Selector Output to the DC Bias Input Guard.

Step 6. Using a SHV cable and an adaptor, connect the MFCMU Low output to the terminal 1 Force (Gate) of the Inline Package Socket.

Step7. Using a SHV cable and an adaptor, connect the MFCMU High output to the terminal 2 Force (Drain) of the Inline Package Socket.

Close the N1259A fixture cover.

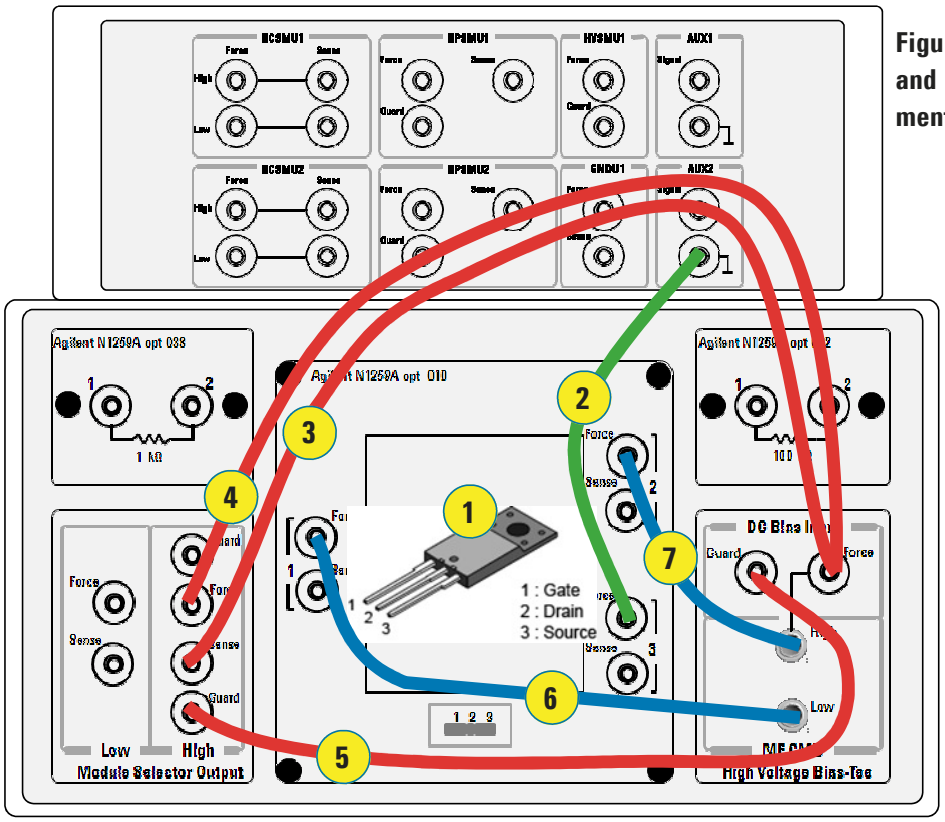


Figure A2-7. Connection for Cgd and Crss capacitance measurement.

Cds measurement

Open the N1259A test fixture cover, and connect the test leads and SHV cables as follows. Refer to the drawing on figure A2-8. The numbers on the drawing correspond to the procedure steps.

Step 1. Insert the device (2SK3745LS) into the socket on the N1259A.

Step 2. Using test lead, connect the AUX2 outer shield (GND) to the terminal 1 Force (Gate) of the Inline Package Socket.

Step 3. Using test lead, connect the High Sense of the Module Selector Output to the DC Bias Input Force.

Step 4. Using test lead, connect the High Force of the Module Selector Output to the DC Bias Input Force.

Step 5. Using test lead, connect the High Guard of the Module Selector Output to the DC Bias Input Guard.

Step 6. Using a SHV cable and an adaptor, connect the MFCMU Low output to the terminal 3 Force (Source) of the Inline Package Socket.

Step7. Using a SHV cable and an adaptor, connect the MFCMU High output to the terminal 2 Force (Drain) of the Inline Package Socket.

Close the N1259A fixture cover.

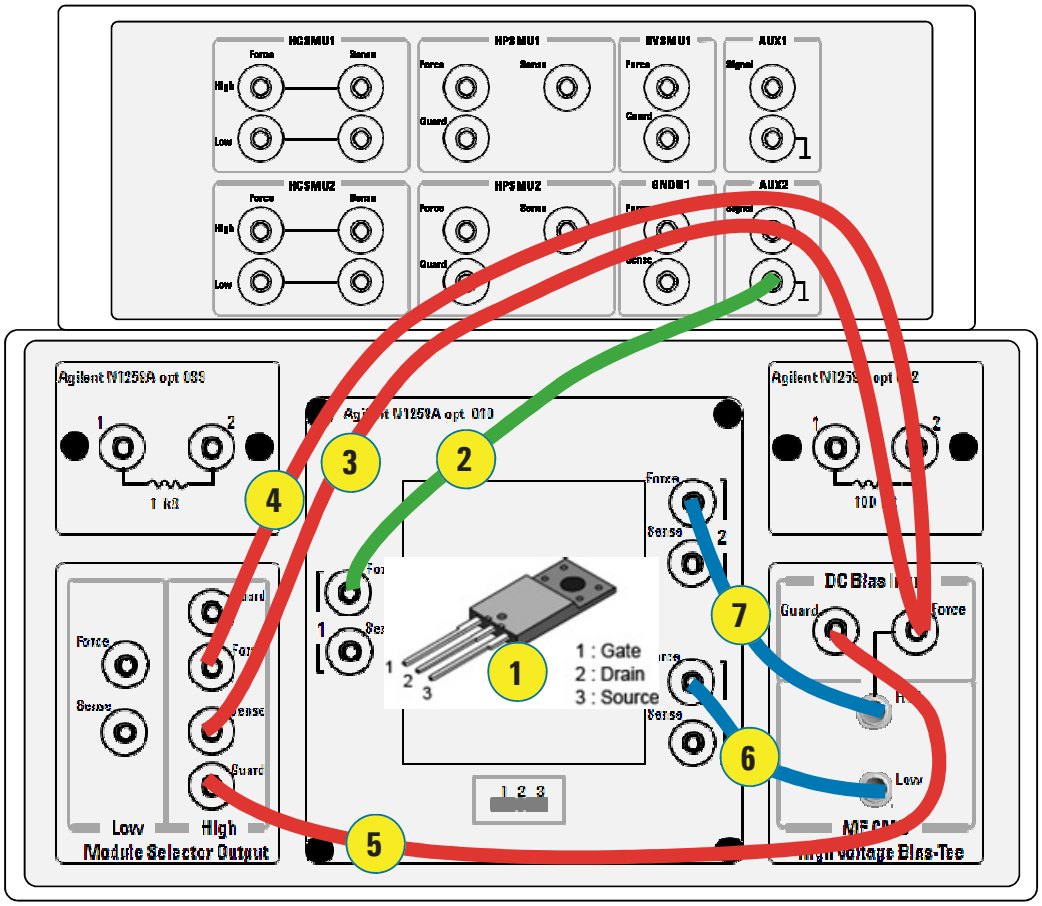


Figure A2-8. Connection for Cds capacitance measurement.

Coss measurement

Open the N1259A test fixture cover, and connect the test leads and SHV cables as follows. Refer to the drawing on figure A2-9. The numbers on the drawing correspond to the procedure steps.

Step 1. Insert the device (2SK3745LS) into the socket on the N1259A.

Step 2. Using test lead, connect the terminal 3 Force (Gate) to the terminal 3 Sense (Source) of the Inline Package Socket.

Step 3. Using test lead, connect the High Sense of the Module Selector Output to the DC Bias Input Force.

Step 4. Using test lead, connect the High Force of the Module Selector Output to the DC Bias Input Force.

Step 5. Using test lead, connect the High Guard of the Module Selector Output to the DC Bias Input Guard.

Step 6. Using a SHV cable and an adaptor, connect the MFCMU Low output to the terminal 3 Force (Source) of the Inline Package Socket.

Step7. Using a SHV cable and an adaptor, connect the MFCMU High output to the terminal 2 Force (Drain) of the Inline Package Socket.

Close the N1259A fixture cover.

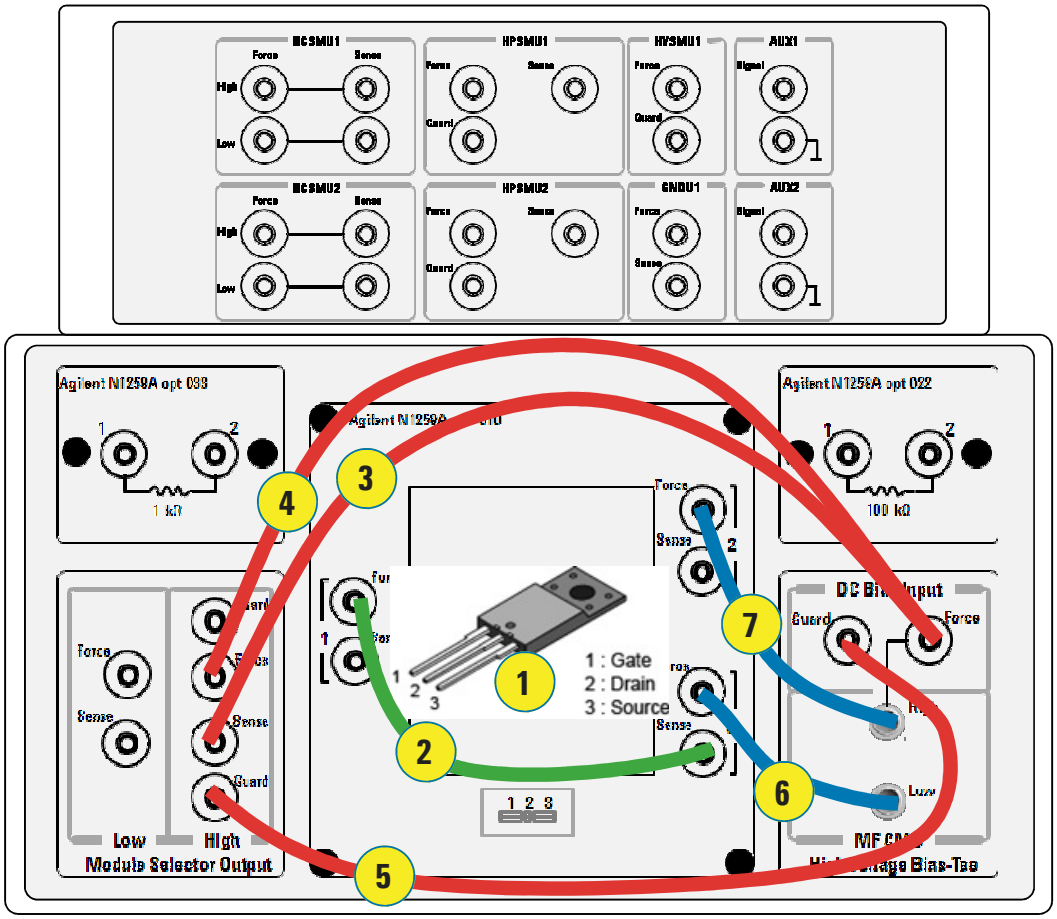


Figure A2-9. Connection for Coss capacitance measurement.

Cgs and Ciss measurement

Open the N1259A test fixture cover, and connect the test leads and SHV cables as follows. Refer to the drawing on figure A2-10. The numbers on the drawing correspond to the procedure steps.

Step 1. Insert the device (2SK3745LS) into the socket on the N1259A.

Step 2. Connect the HPSMU2 Force to terminal 2 Force (Drain) on the Inline Package Socket.

Step 3. Connect the HPSMU2 Sense to terminal 2 Sense (Drain) on the Inline Package Socket.

Step 4. Using test lead, connect the High Sense of the Module Selector Output to the DC Bias Input Force.

Step 5. Using test lead, connect the High Force of the Module Selector Output to the DC Bias Input Force.

Step 6. Using test lead, connect the High Guard of the Module Selector Output to the DC Bias Input Guard.

Step 7. Using a SHV cable and an adaptor, connect the MFCMU Low output to the terminal 3 Force (Source) of the Inline Package Socket.

Step8. Using a SHV cable and an adaptor, connect the MFCMU High output to the terminal 1 Force (Gate) of the Inline Package Socket.

Close the N1259A fixture cover.

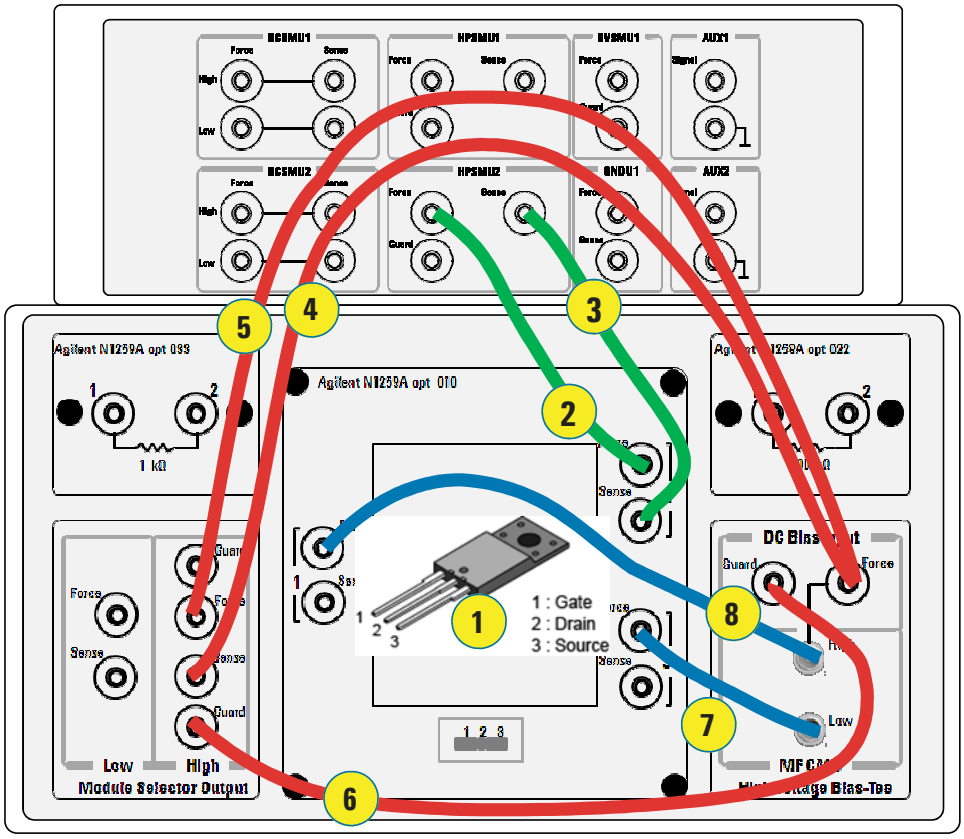


Figure A2-10. Connection for Cgs capacitance measurement.

Appendix 3. Measurement Basic/Tips

There are several useful measurement tips when measuring power MOS-FETs by using the B1505A.

The important test of the power MOS-FET can be categorized in two operating regions; one is the characterization in high current performance and the other is high voltage characterization.

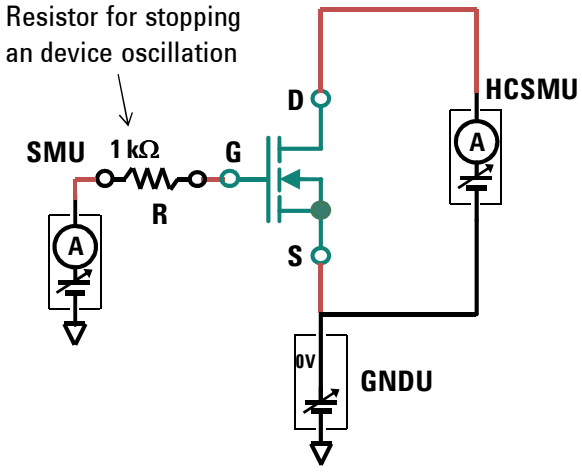


Figure A3-1. Option 033 Series R inserted between gate SMU and the gate.

In high current measurements, there are two considerations. One is inserting a series resistor to gate terminal as shown in figure A3-1 for achieving a stable measurement by suppressing an oscillation typically observed in higher gm operating region of power MOS-FET.

The other consideration is relating to a pulsed measurement for reducing a self-heating effect of the power MOS-FET.
Traditionally a pulsed Id-Vd or Id-Vg measurements are performed by applying a pulse to the gate while DC voltage is applied to the drain. In the case of the B1505A, easiest way is applying a pulse to the drain by using the pulse capability of HCSMU considering HCSMU can only output a pulsed voltage or current when measuring current is greater than 1 A. There is no problem for smaller size power MOS-FET with this configuration. In later section, a useful measurement tips for evaluating high current power MOS-FET is introduced.

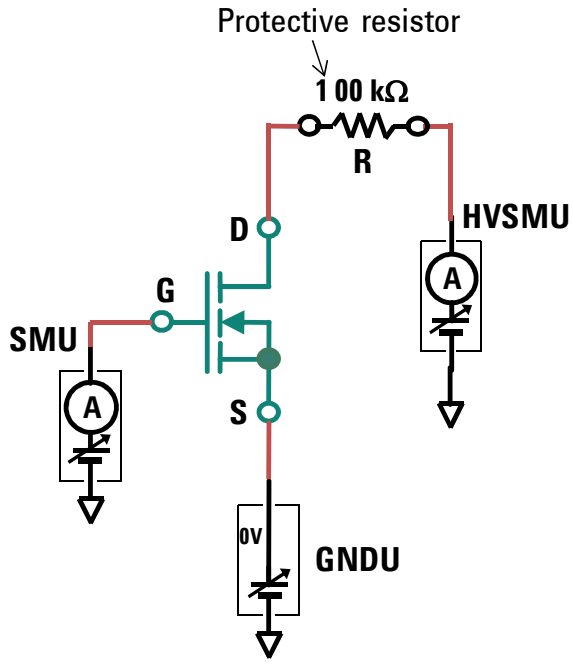


Figure A3-2. Option 022 Series R inserted between the drain and drain HVSMU.

In high voltage measurements, sometimes people insert a resistor in series between the drain and drain SMU for protecting the device from a possible damage when the device breaks down as shown in figure A3-2. We have a 100 kΩ resistor as Option 22 of N1259A Test Fixture. We`ll discuss how to compensate the voltage drop by this resistor.

A3-1 DC Measurement Basic

DC measurement of power MOS-FET is roughly categorized in two operating regions; high current and high voltage or breakdown characteristics,

A3-1-1 SMU- Spot and sweep measurement

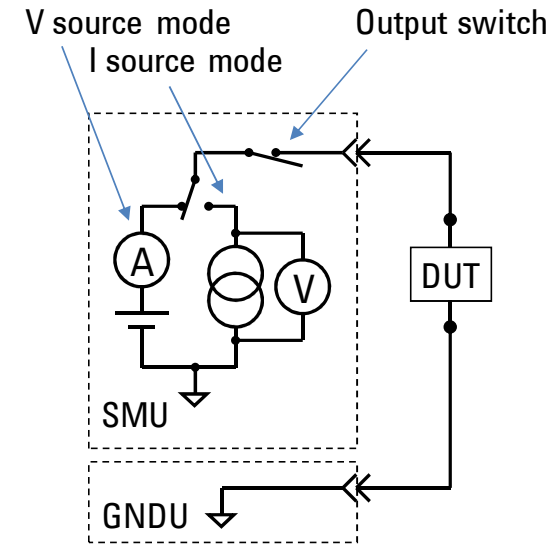


Figure A3-3. DC measurement using SMU.

DC measurements of the B1505A using SMU is performed by forcing either a voltage or current and measures voltage or current as shown in figure A3-3 between the SMU and the Ground Unit (GNDU). This means that SMU can make a spot measurement very easy by forcing a voltage and measures the current or forcing a current and measures the voltage. This capability is very useful for speed up the measurement throughput for testing many devices if the sweep data is not necessary.

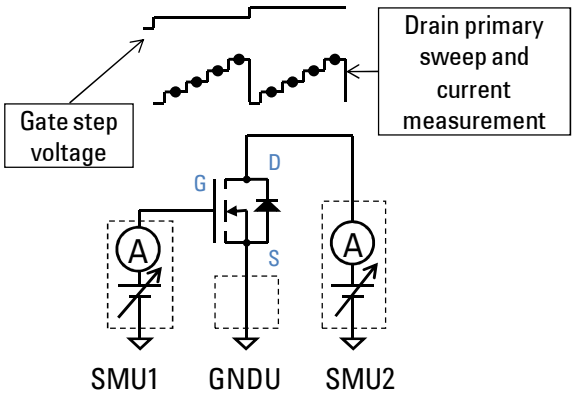


Figure A3-4 shows Id-Vd measurement example of power MOS-FET by using several SMUs where the drain is swept as a primary sweep while the gate is stepped as secondary sweep for the each drain sweep.
The Drain SMU sweeps a voltage and measures the current flown from the drain while the gate SMU applies a step voltage. The gate current can be also measured for each drain sweep by SMU when it is needed.

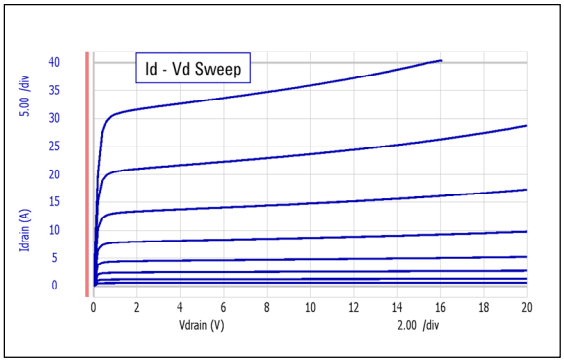


Figure A3-4. Measurement example using SMUs.

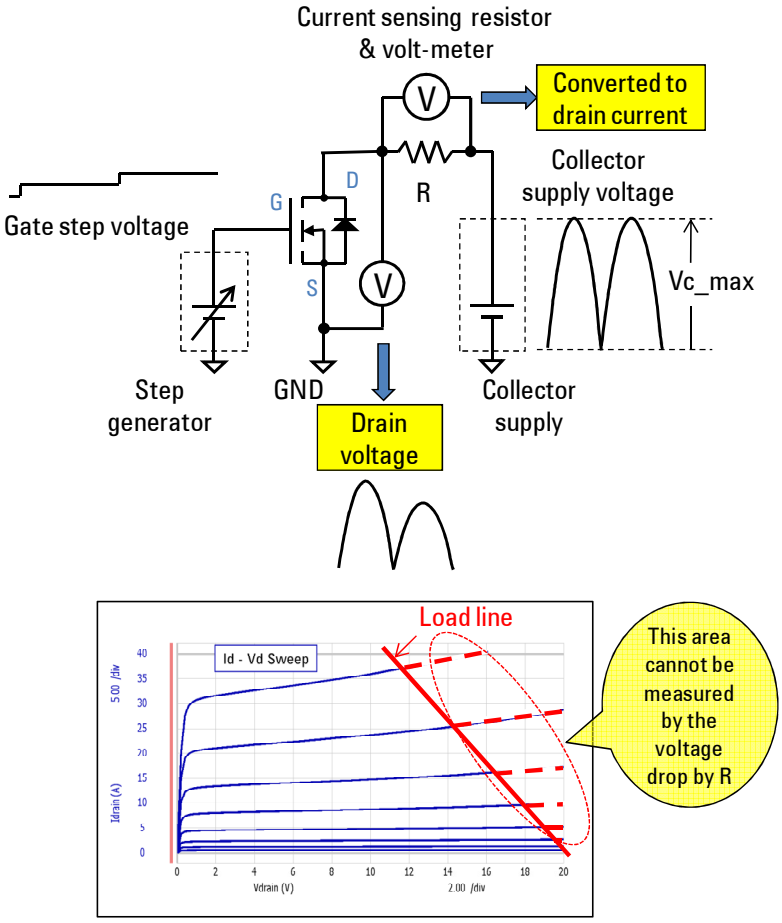


Figure A3-5. Measurement example of traditional curve tracer.

Traditional curve tracer

Figure A3-5 shows a measurement example of traditional analog curve tracer and its equivalent circuit. Since the traditional curve tracer supplies the drain voltage through the current sensing resistor "R", the actual voltage applied to the drain is different from the collector supply voltage as shown in the blue solid line separated by the load line decided by the collector supply voltage and the current sensing resistor. The load line is expressed as the following equation: Vd=Vc_max-Id x R. The dotted red line in the right half of the load line shows the voltage drop by the current sensing resistor. This means that it is impossible to apply an accurate voltage to the drain without manually adjusting the collector supply voltage and this is one of the major factors that an automatic measurement is limited in the application of the traditional curve tracers.

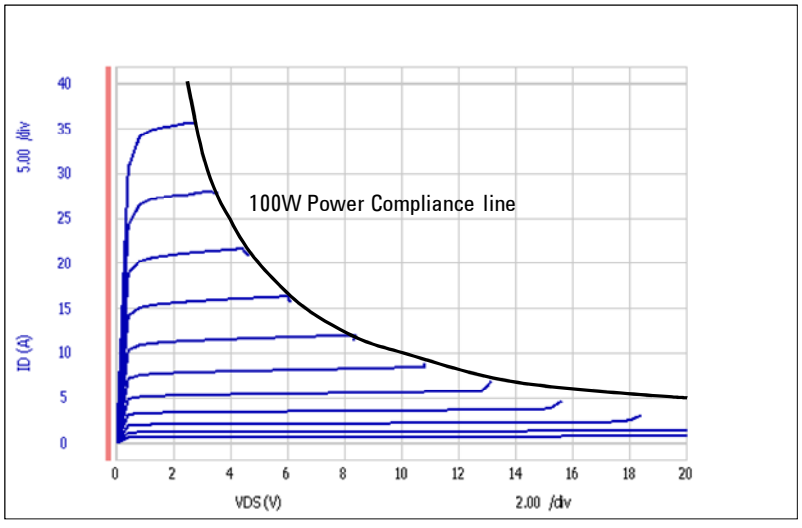


Figure A3-6. Power compliance of the B1505A.

SMU can measure whole area specified by the setup as in figure A3-4 without any limitation. The voltage drop by the current sensing resistor is sometimes useful for limiting a power applied to power MOS-FET. In that case a power compliance functionality of the B1505A can be used as shown in figure A3-6.

A3-1-2 High current measurement tips – Avoiding an oscillation

We recommend using a figure A3-1 connection for higher current measurements where a 1 kΩ resistor inserted in series between gate SMU and the gate for reducing the possibility of the FET oscillation when measuring in a high gm operating region of power MOS-FETs, i.e. typically in high current condition.

Figure A3-7 shows a rough AC equivalent circuit of figure A3-1 expressed by focusing to the oscillation conditions including a parasitic inductance of connecting cables, output impedance of SMUs and the capacitance components of the power MOS-FET. The figure looks very complicated for solving an oscillation condition, but a circuit simulator solved the generic answers for reducing the possibility of the oscillation.

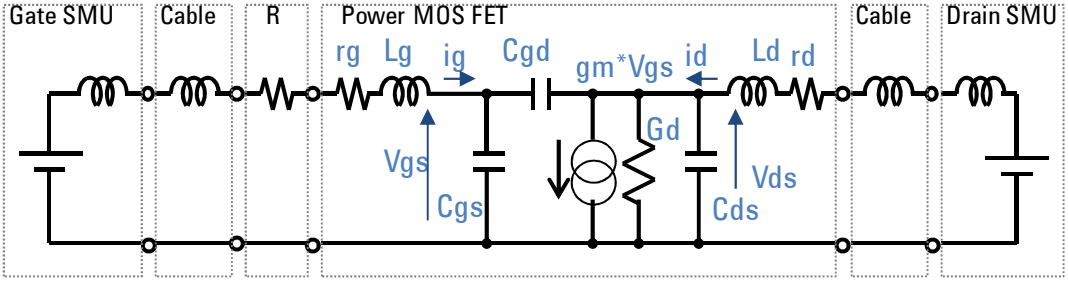


Figure A3-7. AC Equivalent Circuit of figure A3-1.

Tips:
- Reduce gm of power MOS-FET.
- Reduce the inductance connected to the gate.
- Reduce the inductance connected to the drain.
- Increase the resistance connected to the gate.

Figure A3-8. Tips for reducing the oscillation condition of power MOS-FET.

Four tips obtained from the circuit simulator for reducing the possibility of an oscillation are summarized to the following list;

1. Reduce the gm of power MOS-FET.
2. Reduce the inductance connected to the gate;
   Possible by shortening the SMU cable length and change routing, and use larger SMU current range.
3. Reduce the inductance connected to the drain;
   Possible by shortening the SMU cable length and change routing, and use larger SMU current range.
4. Increase a resistance connected to the gate;
   Possible by inserting a resistor in series to the gate.

All of these items meet our past experience for reducing oscillation, and inserting a resistor to the gate is the most effective solution that you should better try in the first place. Since the voltage drop by a 1 kΩ series resistor can be neglected in almost all of the case considering a very small gate current of the power MOS FET, adding a 1 kΩ resistor to the gate seems no problem except checking a transient response of a power MOS FET.

A3-1-3 High voltage measurements

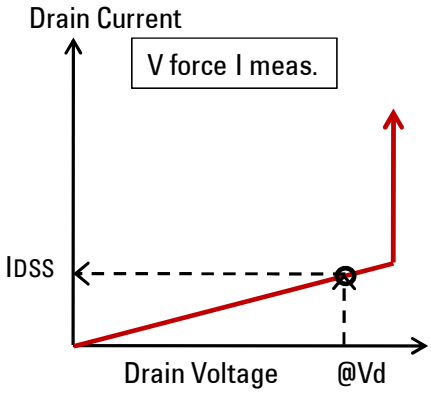
The most frequently measured parameters in high voltage application in power MOS FET are drain to source breakdown voltage (V(BR)DSS) and drain to source leakage current (IDSS).

Spot Measurement

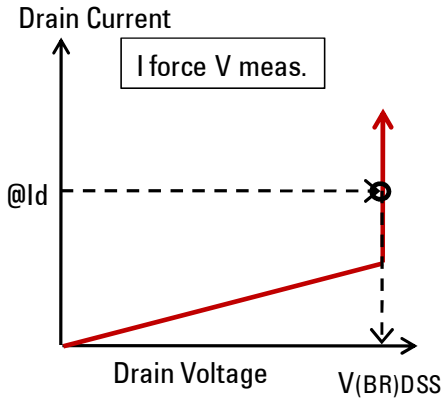
The simplest and fastest methods for measuring these parameters are spot measurements as shown in figure A3-9.

IDSS can be measured by forcing a specified voltage and read a current as shown in figure A3-9(a) and V(BR)DSS can be measured by forcing a specified current as shown in figure A3-9(b).

Though the spot measurement is the simplest method, these tests are typically made by using a voltage sweep measurement. In that case, an appropriate voltage sweep scheme is important for achieving an accurate and fast measurement result.



(a) Drain to source leakage current: IDSS



(b) Drain to source breakdown voltage: V(BR)DSS

Figure A3-9. High voltage measurements using spot I or V force measurement mode.

Knob sweep and Protective resistor

In case the device characteristics are unknown and the number of device samples which can be used for the test is limited, then you may want to measure with the maximum caution. There are two measurement tips in such a case; one is using a knob sweep capability in Tracer Test mode where you can Interactively control the sweep in real time by monitoring the display data and the other is inserting a 100 k Ω resistor to the drain.

A 100 kΩ series resistor inserted to the drain as shown in figure A3-2 adds an extra margin for protecting the device from unexpected behavior such as the device breakdown or oscillation.

The voltage drop by the drain current and the resistor can be compensated by using a USER FUNCTION of Classic Test mode and such example is shown in the later section. Unfortunately this compensation scheme cannot be used in knob sweep of Tracer Test mode.

A3-2 Pulsed measurement

Power devices are typically tested using a pulse for eliminating the test device to be self heated while in the test. Testing devices in a stable condition is very important when comparing the data in different production lot in different timing or between the different site like as a factory QA department and the incoming inspection at the end users.

Pulsed measurement is a technique for reducing the temperature rise of the device while device testing and it essentially reduces one error component when comparing the data.

A3-2-1 Traditional pulsed IV

Although the pulsed measurements provide a stable result when the measurement setup is made in right way and the same measurement parameters are used. Figure A3-10 shows a traditional method used in the pulsed measurements for Id-Vg and Id -Vd measurements where the pulse is applied to the gate.

The origin of this test approach goes back to the bipolar transistor age where the base bias is zero when there is no collector voltage under the normal operating condition because a large base current flows into the gate when the collector voltage is zero.

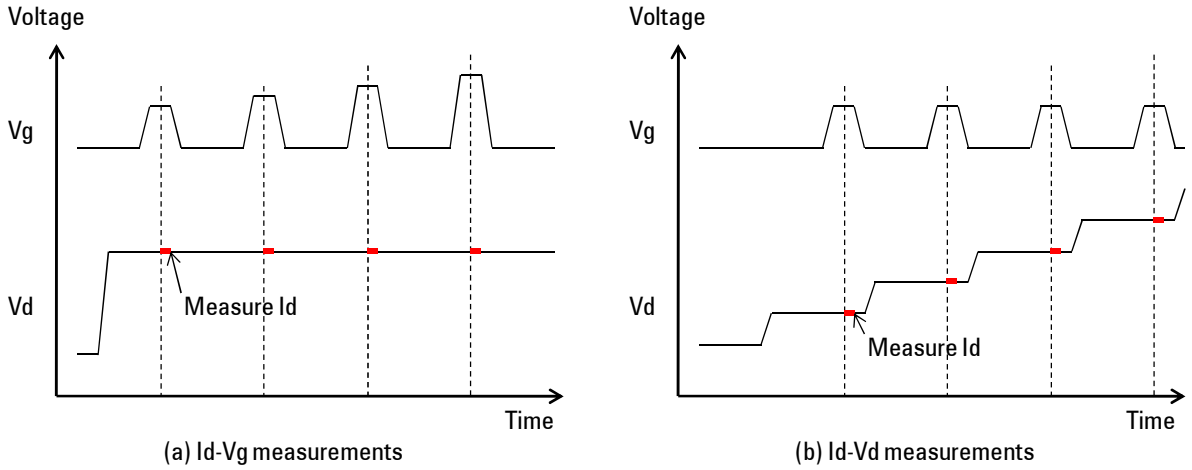
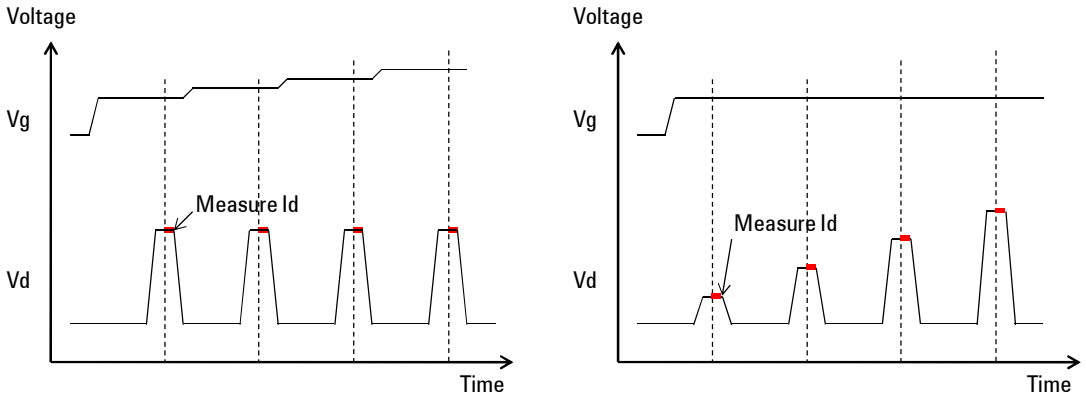


Figure A3-10. Traditional one pulse source "pulsed I/V" applying a pulse to the gate.

A3-2-2 Alternative one pulse source I/V

Figure A3-11 shows an alternative pulsed measurement approach by using HCSMU when only one pulsed source is available. This approach works fine for relatively low gm FETs.

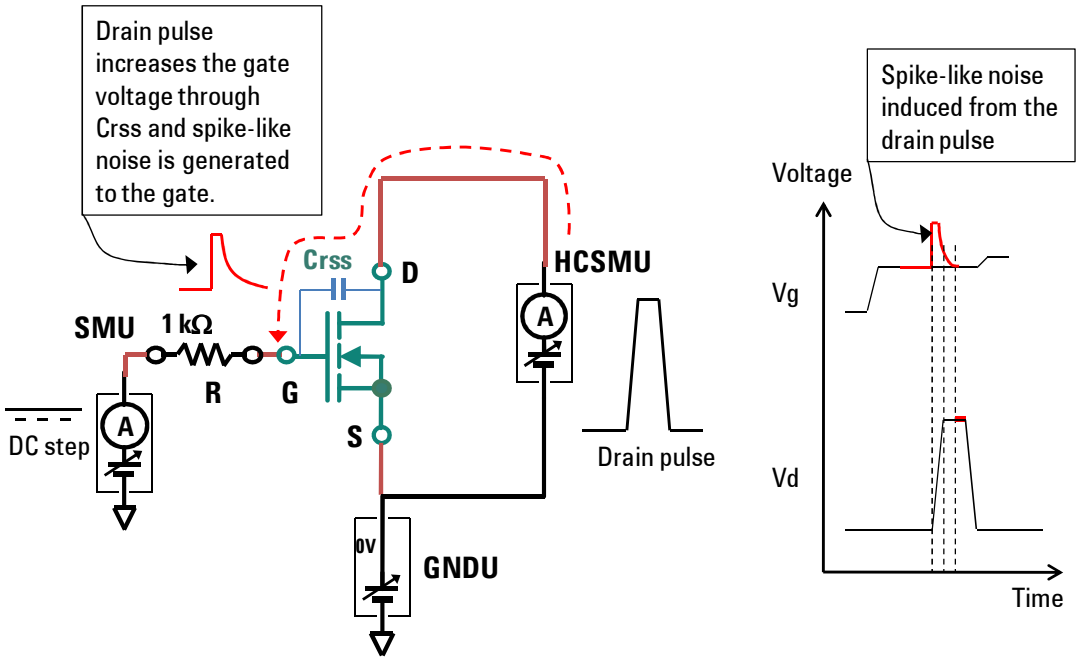
Figure A3-12 shows a measurement circuit behavior by focusing to the gate signal when measuring a high-gm and high-current power MOS-FET with the figure A3-11 measurement approach. The



(a) Alternative pulsed Id-Vg measurements (b) Alternative pulsed Id-Vd measurements

Figure A3-11. Alternative one pulse source I/V using a HCSMU pulse applied to the drain.

transient current generated by the HCU pulse and the relatively large Crss reverse transfer capacitance is converted to a spike-like noise in gate signal by the 1 kΩ resistor that is inserted for stabilizing the power MOS-FET operation. This spike-like voltage added on the normal gate bias as shown in figure A3-12(b) reflects back to the FET and the drain current increases more than the normal operating condition.



(a) Equivalent circuit diagram of pulsed measurement (b) Timing chart of the pulse

Figure A3-12. High current and high gm power MOS-FET measurement.

Figure A3-13 shows such an example as the current requested from the FET exceeds the current compliance of the HCSMU and the drain voltage is limited to a lower voltage than expected by the user.

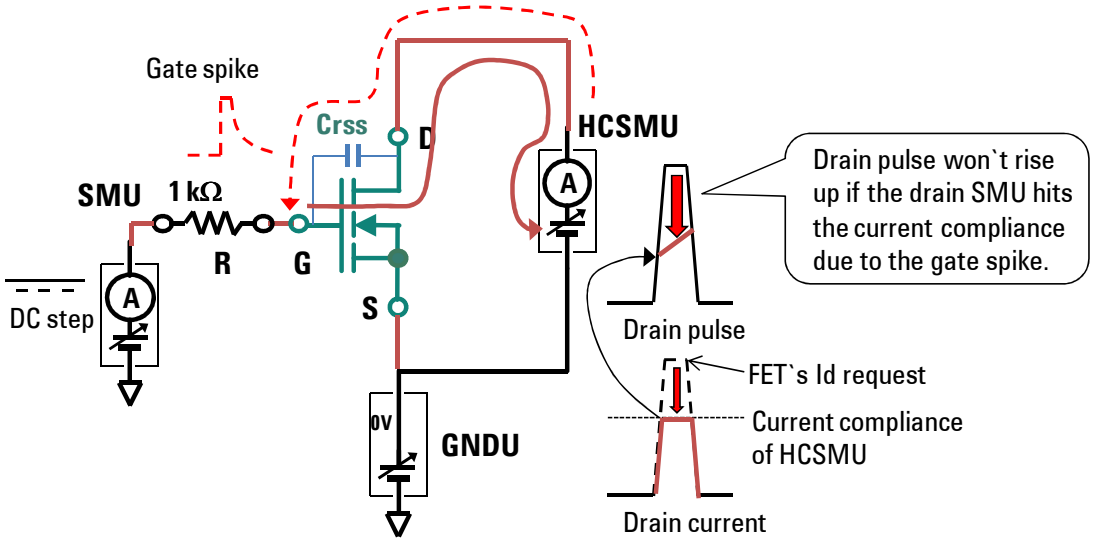


Figure A3-13. Drain pulse induced gate voltage rise-up (spike) unexpectedly increases the drain current.

Figure A3-14 shows an example of abnormal plot (thick line) measured by using the figure A3-11 approach where gate bias is a DC and a normal output (thin line) measured using the improved methods shown next. Figure A3-14 can be interpreted as the gate spike-like noise that increases the drain current to about or exceeding level of the current compliance of HCSMU around the area surrounded by a red circle of figure A3-14 and the measurement is aborted after HCSMU detects the current compliance status.

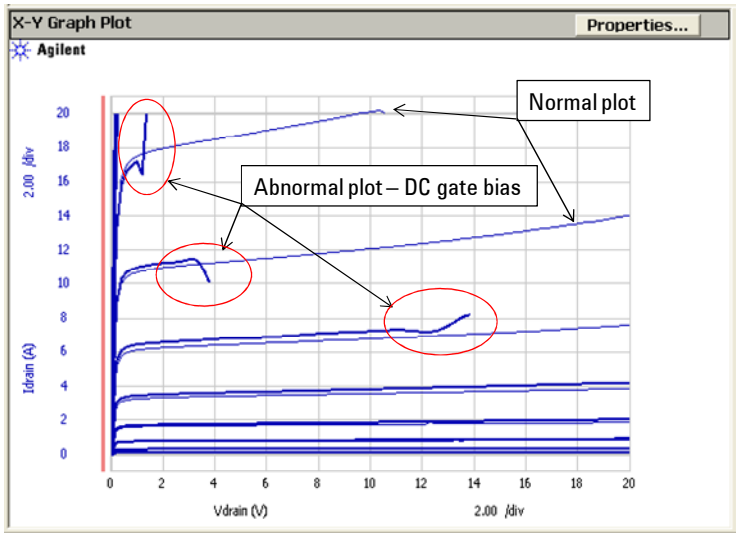
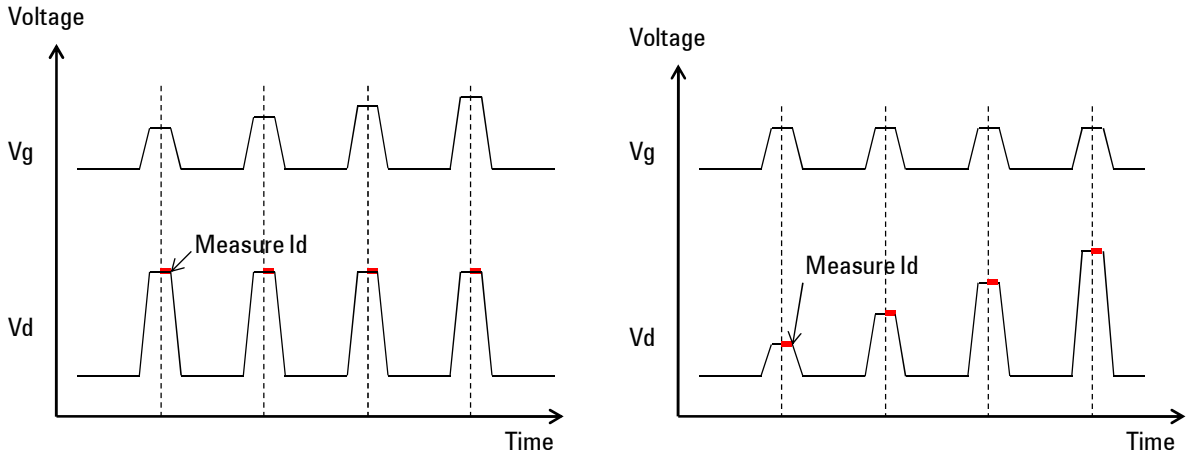


Figure A3-14. Example of an abnormal plot (thick line) of high-gm power MOS-FET.

A3-2-3 Improved two pulse source I/V

Figure A3-15 shows an improved pulsed IV approach for B1505A where the pulse is used for both the drain and the gate for power MOS-FET. Figure A3-16 shows the gate signal with both the gate pulse and the pulse-like noise from the drain pulse added. There is no obvious noise signal appearing to the gate because the spike-like noise from the drain is added to the base level of the gate pulse and it generally does not appear on the pulse level of the gate signal.



(a) Improved pulsed Id-Vg measurements

(b) Improved pulsed Id-Vd measurements

Figure A3-15. Improved two pulse source I/V applying pulses to both the drain and the gate.

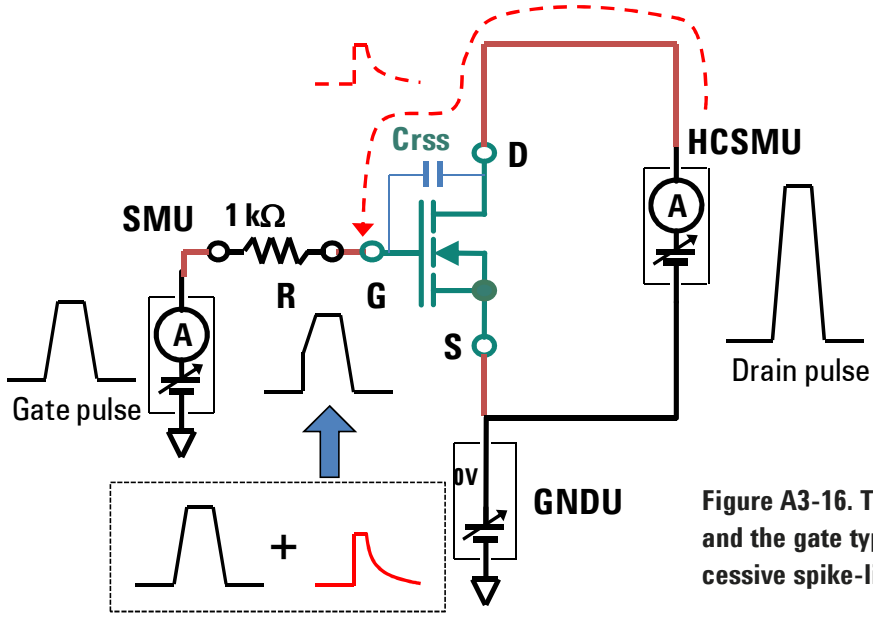


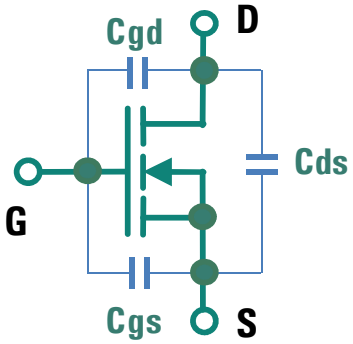
Figure A3-16. The pulse to both the drain and the gate typically suppresses an excessive spike-like noise.

Users are recommended to use this approach for all the pulsed I/V measurement of the power MOS-FET because the traditional approach also applying a pulse to the gate and this rule makes the pulsed I/V measurements of the B1505A much simpler and error free.

Figure A3-17 shows the stray capacitance components (Cds, Cgd, and Cgs) of MOS-FETs and these components can be measured by using the B1505A. The B1505A High Voltage Bias-T adapter facilitates these measurements by allowing the Multi-Frequency Capacitance Measurement Unit (MFCMU) to be used with the HVSMU to make capacitance measurements at up to 3000 V of DC bias.

In general, power MOS-FET specifications/data sheets list the capacitance components as input capacitance Ciss, output capacitance Coss, and reverse transfer capacitance Crss. Usually, these parameters are calculated from Cds, Cgs, and Cgd using the equations shown in Figure A3-17.

It is essential for using an AC guard technique when measuring one capacitance component separating from the other components connected in a circle chain like the MOS-FET.



MOS-FET parameters:
Coss: output capacitance
= Cds + Cgd
Ciss : input capacitance
= Cgs + Cgd
Crss : reverse transfer capacitance
= Cgd

Figure A3-17. Stray capacitances of MOS-FET and the MOS-FET parameters.

AC guard technique

Figure A3-18 shows the basic block diagram of MFCMU with high, low and guard terminal where the guard is basically a circuit common potential. “V” is the vector voltage of the AC output signal and “i” is the vector current flowing into the low terminal and the measured impedance is expressed as Z=V/i or C=1/(2 x pi x f x Z) where f is the AC signal frequency. The figure also shows three capacitors C1, C2 and C3 where C1 and C2 are connected to guard.

The AC signal i1 passing through the capacitor component C1 is flowing into the guard terminal and goes back to the AC signal source without passing through the AC meter. Since the signal passing through C1 is not measured by the AC meter, C1 is not counted as a measured component. For C2, there is no signal passing through C2 because there is no potential between the guard and the low terminal, and no current is measured by the AC meter as well as C1. Only the current i3 passing through C3 is measured by the AC meter and this is converted to C3 as MFCMU measured capacitance.

If C1 and C2 are not connected to the guard, then the current flowing through C1 and C2 are measured by the AC meter and count as an additional capacitance.

In this way, you can distinguish capacitive components by effectively utilizing the guarding technique.

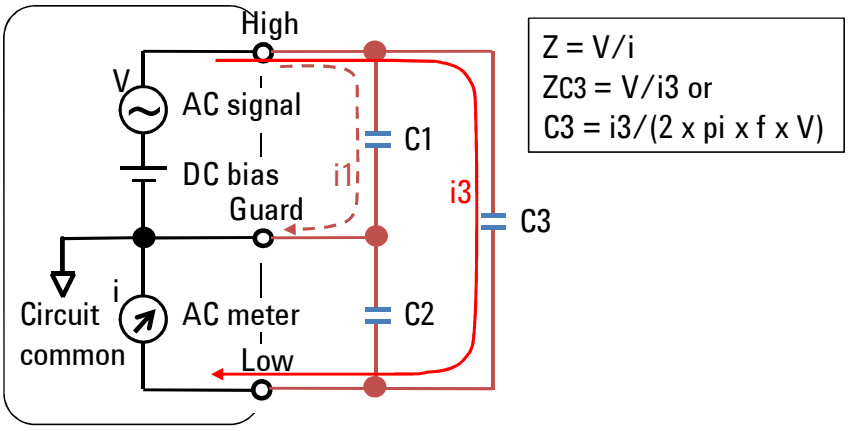


Figure A3-18. Basic CV measurement block diagram of the MFCMU.

Measurement frequency and SMU guard

Traditionally, a 1 MHz test signal is used for measuring the capacitive components of semiconductor devices.

Using 100 kHz test signal sometimes make the test much easier or more accurate when extracting the stray capacitor components. Figure A3-19, as an example, shows an equivalent circuit for measuring Cgs including the inductance Lsmu of the SMU measurement cable and extra DC blocking & AC bypass capacitor Cguard for guarding purpose.

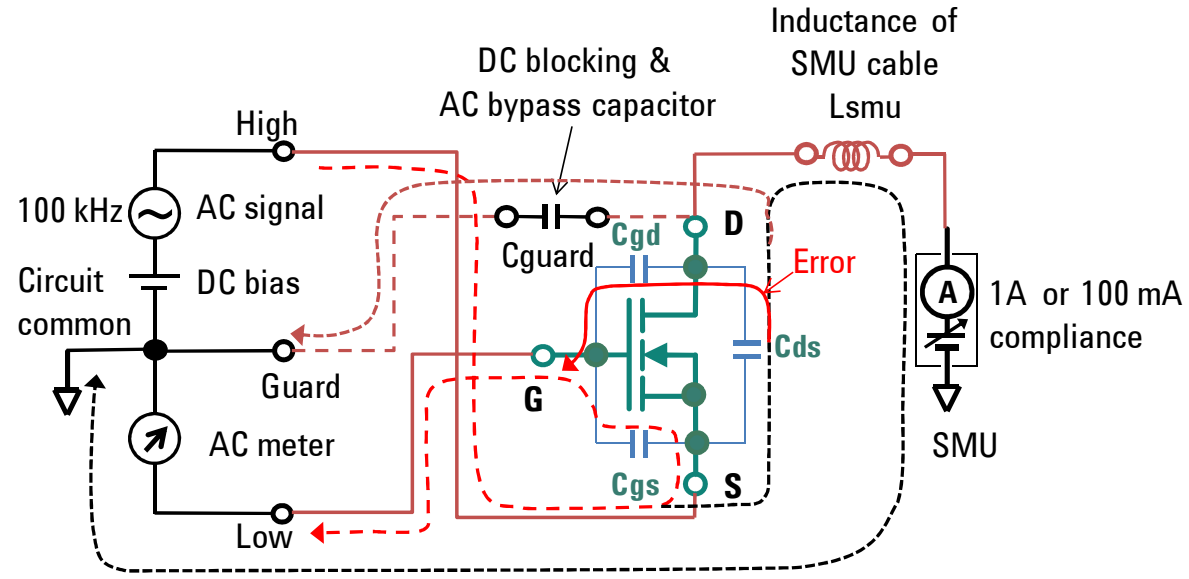


Figure A3-19. Cgs measurement tips.

When measuring Cgs, we want to measure only the AC signal passing through Cgs and the other signals blanching out to the drain terminal are to return to guard contact. In the figure, there are two paths: one is goes through the drain bias SMU, and the other is Cguard. If we use 1MHz AC measurement frequency, then about 1 μF capacitor Cguard is necessary. But if we reduce the AC measurement frequency to 100 kHz, then we may disconnect the extra 1 μF capacitor and just replace it by a direct connected SMU.

If we reduce the AC measurement frequency from 1 MHz to 100 kHz, the impedance of the capacitor increases ten times and the impedance of the inductance of the cable decreases to one tenth and the impedance ratio of the capacitor and the inductance becomes one hundred times different ratio.
The impedance of 1 μF capacitor and 3 μH inductance (rough number considering the inductance of the SMU cable) is almost the same at 100 kHz. It means the drain SMU can be considered as doing the same function as the Cguard with an assumption that the SMU potential is almost the same as the guard potential at 100 kHz.

Note that an error signal passing through Cdg becomes larger when any of the stray capacitor components get larger and the measurement accuracy degrades. In such a case, a better solution is further reducing the AC measurement frequency by taking the SMU

For verifying the SMU guarding capability below 100 kHz test signal, a comparison as an experiment for measuring the Cds parameter is made by using the connection of figure A3-20 by switching the gate connection between the AC guard and the SMU guard measurement

Figure A3-21 shows one verification of SMU guarding capability by Cds measurements where thick line is the data with AC guard and thin line is with SMU guard. You can see about 1.5% differences in the magnified window. The capacitance without the guard connection shows about 300 pF larger number and we can conclude the guard technique works well even for the SMU guard if the measurement frequency is less than 100 kHz.

Note: The SMU guard technique is only effective with a measurement signal of less than around 100 kHz because the resonant frequency of the cable and the capacitor is in a MHz range and the error becomes extremely large above 100 kHz.

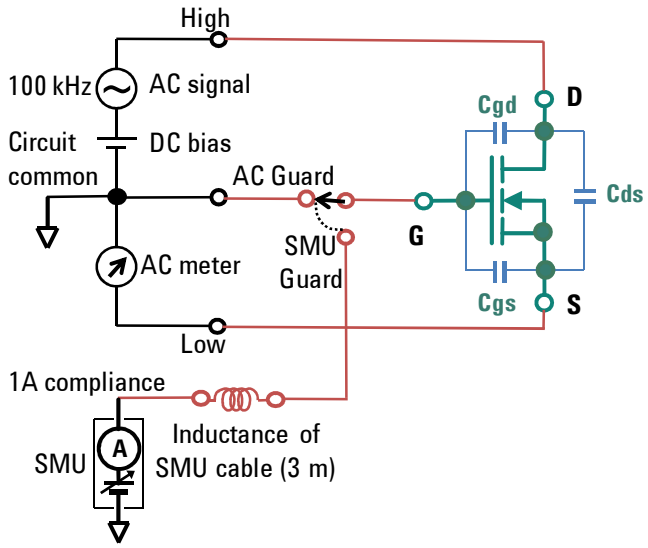


Figure A3-20. Switch between the AC Guard and the SMU Guard for experiment

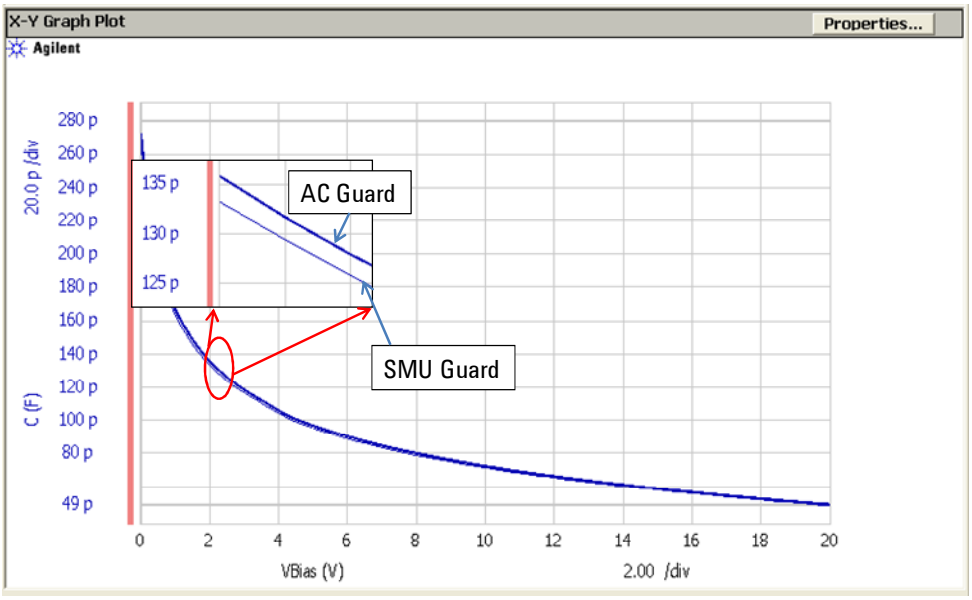


Figure A3-21. Cds data comparison at 100 KHz measurement signal.

Appendix 4: Before returning the demo-B1505A

If your practice of this measurement handbook is with an Agilent demo-B1505A, you may want to keep your measurement data for future reference and want to delete your foot print from the demo-B1505A before returning it to Agilent.

This section provides information about this topic.

A4-1. Saving the measurement data

You can save the measurement data in several formats.
This section introduces to save the data in EasyEXPERT format so that you can import the data to B1505A or Desktop EasyEXPERT for keeping the maximum flexibility for managing the data.

You can download Desktop EasyEXPERT software and can install to your Windows® PC.

Please keep the original Application Test library of this measurement handbook if you are exporting your data as EasyEXPERT format.
When you upload your data to Desktop EasyEXPERT software, you are required to install the Application Test library first before importing the measurement data in case where the parent application library is not installed in the EasyEXPERT.

[Exporting procedure]

Follow the instructions shown in figure A4-1. The number in the figure corresponds to the following step number.

Step 1. Click the upper arrow for expanding the results area.

Step 2. Results area expands as shown in the right side figure.

Step 3. Select the data to export. Selected data changes the background color to blue as shown in the figure.

Step 4. Left click "Results" bar.
Result area menu opens.

Step 5. Select "Transport Data".
Next menu appears.

Step 6. Select "Export As Compressed Test Result ...".
Then "Compressed Test Result Export" Explore opens.
Enter file name and save your data to an appropriate recording media.

Note: Your saved data is the same format as the example results data used in this measurement handbook.
Use the same steps when you recover your data in different EasyEXPERT software.

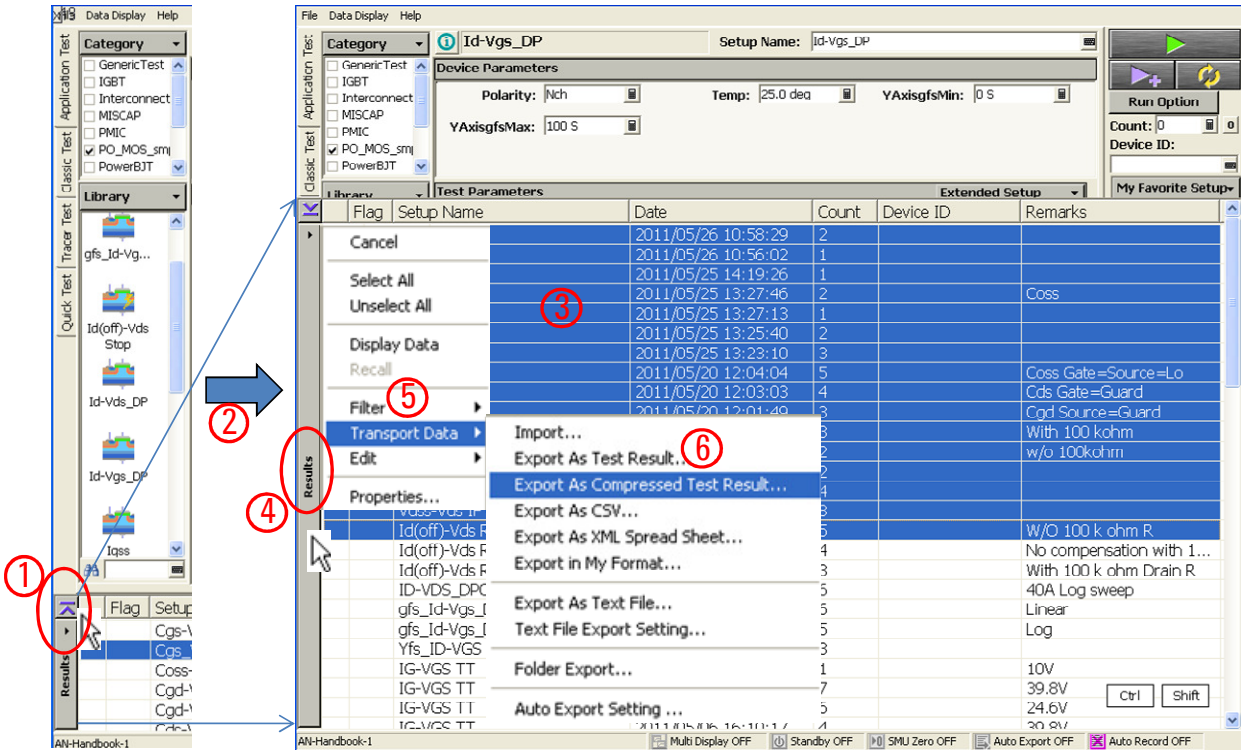


Figure A4-1. Expanding the Results area and select measurement data sets.

A4-2. Deleting the workspace and measured data

Deleting of your foot print from the demo B1505A is easiest by deleting your workspace from the Workspace management page.

You can open the Workspace management page by standard startup process or using the methods shown in appendix section A1-2.

Figure A4-2 shows the steps for deleting existing Workspace.
Follow the instruction steps as follows. The instruction steps match the number in the figure.

Please be careful doing your work since there is no way for recovering the data once it has been erased.

[Deleting procedure]

Step 1. Check "Your Workspaces:".

Step 2. Press "Manage Workspace" button.

Step 3. Workspace manager sub window opens.

Step 4. Select the Workspace name from the "Available Workspaces:" list.

Step 5. Press "Delete" button. Confirmation sub-window pops up.

Step 6. Press "OK" button in the Confirmation sub-window.

Your Workspace is deleted with all of your data and setups from EasyEXPERT.

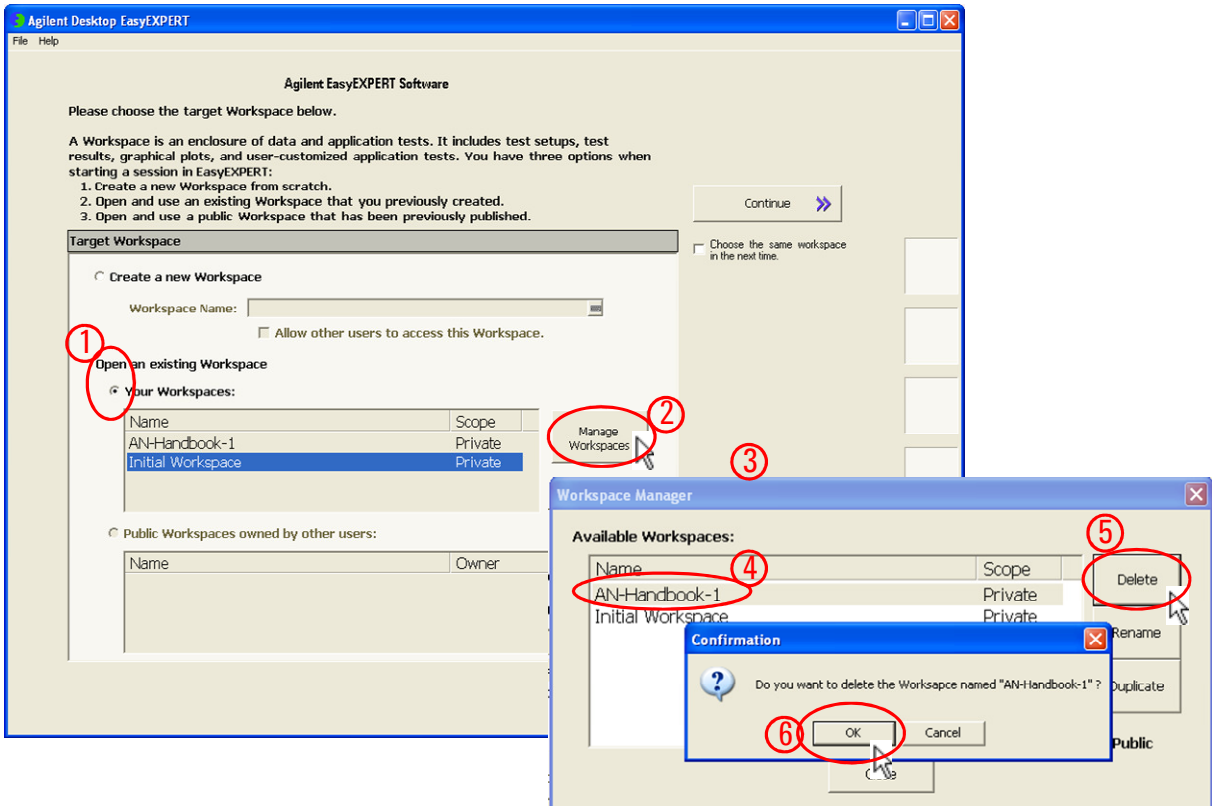


Figure A4-2. Deleting existing Workspace from EasyEXPERT.

B1505-90080
www.keysight.com