SD1 3.x Software Drivers

The SD1 3.x software drivers are designed to work on M31xxA Digitizers, M32xxA AWGs, M33xxA Combos.

This document contains information about the new and modified features in the SD1 3.x software drivers.

Related Documents

For detailed information, refer to the following Help documents. The Online Help format can be accessed from within the SD1 3.x Software after installation.

Document name	Location	Format
SD1 3.x Software Startup Guide SD1 3.x Software for M320xA / M330xA Arbitrary Waveform Generators User's Guide SD1 3.x Software for M310xA / M330xA Digitizers User's Guide	M3201A PXIe Arbitrary Waveform Generators Document Library M3202A PXIe Arbitrary Waveform Generators Document Library M3100A PXIe Digitizer Document Library M3102A PXIe Digitizer Document Library M3300A PXIe AWG & Digitizer Combo Document Library M3302A PXIe AWG & Digitizer Combo Document Library	PDF
AWG User Guide.htm	C:\Program Files\Keysight\SD1\help\M32_M33XX_AWG	WebHelp
Digitizer User Guide.htm	C:\Program Files\Keysight\SD1\help\M31_M33XX_Digitizer	WebHelp

Refer to the SD1 3.x Startup Guide for information pertaining to the various module types and the corresponding configuration/options supported for each module.

SD1 3.x Software

Release Version 3.04.08

Released Date	4th August, 2022
Operating System	Microsoft Windows 10 (x64 bit)
HVI Core	2.7.0
HVI Engine	1.7.2
PathWave Test Sync Executive software version	2022 (version 2.7.7) released on 1st July 2022
Board Support Package (BSP)	0.3.206.0
PathWave FPGA software version	2021 Update 1.0 (version 2021_2.5.11.0) released on 4th Oct. 2021
Firmware Update Packages (Upgrade FW for SW & BSP compatibility)	M3202A (AWG 1G) FW version >= 4.03.00 M3201A (AWG 500) FW version >= 4.04.00 M3102A (DIG 500) FW version >= 2.03.00 M3100A (DIG 100) FW version >= 2.03.00 M3302A (COMBO 500 500) FW version >= 4.03.00 M3300A (COMBO 500 100) FW version >= 4.03.00
File Name:	SD1software_3.04.08_installer.exe

Changes

- End-of-Support for the CLV option in the M32xxA modules. Any references to CLV in the documentation pertaining to the M3xxxA modules shall be considered void.
- Added a new API
    - initializeClock() for clock alignment between M32XXA modules and M5000-series modules, in case SD1 modules have not been added to the HVI sequence.

Known behavior

- You may encounter issues with M3xxxA module functionality when you install the M3xxxA cards in the M9046A PXIe High-Performance chassis, as part of a multi-chassis multi-module setup. To recover the system from such issues, refer to the Troubleshooting steps documented in the *SD1 3.x Software Startup Guide*.

Release Version 3.03.12

Released Date	14th December, 2021
Operating System	Microsoft Windows 10 (x64 bit)
HVI Core	1.15.6
HVI Engine	1.6.0
PathWave Test Sync Executive software version	2021 (version 1.15.7) released on 13th Dec. 2021
Board Support Package (BSP)	0.3.135.0
PathWave FPGA software version	2021 Update 1.0 (version 2021_2.5.11.0) released on 4th Oct. 2021
Firmware Update Packages (Upgrade FW for SW & BSP compatibility)	M3202A (AWG 1G) FW version >= 04.02.45 M3201A (AWG 500) FW version >= 04.03.67 M3102A (DIG 500) FW version >= 02.02.46 M3100A (DIG 100) FW version >= 02.02.44 M3302A (COMBO 500 500) FW version >= 04.02.45 M3300A (COMBO 500 100) FW version >= 04.02.47
File Name:	SD1software_3.03.12_installer.exe

Changes

- Added new APIs:
  - firmwareUpdate() to update module's firmware in offline mode using an **.sdpkg* file.
  - setTriggerBehaviourMode() to switch AWG trigger behavior from that of SD1 3.x to SD1 2.x and vice-versa.

Defect fixes

- Fixed issue with AWGqueueMarkerConfig() API, which was throwing an unexpected Windows error, whenever the API was called with HVI sequence loaded to hardware.
- Fixed issue in M33xxA Combo with playback and acquisition while acquiring waveform data generated from the same module.
- Fixed DAQcounterRead() API when DAQ is configured with negative delay.
- Fixed issue with loading k7z bitstream on M3100A DIG 100 cards using the PathWave Test Sync Executive API load_from_k7z().
- Fixed issue with *DAQdigitalTriggerConfig.vi*, where an unexpected error code (-8040) occurred when PXI trigger was selected as trigger source.

Known behavior

- Modules with Variable Clock (-CLV) option support only the default clock frequency of 500 MHz on AWG 500 (M3201A) and 1 GHz on AWG 1G (M3202A), respectively. Other clock frequencies are not supported currently.

Release Version 3.02.52

Released Date	23rd June, 2021
Operating System	Microsoft Windows 10 (x64 bit)
HVI Core	1.4.15 (beta)
HVI Engine	0.17.32
Board Support Package (BSP)	0.3.61.0
Firmware Update Packages (Upgrade FW for SW & BSP compatibility)	M3202A (AWG 1G) FW version >= 4.02.11 M3201A (AWG 500) FW version >= 4.03.27 M3102A (DIG 500) FW version >= 2.02.06 M3100A (DIG 100) FW version >= 2.02.10 M3302A (COMBO 500 500) FW version >= 4.02.10 M3300A (COMBO 500 100) FW version >= 4.02.11
File Name:	SD1software_3.02.52_installer.exe

Changes

- The source files for Python wrapper at *C:\Program Files\Keysight\SD1\Libraries\Python* are no longer available to be added to the Python path directly. SD1 Python wrapper is now installed as a Python package in the site-packages directory. To setup other python environments after SD1 installation, package file (*.tar.gz) is still available in the *C:\Program Files\Keysight\SD1\Libraries\Python* folder.

Defect fixes

- For M3300A modules with C48 option, the DAQ HVI Actions and Events for all channels are now available for Python, C++ and .Net wrappers.
- Fixed issue with triggering a module using PXI line as the external trigger source while using another module with the trigger behavior “TRIGGER_RISE”.

Release Version 3.02.09

Released Date	31st May, 2021
Operating System	Microsoft Windows 10 (x64 bit)
HVI Core	1.4.15 (beta)
HVI Engine	0.17.32
Board Support Package (BSP)	0.3.61.0
Firmware Update Packages (Upgrade FW for SW & BSP compatibility)	M3202A (AWG 1G) FW version >= 4.02.11 M3201A (AWG 500) FW version >= 4.03.27 M3102A (DIG 500) FW version >= 2.02.06 M3100A (DIG 100) FW version >= 2.02.10 M3302A (COMBO 500 500) FW version >= 4.02.10 M3300A (COMBO 500 100) FW version >= 4.02.11
File Name:	SD1software_3.02.09_installer.exe

Changes

- Updated FirmWare to support HVI engine 0.17.32 on all modules.
- SD1 version 3.02.09 software now supports HVI core 1.4.15_beta.
- SD1 Python wrapper is now installed as a Python package in the site-packages directory.
- Support for CH8 option with HVI2 on DIG 100 (M3100A) modules.
- Support for C48 option (4-Ch AWG 8-Ch DIG) with HVI2 on Combo 500 100 (M3300A) modules.
- Added FPGA support to query Kernel UUID for the K7z bitstream loaded onto the module.
- Replaced “newFromArrayDoubleNP()” Python API with “newFromArrayDouble()” API.
- Improved performance of the following APIs by using NumPy conversion methods for faster data conversion from Python to C:
    - newFromArrayDouble()
    - newFromArrayInteger()
    - writeRegisterBuffer()
    - waveformReLoadArrayInt16()
    - AWGfromArray()
    - FFT()

- Improved performance of the following APIs:
    - channelPrescalerConfig()
    - DAQflush()
    - DAQconfig()
    - AWGflush()
    - AWGqueueWaveform()
    - channelAmplitude()
    - channelOffset()

Defect fixes

- Fixed the transient effect and the additional delay of 10 ns observed in Frequency modulation with respect to the other modulation types.

Known behavior

- Modules with Variable Clock (-CLV) option support only the default clock frequency of 500 MHz on AWG 500 (M3201A) and 1 GHz on AWG 1G (M3202A), respectively. Other clock frequencies are not supported currently.
- Setting higher number of acquisition points may result in performance degradation of the SD1 SFP.
- Read/Write operations on the Host Register memory, which exists as PathWave FPGA sub-module, is not supported.
- For M3300A modules with C48 option, the DAQ HVI Actions and Events associated with Channels 5 to 8 are currently not available in the Python, C++ and .Net wrappers.
- If you use a separate module with PXI line as external trigger source to trigger a module, you shall notice that the trigger behavior “TRIGGER_RISE” does not work, whereas only “TRIGGER_FALL” works. However, both “TRIGGER_RISE” and “TRIGGER_FALL” work when PXI trigger is provided by the same module.

Workaround

- When using the DDR interface of the M3xxxA BSPs, there is a known issue that is observed while you load the bitfile (k7z) directly through a script. As a workaround, load the bitfile using the SD1 Soft Front Panel (SFP) and run your script again.

Release Version 3.01.54

Released Date	19th March, 2021
Operating System	Microsoft Windows 10 (x64 bit)
HVI Core	1.4.11 (beta)
HVI Engine	0.17.32 (supported on M3202A, M3201A and M3102A modules only)
	0.17.9 (supported on M3100A, M3302A and M3300A modules only)
Board Support Package (BSP)	0.2.162.0 (supported on M3202A, M3201A and M3102A modules only)
	0.2.139.0 (supported on M3100A, M3302A and M3300A modules only)
Firmware Update Packages (Upgrade FW for SW & BSP compatibility)	M3202A (AWG 1G) FW version >= 4.01.33 M3201A (AWG 500) FW version >= 4.03.02 M3102A (DIG 500) FW version >= 2.01.80 M3100A (DIG 100) FW version >= 2.01.02 M3302A (COMBO 500 500) FW version >= 4.01.02 M3300A (COMBO 500 100) FW version >= 4.01.53
File Name:	SD1software_3.01.54_installer.exe

Changes

- Updated FirmWare to support HVI engine 0.17.32 on AWG 1G, AWG 500 and DIG 500 modules.
- SD1 version 3.01.54 software supports HVI core 1.4.11_beta.
- Enhanced timing performance of the SD1 software.

Defect fixes

- Temp files, which are generated when FPGAconfigureFromK7z() and FPGALoad() APIs are called, are now deleted automatically when using Spyder IDE.
- Bitstream files can now be simultaneously loaded onto more than one module.
- No pop-up windows observed when FPGAload() API is called using the original Python script via pythonw.
- Functionality of trigger mode SWHVITRIG_CYCLE has been fixed in AWG modules.

Workaround

- If you encounter an error, “Unknown error while running C:\Program Files(x86)\Keysight\SD1\uninstall.exe – mode unattended” when installing the SD1 software, a likely cause may be an unsuccessful removal of the previously installed SD1 software. In such cases, manually clean the following directories: *C:\Program Files\Keysight\SD1* and *C:\Program Files (x86)\Keysight\SD1* before trying to install SD1 again.

Release Version 3.01.10

Released Date	6th January, 2021
Operating System	Microsoft Windows 10 (x64 bit)
HVI Core	1.4.3 (alpha)
HVI Engine	0.17.9
Board Support Package (BSP)	0.2.139.0
Firmware Update Packages (Upgrade FW for SW & BSP compatibility)	M3202A (AWG 1G) FW version >= 4.01.20 M3201A (AWG 500) FW version >= 4.02.85 M3102A (DIG 500) FW version >= 2.01.60 M3100A (DIG 100) FW version >= 2.01.02 M3302A (COMBO 500 500) FW version >= 4.01.02 M3300A (COMBO 500 100) FW version >= 4.01.53
File Name:	SD1software_3.01.10_installer.exe

Changes

- Updated SD1 version 3.1 FirmWare to support HVI engine 0.17.9 and SD1 version 3.1 Software supports HVI core 2020 U1 (1.4.3_alpha).
- Modified both SD1 SFP and wrapper interfaces to support x64 architecture only. Removed 32-bit support in SD1 SFP from version 3.1 onwards.
- Modified location of SD1 API libraries to *C:\Program Files\Keysight\SD1\Libraries*.
- Added support for BSP (-FP1 option) on M3100A, M3300A and M3302A modules.
- Added support for Variable Clock (-CLV) option on M3202A and M3201A modules, with synchronization currently restricted to default clock frequency only.
- Added support for LabVIEW and MATLAB programming in SD1 software API.
- Modified list in SD1 SFP Hardware Manager to display firmware versions that are compatible with SD1 version 3.1 only. Incompatible (backward) firmware versions will not be displayed.
- Installing / Upgrading to SD1 version 3.1 is mandatory prior to upgrading module with the latest FW versions, which are compatible with SD1 3.1 software and latest BSP version.
- Fixed issue with Trigger IO Read on M3100A and M3300A modules.
- Added new APIs to configure sandbox registers and to obtain Kernel UUID from K7z bitfile.
- Modified certain APIs to verify that the values you input for the related parameters are within the defined range.

Known behavior

- Temp files, which are generated when FPGAconfigureFromK7z() and FPGALoad() APIs are called, are not deleted automatically when using Spyder IDE only.
- Keysight does not recommend simultaneous loading of bitstream files to more than one module.
- Modules with variable clock (-CLV) option currently do not support synchronization with clock frequencies different from the default clock frequency.

- SD1 SFP may show performance degradation upon setting higher number of acquisition points.

Release Version 3.00.95

Released Date	30th September, 2020
Operating System	Microsoft Windows 10 (x64 bit)
HVI Core	1.0.14
HVI Engine	0.17.8
Board Support Package (BSP) (for M3202A, M3201A and M3102A modules only)	0.2.101.0
Firmware Update Packages (Upgrade FW for latest BSP compatibility on supported modules)	M3202A (AWG 1G) FW version >= 4.00.95 M3201A (AWG 500) FW version >= 4.02.65 M3102A (DIG 500) FW version >= 2.01.40 M3100A (DIG 100) FW version >= 2.00.30 M3302A (COMBO 500 500) FW version >= 4.00.31 M3300A (COMBO 500 100) FW version >= 4.01.32
File Name:	SD1software_3.00.95_installer.exe

Changes

- Updated HVI Core 1.0.14 and HVI Engine 0.17.8 in SD1.
- Added 48-bit HVI register support on all AWG and DIG modules.
- Updated the M3XXXA driver software for compatibility on National Instruments (NI) equipment and with NI software.
- Added Literals APIs for DIG HVI instructions.
- Fixed defects in M3100A DIG 100, M3201A AWG 500, M3202A AWG 1G modules and Soft Front Panel (SFP).

Release Version 3.00.89

Released Date:	17th August, 2020
Operating System:	Microsoft Windows 10 (x64 bit)
HVI Core	1.0.2
HVI Engine	0.17.1
Supported Modules (with corresponding Firmware version)	M3100A (DIG 100) FW version >= 2.0 M3102A (DIG 500) FW version >= 2.0 M3201A (AWG 500) FW version >= 4.0 M3202A (AWG 1G) FW version >= 4.0 M3300A (COMBO 500 100) FW version >= 4.0 M3302A (COMBO 500 500) FW version >= 4.0
File Name:	SD1software_3.00.89_installer.exe

New Features

- Modules supported for HVI integration using KS2201A PathWave Test Sync Executive software
  - M3202A AWG 1G (Fixed Clock) (4 CH) (FPGA - K16 / K32 / K41)
  - M3201A AWG 500 (Fixed Clock) (4 CH) (FPGA - K16 / K32 / K41)
  - M3102A DIG 500 (Fixed Clock) (4 CH) (FPGA - K16 / K32 / K41)
  - M3100A DIG 100 (Fixed Clock) (4 CH) (FPGA - K32 / K41)
  - M3302A Combo 500-500 (Fixed Clock) (2 CH AWG, 2 CH DIG) (FPGA - K41)
  - M3300A Combo 500-100 (Fixed Clock) (2 CH AWG, 4 CH DIG) (FPGA - K41)
- BSP (PathWave FPGA) Support for M3202A AWG 1G, M3201A AWG 500, M3102A DIG 500
- Software Interfaces Supported : Python, .NET, C++