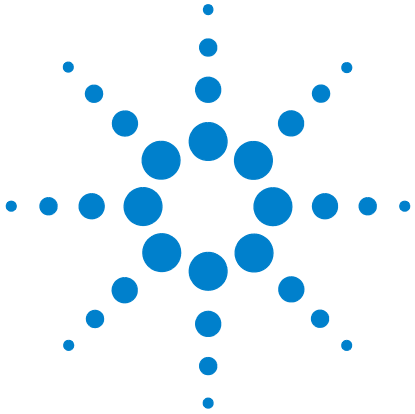

Agilent U7245A GDDR5 Compliance Test Application

Compliance Testing Notes

Agilent Technologies

Notices

Manual Part Number

U7245-97000

Edition

First edition, September 2010

Printed in USA

Agilent Technologies, Inc.
1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

Warranty

The material contained in this document is provided "as is," and is subject to being changed, without notice, in future editions. Further, to the maximum extent permitted by applicable law, Agilent disclaims all warranties, either express or implied, with regard to this manual and any information contained herein, including but not limited to the implied warranties of merchantability and fitness for a particular purpose. Agilent shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein. Should Agilent and the user have a separate written agreement with warranty terms covering the material in this document that conflict with these terms, the warranty terms in the separate agreement shall control.

Technology Licenses

The hardware and/or software described in this document are furnished under a license and may be used or copied only in accordance with the terms of such license.

Restricted Rights Legend

If software is for use in the performance of a U.S. Government prime contract or subcontract, Software is delivered and licensed as "Commercial computer software" as defined in DFAR 252.227-7014 (June 1995), or as a "commercial item" as defined in FAR 2.101(a) or as "Restricted computer software" as defined in FAR 52.227-19 (June 1987) or any equivalent agency regulation or contract clause. Use, duplication or disclosure of Software is subject to Agilent Technologies' standard commercial license terms, and non-DOD Departments and Agencies of the U.S. Government will receive no greater than Restricted Rights as defined in FAR 52.227-19(c)(1-2) (June 1987). U.S. Government users will receive no greater than Limited Rights as defined in FAR 52.227-14 (June 1987) or DFAR 252.227-7015 (b)(2) (November 1995), as applicable in any technical data.

Safety Notices

CAUTION

A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

GDDR5 —Quick Reference

Table 1 GDDR5 Cycles and Signals

NOTE: 1 = Single Ended probing; 2 = Differential probing; 3 = 2 x Single Ended probing

TEST	Cycle		Based on Test Definition						Required to Perform on Scope						Opt.
	Read	Write	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	CS#
tJIT(per)					√						√[2]				
tJIT(cc)					√						√[2]				
tERR(nper)					√						√[2]				
tCH(avg)					√						√[2]				
tCL(avg)					√						√[2]				
tJIT(duty)					√						√[2]				
tCK(avg)					√						√[2]				
SlewR		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
SlewF		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
VIH(ac)		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
VIH(dc)		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
VIL(ac)		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
VIL(dc)		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
SRQseR	√		√	√					√[1]	√[1,2]					
SRQseF	√		√	√					√[1]	√[1,2]					
VOH(ac)	√		√	√					√[1]	√[1,2]					
VOH(dc)	√		√	√					√[1]	√[1,2]					
VOL(ac)	√		√	√					√[1]	√[1,2]					
VOL(dc)	√		√	√					√[1]	√[1,2]					
AC Overshoot			√	√	√	√	√	√	√[1]	√[1]	√[1]	√[1]	√[1]	√[1]	
AC Undershoot			√	√	√	√	√	√	√[1]	√[1]	√[1]	√[1]	√[1]	√[1]	
VIX(ac)		√		√	√					√[3]	√[3]				

Table 1 GDDR5 Cycles and Signals

NOTE: 1 = Single Ended probing; 2 = Differential probing; 3 = 2 x Single Ended probing

TEST	Cycle		Based on Test Definition						Required to Perform on Scope						Opt.
	Read	Write	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	CS#
Eye Diagram - Read	√		√	√					√[1]	√[2]					
Eye Diagram - Write		√	√	√					√[1]	√[2]					
tDQSCK	√			√	√				√[1]	√[2]	√[2]				√
tHZ(DQ)	√		√		√				√[1]	√[2]	√[2]				√
tLZ(DQS)	√			√	√				√[1]	√[2]	√[2]				√
tLZ(DQ)	√		√		√				√[1]	√[2]	√[2]				√
tDQSQ	√		√	√					√[1]	√[2]	√[2]				√
tQH	√		√	√					√[1]	√[2]	√[2]				√
tDQSS		√		√	√				√[1]	√[2]	√[2]				√
tDQSH		√		√					√[1]	√[2]	√[2]				√
tDQSL		√		√					√[1]	√[2]	√[2]				√
tDSS		√		√	√				√[1]	√[2]	√[2]				√
tDSH		√		√	√				√[1]	√[2]	√[2]				√
tWPST		√		√					√[1]	√[2]	√[2]				√
tWPRE		√		√					√[1]	√[2]	√[2]				√
tRPRE	√			√					√[1]	√[2]	√[2]				√
tRPST	√			√					√[1]	√[2]	√[2]				√
tDS(base)		√	√						√[1]	√[2]	√[2]				√
tDH(base)		√	√						√[1]	√[2]	√[2]				√
tIS(base)		√			√	√	√				√[2]	√[1]	√[1]		√
tIH(base)		√			√	√	√				√[2]	√[1]	√[1]		√

GDDR5 Compliance Test Application — At A Glance

The Agilent U7245A GDDR5 Compliance Test Application is a GDDR5 (Graphics Double Data Rate 5) test solution that covers electrical, clock and timing parameters of the JEDEC (Joint Electronic Device Engineering Council) specifications, specifically *JESD212*. The software helps you in testing all the device under test (DUT) compliance, with the Agilent 90000A or 90000X Series Infiniium digital storage oscilloscope.

There are 2 main categories of test modes:

- Compliance Tests - These tests are based on the GDDR5 JEDEC compliance specifications and are compared to corresponding compliance test limits.
- Custom Tests - These tests are not based on any compliance specification. The primary use of these tests is to perform signal debugging.

The GDDR5 Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Allows you to determine the number of trials for each test, with the new multi trial run capability.
- Provides detailed information of each test that has been run. The result of maximum twenty five worst trials can be displayed at any one time.
- Creates a printable HTML report of the tests that have been run.

The minimum number of probes required for the tests are:

- Clock tests - 1 probe.
- Electrical tests - 3 probes.
- Clock Timing tests - 3 probes.
- Custom tests - 3 probes.

NOTE The tests performed by the GDDR5 Compliance Test Application are intended to provide a quick check of the physical layer performance of the DUT. These testing are not replacement for an exhaustive test validation plan.

GDDR5 SGRAM electrical, clock and timing test standards and specifications are described in the *JESD212* document. For more information, please refer to JEDEC web site at www.jedec.org.

Required Equipment and Software

In order to run the GDDR5 automated tests, you need the following equipment and software:

- 90000A or 90000X Series Infiniium Digital Storage Oscilloscope. Agilent recommends using 10 GHz and higher bandwidth oscilloscope.
- Infiniium software revision revision 2.10 (90000 Series) or later.
- U7245A GDDR5 Compliance Test Application.
- 116xA, 113xA, N280xA InfiniiMax probe amplifiers.
- N5381A or E2677A differential solder-in probe head, N5382A or E2675A differential browser probe head, N5425A ZIF probe head or N5426A ZIF tips.
- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).

Below are the required licenses:

- U7245A GDDR5 Compliance Test Application license.
- N5414A InfiniiScan software license. (90000A, 90000X Series)
- E2688A Serial Data Analysis and Clock Recovery software license.
- N5465A InfiniiSim Waveform Tranformation Toolset (NOTE: This is optional if user does not need to perform probe de-embedding)

Contact Agilent

For more information on GDDR5 Compliance Test Application or other Agilent Technologies' products, applications and services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Phone or Fax

United States:

(tel) 800 829 4444

(fax) 800 829 4433

Canada:

(tel) 877 894 4414

(fax) 800 746 4866

China:

(tel) 800 810 0189

(fax) 800 820 2816

Europe:

(tel) 31 20 547 2111

Japan:

(tel) (81) 426 56 7832

(fax) (81) 426 56 7840

Korea:

(tel) (080) 769 0800

(fax) (080) 769 0900

Latin America:

(tel) (305) 269 7500

Taiwan:

(tel) 0800 047 866

(fax) 0800 286 331

Other Asia Pacific Countries:

(tel) (65) 6375 8100

(fax) (65) 6755 0042

E-mail: tm_ap@agilent.com

Contents

8 WCK Input Operating Conditions Tests

9 Data Input and Output Timing Tests

10 Custom Debug - Data Mask

11 Calibrating the Infiniium Oscilloscope and Probe

1 Installing the GDDR5 Compliance Test Application

If you purchased the U7245A GDDR5 Compliance Test Application separately, you need to install the software and license key.

Installing the Software

1 Make sure you have version 2.10 (90000 Series) or higher of the Infiniium oscilloscope software by choosing **Help>About Infiniium...** from the main menu.

2 To obtain the GDDR5 Compliance Test Application, go to Agilent website: http://www.agilent.com/find/U7245A.

3 The link for GDDR5 Compliance Test Application will appear. Double-click on it and follow the instructions to download and install the application software.

Installing the License Key

1 Request a license code from Agilent by following the instructions on the Entitlement Certificate.

You will need the oscilloscope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog box.

2 After you receive your license code from Agilent, choose **Utilities>Install Option License...**.

3 In the Install Option License dialog, enter your license code and click **Install License**.

4 Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.

5 Click **Close** to close the Install Option License dialog.

6 Choose **File>Exit**.

7 Restart the Infiniium oscilloscope application software to complete the license installation.

2 Preparing to Take Measurements

Before running the GDDR5 automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this GDRR5 application. After the oscilloscope and probe have been calibrated, you are ready to start the GDDR5 Compliance Test Application and perform the measurements.

Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope and probe, see Chapter 13, "Calibrating the Infiniium Oscilloscope and Probe".

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Agilent recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the GDDR5 Compliance Test Application

1 To start the GDDR5 Compliance Test Application: From the Infiniium oscilloscope's main menu, choose **Analyze>Automated Test Apps>GDDR5 Test**.

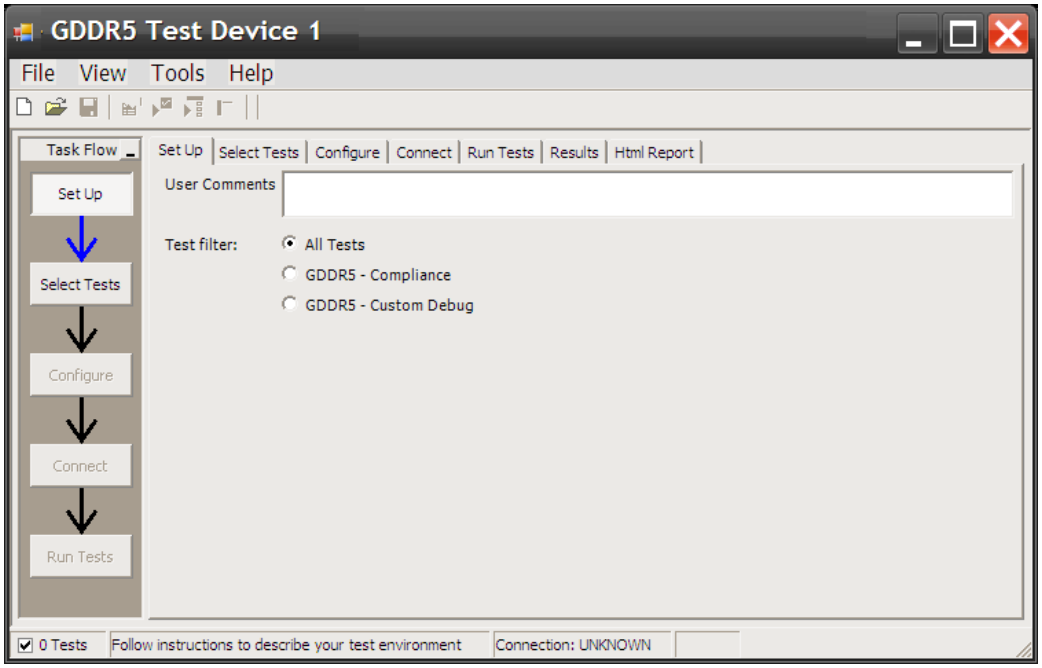

Figure 1 The GDDR5 Compliance Test Application

NOTE If GDDR5 Test does not appear in the Automated Test Apps menu, the GDDR5 Compliance Test Application has not been installed (see Chapter 1, "Installing the GDDR5 Compliance Test Application").

Figure 1 shows the GDDR5 Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Set Up	Lets you identify and setup the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.

Configure	Lets you configure test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE When you close the GDDR5 application, each channel's probe is configured as single-ended or differential depending on the last GDDR5 test that was run.

8 Clock AC Timing Tests

This section provides the Methods of Implementation (MOIs) for Clock Timing tests using an Agilent 90000A or 90000X Series Infiniium oscilloscope, recommended InfiniiMax 116xA, 113xA, or N280xA probe amplifiers, E2677A differential solder-in probe head and the GDDR5 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Clock Timing Tests

When performing the Clock Timing tests, the GDDR5 Compliance Test Application will prompt you to make the proper connections. Refer to the Connection tab in the GDDR5 Electrical Performance Compliance Test application for the exact number of probe connections.

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 185.

Test Procedure

1. Start the automated test application as described in “Starting the GDDR5 Compliance Test Application" on page 25.
2. Connect the differential solder-in probe head to the PUTs on the GDDR5 DUT.
3. Connect the oscilloscope probes to any channels of the oscilloscope.
4. In the GDDR5 Test application, click the Set Up tab.
5. You can select the test mode, GDDR5 compliance mode or custom mode. Enter your comments in the Comments text box.
6. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

Average Clock Period - tCK(avg) - Test Method of Implementation

This test is applicable to the Rising and Falling Edge Measurement. tCK(avg) is average clock period within 200 consecutive cycle window. The tCK(avg) Rising Edge Measurement measures the period from the rising edge of a cycle to the next rising edge within the waveform window. The tCK(avg) Falling Edge measurement measures from falling edge to falling edge.

Signals of Interest

Based on the test definition (Read or Write):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal

Pass Condition

The tCK(avg) measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. This measurement measures a sliding “window” of 200 cycles.
2. Calculate the average period value for periods 1-200, 2-201 and 3-202.
3. Check the results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

Average High Pulse Width - tCH(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the positive pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Based on the test definition (Read or Write):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal

Pass Condition

The tCH measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding “window” of 200 cycles.
2. Measure the width of the high pulses (1-200, 2-201 and 3-202) and determine the average value for this window.
3. Check the total 3 results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

Average Low Pulse Width - tCL(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the negative pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Based on the test definition (Read or Write):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal

Pass Condition

The tCL measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding “window” of 200 cycles.
2. Measure the width of the low pulses (1-200, 2-201 and 3-202) and determine the average value for this window.
3. Check the total 3 results for the smallest and largest values (worst case values).
4. Compare results against the compliance test limits.

Clock N Cycle Jitter - TJN RJNrms - Test Method of Implementation

The purpose of this test is to measure the Tj and Rj of CK/CK# for each N half cycle 1 ...Ntop.

Signals of Interest

- CK/CK#

Pass Condition

The TJN and RJNrms should be within the specified values for each N half cycle as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: Mjtr (set in config tab, based on spec).

1. Set memory depth to capture window of Mjtr half cycles.
2. Measure TIE of each N half cycle 1...Ntop.
3. Separate TJN and RJNrms for each N half cycle 1...Ntop.
4. Compare the test results against the compliance test limits.

8 WClock AC Timing Tests

This section provides the Methods of Implementation (MOIs) for Clock Timing tests using an Agilent 90000A or 90000X Series Infiniium oscilloscope, recommended InfiniiMax 116xA, 113xA, or N280xA probe amplifiers, E2677A differential solder-in probe head and the GDDR5 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Clock Timing Tests

When performing the Clock Timing tests, the GDDR5 Compliance Test Application will prompt you to make the proper connections. Refer to the Connection tab in the GDDR5 Electrical Performance Compliance Test application for the exact number of probe connections.

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 185.

Test Procedure

1. Start the automated test application as described in “Starting the GDDR5 Compliance Test Application" on page 25.
2. Connect the differential solder-in probe head to the PUTs on the GDDR5 DUT.
3. Connect the oscilloscope probes to any channels of the oscilloscope.
4. In the GDDR5 Test application, click the Set Up tab.
5. You can select the test mode. Enter your comments in the Comments text box.
6. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

WCK Clock Cycle Time - tWCK(avg) - Test Method of Implementation

This test is applicable to the Rising and Falling Edge Measurement. tWCK(avg) is average clock period within 200 consecutive cycle window. The tWCK(avg) Rising Edge Measurement measures the period from the rising edge of a cycle to the next rising edge within the waveform window. The tWCK(avg) Falling Edge measurement measures from falling edge to falling edge.

Signals of Interest

Based on the test definition (Read or Write):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal

Pass Condition

The tWCK(avg) measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. This measurement measures a sliding “window” of 200 cycles.
2. Measure the width of the high pulses (1-200, 2-201, 3-202) and determine the average value for this window.
3. Check the results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

WCK Clock Level Width - tWCH(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the positive pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Based on the test definition (Read or Write):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal

Pass Condition

The tWCH measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding “window” of 200 cycles.
2. Measure the width of the high pulses (1-200, 2-201 and 3-202) and determine the average value for this window.
3. Check the total 3 results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

WCK Clock Low Level Width - tWCL(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the negative pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Based on the test definition (Read or Write):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal

Pass Condition

The tWCL measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding “window” of 200 cycles.
2. Measure the width of the low pulses (1-200, 2-201 and 3-202) and determine the average value for this window.
3. Check the total 3 results for the smallest and largest values (worst case values).
4. Compare results against the compliance test limits.

WCK N Cycle Jitter - PLL on - TJN RJNrms - Test Method of Implementation

The purpose of this test is to measure the Tj and Rj of WCK/WCK# for each N half cycle 1 ...Ntop for WCK PLL on.

Signals of Interest

- WCK/WCK#

Pass Condition

The TJN and RJNrms should be within the specified values for each N half cycle as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: Mjtr (set in config tab, based on spec).

1. Set memory depth to capture window of Mjtr half cycles.
2. Measure TIE of each N half cycle 1...Ntop.
3. Separate TJN and RJNrms for each N half cycle 1...Ntop.
4. Compare the test results against the compliance test limits.

WCK N Cycle Jitter - PLL off - TJN RJNrms - Test Method of Implementation

The purpose of this test is to measure the Tj and Rj of WCK/WCK# for each N half cycle 1 ...Ntop for WCK PLL off.

Signals of Interest

- WCK/WCK#

Pass Condition

The TJN and RJNrms should be within the specified values for each N half cycle as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: Mjtr (set in config tab, based on spec).

1. Set memory depth to capture window of Mjtr half cycles.
2. Measure TIE of each N half cycle 1...Ntop.
3. Separate TJN and RJNrms for each N half cycle 1...Ntop.
4. Compare the test results against the compliance test limits.

11 Address and Command Timing Tests

This section provides the Methods of Implementation (MOIs) for Address and Command Timing tests using a 90000A or 90000X Series Infiniium oscilloscope, recommended InfiniiMax 116xA, 113xA, N280xA probe amplifiers, E2677A differential solder-in probe head and the GDDR5 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Command and Address Timing Tests

When performing the Command and Address Timing tests, the GDDR5 Compliance Test Application will prompt you to make the proper connections. The connection for Command and Address Timing tests may look similar to the following diagrams. Refer to the Connection tab in DDR3 Electrical Performance Compliance Test application for the exact number of probe connections.

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the GDDR5 Compliance Test Application..

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 185.

Test Procedure

1. Start the automated test application as described in “Starting the GDDR5 Compliance Test Application" on page 25.
2. Connect the differential solder-in probe head to the PUTs on the GDDR5 DUT.
3. Connect the oscilloscope probes to any channels of the oscilloscope.
4. In the GDDR5 Test application, click the Set Up tab.
5. You can select the test mode, GDDR5 compliance mode or custom mode. Enter your comments in the Comments text box.
6. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

Command Input Setup Time - tCMDS - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) setup time to the associated clock crossing edge is within the conformance limits as specified in the *JEDEC Standard*.

Signals of Interest

Based on the test definition:

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

PASS Condition

The measured time interval between the address/control setup time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1. Precondition the oscilloscope.
2. Trigger on either rising or falling edge of the signal under test that crosses VREFC.
3. Find all crossings on rising edge of the signal under test that cross VREFC.
4. Find all crossings on falling edge of the signal under test that cross VREFC.
5. For all crossings found, locate the nearest Clock crossing that crosses 0V.
6. Take the time difference between the signal under test's crossing and the corresponding clock crossing as tCMDS.
7. Collect all measured tCMDS.
8. Report the worst tCMDS measured as the test result.
9. Compare the test result against the compliance test limit.

Address Input Setup Time - tAS - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) setup time to the associated clock crossing edge is within the conformance limits as specified in the *JEDEC Standard*.

Signals of Interest

Based on the test definition:

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

PASS Condition

The measured time interval between the address/control setup time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1. Precondition the oscilloscope.
2. Trigger on either rising or falling edge of the signal under test that crosses VREFC.
3. Find all crossings on rising edge of the signal under test that cross VREFC.
4. Find all crossings on falling edge of the signal under test that cross VREFC.
5. For all crossings found, locate the nearest Clock crossing that crosses 0V.
6. Take the time difference between the signal under test's crossing and the corresponding clock crossing as tAS.
7. Collect all measured tAS.
8. Report the worst tAS measured as the test result.
9. Compare the test result against the compliance test limit.

Command Input Hold Time - tCMDH - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) hold time to the associated clock crossing edge is within the conformance limits as specified in the *JEDEC Standard*.

Signals of Interest

Based on the test definition:

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

PASS Condition

The measured time interval between the address/control hold time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1. Precondition the oscilloscope.
2. Trigger on either rising or falling edge of the address/control signal under test that crosses VREFC.
3. Find all crossings on rising edge of the signal under test that cross VREFC.
4. Find all crossings on falling edge of the signal under test that cross VREFC.
5. For all crossings found, locate the nearest Clock crossing that crosses 0V.
6. Take the time difference between the signal under test's crossing and the corresponding clock crossing as tCMDH.
7. Collect all measured tCMDH.
8. Report the worst tCMDH measured as the test result.
9. Compare the test result against the compliance test limit.

Address Input Hold Time - tAH - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) hold time to the associated clock crossing edge is within the conformance limits as specified in the *JEDEC Standard*.

Signals of Interest

Based on the test definition:

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

PASS Condition

The measured time interval between the address/control hold time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1. Precondition the oscilloscope.
2. Trigger on either rising or falling edge of the address/control signal under test that crosses VREFC.
3. Find all crossings on rising edge of the signal under test that cross VREFC.
4. Find all crossings on falling edge of the signal under test that cross VREFC.
5. For all crossings found, locate the nearest Clock crossing that crosses 0V.
6. Take the time difference between the signal under test's crossing and the corresponding clock crossing as tAH.
7. Collect all measured tAH.
8. Report the worst tAH measured as the test result.
9. Compare the test result against the compliance test limit.

6 Custom Mode Read-Write Eye-Diagram Tests

This section provides the Methods of Implementation (MOIs) for Custom Mode Read-Write Eye-Diagram tests using an Agilent 90000A or 90000X Series Infiniium oscilloscope, recommended InfiniiMax 116xA, 113xA, N280xA probe amplifiers, E2677A differential solder-in probe head and the GDDR5 Compliance Test Application.

Probing for Custom Mode Read-Write Eye Diagram Tests

When performing the Custom Mode Read-Write Eye Diagram tests, the GDDR5 Compliance Test Application will prompt you to make the proper connections.

You can use any of the oscilloscope channels as the Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the GDDR5 Compliance Test Application.

For more information on the probe amplifiers and differential probe heads, see Chapter 14, “InfiniiMax Probing,” starting on page 185.

Test Procedure

1. Start the automated test application as described in “Starting the GDDR5 Compliance Test Application" on page 25.
2. Connect the differential solder-in probe head to the PUTs on the GDDR5 DUT.
3. Connect the oscilloscope probes to any of the oscilloscope channels.
4. In the GDDR5 Test application, click the Set Up tab.
5. Select Custom as the Test Mode option.
6. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

User Defined Real-Time Eye Diagram Test for Read Cycle Method of Implementation

The Custom Mode Read-Write Eye Diagram test can be divided into two sub-tests. One of them is the User Defined Real-Time Eye Diagram Test for Read Cycle. There is no available specification on the eye test in *JEDEC Standard JESD212* specifications. The purpose of this test is to automate all the required setup procedures in order to generate an eye diagram for the DDR3 data READ cycle. This additional feature of mask test allows you to perform evaluation and debugging on the created eye diagram. The test will show a fail status if the total failed waveforms is greater than 0.

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)

Measurement Algorithm

1. Use the Setup and Hold time to find and capture the Read cycle data.
2. Set up the oscilloscope to generate an eye diagram.
3. Perform mask testing.
4. Loop until the number of required waveforms is acquired.
5. Return the total number of failed waveforms as a test result.

User Defined Real-Time Eye Diagram Test for Write Cycle Method of Implementation

Just as in the previous test, there is no available specification on the eye diagram test in the *JEDEC Standard JESD212* specifications for User Defined Real-Time Eye Diagram Test for Write Cycle. The purpose of this test is to automate all the required setup procedures in order to generate an eye diagram for the DDR3 data WRITE cycle. This additional feature of mask test allows you to perform evaluation and debugging on the created eye diagram. The test will show a fail status if the total failed waveforms is greater than 0.

.

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)

Measurement Algorithm

1. Use the Setup and Hold time to find and capture the Read cycle data.
2. Set up the oscilloscope to generate an eye diagram.
3. Perform mask testing.
4. Loop until the number of required waveforms is acquired.
5. Return the total number of failed waveforms as a test result.

8 CK Input Operating Conditions Tests

This section provides the Methods of Implementation (MOIs) for CK Input Operating Conditions tests using an Agilent 90000A or 90000X Series Infiniium oscilloscope, recommended InfiniiMax 116xA, 113xA, or N280xA probe amplifiers, E2677A differential solder-in probe head and the GDDR5 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

CK Slew Rate Rising Edge - CKslew-rising - Test Method of Implementation

The purpose of this test is to measure the slew rate for CK/CK#.

Signals of Interest

CK/CK#

Pass Condition

The CK slew values should be within the specified values for CKslew as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: 200.

1. Capture 200 cycles.
2. If measuring VREFC, measure VREFC average. If calculating VREFC, calculate from the config setup.
3. Measure slew rate on rising edge from VREFC average to VIXCK(max) as specified in JESD212. Continue across 200 cycles.
4. Compare the worst case slew rate and compare against the compliance test limits.

CK Slew Rate Falling Edge - CKslew-falling - Test Method of Implementation

The purpose of this test is to measure the slew rate for CK/CK#.

Signals of Interest

CK/CK#

Pass Condition

The CK slew values should be within the specified values for CKslew as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: 200.

1. Capture 200 cycles.
2. If measuring VREFC, measure VREFC average. If calculating VREFC, calculate from the config setup.
3. Measure slew rate on falling edge from VREFC average to VIXCK(min) as specified in JESD212. Continue across 200 cycles.
4. Compare the worst case slew rate and compare against the compliance test limits.

CK Crossing Point - Relative to VREFC - VIXCK - Test Method of Implementation

The purpose of this test is to measure VIXCK for CK/CK#.

Signals of Interest

CK/CK#

Pass Condition

The VIXCK values should be within the specified values for VIXCK as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: 200.

1. Capture 200 cycles.
2. If measuring VREFC, measure VREFC average. If calculating VREFC, calculate from the config setup.
3. Measure crossing point of CK and CK#.
   VIXCK = -1(VREFC-MeasuredCrossingVoltage). Continue across 200 cycles.
4. Compare the worst case VIXCK and compare against the compliance test limits.

Clock Input Differential Voltage - CK and CK#(ac) - VIDCK(ac) - Test Method of Implementation

The purpose of this test is to measure the VIDCK(ac) for CK/CK#.

Signals of Interest

CK/CK#

Pass Condition

The VIDCK values should be greater than the specified values for VIDCK(ac) as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: 200.

1. Capture 200 cycles.
2. On first rising edge, measure a window 1/2tCK wide for max positive voltage swing. If this value is less than VIDCK(ac) as specified in JESD212, then report that value as a fail with negative margin to compliance test limits. If this value is greater than VIDCK(ac) as specified in JESD212, then place a marker at the first point where the rising edge crosses the VIDCK(ac) spec. Place a second marker at tDVAC after the first. Move the first marker from Vid(ac) until it does not increase in voltage value or equal the second marker.
3. Measure the minimum voltage within the window. Repeat for negative pulse. Continue across 200 cycles.
4. Compare the worst case VIDCK(ac) and compare against the compliance test limits.

Clock Input Differential Voltage - CK and CK#(dc) - VIDCK(dc) - Test Method of Implementation

The purpose of this test is to measure the VIDCK(dc) for CK/CK#.

Signals of Interest

CK/CK#

Pass Condition

The VIDCK values should be greater than the specified values for VIDCK(dc) as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: 200.

1. Capture 200 cycles.
2. On first rising edge, measure a window 1/2tCK wide for max positive voltage swing. If this value is less than VIDCK(ac) as specified in JESD212, then report that value as a fail with negative margin to compliance test limits. If this value is greater than VIDCK(ac) as specified in JESD212, then place a marker at the first point where the rising edge crosses the VIDCK(ac) spec. Place a second marker at t0 + tCH + 1/[6V/ns/(Vid(dc))]. t0 is the time that CK crosses 0V on the rising edge. Move the first marker from Vid(ac) until it does not increase in voltage value.
3. Measure the minimum voltage within the window. Repeat for negative pulse (measuring max value). Continue across 200 cycles.
4. Compare the worst case VIDCK(dc) and compare against the compliance test limits.

8 WCK Input Operating Conditions Tests

This section provides the Methods of Implementation (MOIs) for WCK Input Operating Conditions tests using an Agilent 90000A or 90000X Series Infiniium oscilloscope, recommended InfiniiMax 116xA, 113xA, or N280xA probe amplifiers, E2677A differential solder-in probe head and the GDDR5 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

WCK Slew Rate Rising Edge - CKslew-rising - Test Method of Implementation

The purpose of this test is to measure the slew rate for WCK/WCK#.

Signals of Interest

WCK/WCK#

Pass Condition

The WCK slew values should be within the specified values for WCKslew as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: 200.

1. Capture 200 cycles.
2. If VREFD is external, measure VREFD average. If VREFD is internal, calculate from the config setup.
3. Measure slew rate on rising edge from VREFD average to VIXWCK(max) as specified in JESD212. Continue across 200 cycles.
4. Compare the worst case slew rate and compare against the compliance test limits.

WCK Slew Rate Falling Edge - CKslew-falling - Test Method of Implementation

The purpose of this test is to measure the slew rate for WCK/WCK#.

Signals of Interest

WCK/WCK#

Pass Condition

The WCK slew values should be within the specified values for WCKslew as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: 200.

1. Capture 200 cycles.
2. If VREFD is external, measure VREFD average. If VREFD is internal, calculate from the config setup.
3. Measure slew rate on falling edge from VREFD average to VIXWCK(min) as specified in JESD212. Continue across 200 cycles.
4. Compare the worst case slew rate and compare against the compliance test limits.

WCK Crossing Point - Relative to VREFD - VIXWCK - Test Method of Implementation

The purpose of this test is to measure VIXWCK for WCK/WCK#.

Signals of Interest

WCK/WCK#

Pass Condition

The VIXWCK values should be within the specified values for VIXWCK as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: 200.

1. Capture 200 cycles.
2. If VREFD is external, measure VREFD average. If VREFD is internal, calculate from the config setup.
3. Measure crossing point of WCK and WCK#.
   VIXWCK = - 1(VREFD- MeasuredCrossingVoltage). Continue across 200 cycles.
4. Compare the worst case VIXWCK and compare against the compliance test limits.

WClock Input Differential Voltage - WCK and WCK#(ac) - VIDWCK(ac) - Test Method of Implementation

The purpose of this test is to measure the VIDWCK(ac) for WCK/WCK#.

Signals of Interest

WCK/WCK#

Pass Condition

The VIDWCK values should be greater than the specified values for VIDWCK(ac) as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: 200.

1. Capture 200 cycles.
2. On first rising edge, measure a window 1/2tWCK wide for max positive voltage swing. If this value is less than VIDWCK(ac) as specified in JESD212, then report that value as a fail with negative margin to compliance test limits. If this value is greater than VIDWCK(ac) as specified in JESD212, then place a marker at the first point where the rising edge crosses the VIDWCK(ac) spec. Place a second marker at tDVAC after the first. Move the first marker from Vid(ac) until it does not increase in voltage value or equal the second marker.
3. Measure the minimum voltage within the window. Repeat for negative pulse (measuring max value). Continue across 200 cycles.
4. Compare the worst case VIDWCK(ac) and compare against the compliance test limits.

WClock Input Differential Voltage - WCK and WCK#(dc) - VIDWCK(dc) - Test Method of Implementation

The purpose of this test is to measure the VIDWCK(dc) for WCK/WCK#.

Signals of Interest

WCK/WCK#

Pass Condition

The VIDWCK values should be greater than the specified values for VIDWCK(dc) as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: 200.

1. Capture 200 cycles.
2. On first rising edge, measure a window 1/2tWCK wide for max positive voltage swing. If this value is less than VIDWCK(ac) as specified in JESD212, then report that value as a fail with negative margin to compliance test limits. If this value is greater than VIDWCK(ac) as specified in JESD212, then place a marker at the first point where the rising edge crosses the VIDWCK(ac) spec. Place a second marker at t0 + tWCKCH + 1/[6V/ns/(Vid(dc))]. t0 is the time that WCK crosses 0V on the rising edge. Move the first marker from Vid(ac) until it does not increase in voltage value.
3. Measure the minimum voltage within the window. Repeat for negative pulse (measuring max value). Continue across 200 cycles.
4. Compare the worst case VIDWCK(dc) and compare against the compliance test limits.

8 Data Input and Output Timing Tests

This section provides the Methods of Implementation (MOIs) for Data Input and Output Timing tests using an Agilent 90000A or 90000X Series Infiniium oscilloscope, recommended InfiniiMax 116xA, 113xA, or N280xA probe amplifiers, E2677A differential solder-in probe head and the GDDR5 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Data Input Valid Window - PLL on (measured Unit Interval) - tDIVW(UI) - PLL on - Test Method of Implementation

This purpose of this test is to measure the tDIVW for DQn for a single unit interval when PLL is on.

Signals of Interest

DQn

Pass Condition

The tDIVW values should be less than the specified values for tDIVW as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: 200

1. Separate write data from read data.
2. Measure the unit interval of each unit in the set “Number of Measurements” as set in the config setup.
3. Compare the worst case tDIVW(UI) against the compliance test limits.

Data Input Valid Window - PLL off (measured Unit Interval) - tDIVW(UI) - PLL off - Test Method of Implementation

This purpose of this test is to measure the tDIVW for DQn for a single unit interval when PLL is off.

Signals of Interest

DQn

Pass Condition

The tDIVW values should be less than the specified values for tDIVW as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: 200

1. Separate write data from read data.
2. Measure the unit interval of each unit in the set “Number of Measurements” as set in the config setup.
3. Compare the worst case tDIVW(UI) against the compliance test limits.

Data Input Pulse Width - positive pulse - tDIPW - positive - Test Method of Implementation

The purpose of this test is to measure the positive pulse of tDIPW for DQn.

Signals of Interest

DQn

Pass Condition

The tDIPW values should be less than the specified values for tDIPW as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: 200

1. Separate write data and read data.
2. Capture “Number of Measurements” as set in the config tab.
3. Measure the pulse width from 50% DQ rising to 50% DQ falling.
4. Compare the measured tDIPW against the compliance test limits.

Data Input Pulse Width - negative pulse - tDIPW - negative - Test Method of Implementation

The purpose of this test is to measure the negative pulse of tDIPW for DQn.

Signals of Interest

DQn

Pass Condition

The tDIPW values should be less than the specified values for tDIPW as specified in the *JEDEC Standard JESD212*.

Measurement Algorithm

Number of cycles acquired: 200

1. Separate write data and read data.
2. Capture “Number of Measurements” as set in the config tab.
3. Measure the pulse width from 50% DQ falling to 50% DQ rising.
4. Compare the measured tDIPW against the compliance test limits.

12
Custom Debug - Data Mask

This section provides the Methods of Implementation (MOIs) for Custom Mode Data Mask tests using an Agilent 90000A or 90000X Series Infiniium oscilloscope, recommended InfiniiMax 116xA, 113xA, N280xA probe amplifiers, E2677A differential solder-in probe head and the GDDR5 Compliance Test Application.

User Defined Real-Time Eye Diagram Test for Read Cycle Method of Implementation

The purpose of this test is to use a user defined eye mask to test the read eye against an expected performance.

Signals of Interest

DQn

Pass Condition

The data eye should not cross into the defined mask.

Measurement Algorithm

Number of cycles acquired: 200

1. Separate the read data from the write data.
2. Capture “Number of Measurements” as set in the config setup and fold around WCK edges within read burst range.
3. Compare the folded data eye to the defined eye mask

User Defined Real-Time Eye Diagram Test for Write Cycle Method of Implementation

The purpose of this test is to use a user defined eye mask to test the write eye against an expected performance.

Signals of Interest

DQn

Pass Condition

The data eye should not cross into the defined mask.

Measurement Algorithm

Number of cycles acquired: 200

1. Separate the read data from the write data.
2. Capture “Number of Measurements” as set in the config setup and fold around WCK edges within write burst range.
3. Compare the folded data eye to the defined eye mask

13 Calibrating the Infiniium Oscilloscope and Probe

This section describes the Agilent Infiniium digital storage oscilloscope calibration procedures.

Required Equipment for Oscilloscope Calibration

To calibrate the Infiniium oscilloscope in preparation for running the GDDR5 automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2 (provided with the Agilent Infiniium oscilloscope).
- Calibration cable (provided with the 90000 Series Infiniium oscilloscopes). Use a good quality 50 Ω BNC cable.

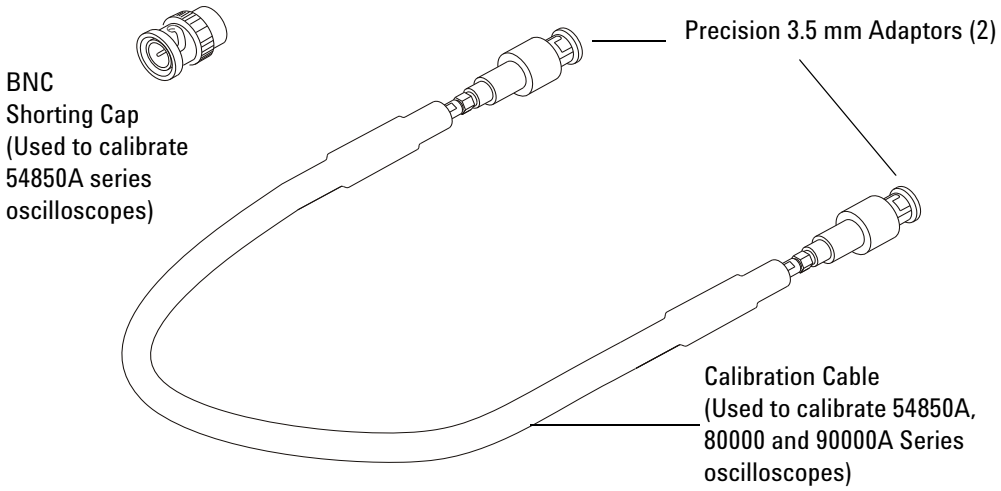

Figure 42 Accessories Provided with the Agilent Infiniium Oscilloscope

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Agilent oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:

   a Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.

   b Plug in the power cord.

   c Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.

   d Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:

   a Locate the BNC shorting cap.

   b Locate the calibration cable.

   c Locate the two Agilent precision SMA/BNC adapters.

   d Attach one SMA adapter to the other end of the calibration cable - hand tighten snugly.

   e Attach another SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 43 below, perform the following steps:

   a Click on the Utilities>Calibration menu to open the Calibration dialog box.

Figure 43 Accessing the Calibration Menu

4 Referring to Figure 44 below, perform the following steps to start the calibration:

   b Uncheck the Cal Memory Protect checkbox.

   c Click the Start button to begin the calibration.

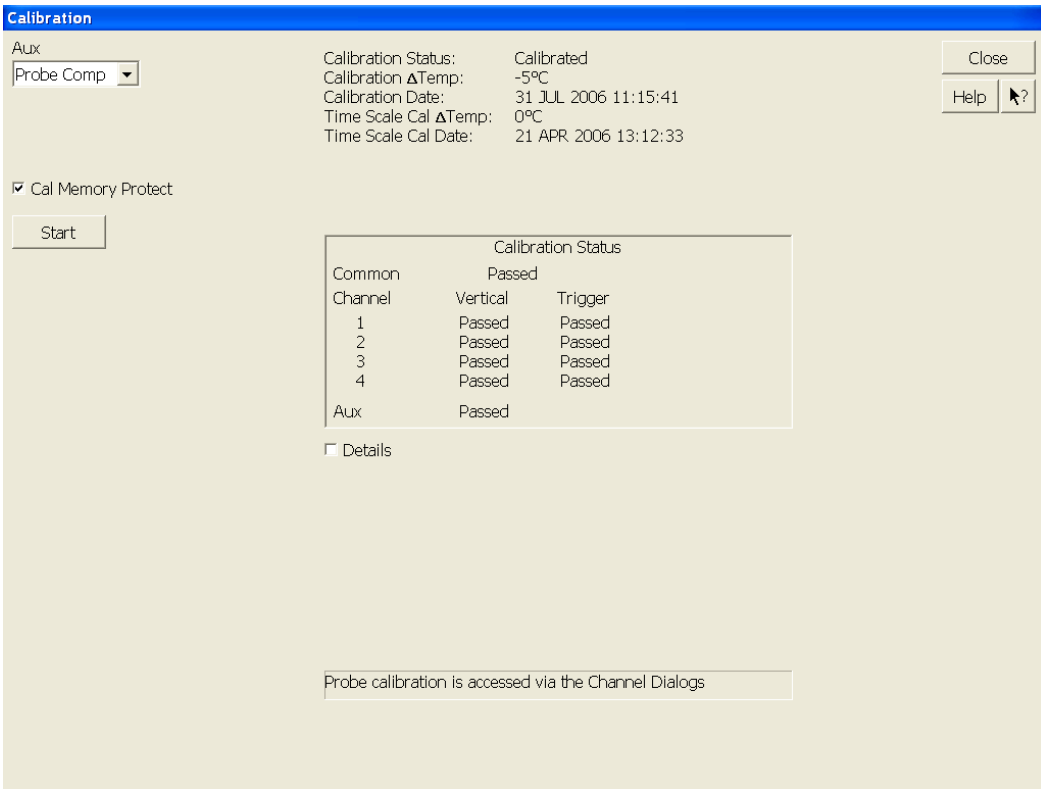

Figure 44 Oscilloscope Calibration Window

d During the calibration of channel 1, if you are prompted to perform a Time Scale Calibration, as shown in Figure 45 below.

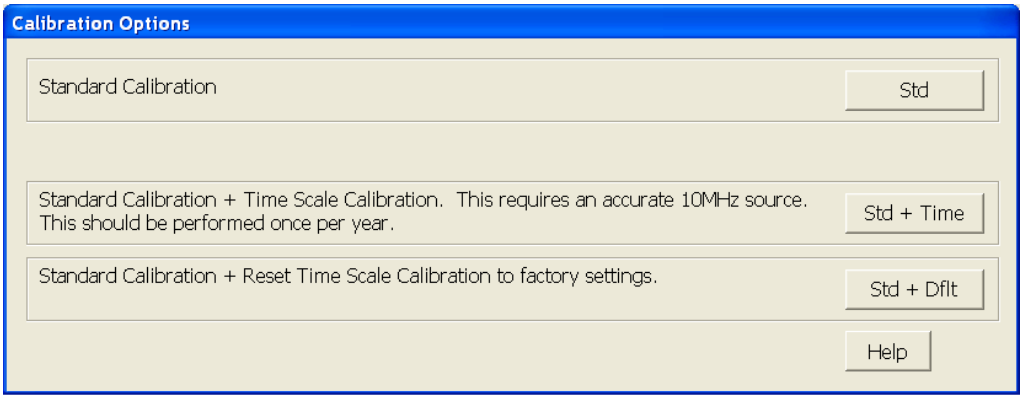

Figure 45 Time Scale Calibration Dialog box

e Click on the Std+Dflt button to continue the calibration, using the Factory default calibration factors.

f When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

g Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

h Click the Close button to close the calibration window.

i The internal calibration is completed.

j Read NOTE below.

NOTE These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Required Equipment for Probe Calibration

Before performing GDDR5 tests you should calibrate the probes. Calibration of the solder-in probe heads consist of a vertical calibration and a skew calibration. The vertical calibration should be performed before the skew calibration. Both calibrations should be performed for best probe measurement performance.

The calibration procedure requires the following parts.

- BNC (male) to SMA (male) adaptor
- Deskew fixture
- 50 Ω SMA terminator

Probe Calibration

Connecting the Probe for Calibration

For the following procedure, refer to Figure 46 below.

1. Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.
2. Connect the 50 Ω SMA terminator to the connector farthest from yellow pincher.
3. Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.
4. Connect the probe to an oscilloscope channel.
5. To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.
6. Push down the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.
7. Release the yellow pincher.

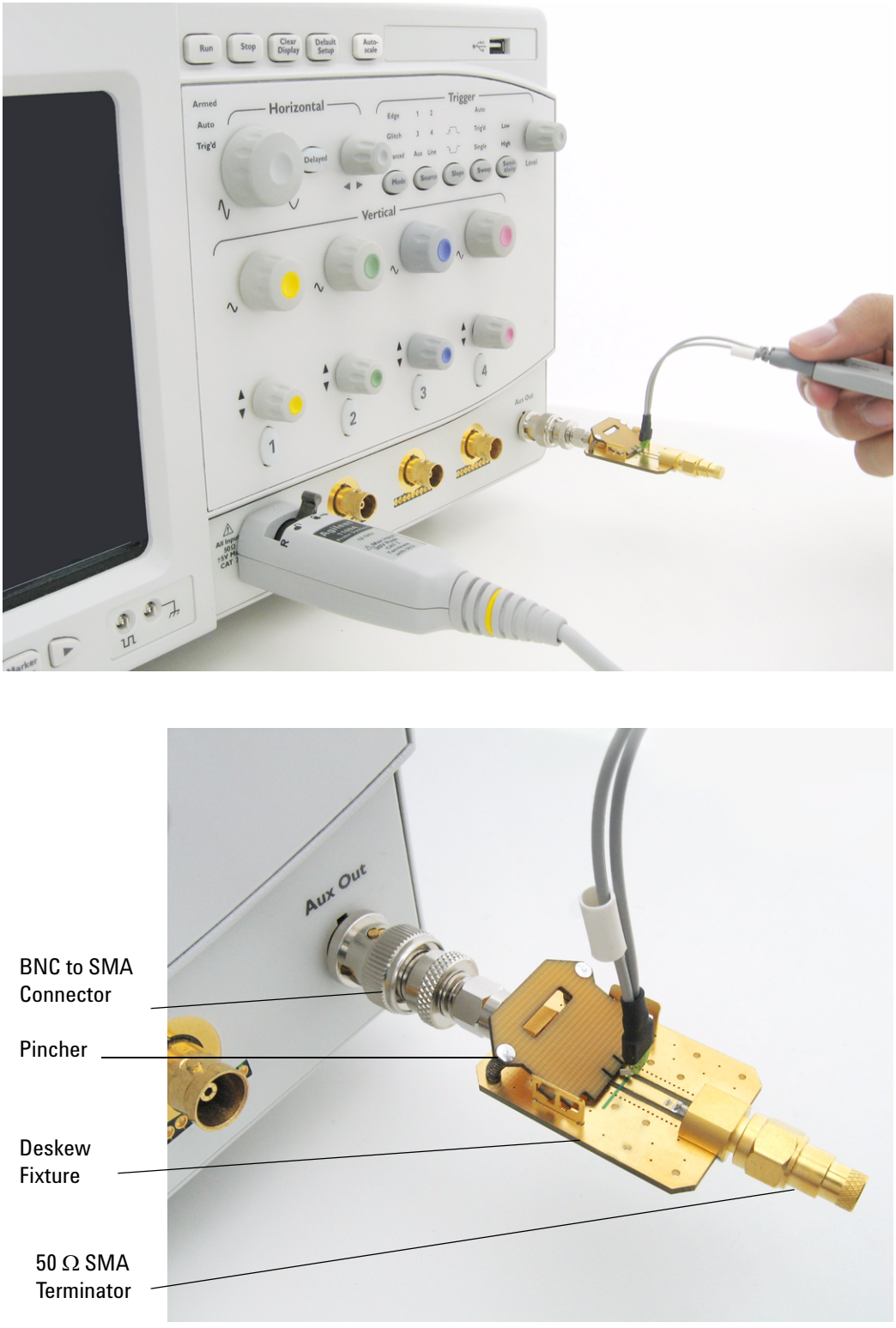

Figure 46 Solder-in Probe Head Calibration Connection Example

Verifying the Connection

1 On the Infiniium oscilloscope, press the autoscale button on the front panel.

2 Set the volts per division to 100 mV/div.

3 Set the horizontal scale to 1.00 ns/div.

4 Set the horizontal position to approximately 3 ns. You should see a waveform similar to that in Figure 47 below.

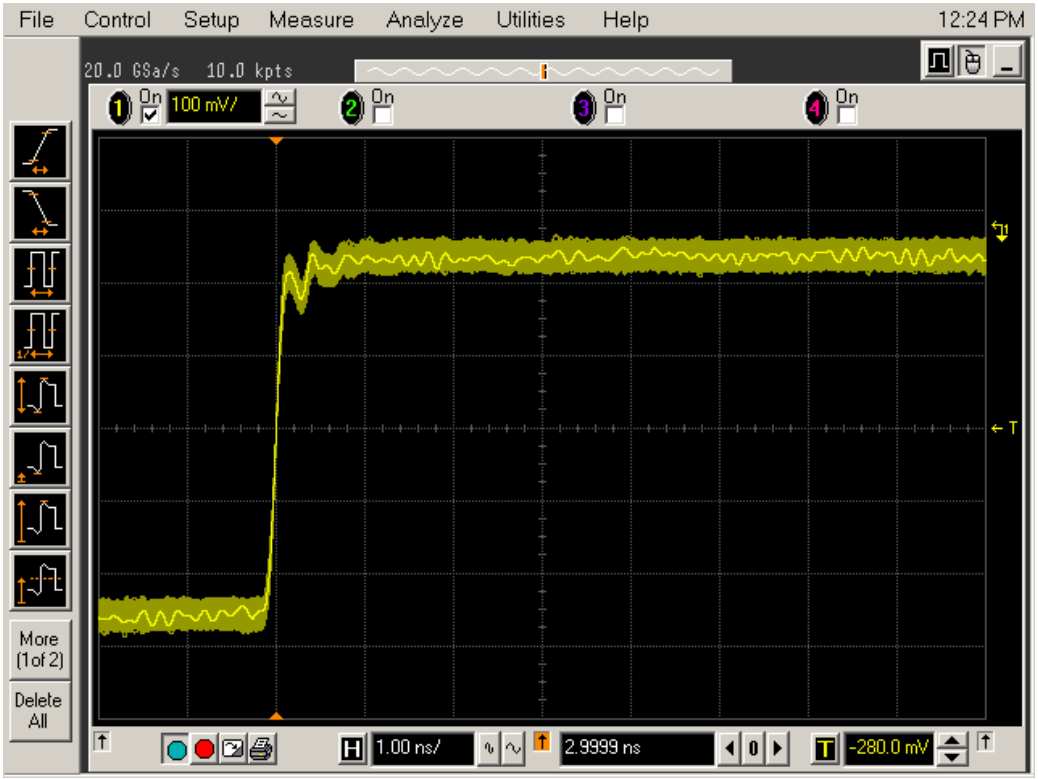

Figure 47 Good Connection Waveform Example

If you see a waveform similar to that of Figure 48 below, then you have a bad connection and should check all of your probe connections.

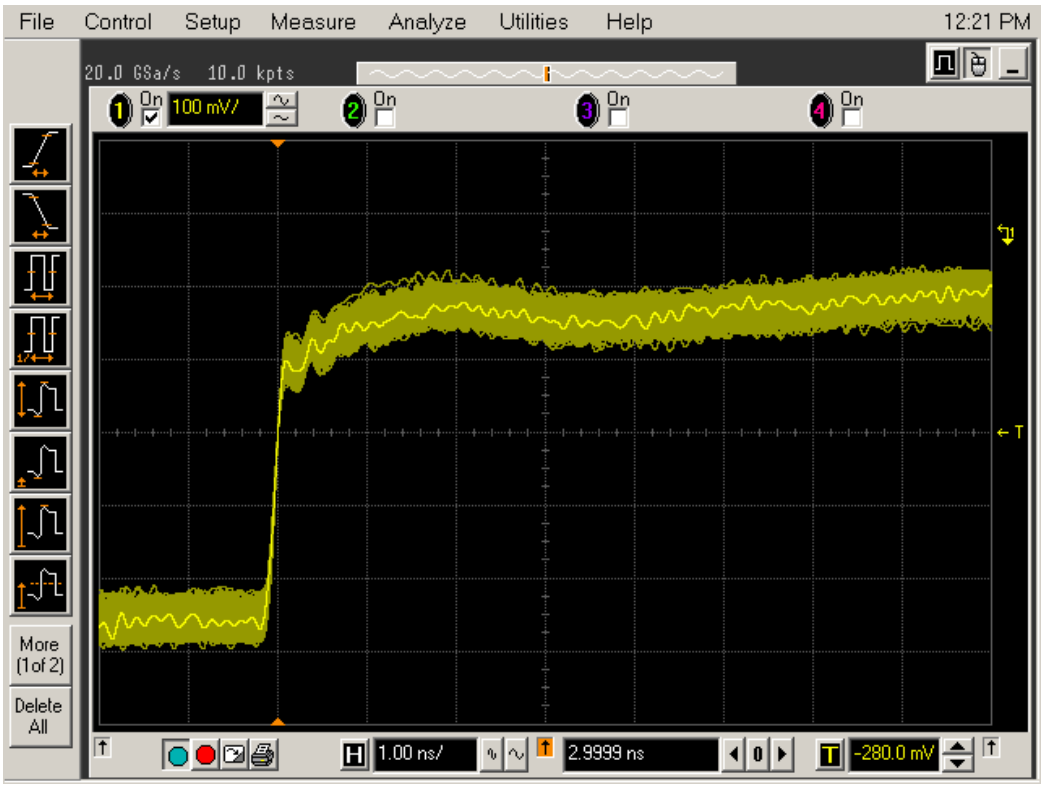

Figure 48 Bad Connection Waveform Example

Running the Probe Calibration and Deskew

1 On the Infiniium oscilloscope in the Setup menu, select the channel connected to the probe, as shown in Figure 49.

Figure 49 Channel Setup Window.

2 In the Channel Setup dialog box, select the Probes... button, as shown in Figure 50.

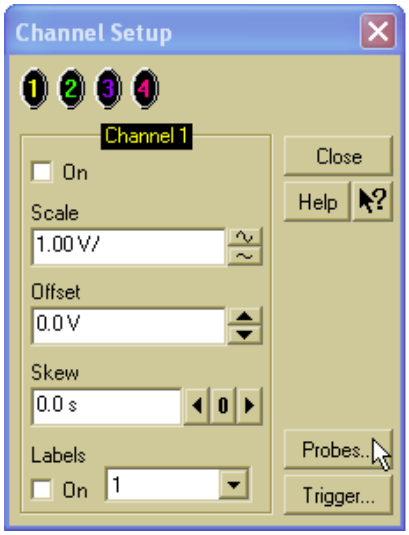

Figure 50 Channel Dialog Box

3 In the Probe Setup dialog box, select the Calibrate Probe... button.

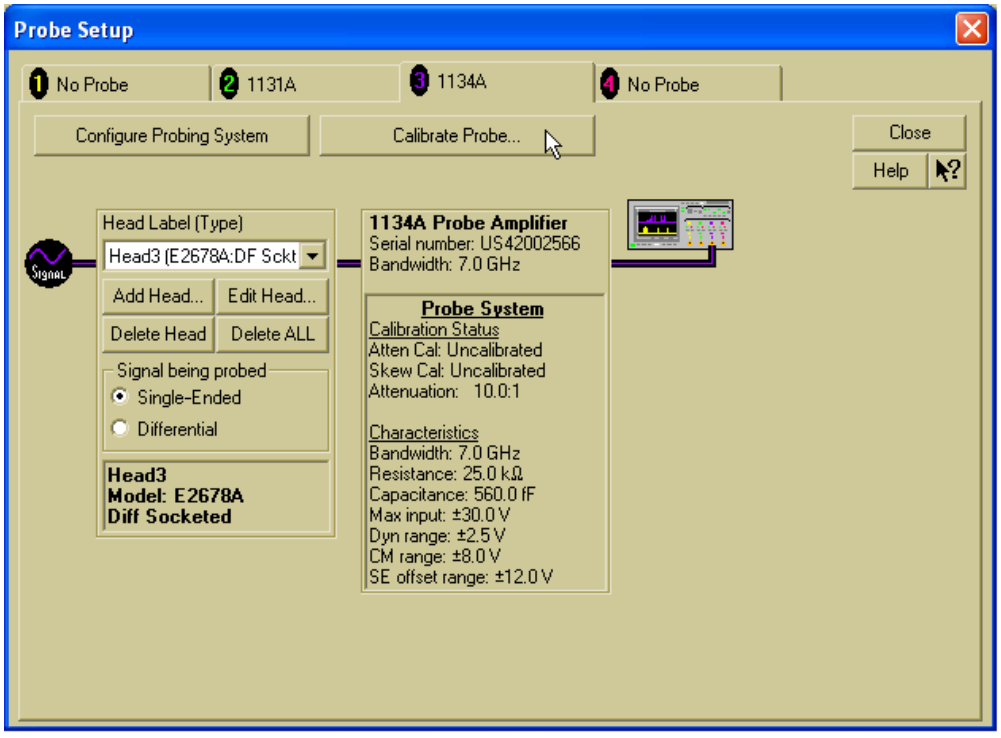

Figure 51 Probe Setup Window.

4 In the Probe Calibration dialog box, select the Calibrated Atten/Offset radio button.

5 Select the Start Atten/Offset Calibration... button and follow the on-screen instructions for the vertical calibration procedure.

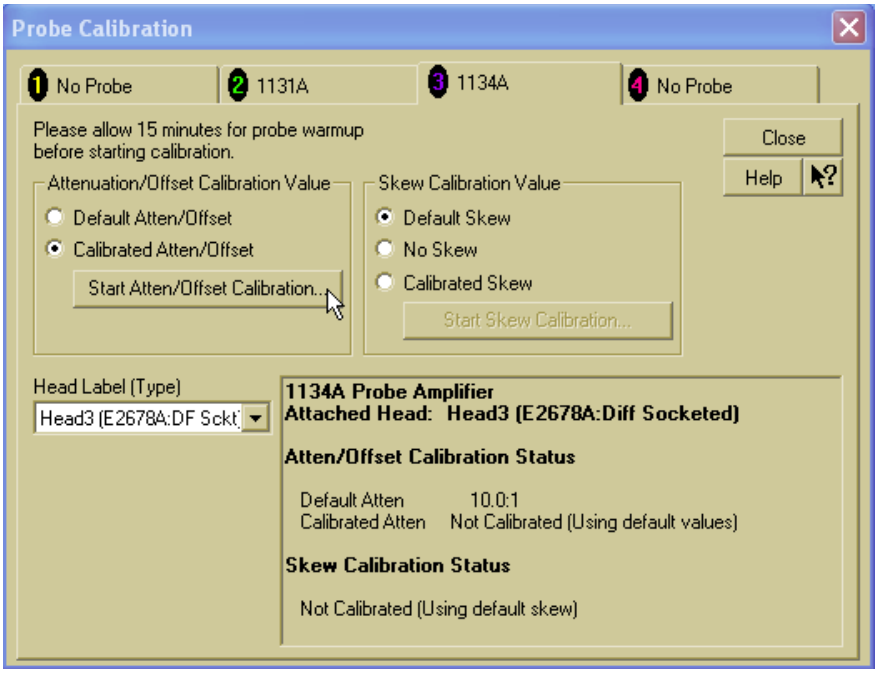

Figure 52 Probe Calibration Window.

6 Once the vertical calibration has successfully completed, select the Calibrated Skew... button.

7 Select the Start Skew Calibration... button and follow the on-screen instructions for the skew calibration.

At the end of each calibration, the oscilloscope will prompt you if the calibration was or was not successful.

Verifying the Probe Calibration

If you have successfully calibrated the probe, it is not necessary to perform this verification. However, if you want to verify that the probe was properly calibrated, the following procedure will help you verify the calibration.

The calibration procedure requires the following parts:

- BNC (male) to SMA (male) adaptor
- SMA (male) to BNC (female) adaptor
- BNC (male) to BNC (male) 12 inch cable such as the Agilent 8120-1838

- Agilent 54855-61620 calibration cable (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Agilent 54855-67604 precision 3.5 mm adaptors (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Deskew fixture

For the following procedure, refer to Figure 53.

1 Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.

2 Connect the SMA (male) to BNC (female) to the connector farthest from the yellow pincher.

3 Connect the BNC (male) to BNC (male) cable to the BNC connector on the deskew fixture to one of the unused oscilloscope channels. For infiniium oscilloscopes with bandwidths of 6 GHz and greater, use the 54855-61620 calibration cable and the two 54855-64604 precision 3.5 mm adaptors.

4 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.

5 Connect the probe to an oscilloscope channel.

6 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.

7 Push down on the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.

8 Release the yellow pincher.

9 On the oscilloscope, press the autoscale button on the front panel.

10 Select Setup menu and choose the channel connected to the BNC cable from the pull-down menu.

11 Select the Probes... button.

12 Select the Configure Probe System button.

13 Select User Defined Probe from the pull-down menu.

14 Select the Calibrate Probe... button.

15 Select the Calibrated Skew radio button.

16 Once the skew calibration is completed, close all dialog boxes.

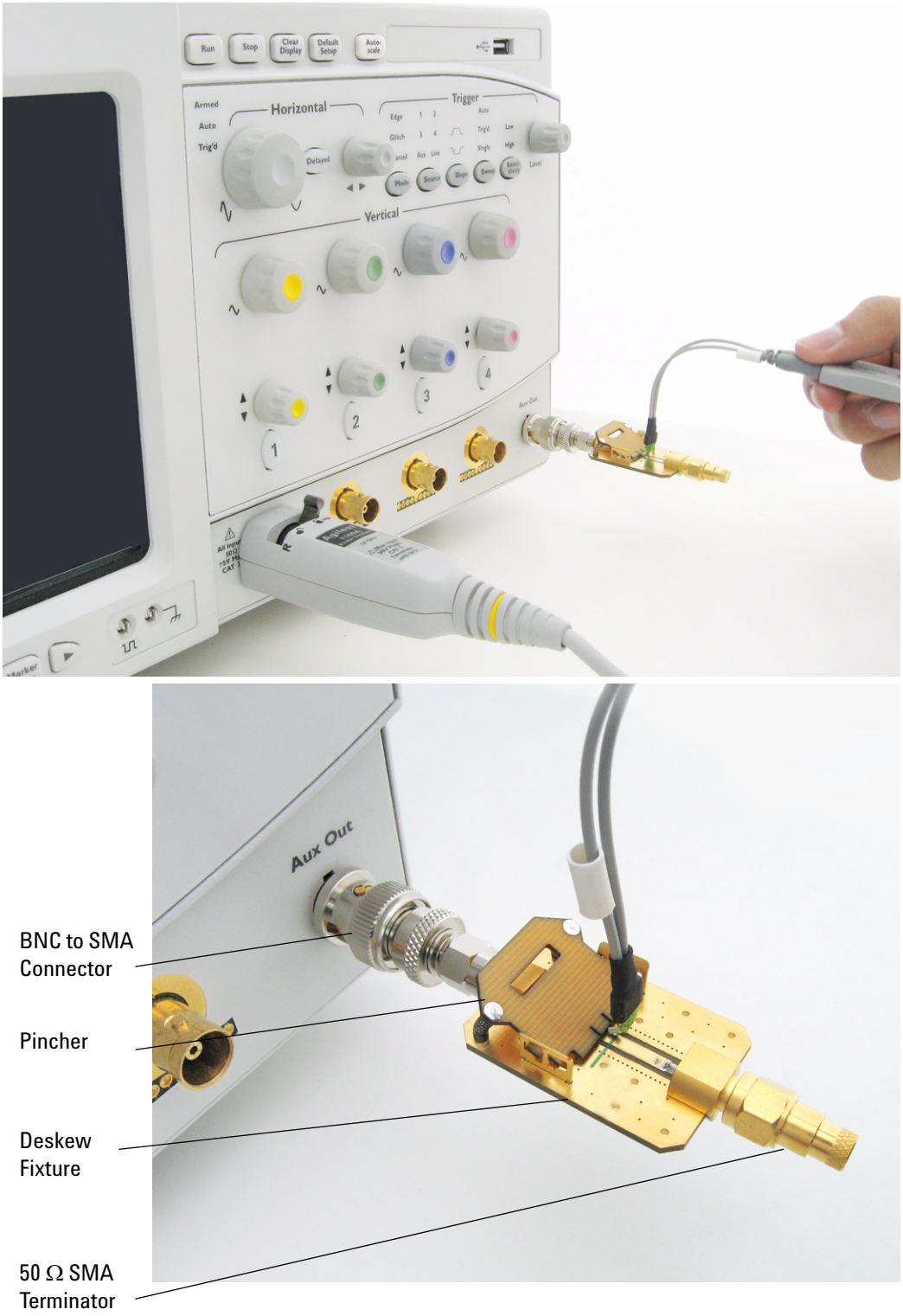

Figure 53 Probe Calibration Verification Connection Example

17 Select the Start Skew Calibration... button and follow the on-screen instructions.

18 Set the vertical scale for the displayed channels to 100 mV/div.

19 Set the horizontal range to 1.00 ns/div.

20 Set the horizontal position to approximately 3 ns.

21 Change the vertical position knobs of both channels until the waveforms overlap each other.

22 Select the Setup menu choose Acquisition... from the pull-down menu.

23 In the Acquisition Setup dialog box enable averaging. When you close the dialog box, you should see waveforms similar to that in Figure 54.

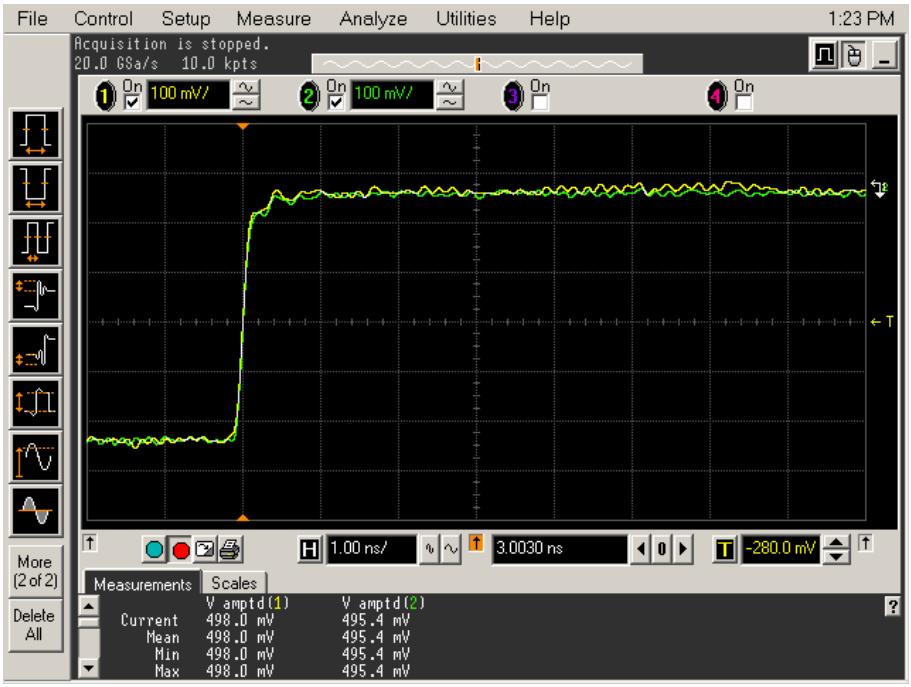

Figure 54 Calibration Probe Waveform Example

NOTE

Each probe is calibrated with the oscilloscope channel to which it is connected. Do not switch probes between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the probes be labeled with the channel on which they were calibrated.

14 InfiniiMax Probing

Figure 55 1134A InfiniiMax Probe Amplifier

Agilent recommends 116xA or 113xA probe amplifiers, which range from 3.5 GHz to 12 GHz, if you are using a 90000A Series oscilloscope. You can also use these with a 90000X Series oscilloscope as long as you also purchase the appropriate adapter. The N280XA InfiniiMax III proeb amplifiers are the recommended probe amps for the 90000X Series oscilloscope.

Agilent also recommends the E2677A differential solder-in probe head (if you are using an InfiniiMax I or II amplifier). Other probe head options include N5381A InfiniiMax II 12 GHz differential solder-in probe head, N5382A InfiniiMax II 12 GHz differential browser, E2675A InfiniiMax differential browser probe head, N5425A InfiniiMax ZIF probe head and N5426A ZIF Tips.

Figure 56 E2677A / N5381A Differential Solder-in Probe Head

Table 51 Probe Head Characteristics (with 1134A probe amplifier)

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential Solder-in	E2677A	7 GHz, 0.27 pF, 50 kOhm	7 GHz, 0.44 pF, 25 kOhm

Used with 1168A or 1169A probe amplifier, the E2677A differential solder-in probe head provides 10 GHz and 12 GHz bandwidth respectively.

Agilent recommends the N5441A solder-in probe head (if you are using an InfiniiMax III amplifier). Other probe head options include the N5445A InfiniiMax III browser, and the N5439A InfiniiMax III ZIF probe head and N5440A/N5447A ZIF Tips.

Index

U

V

W

Z

www.agilent.com

First edition, September 2010
This part is not orderable.

U7245A-97000

Agilent Technologies