D9020DDRC DDR2(+LP) Compliance Test Application

KEYSIGHT

METHODS OF IMPLEMENTATION

Notices

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Keysight Technologies.
1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

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DDR2 —Quick Reference

Table 1 DDR2 Cycles and Signals

NOTE: 1 = Single Ended signal; 2 = Differential signal; 3 = 2 x Single Ended signal

TEST	Cycle		Based on Test Definition						Required Connection Type to Perform Test on Scope						Opt.
	Read	Write	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	CS#
tJIT(per)	√	√			√						√[1,2]				
tJIT(cc)	√	√			√						√[1,2]				
tERR(nper)	√	√			√						√[1,2]				
tCH(avg)	√	√			√						√[1,2]				
tCL(avg)	√	√			√						√[1,2]				
tJIT(duty)	√	√			√						√[1,2]				
tCK(avg)	√	√			√						√[1,2]				
VIH(ac)		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
VIH(dc)		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
VIL(ac)		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
VIL(dc)		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
SlewR		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
SlewF		√	√	√	√	√	√	√	√[1]	√[1,2]	√[1]	√[1]	√[1]	√[1]	
AC Overshoot	√	√	√	√	√	√	√	√	√[1]	√[1]	√[1]	√[1]	√[1]	√[1]	
AC Undershoot	√	√	√	√	√	√	√	√	√[1]	√[1]	√[1]	√[1]	√[1]	√[1]	
VID(ac)		√		√	√				√[3]	√[3]	√[3]				
VIX(ac)		√		√	√				√[3]	√[3]	√[3]				
VOX(ac)	√			√					√[3]	√[3]					
tAC	√		√		√				√[1]	√[1,2]	√[1,2]				√
tDQSCK	√			√	√				√[1]	√[1,2]	√[1,2]				√
tHZ(DQ)	√		√		√				√[1]	√[1,2]	√[1,2]				√
tLZ(DQS)	√			√	√				√[1]	√[1,2]	√[1,2]				√
tLZ(DQ)	√		√		√				√[1]	√[1,2]	√[1,2]				√

Table 1 DDR2 Cycles and Signals

NOTE: 1 = Single Ended signal; 2 = Differential signal; 3 = 2 x Single Ended signal

TEST	Cycle		Based on Test Definition						Required to Perform on Scope						Opt.
	Read	Write	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	CS#
tDQSQ	√		√						√[1]	√[1,2]					√
tQH	√		√						√[1]	√[1,2]					√
tDQSS		√		√	√				√[1]	√[1,2]	√[1,2]				√
tDQSH		√		√					√[1]	√[1,2]					√
tDQSL		√		√					√[1]	√[1,2]					√
tDSS		√		√	√				√[1]	√[1,2]	√[1,2]				√
tDSH		√		√	√				√[1]	√[1,2]	√[1,2]				√
tWPST		√		√					√[1]	√[1,2]					√
tWPRE		√		√					√[1]	√[1,2]					√
tRPRE	√			√					√[1]	√[1,2]					√
tRPST	√			√					√[1]	√[1,2]					√
tDS(base)		√	√					√	√[1]	√[2]				√[1]	√
tDH(base)		√	√					√	√[1]	√[2]				√[1]	√
tDS1(base)		√	√					√	√[1]	√[1]				√[1]	√
tDH1(base)		√	√					√	√[1]	√[1]				√[1]	√
tIS(base)		√			√	√	√				√[1,2]	√[1]	√[1]		√
tIH(base)		√			√	√	√				√[1,2]	√[1]	√[1]		√
Eye Diagram - Read	√		√	√					√[1]	√[1,2]					
Eye Diagram - Write		√	√	√					√[1]	√[1,2]					

DDR2(+LP) Compliance Test Application — At A Glance

The Keysight D9020DDRC DDR2(+LP) Compliance Test Application is a DDR2 (Double Data Rate 2) test solution that covers electrical, clock and timing parameters of the JEDEC (Joint Electronic Device Engineering Council) specifications. The software helps you in testing all the un-buffered DDR2 DUTs (devices under test) compliance, with the Keysight 9000, 90000 series, and UXR series Infiniium digital storage oscilloscope.

There are 2 main categories of test modes:

- Compliance Tests - These tests are based on the DDR2 JEDEC compliance specifications and are compared to corresponding compliance test limits.
- Custom Mode Tests - These tests are not based on any compliance specification. The primary use of these tests is to perform non-JEDEC specific speed signal testing.

The DDR2(+LP) Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Allows you to determine the number of trials for each test, with the new multi trial run capability.
- Allows you to customize the test limits in the application which determines the pass or/and fail of each test.
- Provides detailed information of each test that has been run. The result of maximum twenty five worst trials can be displayed at any one time.
- Creates a printable HTML report of the tests that have been run.

The minimum number of probes required for the tests are:

- Clock tests - 1 probe.
- Electrical tests - 3 probes.
- Clock Timing tests - 3 probes.
- Custom Mode tests - 3 probes.

NOTE

The tests performed by the DDR2(+LP) Compliance Test Application are intended to provide a quick check of the physical layer performance of the DUT. These testing are not replacement for an exhaustive test validation plan.

DDR2 SDRAM electrical, clock and timing test standards and specifications are described in the *JESD79-2E* and *JESD208* document. For more information, please refer to JEDEC web site at www.jedec.org.

Required Equipment and Software

In order to run the DDR2 automated tests, you need the following equipment and software:

- The minimum version of Infiniium oscilloscope software (see the D9020DDRC DDR2(+LP) test application release notes)
- Use one of the following oscilloscope models:
  - Keysight DSO9000A-Series, DSO90000A-Series, and DSOX90000A/Q/Z/V-Series Oscilloscopes with a minimum bandwidth of 8.0 GHz (recommended) for accurate measurements. For faster speed grade devices, a minimum bandwidth of 13 GHz bandwidth is recommended.
  - Keysight UXR Oscilloscopes
  - Keysight MXR Oscilloscopes
- D9020DDRC DDR2(+LP) Compliance Test Application, version 1.40 or higher
- RAM reliability test software
- 1169A, 1168A, 1134A, 1132A, or 1131A InfiniiMax probe amplifiers
- N5381A or E2677A differential solder-in probe head, N5382A or E2675A differential browser probe head, N5425A ZIF probe head with N5426A or N5451A ZIF tip accessories, E2678A differential socketed probe head
- Any computer motherboard system that supports DDR2 memory
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope)

NOTE Keysight D9020DDRC DDR2(+LP) Compliance Test Application supports MXR Oscilloscope.

Below are the required licenses:

- D9020DDRC DDR2(+LP) Compliance Test Application license
- N5414A InfiniiScan software license
- E2688A Serial Data Analysis and Clock Recovery software license
- N5404A Deep memory option (optional)

In This Book

This manual describes the tests that are performed by the DDR2(+LP) Compliance Test Application in more detail; it contains information from (and refers to) the *JESD79-2E* and *JESD208,* and it describes how the tests are performed.

- Chapter 1, “Installing the DDR2(+LP) Compliance Test Application"” shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, “Preparing to Take Measurements" shows how to start the DDR2(+LP) Compliance Test Application and gives a brief overview of how it is used.
- Chapter 3, “Measurement Clock Tests" describes the measurement clock tests including clock period jitter, clock to clock period jitter, cumulative error, average HIGH and LOW pulse width, half period jitter and average clock period tests.
- Chapter 4, “Single-Ended Signals AC Input Parameters Tests" shows how to run the single-ended signals AC input parameters tests. This chapter includes input signal maximum peak to peak swing tests, input signal minimum slew rate (rising) tests, input signal minimum slew rate (falling) tests, input logic HIGH tests and input logic LOW tests.
- Chapter 5, “Single-Ended Signals VIH/VIL (Address, Control) Tests" describes the AC/DC input logic high/low tests (address, control).
- Chapter 6, “Single-Ended Signals VIH/VIL (Data, Mask) Tests" describes the AC/DC input logic high/low tests (data, mask).
- Chapter 7, “Single-Ended Signals AC Parameters Tests for Strobe Signals" describes the $V_{SEH(AC)}$ and $V_{SEL(AC)}$ tests for strobe signals.
- Chapter 8, “Single-Ended Signals AC Parameters Tests for Clock" describes the $V_{SEH(AC)}$ and $V_{SEL(AC)}$ tests for clocks.
- Chapter 9, “Single-Ended Signals Overshoot/Undershoot Tests" describes the AC overshoot and undershoot tests probing and method of implementation.
- Chapter 10, “Differential Signals AC Input Parameters Tests" describes the V_{ID} AC differential input voltage tests and V_{IX} AC differential cross point voltage tests. The V_{IHdiff} and V_{ILdiff} tests for both AC and DC are also described.
- Chapter 11, “Differential Signal AC Output Parameters Tests" contains information on the V_{OX} AC differential cross point voltage tests. It also describes the SRQdiffR (40 and 60 ohm), SQRdiffF (40 and 60 ohm), $V_{OHdiff(AC)}$, and $V_{OLdiff(AC)}$ tests.
- Chapter 12, “Differential Signal Clock Cross Point Voltage Tests" describes the V_{IXCA} Clock Cross Point Voltage test.
- Chapter 13, “Differential Signals Strobe Cross Point Voltage Tests" describes the V_{IXDQ} Strobe Cross Point Voltage test.
- Chapter 14, “Clock Timing (CT) Tests" describes the clock timing operating conditions of DDR2/LPDDR2 SDRAM as defined in the specification.
- Chapter 15, “Data Strobe Timing (DST) Tests" describes various data strobe timing tests including tHZ(DQ), tLZ(DQS), tLZ(DQ), tDQSQ, tQH, tDQSS, tDQSH, tDQSL, tDSS, tDSH, tWPST, tWPRE, tRPRE, tRPST, tHZ(DQ) Low Power, tHZ(DQS) Low Power, tLZ(DQS) Low Power, tLZ(DQ) Low Power, tQSH, tQSL, tDQSS, and tDVAC (Strobe) tests.
- Chapter 16, “Data Timing Tests" describes the measurement clock tests including clock period jitter, clock to clock period jitter, cumulative error, average HIGH and LOW pulse width, half period jitter and average clock period tests.
- Chapter 17, “Command and Address Timing (CAT) Tests" describes the measurement clock tests including clock period jitter, clock to clock period jitter, cumulative error, average HIGH and LOW pulse width, half period jitter and average clock period tests.
- Chapter 18, “Custom Mode Read-Write Eye-Diagram Tests" describes the user defined real-time eye- diagram test for read cycle and write cycle.
- Chapter 19, “Calibrating the Infiniium Oscilloscope and Probe" describes how to calibrate the oscilloscope in preparation for running the DDR2(+LP) automated tests.

- Chapter 20, “InfiniiMax Probing" describes the probe amplifier and probe head recommendations for DDR2(+LP) testing.

See Also

The DDR2(+LP) Compliance Test Application Online Help, which describes:

- D9020DDRC DDR2(+LP) Automated Testing—At a Glance
- Starting the D9020DDRC DDR2(+LP) Test Application
- Creating or Opening a Test Project
- Setting Up the Test Environment
  - Set Mask File
  - Derate Table File
  - Threshold Settings
  - DDR Debug Tool
- Selecting Tests
- Configuring Tests.
  - Critical Configuration
- Verifying Physical Connections
- Running tests.
  - Options to Start Test Runs
  - Settings to Optimize Test Runs
- Configuring Automation in the Test Application
  - Using Script for Automation
  - Using Files for Automation
  - Running Automation Script or Files
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test Application
  - Customizing the Test Application
  - File Menu Option
  - View Menu Option
  - Tools Menu Option
  - Help Menu Option
  - Controlling the Application via a Remote PC
  - Using a Second Monitor

Contact Keysight

For more information on DDR2(+LP) Compliance Test Application or other Keysight Technologies' products, applications and services, please contact your local Keysight office. The complete list is available at:

www.keysight.com/find/contactus

Phone or Fax

United States:
(tel) 800 829 4444
(fax) 800 829 4433
Canada:
(tel) 877 894 4414
(fax) 800 746 4866
China:
(tel) 800 810 0189
(fax) 800 820 2816
Europe:
(tel) 31 20 547 2111
Japan:
(tel) (81) 426 56 7832
(fax) (81) 426 56 7840

Korea:
(tel) (080) 769 0800
(fax) (080) 769 0900
Latin America:
(tel) (305) 269 7500
Taiwan:
(tel) 0800 047 866
(fax) 0800 286 331
Other Asia Pacific Countries:
(tel) (65) 6375 8100
(fax) (65) 6755 0042
E-mail: tm_ap@keysight.com

Contents

1 Installing the DDR2(+LP) Compliance Test Application

If you purchased the D9020DDRC DDR2(+LP) Compliance Test Application separately, you need to install the software and license key.

Installing the Software

1. Make sure you have the minimum version of Infiniium Oscilloscope software (see D9020DDRC release notes). To ensure that you have the minimum version, select **Help** > **About Infiniium...** from the main menu.
2. To obtain the DDR2(+LP) Compliance Test Application, go to Keysight website: http://www.keysight.com/find/D9020DDRC.
3. The link for DDR2(+LP) Compliance Test Application will appear. Double-click on it and follow the instructions to download and install the application software.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

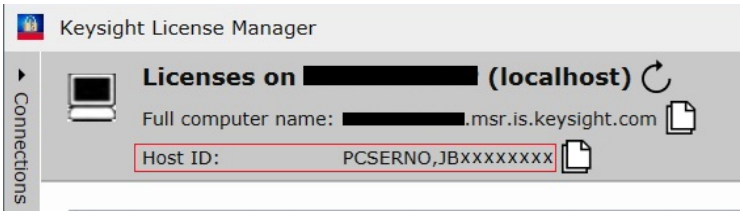

Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager.

3 From the configuration menu, use one of the options to install each license file.

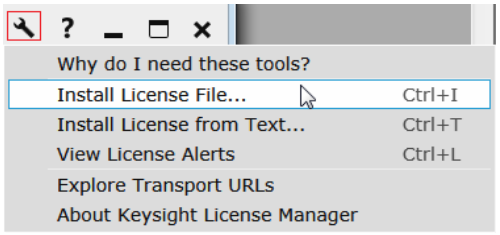

Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1 Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

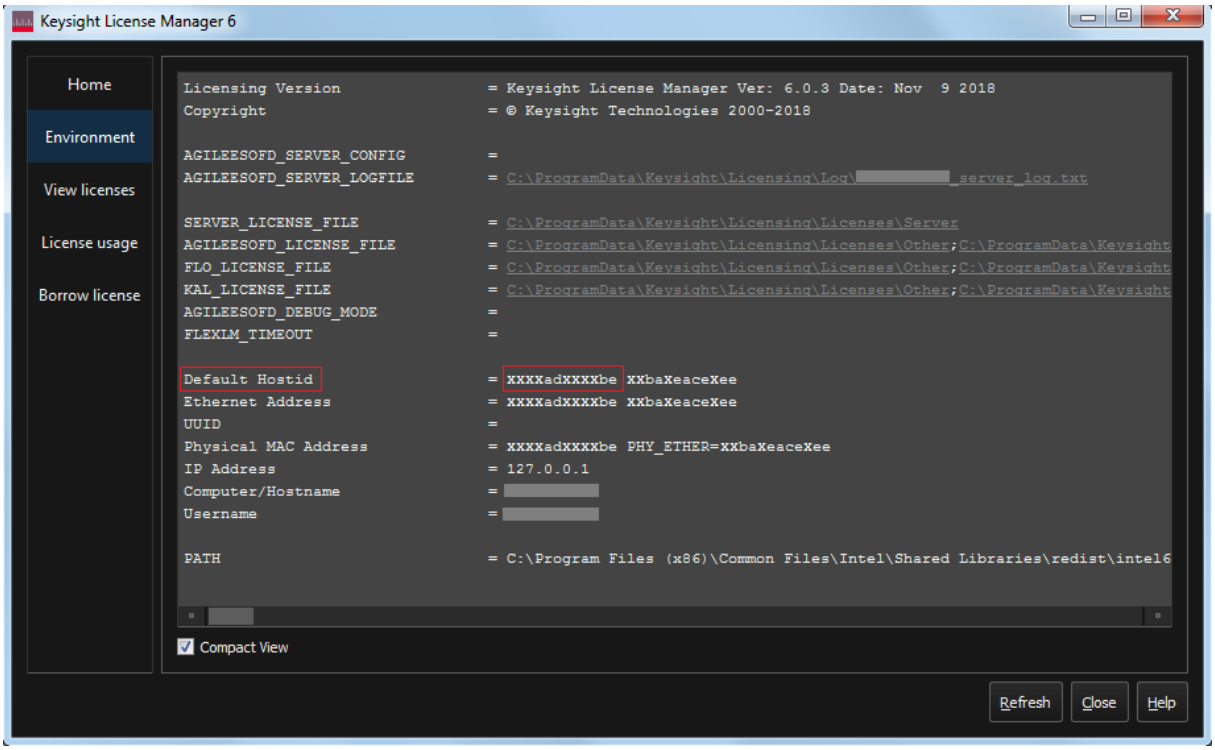

Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager 6.

3 From the Home tab, use one of the options to install each license file.

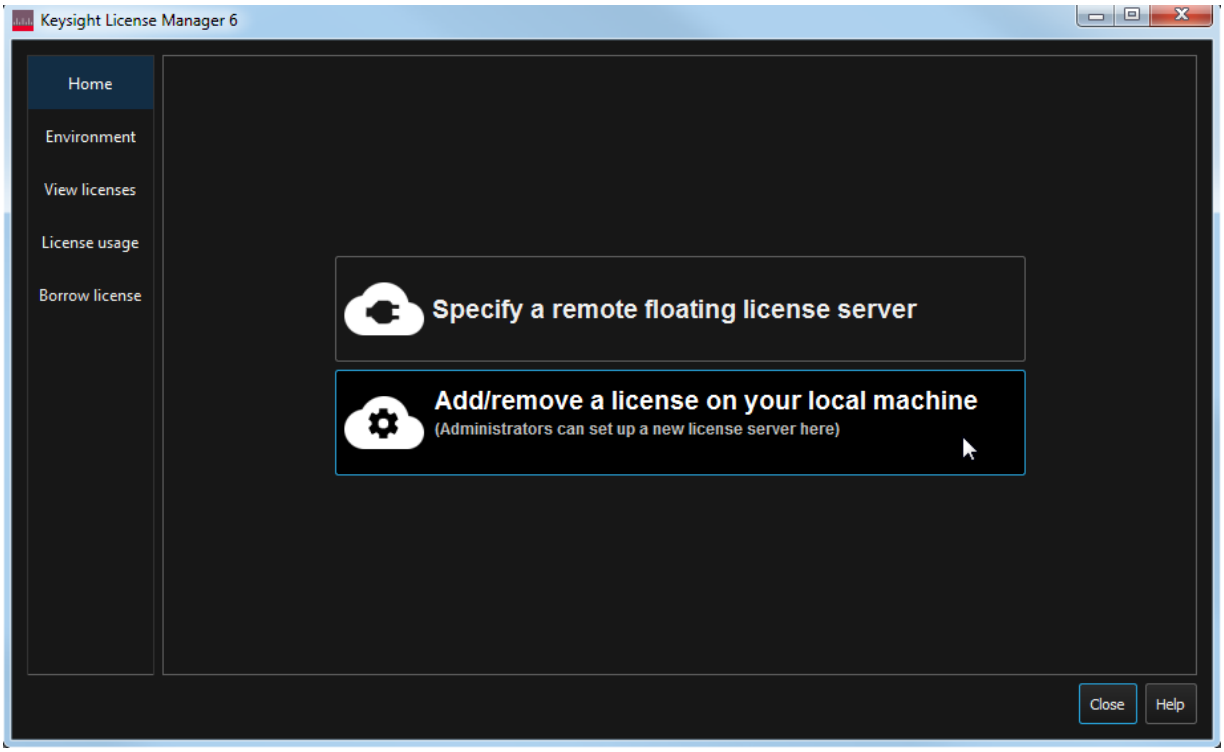

Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

2 Preparing to Take Measurements

Before running the DDR2 automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this DDR2 application. After the oscilloscope and probe have been calibrated, you are ready to start the DDR2(+LP) Compliance Test Application and perform the measurements.

Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope and probe, see Chapter 19, "Calibrating the Infiniium Oscilloscope and Probe.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the DDR2(+LP) Compliance Test Application

1 Ensure that the RAM reliability test software is running in the computer system where the Device Under Test (DUT) is attached. This software performs tests to all unused RAM in the system by producing a repetitive burst of read-write data signals to the DDR2 memory.

2 To start the DDR2(+LP) Compliance Test Application: From the Infiniium oscilloscope's main menu, choose Analyze>Automated Test Apps>DDR2 Test.

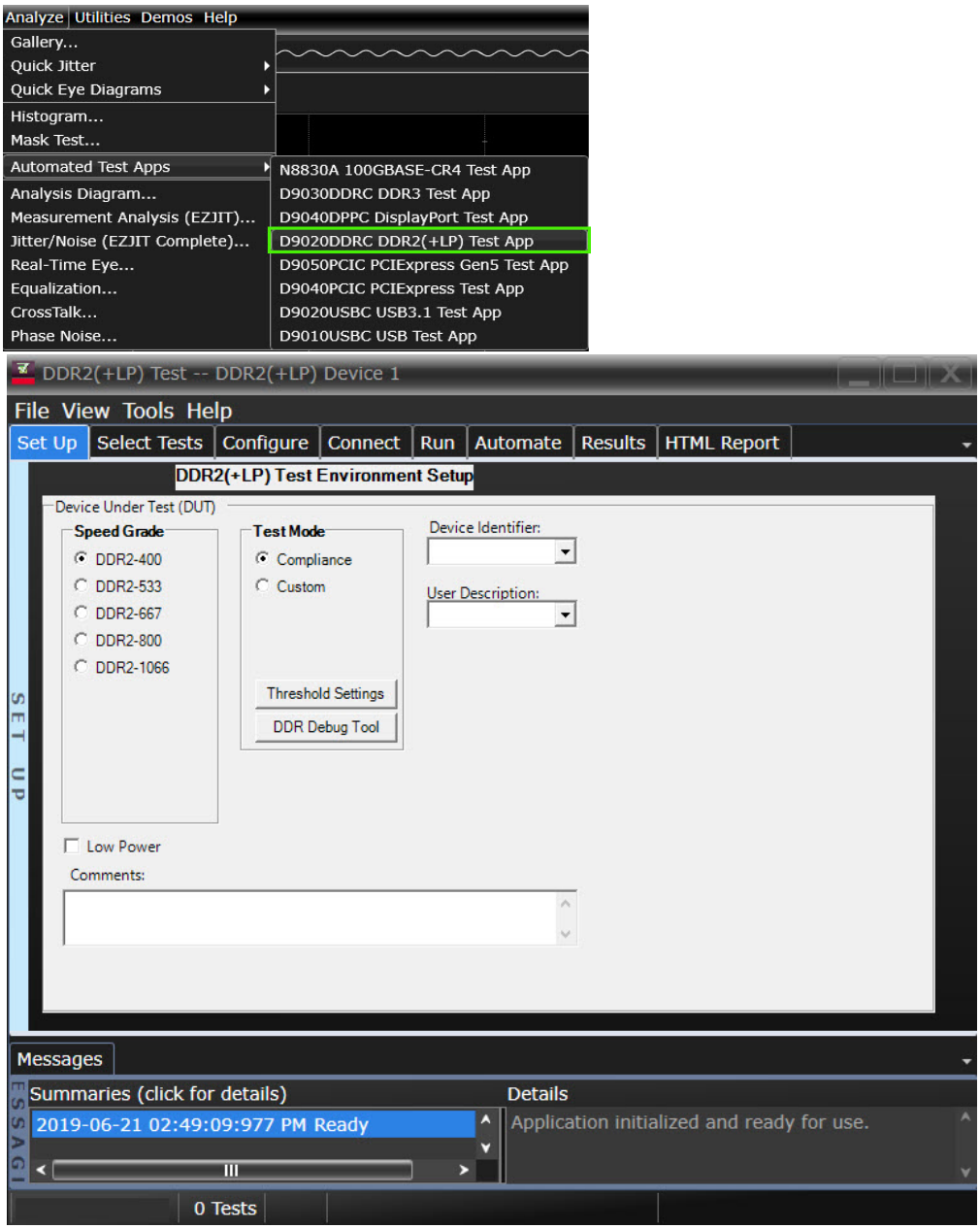

Figure 5 The DDR2(+LP) Compliance Test Application

NOTE If DDR2 Test does not appear in the Automated Test Apps menu, the DDR2(+LP) Compliance Test Application has not been installed (see Chapter 1, "Installing the DDR2(+LP) Compliance Test Application).

Figure 5 shows the DDR2(+LP) Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Tab	Description
Set Up	Lets you identify and setup the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE When you close the DDR2 application, each channel's probe is configured as single-ended or differential depending on the last DDR2 test that was run.

Online Help Topics

For information on using the DDR2(+LP) Compliance Test Application, see its online help (which you can access by choosing **Help > Contents...** from the application's main menu).

The DDR2(+LP) Compliance Test Application's online help describes:

- D9020DDRC DDR2(+LP) Automated Testing—At a Glance
- Starting the D9020DDRC DDR2(+LP) Test Application
- Creating or Opening a Test Project
- Setting Up the Test Environment
  - Set Mask File
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  - Using Script for Automation
  - Using Files for Automation
  - Running Automation Script or Files
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
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- Help Menu Options
- Controlling the Application via a Remote PC
- Using a Second Monitor

3 Measurement Clock Tests

This section provides the Methods of Implementation (MOIs) for Rising Edge and Pulse Measurements Clock tests using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

Probing for Measurement Clock Tests

When performing the Measurement Clock tests, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections. The connections for Rising Edge and Pulse Measurement Clock tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance application for the exact number of probe connections.

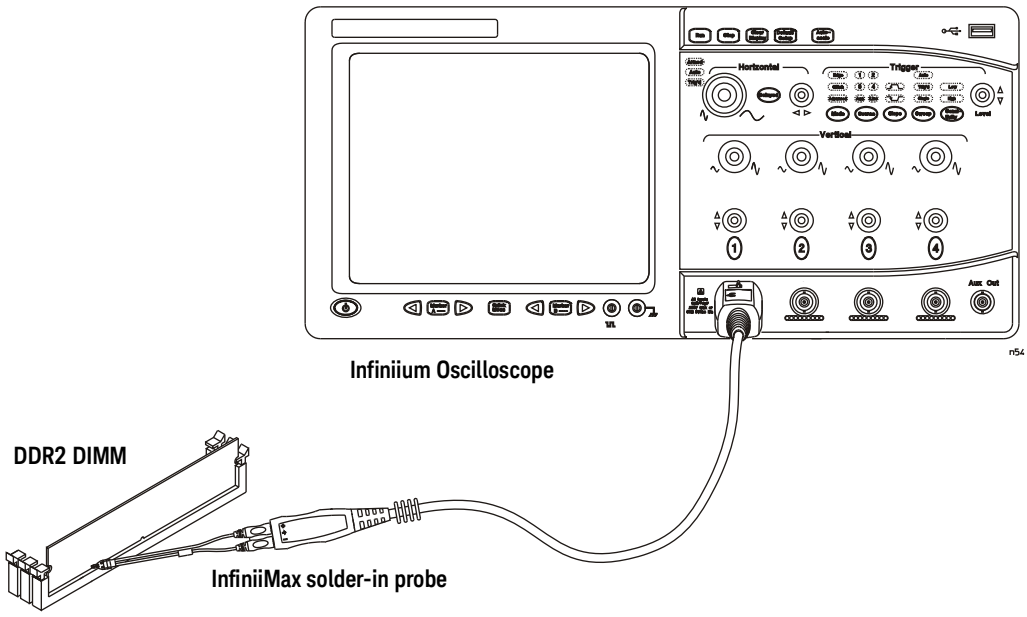


Figure 6 Probing for Measurement Clock Tests

You can use any of the oscilloscope channels as the Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channel shown in Figure 6 is just an example.)

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in "Preparing to Take Measurements" on page 25.
2 Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform a test on all the unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR2 memory.
3 Connect the differential solder-in probe head to the PUT on the DDR2 devices.
4 Connect the oscilloscope probes to any of the oscilloscope channels.
5 In the DDR2 Test application, click the Set Up tab.
6 Select the Speed Grade options. For the DDR2 Measurement Clock tests, you can select either DDR2-667, DDR2-800 and DDR2-1066 speed grade. If other Speed Grade is selected, the Measurement Clock test options will not be displayed at the Select tab.
7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

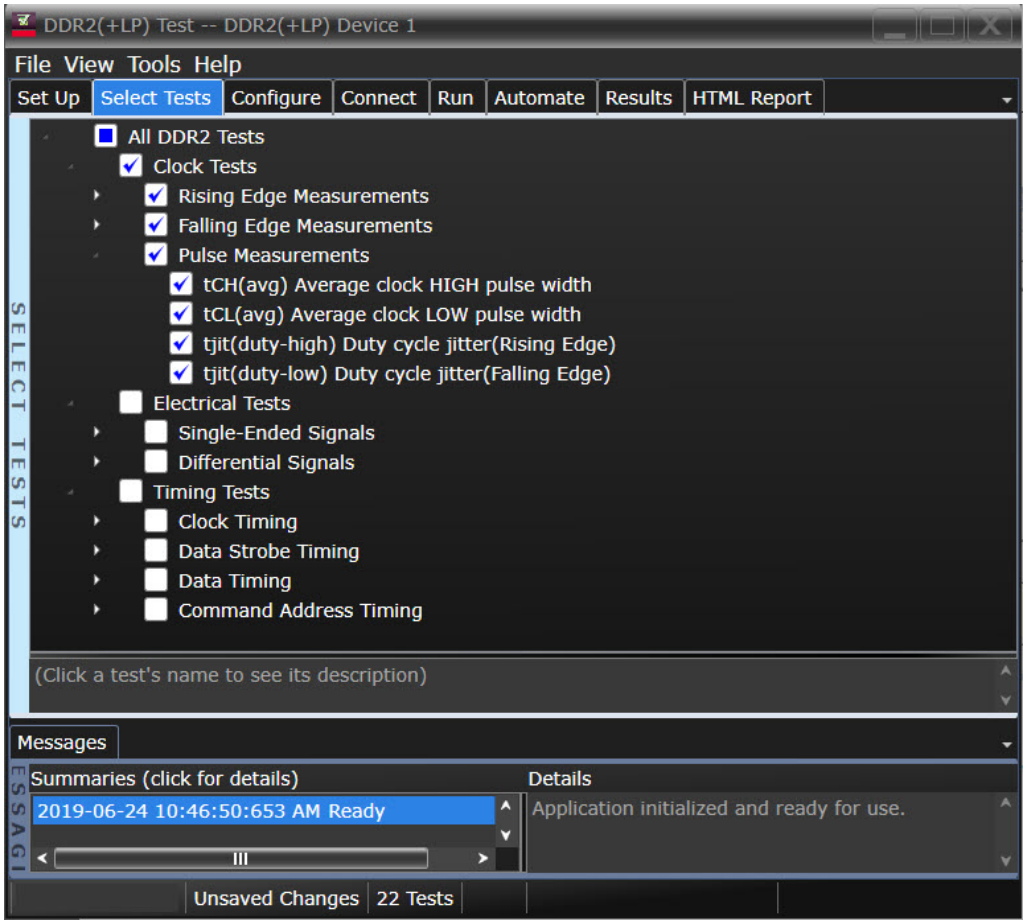


Figure 7 Selecting Measurement Clock Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options, run the test, and view the test results.

Clock Period Jitter - tJIT(per) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement and Falling Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. You can specify the rising and/or the falling edge of your signal for this measurement.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: READ or WRITE

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 2 Specific Note 35

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		Min	Max	Min	Max		
Clock Period Jitter	tJIT(per)	-125	125	-100	100	ps	35

Table 3 Specific Note 30

Parameter	Symbol	DDR2-1066		Units	Notes
		Min	Max		
Clock Period Jitter	tJIT(per)	-90	90	ps	30

Table 4 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
Max. Frequency*4				533	466	400	333	266	233	200	166	133	100	MHz
Clock Timing														
Clock Period Jitter (with allowed jitter)	t_{JIT}(per), allowed	Min		-90	-95	-100	-110	-120	-130	-140	-150	-180	-250	ps
		Max		90	95	100	110	120	130	140	150	180	250	

Test References

See Specific Note 35 in the *JEDEC Standard JESD79-2E* and Specific Note 30 in the *JESD208*, and Table 103 in the *JESD209-2B*.

Pass Condition

The tJIT(per) measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. This measurement measures the difference between every period inside a 200 cycle window with the average of the whole window.
2. Calculate the average for periods 1 to 200.
3. Measure the difference between period #1 with the average and save the answer as a measurement result.
4. Measure the difference between period #2 with the average and save the answer as a measurement result.
5. Continue with the same procedures until you complete the comparison for period #200 with the average. By now, 200 measurement results are generated.
6. Slide the window by one and measure the average of 2-201.
7. Compare period #2 with the new average. Continue the comparison for period #3, #4, ... #200, #201. By now, 200 more measurement results are added, with the total of 400 values.
8. Slide the window by one and measure the average of 3-202.
9. Compare period #3 with the new average. Continue the comparison for period #4, #5, ... #201, #202. By now, 200 more measurement results are added, with the total of 600 values.
10. Check these 600 results for the smallest and largest values (worst cases values).
11. Compare the test results against the compliance test limits.

Cycle to Cycle Period Jitter - tJIT(cc) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement as well as Falling Edge Measurement. The purpose of this test is to measure the difference in the clock period between two consecutive clock cycles. The tJIT(cc) Rising Edge Measurement measures the clock period from the rising edge of a clock cycle to the next rising edge. The tJIT(cc) Falling Edge Measurement measures the clock period from the falling edge to falling edge. The test will show a fail status if the total failed waveforms is greater than 0.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: READ or WRITE

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 5 Specific Note 35

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		Min	Max	Min	Max		
Cycle to Cycle Period Jitter	tJIT(cc)	-250	250	-200	200	ps	35

Table 6 Specific Note 30

Parameter	Symbol	DDR2-1066		Units	Notes
		Min	Max		
Cycle to Cycle Period Jitter	tJIT(cc)	-180	180	ps	30

Table 7 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
Max. Frequency*4				533	466	400	333	266	233	200	166	133	100	MHz
				Clock Timing										
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	t_{JIT}(cc), allowed	Max		180	190	200	220	240	260	280	300	360	500	ps

Test References

See Specific Note 35 in the *JEDEC Standard JESD79-2E*, Specific Note 30 in the *JESD208*, and Table 103 in *JESD209-2B*.

Pass Condition

The tJIT(cc) measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1 Measure the difference between every adjacent pair of periods.

2 Generate 201 measurement results.

3 Check the results for the smallest and largest values (worst case values).

4 Compare the test results against the compliance test limits.

Cumulative Error - tERR(n per) - Test Method of Implementation

This Cumulative Error (across “n” cycles) test is applicable to the Rising Edge Measurement as well as the Falling Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. Supported measurements include multiple cycle windows with values of "n" (for "n" cycle) where n>5 but less than 50.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: READ or WRITE

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 8 Specific Note 35

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		min	max	min	max		
Cumulative error across 2 cycles	tERR(2per)	-175	175	-150	150	ps	35
Cumulative error across 3 cycles	tERR(3per)	-225	225	-175	175	ps	35
Cumulative error across 4 cycles	tERR(4per)	-250	250	-200	200	ps	35
Cumulative error across 5 cycles	tERR(5per)	-250	250	-200	200	ps	35
Cumulative error across n cycles, n = 6....10, inclusive	tERR(6-10 per)	-350	350	-300	300	ps	35
Cumulative error across n cycles, n = 11...50, inclusive	tERR(11-50 per)	-450	450	-450	450	ps	35

Table 9 Specific Note 30

Parameter	Symbol	DDR2-1066		Units	Notes
		min	max		
Cumulative error across 2 cycles	tERR(2per)	-132	132	ps	30
Cumulative error across 3 cycles	tERR(3per)	-157	157	ps	30
Cumulative error across 4 cycles	tERR(4per)	-175	175	ps	30
Cumulative error across 5 cycles	tERR(5per)	-188	188	ps	30
Cumulative error across n cycles, n = 6....10, inclusive	tERR(6-10 per)	-250	250	ps	30
Cumulative error across n cycles, n = 11...50, inclusive	tERR(11-50 per)	-425	425	ps	30

Table 10 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*[5]	400	333	266*[5]	200*[5]	
Max. Frequency*[4]				533	466	400	333	266	233	200	166	133	100	MHz
				Clock Timing										
Cumulative error across 2 cycles	t_{JIT}(2 per), allowed	Min		-132	-140	-147	-162	-177	-191	-206	-221	-265	-368	ps
		Max		132	140	147	162	177	191	206	221	265	368	
Cumulative error across 3 cycles	t_{JIT}(3 per), allowed	Min		-157	-166	-175	-192	-210	-227	-245	-262	-314	-437	ps
		Max		157	166	175	192	210	227	245	262	314	437	
Cumulative error across 4 cycles	t_{JIT}(4 per), allowed	Min		-175	-185	-194	-214	-233	-253	-272	-291	-350	-486	ps
		Max		175	185	194	214	233	253	272	291	350	486	
Cumulative error across 5 cycles	t_{JIT}(5 per), allowed	Min		-188	-199	-209	-230	-251	-272	-293	-314	-377	-524	ps
		Max		188	199	209	230	251	272	293	314	377	524	
Cumulative error across 6 cycles	t_{JIT}(6 per), allowed	Min		-200	-211	-222	-244	-266	-288	-311	-333	-399	-555	ps
		Max		200	211	222	244	266	288	311	333	399	555	
Cumulative error across 7 cycles	t_{JIT}(7 per), allowed	Min		-209	-221	-232	-256	-279	-302	-325	-248	-418	-581	ps
		Max		209	221	232	256	279	302	325	248	418	581	
Cumulative error across 8 cycles	t_{JIT}(8 per), allowed	Min		-217	-229	-241	-256	-290	-314	-338	-362	-435	-604	ps
		Max		217	229	241	256	290	314	338	362	435	604	
Cumulative error across 9 cycles	t_{JIT}(9 per), allowed	Min		-224	-237	-249	-274	-299	-324	-349	-374	-449	-624	ps
		Max		224	237	249	274	299	324	349	374	449	624	
Cumulative error across 10 cycles	t_{JIT}(10 per), allowed	Min		-231	-244	-257	-282	-308	-334	-359	-385	-462	-641	ps
		Max		231	244	257	282	308	334	359	385	462	641	
Cumulative error across 11 cycles	t_{JIT}(11 per), allowed	Min		-237	-250	-263	-289	-316	-342	-368	-395	-474	-658	ps
		Max		237	250	263	289	316	342	368	395	474	658	
Cumulative error across 12 cycles	t_{JIT}(12 per), allowed	Min		-242	-256	-269	-296	-323	-350	-377	-403	-484	-672	ps
		Max		242	256	269	296	323	350	377	403	484	672	

Test References

See Specific Note 35 in the *JEDEC Standard JESD79-2E,* Specific Note 30 in the *JESD208* and Table 103 in the *JESD209-2B*.

Pass Condition

The tERR measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. tERR(2per) is similar to tJIT(per), except it makes a small 2-cycle window inside the big 200 cycle window and compares the average of the small window with the average of the big window.
2. Calculate the average for periods 1 to 200.
3. Calculate the average for periods 1 and 2.
4. Measure the difference of these two averages and save the answer as a measurement result.
5. Calculate the average of periods 2 and 3, and measure the difference between this average and the big window average.
6. Continue with the same procedures until the average of periods 199 and 200 to the big window average is compared. By now, 199 measurement results are generated.
7. Slide the big window by one and start comparing the average of periods 2 and 3 with the new big window average until the comparison for periods 200 and 201 with the big window is completed. By now, 199 more measurements are added, with the total of 398 measurement values.
8. Slide the big window by one again and repeat the same procedures. By now, 199 more measurements are added, with the total of 597 measurement values.
9. Check the 597 results for the smallest and largest values (worst case values).
10. Compare the test results to the compliance test limits.
11. tERR(3per) is the same as tERR(2per) except the small window size is three periods wide. tERR(4per) uses small window size of four periods, and tERR(5per) uses five periods.
12. tERR(6-10per) executes tERR(6per), tERR(7per), tERR(8per), tERR(9per) and tERR(10per), combines all the measurement results together into one big pool, and checks for the smallest and largest values.
13. tERR(11-50per) does the same for tERR(11per) through tERR(50per).

Cumulative Error (across 13-50 cycles) - tERR (13-50 per) (Low Power) - Test Method of Implementation

This Cumulative Error (across 13- 50 cycles) test is applicable to the Rising Edge Measurement as well as the Falling Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock from 13 cycles to 50 cycles.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ or WRITE

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 11 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
Max. Frequency*4				533	466	400	333	266	233	200	166	133	100	MHz
Clock Timing														
Cumulative error across n = 13, 14, ... 49, 50 cycles	t_{ERR}(nper), allowed	Min		t_{ERR}(nper), allowed, min = {1 + 0.68ln(n)} * t_{JIT}(per), allowed, min										ps
		Max		t_{ERR}(nper), allowed, max = {1 + 0.68ln(n)} * t_{JIT}(per), allowed, max										

Test References

See Table 103 in the *JEDEC Standard JESD209-2B*.

Pass Condition

The tERR measurement value from 13- cycle through 50 cycle should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202. tERR(13- 50per) executes tERR(13per) through tERR(50per). For tERR(13per):

1 Calculate the average for periods 1-200.

2 Calculate the average for periods 1-13.

3 Measure the difference between these two averages and save the answer as a tERR(13per) result.

4 Continue with the same procedures until the average of the last thirteen periods (188-200) is compared to the average for periods 1-200.Continue with the same procedures until the average of the last thirteen periods (188-200) is compared to the average for periods 1-200.

5 Slide the window by one and start comparing the average of periods 2-14 and end by comparing the average of periods 189-201.

6 Slide the window by one again and repeat the same procedures.

7 Calculate the compliance upper and lower limits for tERR(13per):
Upper limit = $\{1 + 0.68\ln(n)\} * t_{JIT}(per),max.$ (where n=13)
Lower limit = $\{1 + 0.68\ln(n)\} * t_{JIT}(per),min.$ (where n=13)
NOTE: $t_{JIT}(per),max$ and $t_{JIT}(per),min$ vary depending on the speed grade selected.

8 Check all tERR(13per) results for the smallest and largest values (worst case values).

9 Compare the worst case tERR(13per) results to the compliance test limit.

10 Perform the same procedure for tERR(14per) through tERR(50per).

Average HIGH Pulse Width - tCH(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the positive pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: READ or WRITE

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 12 Timing Parameters by Speed Grade (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Average clock HIGH pulse width	tCH(avg)	0.48	0.52	0.48	0.52	tCK(avg)	35,36

Table 13 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
Average clock HIGH pulse width	tCH(avg)	0.48	0.52	tCK(avg)	30,31

Table 14 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
Max. Frequency*4				533	466	400	333	266	233	200	166	133	100	MHz
Clock Timing														
Average high pulse width	t_{CH}(avg)	Min							0.45					t_{CK}(avg)
		Max							0.55					

Test References

See Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*, Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*, and Table 103 in the *JESD209-2B*.

Pass Condition

The tCH measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding “window” of 200 cycles.
2. Measure the width of the high pulses 1-200 and determine the average value for this window. By now, one measurement result is generated.
3. Measure the width of the high pulses 2-201 and determine the average value for this window. By now, one measurement result is generated, with the total of two measurement results.
4. Measure the width of the high pulses 3-202 and determine the average value for this window. By now, one measurement result is generated, with the total of three measurement results.
5. Check the total 3 results for the smallest and largest values (worst case values).
6. Compare the test results against the compliance test limits.

Absolute HIGH Pulse Width - tCH(abs) - Test Method of Implementation

The purpose of this test is to measure the absolute duty cycle of all the positive pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ or WRITE

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 15 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
Max. Frequency*4				533	466	400	333	266	233	200	166	133	100	MHz
Clock Timing														
Average clock HIGH pulse width (with allowed jitter)	t_{CH}(abs), allowed	Min							0.43					t_{CK}(avg)
		Max							0.57					

Test References

See Table 103 in the *JESD209-2B*.

Pass Condition

The absolute tCH measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1 Find the average period, tCK(avg) for cycle 1-202.

2 Find the maximum high pulse width, PW_{MAX}(s) for cycle 1-202.

3 Find the minimum high pulse width, PW_{MIN}(s) for cycle 1-202.

4 Calculate $PW_{MAX}(tCK) = PW_{MAX}(s)/tCK(avg)$.

5 Calculate $PW_{MIN}(tCK) = PW_{MIN}(s)/tCK(avg)$.

6 Check PW_{MAX}(tCK) and PW_{MIN}(tCK) for the worst case values.

7 Compare the test result to the compliance test limit.

Average Low Pulse Width - tCL(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the negative pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: READ or WRITE

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 16 Timing Parameters by Speed Grade (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		Min	Max	Min	Max		
Average clock LOW pulse width	tCL(avg)	0.48	0.52	0.48	0.52	tCK(avg)	35,36

Table 17 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Notes
		Min	Max		
Average clock LOW pulse width	tCL(avg)	0.48	0.52	tCK(avg)	30,31

Table 18 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
Max. Frequency*4				533	466	400	333	266	233	200	166	133	100	MHz
Clock Timing														
Average Low pulse width	t_{CL}(avg)	Min							0.45					t_{CK}(avg)
		Max							0.55					

Test References

See Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*, Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208* and Table 103 in the *JESD209-2B*.

Pass Condition

The tCL measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding “window” of 200 cycles.
2. Measure the width of the low pulses 1-200 and determine the average value for this window. By now, one measurement result is generated.
3. Measure the width of the low pulses 2-201 and determine the average value for this window. By now, one measurement result is generated, with the total of two measurement results.
4. Measure the width of the low pulses 3-202 and determine the average value for this window. By now, one measurement result is generated, with the total of three measurement results.
5. Check the total results (three values) for the smallest and largest values (worst case values).
6. Compare results against the compliance test limits.

Absolute Low Pulse Width - tCL(abs) - Test Method of Implementation

The purpose of this test is to measure the absolute duty cycle of all the negative pulse widths within a window of 202 consecutive cycles.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ or WRITE

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 19 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
Max. Frequency*4				533	466	400	333	266	233	200	166	133	100	MHz
Clock Timing														
Absolute clock LOW pulse width (with allowed jitter)	t_{CL}(abs), allowed	Min							0.43					t_{CK}(avg)
		Max							0.57					

Test References

See Table 103 in the *JESD209-2B*.

Pass Condition

The absolute tCL measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1 Find the average period, tCK(avg) for cycle 1-202.

2 Find the maximum low pulse width, PW_{MAX}(s) for cycle 1-202.

3 Find the minimum low pulse width, PW_{MIN}(s) for cycle 1-202.

4 Calculate $PW_{MAX}(tCK) = PW_{MAX}(s)/tCK(avg)$.

5 Calculate $PW_{MIN}(tCK) = PW_{MIN}(s)/tCK(avg)$.

6 Check $PW_{MAX}(tCK)$ and $PW_{MIN}(tCK)$ for the worst case values.

7 Compare the test result to the compliance test limit.

Half Period Jitter - tJIT(duty) - Test Method of Implementation

The Half Period Jitter tJIT(duty) can be divided into tJIT(CH) Jitter Average HIGH and tJIT(LH) Jitter Average Low. The tJIT(CH) Jitter Average HIGH Measurement measures between a positive pulse width of a cycle in the waveform, and the average positive pulse width of all cycles in a 200 consecutive cycle window. tJIT(LH) Jitter Average Low Measurement measures between a negative pulse width of a cycle in the waveform and the average negative pulse width of all cycles in a 200 consecutive cycle window.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: READ or WRITE

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 20 Specific Note 35

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		Min	Max	Min	Max		
Duty cycle jitter	tJIT(duty)	-125	125	-100	100	ps	35

Table 21 Specific Note 30

Parameter	Symbol	DDR2-1066		Units	Notes
		Min	Max		
Duty cycle jitter	tJIT(duty)	-75	75	ps	30

Table 22 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
Max. Frequency*4				533	466	400	333	266	233	200	166	133	100	MHz
Clock Timing														
Duty cycle jitter (with allowed jitter)	t_{JIT}(duty), allowed	Min		$\min((t_{CH}(abs),min - t_{CH}(avg),min), (t_{CL}(abs),min - t_{CL}(avg),min)) * t_{CK}(avg)$										$t_{CK}(avg)$
		Max		$\max((t_{CH}(abs),max - t_{CH}(avg),max), (t_{CL}(abs),max - t_{CL}(avg),max)) * t_{CK}(avg)$										

Test References

See Specific Note 35 in the *JEDEC Standard JESD79-2E,* Specific Note 30 in the *JESD208*, and Table 103 in the *JESD209-2B.*

Pass Condition

The tJIT(duty) measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

tJIT(CH)

1 This measurement measures the difference between every high pulse width inside a 200 cycle window with the average of the whole window.
2 Calculate the average for high pulse widths 1 to 200.
3 Measure the difference between high pulse width #1 with the average and save the answer as a measurement result.
4 Measure the difference between high pulse width #2 with the average and save the answer as a measurement result.
5 Continue the same procedures until the comparison for high pulse width #200 with the average is completed. By now, 200 measurement results are generated.
6 Slide the window by one and measure the average of 2-201.
7 Compare high pulse width #2 with the new average. Continue the comparison for high pulse width #3, #4, ... #200, #201. By now, 200 more measurement results are added, with the total of 400 values.
8 Slide the window by one and measure the average of 3-202.
9 Compare high pulse width #3 with the new average. Continue the comparison for high pulse width #4, #5, ... #201, #202. By now, 200 more measurement results are added, with the total of 600 values.
10 Check these 600 results for the smallest and largest values (worst cases values).
11 Compare the test results against the compliance test limits.

tJIT(LH)

1 This measurement is similar to tJIT(CH) above except, instead of using high pulse widths, it uses LOW pulse widths for testing comparison.

Average Clock Period - tCK(avg) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement as well as the Falling Edge Measurement. tCK(avg) is average clock period within 200 consecutive cycle window. The tCK(avg) Rising Edge Measurement measures the period from the rising edge of a cycle to the next rising edge within the waveform window. The tCK(avg) Falling Edge Measurements measures from the falling edge to the falling edge.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: READ or WRITE

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 23 Timing Parameters by Speed Grade (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Average clock period	tCK(avg)	3000	8000	2500	8000	ps	35,36

Table 24 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
Average clock period	tCK(avg)	1875	7500	ps	30,31

Table 25 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
Max. Frequency*4				533	466	400	333	266	233	200	166	133	100	MHz
Clock Timing														
Average clock Period	t_{CK}(avg),	Min		1.875	2.15	2.5	3	3.75	4.3	5	6	7.5	10	ns
		Max		100										

Test References

See Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E,* Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*, and Table 103 in the *JESD209-2B*.

Pass Condition

The tCK(avg) measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1 This measurement measures a sliding “window” of 200 cycles.
2 Calculate the average period value for periods 1-200. By now, one measurement result is generated.
3 Calculate the average period value for periods 2-201. By now, one measurement result is generated, with the total of two measurement results.
4 Calculate the average period value for periods 3-202. By now, one measurement result is generated, with the total of three measurement results.
5 Check the results for the smallest and largest values (worst case values).
6 Compare the test results against the compliance test limits.

Absolute Clock Period - tCK(abs) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement as well as the Falling Edge Measurement. tCK(abs) is absolute clock period within 202 consecutive cycle window. The tCK(abs) Rising Edge Measurement measures the period from the rising edge of a cycle to the next rising edge within the waveform window. The tCK(abs) Falling Edge Measurements measures from the falling edge to the falling edge.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ or WRITE

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 26 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
Max. Frequency*4				533	466	400	333	266	233	200	166	133	100	MHz
Clock Timing														
Absolute Clock Period	$t_{CK}(abs)$	min		$t_{CK}(avg),min + t_{JIT}(per),min$										ps

Test References

See Table 103 in the *JESD209-2B*.

Pass Condition

The tCK(abs) measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1 Find the maximum period value for period 1-202.

2 Find the minimum period value for period 1-202.

3 Check these two results for the worst case values.

4 Compare the test result against the compliance test limit.

4 Single-Ended Signals AC Input Parameters Tests

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals AC Input tests using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

Probing for Single-Ended Signals AC Input Parameters Tests

When performing the Single-Ended Signals AC Input Parameters tests, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections. The connection for the Single-Ended Signals AC Input Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance application for the exact number of probe connections.

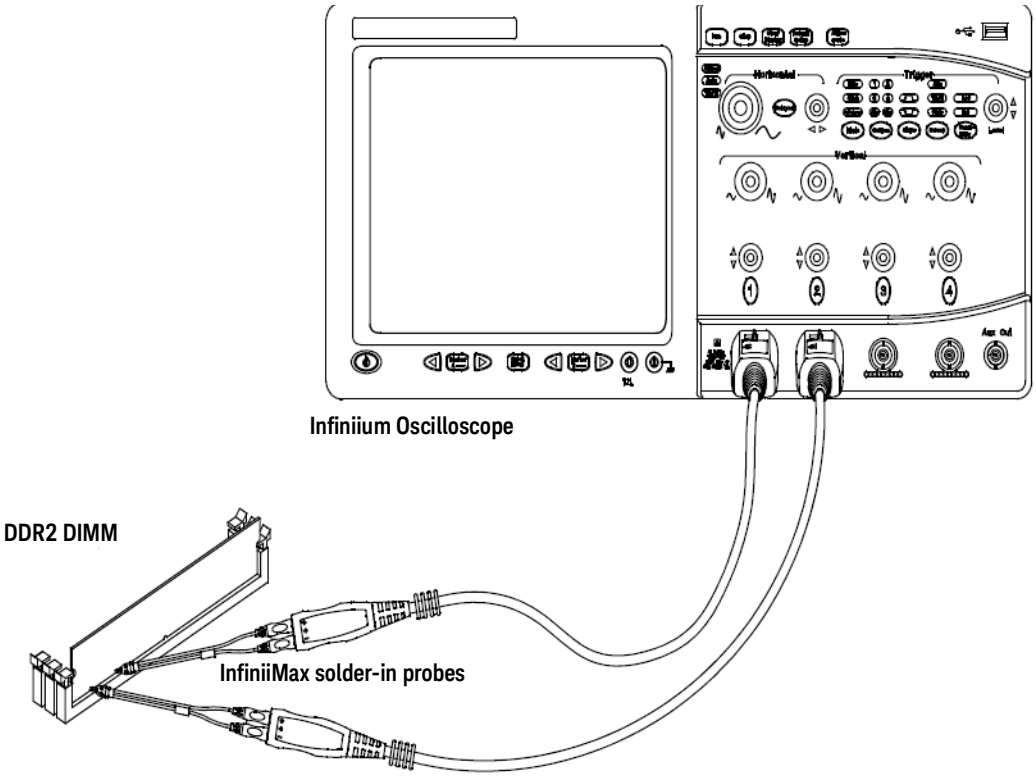


Figure 8 Probing for Single-Ended Signals AC Input Parameters Tests with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channels shown in Figure 8 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in "Starting the DDR2(+LP) Compliance Test Application" on page 27.
2 Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR2 memory.
3 Connect the differential solder-in probe head to the PUTs on the DDR2 devices.
4 Connect the oscilloscope probes to any channels of the oscilloscope.
5 In the DDR2 Test application, click the Set Up tab.

6 Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800, DDR2-1066.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

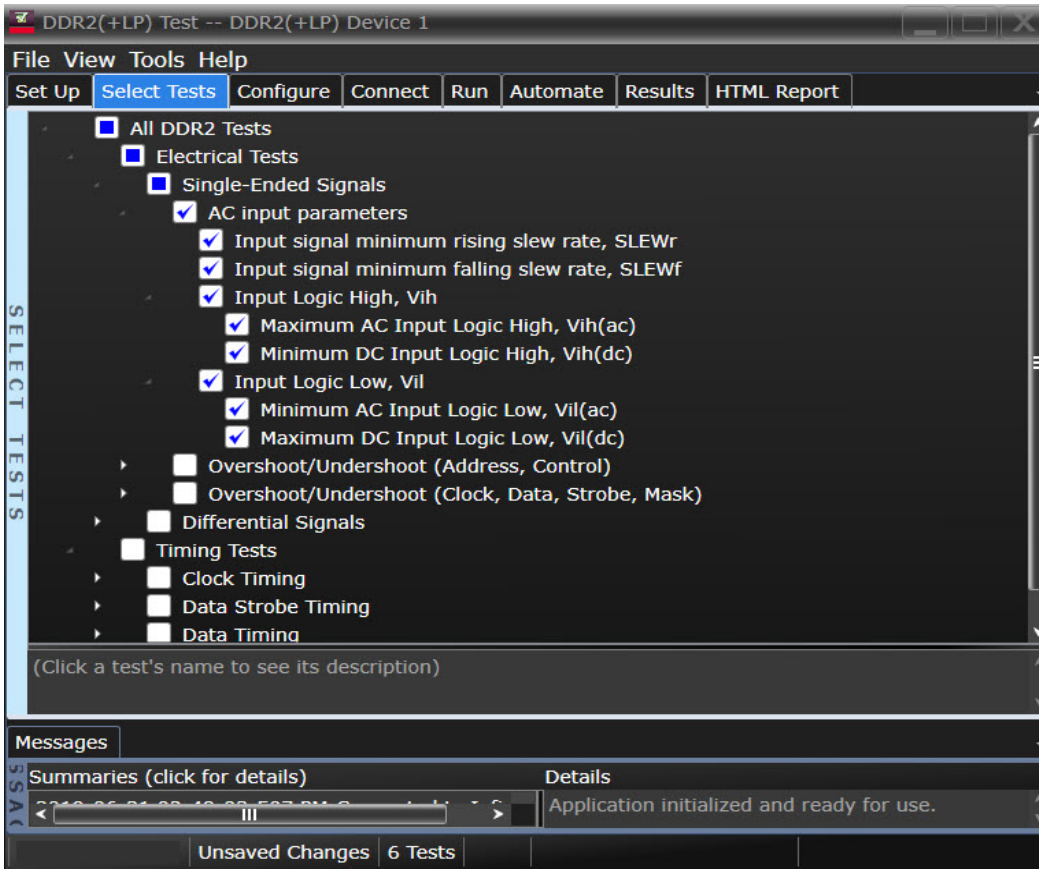


Figure 9 Selecting Single-Ended Signals AC Input Parameters Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options, run the tests and view the tests results.

$V_{IH(AC)}$ Test for DQ, DM - Test Method of Implementation

$V_{IH(AC)}$ - Maximum AC Input Logic HIGH for DQ, DM.

The purpose of this test is to verify that voltage level of test signal at tDS (DM and DQ input setup time in JEDEC specification) before DQS midpoint is greater than the conformance lower limits of the $V_{IH(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

The value of V_{PEAK} which directly affects the conformance upper limit is set to 0.5V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{PEAK}.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signal) OR
- Data Mask Signals (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above.
- Supporting Pin - Data Strobe Signals.

Test Definition Notes from the Specification

Table 27 Input AC Logic Level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units	Notes
		Min	Max	Min	Max		
$V_{IH(AC)}$	AC input logic HIGH	V_{REF} + 0.250	V_{DDQ}+V_{PEAK}	V_{REF} + 0.200	V_{DDQ}+V_{PEAK}	V	1

Table 28 Input AC Logic Level (DDR2-1066)

Symbol	Parameter	DDR2-1066		Units	Notes
		Min	Max		
$V_{IH(AC)}$	AC input logic HIGH	V_{REF} + 0.200	-	V	-

Test References

See Table 20 - Input AC Logic Level in the *JEDEC Standard JESD79-2E* and Table 20 - Input AC Logic Level in the *JESD208*.

PASS Condition

The voltage level at tDS (DM and DQ input setup time in JEDEC specification) before DQS midpoint for the high level voltage shall be greater than or equal to the minimum $V_{IH(AC)}$ value.

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising DQ crossings that cross $V_{IH(AC)}$ in the burst.
4. For all DQ crossings found, locate all the following DQS crossings that cross 0V.
5. Calculate the time where the test result is taken. Calculation is expressed as:
   $T_{TESTRESULT} = T_{DQS\ MIDPOINT}$ - tDS.
   (tDS - DM and DQ input setup time in JEDEC specification which is due to speed grade.)
6. Take voltage level of DQ signal at $T_{TESTRESULT}$ as the test result for $V_{IH(AC)}$.
7. Collect all $V_{IH(AC)}$.
8. Determine the worst result from the set of $V_{IH(AC)}$ measured.

$V_{IH(AC)}$ Test for DQS - Test Method of Implementation

$V_{IH(AC)}$ - Maximum AC Input Logic HIGH for DQS.

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window is greater than the conformance lower limits of the $V_{IH(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

The value of V_{PEAK} which directly affects the conformance upper limit is set to 0.5V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{PEAK}.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: Yes

Signal(s) of Interest:

Data Strobe Signals (supported by Data Signals).

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 29 Input AC Logic Level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units	Notes
		Min	Max	Min	Max		
$V_{IH(AC)}$	AC input logic HIGH	V_{REF} + 0.250	$V_{DDQ}+V_{PEAK}$	V_{REF} + 0.200	$V_{DDQ}+V_{PEAK}$	V	1

Table 30 Input AC Logic Level (DDR2-1066)

Symbol	Parameter	DDR2-1066		Units	Notes
		Min	Max		
$V_{IH(AC)}$	AC input logic HIGH	V_{REF} + 0.200	-	V	-

Test References

See Table 20 - Input AC Logic Level in the *JEDEC Standard JESD79-2E* and Table 20 - Input AC Logic Level in the *JESD208*.

PASS Condition

The voltage level at tDS (DM and DQ input setup time in JEDEC specification) before DQS midpoint for the high level voltage shall be greater than or equal to the minimum $V_{IH(AC)}$ value.

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising DQ crossings that cross $V_{IH(AC)}$ in the burst.
4. For all DQ crossings found, locate all the following DQS crossings that cross 0V.
5. Calculate the time where the test result is taken. Calculation is expressed as:
   $T_{TESTRESULT} = T_{DQS\ MIDPOINT}$ - tDS.
   (tDS - DM and DQ input setup time in JEDEC specification which is due to speed grade.)
6. Take voltage level of DQ signal at $T_{TESTRESULT}$ as the test result for $V_{IH(AC)}$.
7. Collect all $V_{IH(AC)}$.
8. Determine the worst result from the set of $V_{IH(AC)}$ measured.

$V_{IH(AC)}$ Test for Address, Control - Test Method of Implementation

$V_{IH(AC)}$ - Maximum AC Input Logic HIGH for Address, Control.

The purpose of this test is to verify that the mode of histogram of the high level voltage value of the test signal within a valid sampling window is greater than the conformance lower limits of the $V_{IH(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

The value of V_{PEAK} which directly affects the conformance upper limit is set to 0.5V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{PEAK}.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: No

Signal(s) of Interest:

- Address Signals OR
- Control Signals OR
- Clock Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any of the signal of interest defined above.

Test Definition Notes from the Specification

Table 31 Input AC Logic Level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units	Notes
		Min	Max	Min	Max		
$V_{IH(AC)}$	AC input logic HIGH	V_{REF} + 0.250	$V_{DDQ}+V_{PEAK}$	V_{REF} + 0.200	$V_{DDQ}+V_{PEAK}$	V	1

Table 32 Input AC Logic Level (DDR2-1066)

Symbol	Parameter	DDR2-1066		Units	Notes
		Min	Max		
$V_{IH(AC)}$	AC input logic HIGH	V_{REF} + 0.200	-	V	-

Test References

See Table 20 - Input AC Logic Level in the *JEDEC Standard JESD79-2E* and Table 20 - Input AC Logic Level in the *JESD208*.

PASS Condition

The mode value for the high level voltage shall be greater than or equal to the minimum $V_{IH(AC)}$ value.

Measurement Algorithm

1 Sample/acquire signal data.
2 Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at valid rising edge and end at V_{REF} crossing at the following valid falling edge (See notes on threshold).
3 Zoom in on the first valid positive pulse and perform VTOP measurement. Take the VTOP measurement results as $V_{IH(AC)}$ value.
4 Continue the previous step with another 9 valid positive pulses that were found in the burst.
5 Determine the worst result from the set of $V_{IH(AC)}$ measured

.

$V_{IH(DC)}$ Test for DQ, DM - Test Method of Implementation

$V_{IH(DC)}$ - Minimum DC Input Logic HIGH for DQ, DM.

The purpose of this test is to verify that the min of histogram of the high level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{IH(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals) OR
- Data Mask Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - Data Strobe Signals

Test Definition Notes from the Specification

Table 33 Input DC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IH(DC)}$	DC input logic HIGH	V_{REF} + 0.125	V_{DDQ} + 0.3	V	-

Table 34 Input DC Logic Level (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{IH(DC)}$	DC input logic HIGH	V_{REF} + 0.125	V_{DDQ} + 0.3	V	-

Test References

See Table 19 - Input DC Logic Level, in the *JEDEC Standard JESD79-2E* and Table 19 - Input DC Logic Level in the *JESD208*.

PASS Condition

The minimum value of test signal from tDS before DQS midpoint to tDH after DQS midpoint for the high level voltage shall be greater than or equal to the minimum $V_{IH(DC)}$ value.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IH(AC)}$ in the burst.
4 For all DQ crossings found, locate all the following DQS crossings that cross midpoint. (0V for differential DQS and V_{REF} for single ended DQS)
5 Setup the histogram function settings where the X region is:
   - Ax: X-time position where tDS (DM and DQ input setup time in JEDEC specification) before DQS crossing midpoint.
   - Bx: X-time position where tDH (DM and DQ input hold time in JEDEC specification) after DQS crossing midpoint.
   - By: Y- position at VREF voltage level.
   - Ay: Top of the displaying window just to make sure it covers the maximum level of the respective signal.
6 Take histogram 'Min' value as the test result for $V_{IH(DC)}$.
7 Collect all $V_{IH(DC)}$.
8 Determine the worst result from the set of $V_{IH(DC)}$ measured.

$V_{IH(DC)}$ Test for DQS - Test Method of Implementation

$V_{IH(DC)}$ - Minimum DC Input Logic HIGH for DQS.

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window is greater than the conformance lower limits of the $V_{IH(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 35 Input DC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IH(DC)}$	DC input logic HIGH	V_{REF} + 0.125	V_{DDQ} + 0.3	V	-

Table 36 Input DC Logic Level (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{IH(DC)}$	DC input logic HIGH	V_{REF} + 0.125	V_{DDQ} + 0.3	V	-

Test References

See Table 19 - Input DC Logic Level, in the *JEDEC Standard JESD79-2E* and Table 19 - Input DC Logic Level in the *JESD208*.

PASS Condition

The high level voltage of DQS shall be greater than or equal to the minimum $V_{IH(DC)}$ value.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation).
2 Take the first valid WRITE burst found.
3 Find all valid Strobe positive pulse in the said burst. A valid Strobe positive pulse starts at V_{ref} crossing at valid Strobe rising edge (See notes on threshold) and end at V_{ref} crossing at following valid Strobe falling edge (See notes on threshold).
4 For valid Strobe positive pulse #1, zoom on the pulse so that it appears on oscilloscope main screen and perform V_{TOP} measurement. Take result from V_{TOP} measurement as $V_{IH(DC)}$ value.
5 Continue previous step with the rest of found valid Strobe positive pulse in the said burst.
6 Determine the worst result from the set of $V_{IH(DC)}$ measured.

$V_{IH(DC)}$ Test for Address, Control - Test Method of Implementation

$V_{IH(DC)}$ - Minimum DC Input Logic HIGH for Address, Control.

The purpose of this test is to verify that the mode of histogram of the high level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{IH(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: No

Signal(s) of Interest:

- Address Signals OR
- Control Signals OR
- Clock Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any of the signal of interest defined above.

Test Definition Notes from the Specification

Table 37 Input DC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IH(DC)}$	DC input logic HIGH	V_{REF} + 0.125	V_{DDQ} + 0.3	V	-

Table 38 Input DC Logic Level (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{IH(DC)}$	DC input logic HIGH	V_{REF} + 0.125	V_{DDQ} + 0.3	V	-

Test References

See Table 19 - Input DC Logic Level, in the *JEDEC Standard JESD79-2E* and Table 19 - Input DC Logic Level in the *JESD208*.

PASS Condition

The mode value for the high level voltage shall be greater than or equal to the minimum $V_{IH(DC)}$ value.

Measurement Algorithm

1 Sample/acquire signal data.
2 Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at a valid rising edge and ends at V_{REF} crossing at the following valid falling edge (See notes on threshold).
3 Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement results as $V_{IH(DC)}$ value.
4 Continue the previous step with another 9 valid positive pulses that were found in the burst.
5 Determine the worst result from the set of $V_{IH(DC)}$ measured.

$V_{IL(AC)}$ Test for DQ, DM - Test Method of Implementation

$V_{IL(AC)}$ - Minimum AC Input Logic Low for DQ, DM.

The purpose of this test is to verify that voltage level of test signal at tDS (DM and DQ input setup time in JEDEC specification) before DQS midpoint is lower than the conformance maximum limits of the $V_{IL(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

The value of V_{PEAK} which directly affects the conformance upper limit is set to 0.5V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{PEAK}.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

The value of V_{SSQ} which directly affect the conformance upper limit is set to 0V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of V_{SSQ}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Mask Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - Data Strobe Signals

Test Definition Notes from the Specification

Table 39 Input AC Logic Level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units	Notes
		Min	Max	Min	Max		
$V_{IL(AC)}$	AC input logic LOW	V_{SSQ}-V_{PEAK}	V_{REF} - 0.250	V_{SSQ}-V_{PEAK}	V_{REF} - 0.200	V	1

Table 40 Input AC Logic Level (DDR2-1066)

Symbol	Parameter	DDR2-1066		Units	Notes
		Min	Max		
$V_{IL(AC)}$	AC input logic LOW	-	V_{REF} - 0.200	V	-

Test References

See Table 20 - Input AC Logic Level, in the *JEDEC Standard JESD79-2E* and Table 20 - Input AC Logic Level in the *JESD208*.

PASS Condition

The voltage level at tDS (DM and DQ input setup time in JEDEC specification) before DQS midpoint for the low level voltage shall be less than or equal to the maximum $V_{IL(AC)}$ value.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid falling DQ crossings that cross $V_{IL(AC)}$ in the burst.
4. For all DQ crossings found, locate all the following DQS crossings that cross Midpoint. (0V for differential DQS and V_{REF} for single ended DQS)
5. Calculate the time where the test result is taken. Calculation is expressed as $T_{TESTRESULT} = T_{DQS\ MIDPOINT}$ - tDS.
   (tDS - DM and DQ input setup time in JEDEC specification which is due to speed grade.)
6. Take voltage level of DQ signal at $T_{TESTRESULT}$ as the test result for $V_{IL(AC)}$.
7. Collect all $V_{IL(AC)}$.
8. Determine the worst result from the set of $V_{IL(AC)}$ measured.

$V_{IL(AC)}$ Test for DQS - Test Method of Implementation

$V_{IL(AC)}$ - Minimum AC Input Logic Low for DQS.

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window is lower than the conformance maximum limits of the $V_{IL(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

The value of V_{PEAK} which directly affects the conformance upper limit is set to 0.5V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{PEAK}.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

The value of V_{SSQ} which directly affect the conformance upper limit is set to 0V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of V_{SSQ}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 41 Input AC Logic Level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units	Notes
		Min	Max	Min	Max		
$V_{IL(AC)}$	AC input logic LOW	V_{SSQ}-V_{PEAK}	V_{REF} - 0.250	V_{SSQ}-V_{PEAK}	V_{REF} - 0.200	V	1

Table 42 Input AC Logic Level (DDR2-1066)

Symbol	Parameter	DDR2-1066		Units	Notes
		Min	Max		
$V_{IL(AC)}$	AC input logic LOW	-	V_{REF} - 0.200	V	-

Test References

See Table 20 - Input AC Logic Level, in the *JEDEC Standard JESD79-2E* and Table 20 - Input AC Logic Level in the *JESD208*.

PASS Condition

The low level voltage of DQS shall be less than or equal to the maximum $V_{IL(AC)}$ value.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation)
2. Take the first valid WRITE burst found.
3. Find all valid Strobe negative pulse in the said burst. A valid Strobe negative pulse starts at V_{ref} crossing at valid Strobe falling edge (See notes on threshold) and end at V_{ref} crossing at following valid Strobe rising edge (See notes on threshold).
4. For valid Strobe negative pulse #1, zoom on the pulse so that it appears on oscilloscope main screen and perform V_{BASE} measurement. Take result from V_{BASE} measurement as $V_{IL(AC)}$ value.
5. Continue previous step with the rest of found valid Strobe negative pulse in the said burst.
6. Determine the worst result from the set of $V_{IL(AC)}$ measured.

$V_{IL(AC)}$ Test for Address, Control - Test Method of Implementation

$V_{IL(AC)}$ - Minimum AC Input Logic Low Address, Control.

The purpose of this test is to verify that the mode low level voltage value of the histogram for the test signal is lower than the conformance maximum limits of the $V_{IL(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

The value of V_{PEAK} which directly affects the conformance upper limit is set to 0.5V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{PEAK}.

The value of V_{DDQ} which directly affects the conformance upper limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

The value of V_{SSQ} which directly affect the conformance upper limit is set to 0V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of V_{SSQ}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: No

Signal(s) of Interest:

- Address Signal OR
- Control Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 43 Input AC Logic Level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units	Notes
		Min	Max	Min	Max		
$V_{IL(AC)}$	AC input logic LOW	V_{SSQ}-V_{PEAK}	V_{REF} - 0.250	V_{SSQ}-V_{PEAK}	V_{REF} - 0.200	V	1

Table 44 Input AC Logic Level (DDR2-1066)

Symbol	Parameter	DDR2-1066		Units	Notes
		Min	Max		
$V_{IL(AC)}$	AC input logic LOW	-	V_{REF} - 0.200	V	-

Test References

See Table 20 - Input AC Logic Level, in the *JEDEC Standard JESD79-2E* and Table 20 - Input AC Logic Level in the *JESD208*.

PASS Condition

The mode value for the histogram for the low level voltage shall be less than or equal to the maximum $V_{IL(AC)}$ value.

Measurement Algorithm

1 Sample/acquire signal data.
2 Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at a valid falling edge and ends at V_{REF} crossing at the following rising valid edge (See notes on threshold).
3 Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement results as $V_{IL(AC)}$ value.
4 Continue the previous step with another nine valid negative pulses.
5 Determine the worst result from the set of $V_{IL(AC)}$ measured.

$V_{IL(DC)}$ Test for DQ, DM - Test Method of Implementation

$V_{IL(DC)}$ - Maximum DC Input Logic Low for DQ, DM.

The purpose of this test is to verify that the max of histogram of the low level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{IL(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals) OR;
- Data Mask Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - Data Strobe Signals

Test Definition Notes from the Specification

Table 45 Input DC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IL(DC)}$	DC input logic LOW	-0.3	V_{REF} - 0.125	V	-

Table 46 Input DC Logic Level (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{IL(DC)}$	DC input logic LOW	-0.3	V_{REF} - 0.125	V	-

Test References

See Table 19 - Input DC Logic Level, in the *JEDEC Standard JESD79-2E* and Table 19 - Input DC Logic Level in the *JESD208*.

PASS Condition

The maximum value of test signal from tDS before DQS midpoint to tDH after DQS midpoint for the low level voltage shall be less than or equal to the maximum $V_{IL(DC)}$ value.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IL(AC)}$ in the burst.
4 For all DQ crossings found, locate all the following DQS crossings that cross midpoint. (0V for differential DQS and V_{REF} for single ended DQS)
5 Setup the histogram function settings where the X region is:
   - Ax: X-time position where tDS (DM and DQ input setup time in JEDEC specification) before DQS crossing midpoint.
   - Bx: X-time position where tDH (DM and DQ input hold time in JEDEC specification) after DQS crossing midpoint.
   - Ay: Top of the displaying window just to make sure it covers the maximum level of the respective signal.
   - By: Y- position at V_{REF} voltage level.
6 Take histogram 'Max' value as the test result for $V_{IL(DC)}$.
7 Collect all $V_{IL(DC)}$.
8 Determine the worst result from the set of $V_{IL(DC)}$ measured.

$V_{IL(DC)}$ Test for DQS - Test Method of Implementation

$V_{IL(DC)}$ - Maximum DC Input Logic Low for DQS.

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window is lower than the conformance maximum limits of the $V_{IL(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 47 Input DC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IL(DC)}$	DC input logic LOW	-0.3	V_{REF} - 0.125	V	-

Table 48 Input DC Logic Level (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{IL(DC)}$	DC input logic LOW	-0.3	V_{REF} - 0.125	V	-

Test References

See Table 19 - Input DC Logic Level, in the *JEDEC Standard JESD79-2E* and Table 19 - Input DC Logic Level in the *JESD208*.

PASS Condition

The low level voltage of DQS shall be less than or equal to the maximum $V_{IL(DC)}$ value.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation).
2 Take the first valid WRITE burst found.
3 Find all valid Strobe negative pulse in the said burst. A valid Strobe negative pulse starts at V_{ref} crossing at valid Strobe falling edge (See notes on threshold) and end at V_{ref} crossing at following valid Strobe rising edge (See notes on threshold).
4 For valid Strobe negative pulse #1, zoom on the pulse so that it appears on oscilloscope main screen and perform V_{BASE} measurement. Take result from V_{BASE} measurement as $V_{IL(DC)}$ value.
5 Continue previous step with the rest of found valid Strobe negative pulse in the burst.
6 Determine the worst result from the set of $V_{IL(DC)}$ measured.

$V_{IL(DC)}$ Test for Address, Control - Test Method of Implementation

$V_{IL(DC)}$ - Maximum DC Input Logic Low for Address, Control.

The purpose of this test is to verify that the mode of histogram of the low level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{IL(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.9V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{REF}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: No

Signal(s) of Interest:

- Address Signal OR
- Control Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 49 Input DC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IL(DC)}$	DC input logic LOW	-0.3	V_{REF} - 0.125	V	-

Table 50 Input DC Logic Level (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{IL(DC)}$	DC input logic LOW	-0.3	V_{REF} - 0.125	V	-

Test References

See Table 19 - Input DC Logic Level, in the *JEDEC Standard JESD79-2E* and Table 19 - Input DC Logic Level in the *JESD208*.

PASS Condition

The mode value for the histogram for the low level voltage shall be less than or equal to the maximum $V_{IL(DC)}$ value.

Measurement Algorithm

1 Sample/acquire signal data.
2 Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at valid falling edge and end at V_{REF} crossing at the following rising valid edge (See notes on threshold).
3 Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement results as $V_{IL(DC)}$ value.
4 Continue the previous step with another nine valid negative pulses.
5 Determine the worst result from the set of $V_{IL(DC)}$ measured.

$Slew_R$ Test for DQ, DM, DQS - Test Method of Implementation

$Slew_R$ - Input Signal Minimum Slew Rate (Rising) for DQ, DM, DQS.

The purpose of this test is to verify that the rising slew rate value of the test signal is greater than or equal to the conformance limit of the input SLEW value specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal) OR
- Data Mask Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - Data Strobe Signals if PUT is DQ,DM. Else Data Signals if PUT is DQS

Test Definition Notes from the Specification

Table 51 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Figure 73 — AC input test signal waveform JEDEC Standard No. 79-2E

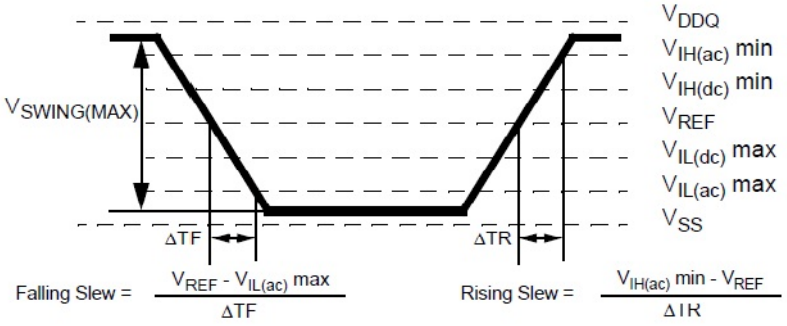
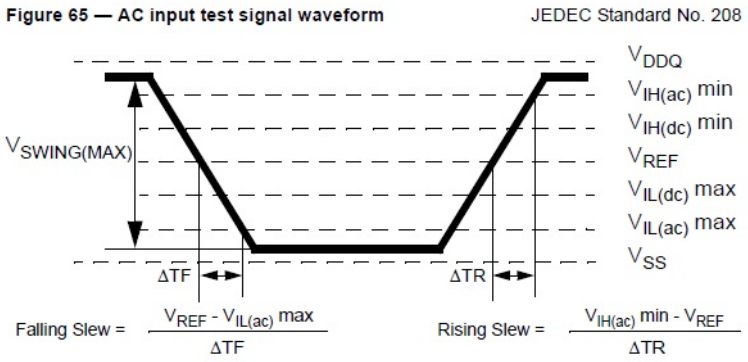


Table 52 AC Input Test Conditions (DDR2-1066)

Symbol	Condition	Value	Units	Notes
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3



Test References

See Table 21 - AC Input Test Conditions in the *JEDEC Standard JESD79-2E* and Table 21 - AC Input Test Conditions in the *JESD208*.

PASS Condition

The calculated Rising Slew value of the test signal should be greater than or equal to the SLEW value.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation.)

2 Take the first valid WRITE burst found.

3 Find all valid DQ/DM/DQS rising edges in the burst. A valid rising edge starts at $V_{IL(AC)}$ crossing and ends at the following $V_{IH(AC)}$ crossing.

4 For all valid rising edges, find the transition time, delta TR, which is the time starting at V_{REF} crossing and ending at the following $V_{IH(AC)}$ crossing.

5 Calculate the Rising Slew:

$$\mathrm{RisingSlew} = \frac{V_{IH(AC)}\mathrm{min} - V_{REF}}{\Delta TR}$$

6 Determine the worst result from the set of $Slew_R$ measured.

$Slew_R$ Test for Address, Control, Clock - Test Method of Implementation

$Slew_R$ - Input Signal Minimum Slew Rate (Rising) for Address, Control, Clock.

The purpose of this test is to verify that the rising slew rate value of the test signal is greater than or equal to the conformance limit of the input SLEW value specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: No

Signal(s) of Interest:

- Address Signal OR
- Control Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 53 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Figure 73 — AC input test signal waveform JEDEC Standard No. 79-2E

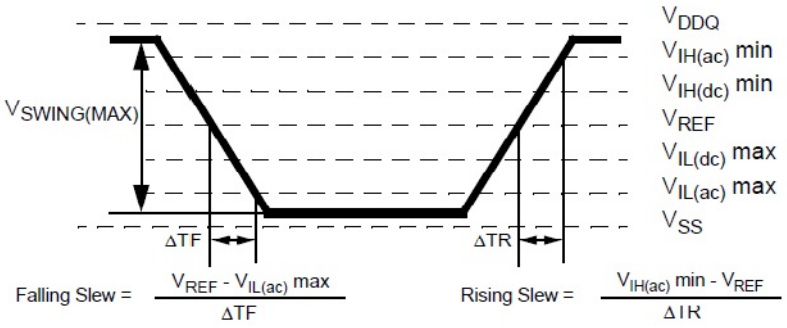
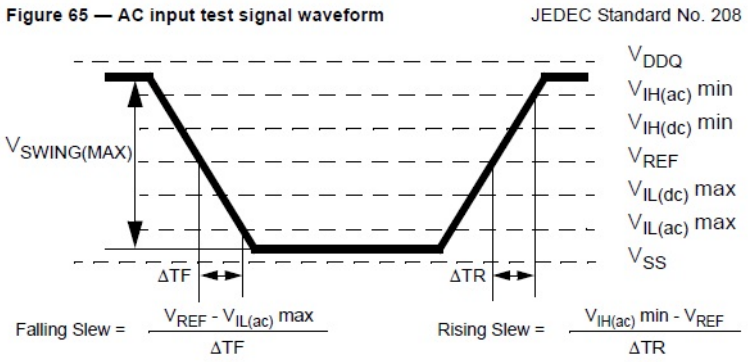


Table 54 AC Input Test Conditions (DDR2-1066)

Symbol	Condition	Value	Units	Notes
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3



Test References

See Table 21 - AC Input Test Conditions in the *JEDEC Standard JESD79-2E* and Table 21 - AC Input Test Conditions in the *JESD208*.

PASS Condition

The calculated Rising Slew value of the test signal should be greater than or equal to the SLEW value.

Measurement Algorithm

1 Acquire the signal.

2 Find all valid rising edges in the whole acquisition. A valid rising edge starts at $V_{IL(AC)}$ crossing and ends at the following $V_{IH(AC)}$ crossing.

3 For all valid rising edges, find the transition time, delta TR, which is the time starting at V_{REF} crossing and ending at the following $V_{IH(AC)}$ crossing.

4 Calculate the Rising Slew:

$$\mathrm{RisingSlew} = \frac{V_{IH(AC)}\mathrm{min} - V_{REF}}{\Delta TR}$$

5 Determine the worst result from the set of $Slew_R$ measured.

$Slew_F$ Test for DQ, DM, DQS - Test Method of Implementation

$Slew_F$ - Input Signal Minimum Slew Rate (Falling) for DQ, DM, DQS.

The purpose of this test is to verify that the falling slew rate value of the test signal is greater than or equal to the conformance limit of the input SLEW value specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal) OR
- Data Mask Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - Data Strobe Signals if PUT is DQ,DM. Else Data Signals if PUT is DQS

Test Definition Notes from the Specification

Table 55 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Figure 73 — AC input test signal waveform JEDEC Standard No. 79-2E

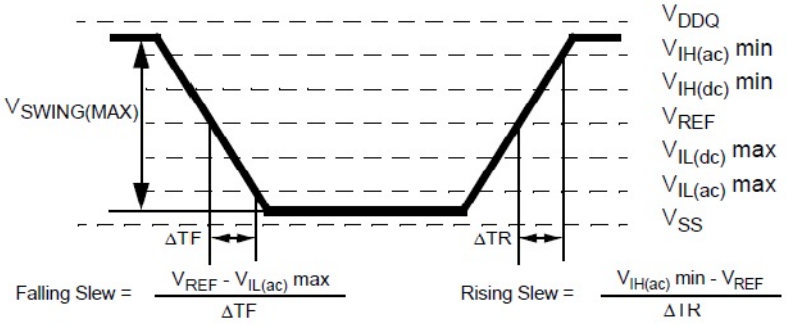
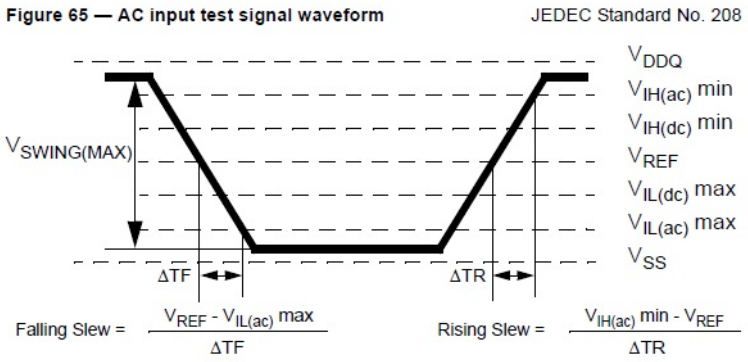


Table 56 AC Input Test Conditions (DDR2-1066)

Symbol	Condition	Value	Units	Notes
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3



Test References

See Table 21 - AC Input Test Conditions in the *JEDEC Standard JESD79-2E* and Table 21 - AC Input Test Conditions in the *JESD208*.

PASS Condition

The calculated Falling Slew value for the test signal should be greater than or equal to the SLEW value.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation.).

2 Take the first valid WRITE burst found.

3 Find all valid DQ/DM/DQS falling edges in the burst. A valid falling edge starts at $V_{IH(AC)}$ crossing and ends at the following $V_{IL(AC)}$ crossing.

4 For all valid falling edges, find the transition time, delta TR, which is time starting at V_{REF} crossing and ending at the following $V_{IL(AC)}$ crossing.

5 Calculate the Falling Slew:

$$\text{FallingSlew} = \frac{V_{REF} - V_{IL(AC)}\text{max}}{\Delta TF}$$

6 Determine the worst result from the set of $Slew_F$ measured.

$Slew_F$ Test for Address, Control, Clock - Test Method of Implementation

$Slew_F$ - Input Signal Minimum Slew Rate (Falling) for Address, Control, Clock.

The purpose of this test is to verify that the falling slew rate value of the test signal is greater than or equal to the conformance limit of the input SLEW value specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: No

Signal(s) of Interest:

- Address Signal OR
- Control Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 57 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Figure 73 — AC input test signal waveform JEDEC Standard No. 79-2E

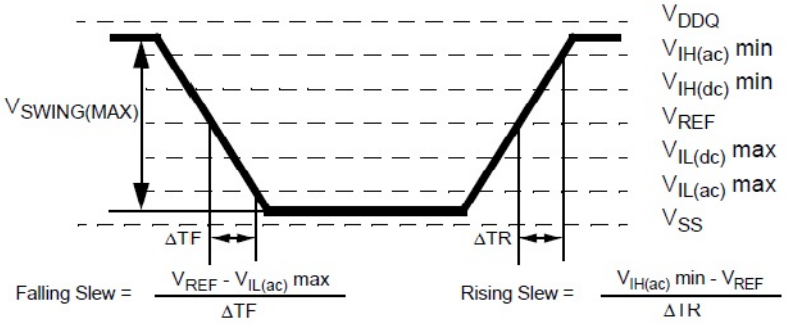
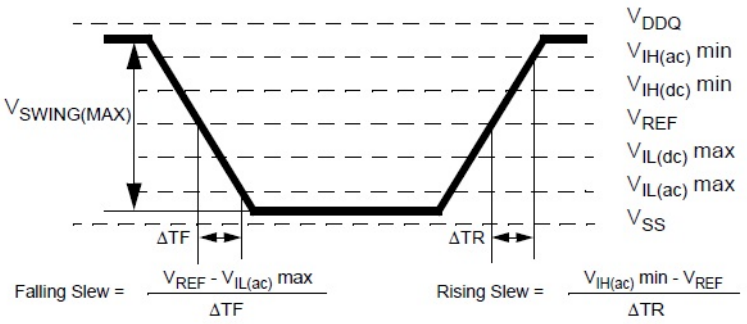


Table 58 AC Input Test Conditions (DDR2-1066)

Symbol	Condition	Value	Units	Notes
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Figure 65 — AC input test signal waveform JEDEC Standard No. 208



Test References

See Table 21 - AC Input Test Conditions in the *JEDEC Standard JESD79-2E* and Table 21 - AC Input Test Conditions in the *JESD208*.

PASS Condition

The calculated Falling Slew value for the test signal should be greater than or equal to the SLEW value.

Measurement Algorithm

1 Acquire the signal.

2 Find all valid falling edges in the whole acquisition. A valid falling edge starts at $V_{IH(AC)}$ crossing and ends at the following $V_{IL(AC)}$ crossing.

3 For all valid rising edges, find the transition time, delta TR, which is the time starting at V_{REF} crossing and ending at the following $V_{IL(AC)}$ crossing.

4 Calculate the Falling Slew:

$$\mathrm{FallingSlew} = \frac{V_{REF} - V_{IL(AC)}\mathrm{max}}{\Delta TF}$$

5 Determine the worst result from the set of $Slew_F$ measured.

SRQseR (40ohm) - Test Method of Implementation

AC Output Parameter Tests can be divided into eight sub tests:

- SRQseR(40ohm) test
- SRQseF(40ohm) test
- SRQseR(60ohm) test
- SRQseF(60ohm) test
- $V_{OH(AC)}$ test
- $V_{OH(DC)}$ test
- $V_{OL(AC)}$ test
- $V_{OL(DC)}$ test

SRQseR (40ohm) - Single-ended Output Rising Slew Rate (40ohms).

The purpose of this test is to verify that the single-ended rising slew rate value of the test signal must be within the conformance limit of the SRQse value as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin

Test Definition Notes from the Specification

Table 59 LPDDR2 Output Slew Rate (single-ended)

Parameter	Symbol	LPDDR2-1066 to LPDDR2-200		Units
		Min	Max	
Single-ended Output Slew Rate (RON = 40ohms +/- 30%)	SRQse	1.5	3.5	V/ns

Test References

See Table 85 - Output Slew Rate (single-ended) in the *JESD209-2B*.

PASS Condition

The worst measured SRQseR shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid signal rising edges in this burst. A valid signal rising edge starts at the $V_{OL(AC)}$ crossing and ends at the following $V_{OH(AC)}$ crossing.
4 For all valid signal rising edges, find the transition time, T_R, which is the time that starts at the $V_{OL(AC)}$ crossing and ends at the following $V_{OH(AC)}$ crossing. Then calculate SRQseR = $[V_{OH(AC)} - V_{OL(AC)}]/T_R$.
5 Determine the worst result from the set of SRQseR measured.

SRQseF (40ohm) - Test Method of Implementation

SRQseF (40ohm) - Single-ended Output Falling Slew Rate (40ohms).

The purpose of this test is to verify that the single-ended falling slew rate value of the test signal must be within the conformance limit of the SRQse value as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin

Test Definition Notes from the Specification

Table 60 LPDDR2 Output Slew Rate (single-ended)

Parameter	Symbol	LPDDR2-1066 to LPDDR2-200		Units
		Min	Max	
Single-ended Output Slew Rate (RON = 40ohms +/- 30%)	SRQse	1.5	3.5	V/ns

Test References

See Table 85- Output Slew Rate (single-ended) in the *JESD209-2B*.

PASS Condition

The worst measured SRQseF shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid signal falling edges in this burst. A valid signal falling edge starts at the $V_{OH(AC)}$ crossing and ends at the following $V_{OL(AC)}$ crossing.

4 For all valid signal falling edges, find the transition time, T_R, which is the time that starts at the $V_{OH(AC)}$ crossing and ends at the following $V_{OL(AC)}$ crossing. Then calculate SRQseF = $[V_{OH(AC)} - V_{OL(AC)}]/T_R$.

5 Determine the worst result from the set of SRQseF measured.

SRQseR (60ohm) - Test Method of Implementation

SRQseR (60ohm) - Single-ended Output Rising Slew Rate (60ohms).

The purpose of this test is to verify that the single-ended rising slew rate value of the test signal must be within the conformance limit of the SRQse value as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin

Test Definition Notes from the Specification

Table 61 LPDDR2 Output Slew Rate (single-ended)

Parameter	Symbol	LPDDR2-1066 to LPDDR2-200		Units
		Min	Max	
Single-ended Output Slew Rate (RON = 60ohms +/- 30%)	SRQse	1.0	2.5	V/ns

Test References

See Table 85- Output Slew Rate (single-ended) in the *JESD209-2B*.

PASS Condition

The worst measured SRQseR shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid signal rising edges in this burst. A valid signal rising edge starts at the $V_{OL(AC)}$ crossing and ends at the following $V_{OH(AC)}$ crossing.

4 For all valid signal rising edges, find the transition time, T_R, which is the time that starts at the $V_{OL(AC)}$ crossing and ends at the following $V_{OH(AC)}$ crossing. Then calculate $SRQseR = [V_{OH(AC)} - V_{OL(AC)}]/T_R$.

5 Determine the worst result from the set of SRQseR measured.

SRQseF (60ohm) - Test Method of Implementation

SRQseF (60ohm) - Single-ended Output Falling Slew Rate (60ohms).

The purpose of this test is to verify that the single-ended falling slew rate value of the test signal must be within the conformance limit of the SRQse value as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin

Test Definition Notes from the Specification

Table 62 LPDDR2 Output Slew Rate (single-ended)

Parameter	Symbol	LPDDR2-1066 to LPDDR2-200		Units
		Min	Max	
Single-ended Output Slew Rate (RON = 60ohms +/- 30%)	SRQse	1.0	2.5	V/ns

Test References

See Table 85- Output Slew Rate (single-ended) in the *JESD209-2B*.

PASS Condition

The worst measured SRQseF shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid signal falling edges in this burst. A valid signal falling edge starts at the $V_{OH(AC)}$ crossing and ends at the following $V_{OL(AC)}$ crossing.

4 For all valid signal falling edges, find the transition time, T_R, which is the time that starts at the $V_{OH(AC)}$ crossing and ends at the following $V_{OL(AC)}$ crossing. Then calculate SRQseF = $[V_{OH(AC)} - V_{OL(AC)}]/T_R$.

5 Determine the worst result from the set of SRQseF measured.

$V_{OH(AC)}$ - Test Method of Implementation

$V_{OH(AC)}$ - Single-ended AC Output Logic High Voltage.

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{OH(AC)}$ value as specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance limit) is set to 0.6V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin

Test Definition Notes from the Specification

Table 63 LPDDR2 Single-ended AC and DC Output Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200	Units	Notes
$V_{OH(AC)}$	AC output high measurement level (for output slew rate)	V_{REFDQ} + 0.12	V	

Test References

See Table 82 - Single-ended AC and DC Output Levels in the *JESD209-2B*.

PASS Condition

The worst measured $V_{OH(AC)}$ shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid signal positive pulses in this burst. A valid signal positive pulse starts at the V_{REF} crossing on a valid signal rising edge and ends at the V_{REF} crossing on the following valid signal falling edge.

4 For the first valid positive pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the V_{TOP} measurement. Take the V_{TOP} measurement result as the $V_{OH(AC)}$ value.

5 Continue the previous step for the rest of the valid signal positive pulses that were found in the burst.

6 Determine the worst result from the set of $V_{OH(AC)}$ measured.

$V_{OH(DC)}$ - Test Method of Implementation

$V_{OH(DC)}$ - Single-ended DC Output Logic High Voltage.

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{OH(DC)}$ value as specified in the JEDEC specification.

The value of V_{DDQ} (which directly affects the conformance limit) is set to 1.2V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DDQ}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin

Test Definition Notes from the Specification

Table 64 LPDDR2 Single-ended AC and DC Output Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200	Units	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.9 x V_{DDQ}	V	1

Test References

See Table 82 - Single-ended AC and DC Output Levels in the *JESD209-2B*.

PASS Condition

The worst measured $V_{OH(DC)}$ shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid signal positive pulses in this burst. A valid signal positive pulse starts at the V_{REF} crossing on a valid signal rising edge and ends at the V_{REF} crossing on the following valid signal falling edge.
4 For the first valid positive pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the V_{TOP} measurement. Take the V_{TOP} measurement result as the $V_{OH(DC)}$ value.
5 Continue the previous step for the rest of the valid signal positive pulses that were found in the burst.
6 Determine the worst result from the set of $V_{OH(DC)}$ measured.

$V_{OL(AC)}$ - Test Method of Implementation

$V_{OL(AC)}$ - Single-ended AC Output Logic Low Voltage.

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{OL(AC)}$ value as specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance limit) is set to 0.6V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin

Test Definition Notes from the Specification

Table 65 LPDDR2 Single-ended AC and DC Output Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200	Units	Notes
$V_{OL(AC)}$	AC output low measurement level (for output slew rate)	V_{REFDQ} - 0.12	V	

Test References

See Table 82 - Output Slew Rate (single-ended) in the *JESD209-2B*.

PASS Condition

The worst measured $V_{OL(AC)}$ shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid signal negative pulses in this burst. A valid signal negative pulse starts at the V_{REF} crossing on a valid signal falling edge and ends at the V_{REF} crossing on the following valid signal rising edge.

4 For the first valid negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the V_{BASE} measurement. Take the V_{BASE} measurement result as the $V_{OL(AC)}$ value.

5 Continue the previous step for the rest of the valid signal negative pulses that were found in the burst.

6 Determine the worst result from the set of $V_{OL(AC)}$ measured.

$V_{OL(DC)}$ - Test Method of Implementation

$V_{OH(DC)}$ - Single-ended DC Output Logic High Voltage.

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{OL(DC)}$ value as specified in the JEDEC specification.

The value of V_{DDQ} (which directly affects the conformance limit) is set to 1.2V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DDQ}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin

Test Definition Notes from the Specification

Table 66 LPDDR2 Single-ended AC and DC Output Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200	Units	Notes
$V_{OH(DC)}$	DC output low measurement level (for IV curve linearity)	0.1 x V_{DDQ}	V	2

Test References

See Table 82 - Output Slew Rate (single-ended) in the *JESD209-2B*.

PASS Condition

The worst measured $V_{OL(DC)}$ shall be within the specification limit.

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid signal negative pulses in this burst. A valid signal negative pulse starts at the V_{REF} crossing on a valid signal falling edge and ends at the V_{REF} crossing on the following valid signal rising edge.
4. For the first valid negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the V_{BASE} measurement. Take the V_{BASE} measurement result as the $V_{OL(DC)}$ value.
5. Continue the previous step for the rest of the valid signal negative pulses that were found in the burst.
6. Determine the worst result from the set of $V_{OL(DC)}$ measured.

5 Single-Ended Signals V_{IH}/V_{IL} (Address, Control) Tests

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals V_{IH}/V_{IL} (Address, Control) tests using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

Probing for Single-Ended Signals V_{IH}/V_{IL} (Address, Control) Tests

When performing the Single-Ended Signals V_{IH}/V_{IL} (Address, Control) tests, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections. The connection for the Single-Ended Signals V_{IH}/V_{IL} (Address, Control) tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance application for the exact number of probe connections.

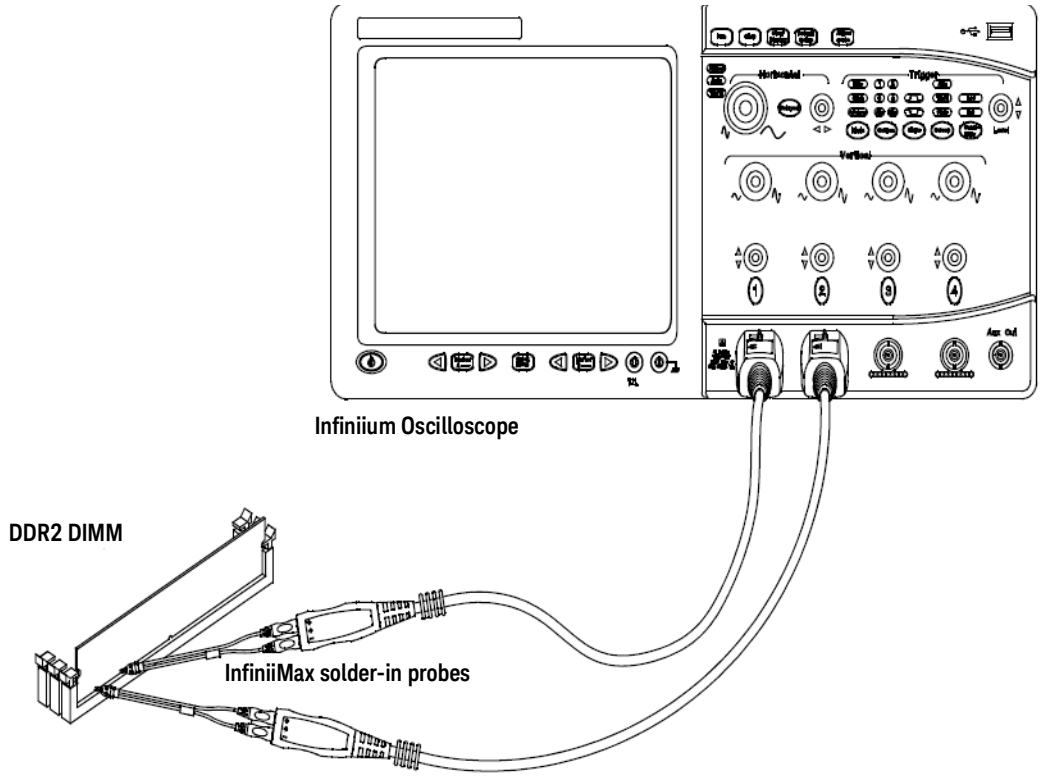


Figure 10 Probing for Single-Ended Signals V_{IH}/V_{IL} (Address, Control) Tests with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channels shown in Figure 10 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in "Starting the DDR2(+LP) Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the LPDDR2 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the LPDDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the LPDDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2(+LP) Test application, click the Set Up tab.

6 Select the Speed Grade options. For the Single-Ended Signals V_{IH}/V_{IL} (Address, Control) tests, you can select any LPDDR2 speed grade within the selection. To see the LPDDR2 Speed Grades, check the Low Power box.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

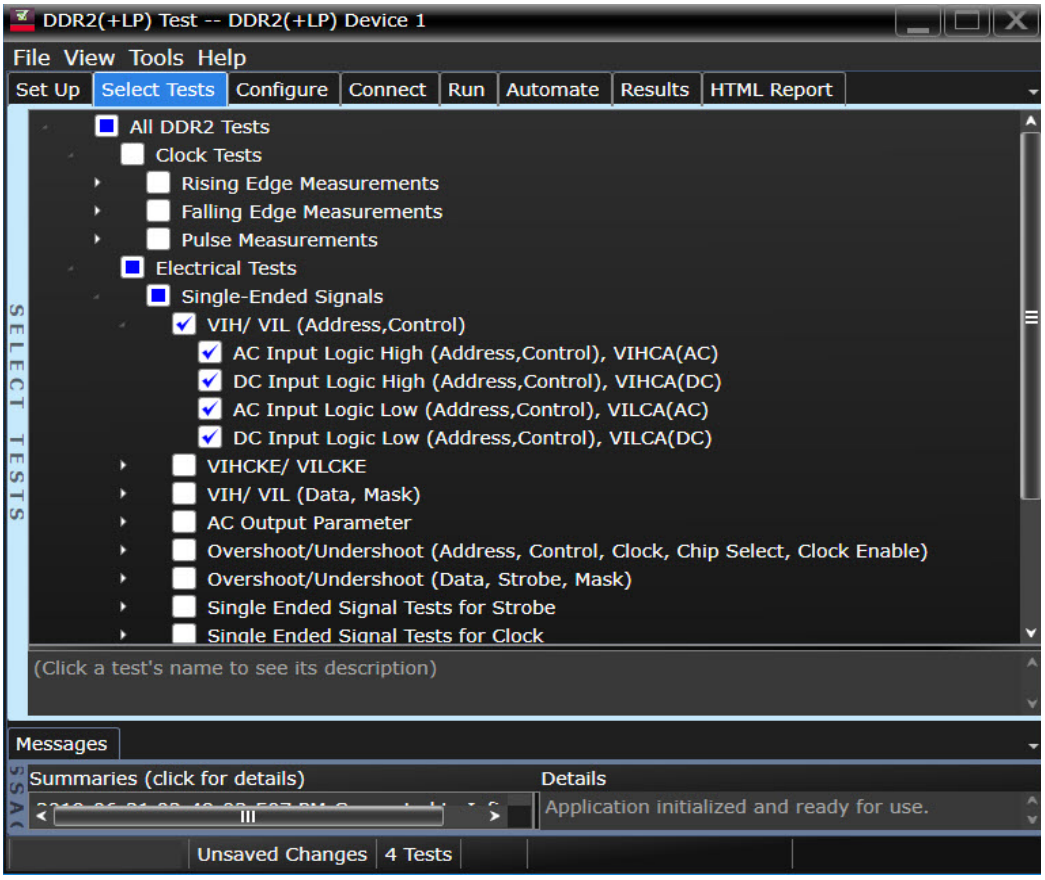


Figure 11 Selecting Single-Ended Signals V_{IH}/V_{IL} (Address, Control) Tests

9 Follow the DDR2(+LP) Test application's task flow to set up the configuration options, run the tests and view the tests results.

$V_{IHCA(AC)}$ - Test Method of Implementation

V_{IH} Input Logic HIGH (Address, Control) test can be divided into two subtests:

- $V_{IHCA(AC)}$ test
- $V_{IHCA(DC)}$ test

$V_{IHCA(AC)}$ - AC Input Logic HIGH (Address, Control).

The purpose of this test is to verify that the histogram mode high level voltage value of the test signal within a valid sampling window is greater than the conformance lower limits of the $V_{IHCA(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance lower limit) is set to 0.6V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Command/Address Signals
- Chip Select Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above.

Test Definition Notes from the Specification

Table 67 Single-ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{IHCA(AC)}$	AC input logic HIGH	V_{REF} + 0.220	Note 2	V_{REF} + 0.300	Note 2	V	1, 2

Test References

See Table 74 - Single-ended AC and DC Input Levels for CA and CS_n Inputs in the *JESD209-2B*.

PASS Condition

The mode value for the high level voltage must be greater than or equal to the minimum $V_{IHCA(AC)}$ value.

Measurement Algorithm

1 Sample/acquire signal data.
2 Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at valid rising edge and end at V_{REF} crossing at the following valid falling edge (See notes on threshold).
3 Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement results as $V_{IHCA(AC)}$ value.
4 Continue the previous step with another nine valid positive pulses.
5 Determine the worst result from the set of $V_{IHCA(AC)}$ measured.

$V_{IHCA(DC)}$ - Test Method of Implementation

$V_{IHCA(DC)}$ - DC Input Logic HIGH (Address, Control).

The purpose of this test is to verify that the histogram mode high level voltage value of the test signal within a valid sampling window is greater than the conformance lower limits of the $V_{IHCA(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance lower limit) is set to 0.6V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of V_{DDCA} (which directly affects the conformance lower limit) is set to 1.2V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DDCA}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Command/Address Signals
- Chip Select Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above.

Test Definition Notes from the Specification

Table 68 Single-ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{IHCA(DC)}$	DC input logic HIGH	V_{REF} + 0.130	V_{DDCA}	V_{REF} + 0.200	V_{DDCA}	V	1

Test References

See Table 74 - Single-ended AC and DC Input Levels for CA and CS_n Inputs in the *JESD209-2B*.

PASS Condition

The mode value for the high level voltage must be greater than or equal to the minimum $V_{IHCA(DC)}$ value.

Measurement Algorithm

1 Sample/acquire signal data.
2 Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at valid rising edge and end at V_{REF} crossing at the following valid falling edge (See notes on threshold).
3 Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement results as $V_{IHCA(DC)}$ value.
4 Continue the previous step with another nine valid positive pulses.
5 Determine the worst result from the set of $V_{IHCA(DC)}$ measured.

$V_{ILCA(AC)}$ - Test Method of Implementation

V_{IL} Input Logic Low (Address, Control) test can be divided into two subtests:

- $V_{ILCA(AC)}$ test
- $V_{ILCA(DC)}$ test

$V_{ILCA(AC)}$ - AC Input Logic Low (Address, Control).

The purpose of this test is to verify that the histogram mode low level voltage value of the test signal within a valid sampling window is lower than the conformance lower limits of the $V_{ILCA(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance upper limit) is set to 0.6V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Command/Address Signals
- Chip Select Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above.

Test Definition Notes from the Specification

Table 69 Single-ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{ILCA(AC)}$	AC input logic LOW	Note 2	V_{REF} - 0.220	Note 2	V_{REF} - 0.300	V	1, 2

Test References

See Table 74 - Single-ended AC and DC Input Levels for CA and CS_n Inputs in the *JESD209-2B*.

PASS Condition

The mode value for the low level voltage must be less than or equal to the minimum $V_{ILCA(AC)}$ value.

Measurement Algorithm

1 Obtain sample or acquire signal data.

2 Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at valid falling edge and end at V_{REF} crossing at the following valid rising edge (See notes on threshold).

3 Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement results as $V_{ILCA(AC)}$ value.

4 Continue the previous step with another nine valid negative pulses.

5 Determine the worst result from the set of $V_{ILCA(AC)}$ measured.

$V_{ILCA(DC)}$ - Test Method of Implementation

$V_{ILCA(DC)}$ - DC Input Logic Low (Address, Control).

The purpose of this test is to verify that the histogram mode low level voltage value of the test signal within a valid sampling window is lower than the conformance lower limits of the $V_{ILCA(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance upper limit) is set to 0.6V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of V_{SSCA} (which directly affects the conformance lower limit) is set to 0V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{SSCA}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Command/Address Signals
- Chip Select Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above.

Test Definition Notes from the Specification

Table 70 Single-ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{ILCA(DC)}$	DC input logic LOW	V_{SSCA}	V_{REF} - 0.130	V_{SSCA}	V_{REF} - 0.200	V	1

Test References

See Table 74 - Single-ended AC and DC Input Levels for CA and CS_n Inputs in the *JESD209-2B*.

PASS Condition

The mode value for the histogram of the low level voltage must be less than or equal to the maximum $V_{ILCA(DC)}$ value.

Measurement Algorithm

1 Obtain sample or acquire signal data.
2 Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at valid falling edge and end at V_{REF} crossing at the following valid rising edge (See notes on threshold).
3 Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement results as $V_{ILCA(DC)}$ value.
4 Continue the previous step with another nine valid negative pulses.
5 Determine the worst result from the set of $V_{ILCA(DC)}$ measured.

6 Single-Ended Signals V_{IH}/V_{IL} (Data, Mask) Tests

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals V_{IH}/V_{IL} (Data, Mask) tests using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

Probing for Single-Ended Signals V_{IH}/V_{IL} (Data, Mask) Tests

When performing the Single-Ended Signals V_{IH}/V_{IL} (Data, Mask) tests, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections. The connection for the Single-Ended Signals V_{IH}/V_{IL} (Data, Mask) tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance application for the exact number of probe connections.

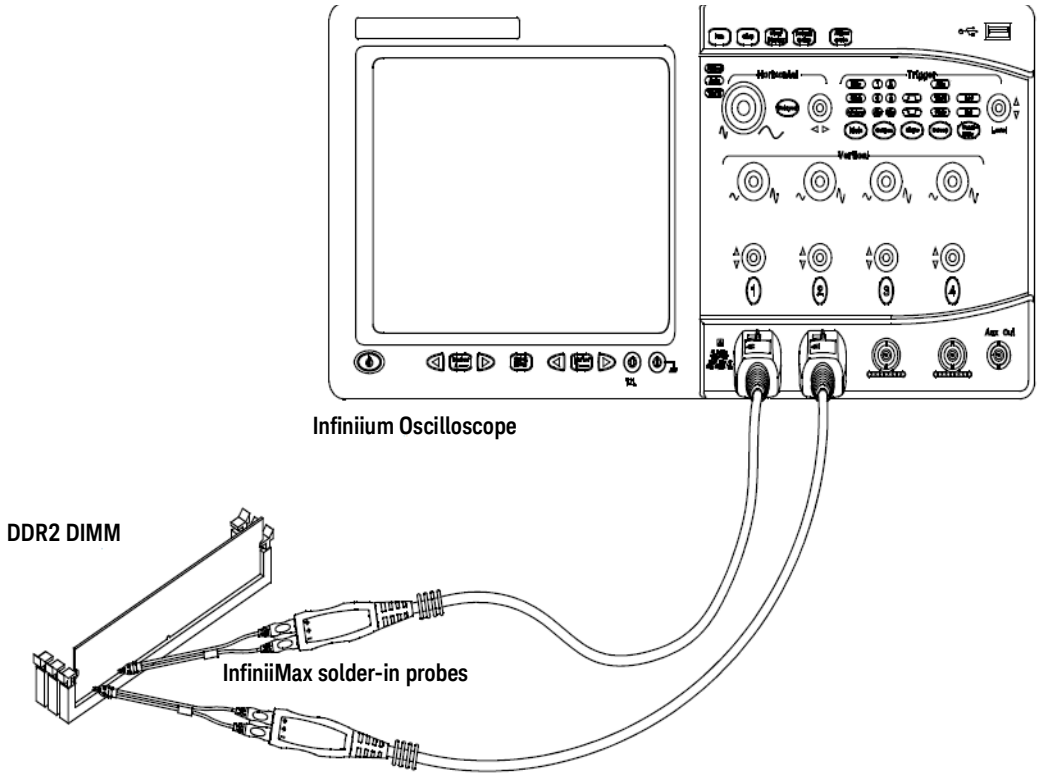


Figure 12 Probing for Single-Ended Signals V_{IH}/V_{IL} (Data Mask) Tests with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channels shown in Figure 12 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in “Starting the DDR2(+LP) Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the LPDDR2 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the LPDDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the LPDDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2(+LP) Test application, click the Set Up tab.

6 Select the Speed Grade options. For the Single-Ended Signals V_{IH}/V_{IL} (Data, Mask) tests, you can select any LPDDR2 speed grade within the selection. To see the LPDDR2 Speed Grades, check the Low Power box.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

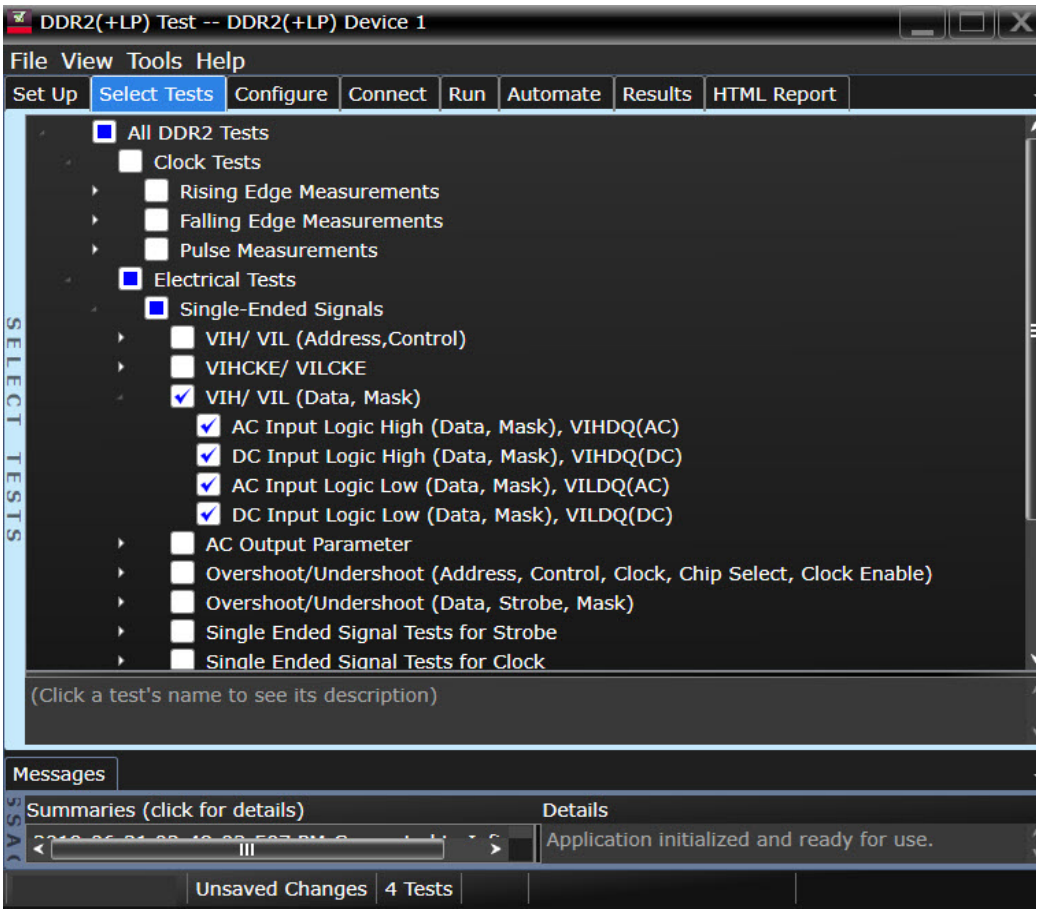


Figure 13 Selecting Single-Ended Signals V_{IH}/V_{IL} (Data, Mask) Tests

9 Follow the DDR2(+LP) Test application's task flow to set up the configuration options, run the tests and view the tests results.

$V_{IHDQ(AC)}$ - Test Method of Implementation

V_{IH} Input Logic HIGH (Data, Mask) test can be divided into two subtests:

- $V_{IHDQ(AC)}$ test
- $V_{IHDQ(DC)}$ test

$V_{IHDQ(AC)}$ - AC Input Logic HIGH (Data, Mask).

The purpose of this test is to verify that the voltage level of the test signal at tDS (DM and DQ input setup time in JEDEC specification) before the DQS midpoint is greater than the conformance lower limits of the $V_{IHDQ(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance lower limit) is set to 0.6V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals) OR
- Data Mask Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above.
- Supporting Pin - Data Strobe Signals

Test Definition Notes from the Specification

Table 71 Single-ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{IHDQ(AC)}$	AC input logic HIGH	V_{REF} + 0.220	Note 2	V_{REF} + 0.300	Note 2	V	1, 2, 5

Test References

See Table 76 - Single-ended AC and DC Input Levels for DQ and DM in the *JESD209-2B*.

PASS Condition

The voltage level at tDS (DM and DQ input setup time in JEDEC specification) before the DQS midpoint for the high level voltage shall be greater than or equal to the minimum $V_{IHDQ(AC)}$ value.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IH(AC)}$ in the burst.
4 For all DQ crossings found, locate all the following DQS crossings that cross 0V.
5 Calculate the time where the test result is taken. Calculation is expressed as:
$T_{TESTRESULT} = T_{DQS\ MIDPOINT} - tDS$.
(tDS – DM and DQ input setup time in JEDEC specification which is due to speed grade).
6 Take voltage level of DQ signal at $T_{TESTRESULT}$ as the test result for $V_{IHDQ(AC)}$.
7 Collect all $V_{IHDQ(AC)}$.
8 Determine the worst result from the set of $V_{IHDQ(AC)}$ measured.

$V_{IHDQ(DC)}$ - Test Method of Implementation

$V_{IHDQ(DC)}$ - DC Input Logic HIGH (Data, Mask).

The purpose of this test is to verify that the histogram min high level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{IHDQ(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance lower limit) is set to 0.6V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of V_{DDQ} (which directly affects the conformance lower limit) is set to 1.2V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DDQ}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals) OR
- Data Mask Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above.
- Supporting Pin - Data Strobe Signals

Test Definition Notes from the Specification

Table 72 Single-ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{IHDQ(DC)}$	DC input logic HIGH	V_{REF} + 0.130	V_{DDQ}	V_{REF} + 0.200	V_{DDQ}	V	1

Test References

See Table 76 - Single-ended AC and DC Input Levels for DQ and DM in the *JESD209-2B*.

PASS Condition

The minimum value of the test signal from tDS before the DQS midpoint to tDH after the DQS midpoint for the high level voltage shall be greater than or equal to the minimum $V_{IHDQ(DC)}$ value.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IH(AC)}$ in the burst.
4 For all DQ crossings found, locate all the following DQS crossings that cross midpoint. (0V is for differential DQS and V_{REF} is for single ended DQS.)
5 Set up histogram function settings.
   - Ax: X- time position where tDS (DM and DQ input setup time in JEDEC specification) before DQS crossing midpoint.
   - Bx: X- time position where tDH (DM and DQ input hold time in JEDEC specification) after DQS crossing midpoint.
   - Ay: Top of the displaying window just to make sure it covers the maximum level of the respective signal.
   - By: Y- position at the V_{REF} voltage level.
6 Take the 'Min' value of the histogram as the test result for $V_{IHDQ(DC)}$.
7 Collect all $V_{IHDQ(DC)}$.
8 Determine the worst result from the set of $V_{IHDQ(DC)}$ measured.

$V_{ILDQ(AC)}$ - Test Method of Implementation

V_{IL} Input Logic Low (Data, Mask) test can be divided into two subtests:

- $V_{ILDQ(AC)}$ test
- $V_{ILDQ(DC)}$ test

$V_{ILDQ(AC)}$ - AC Input Logic Low (Data, Mask).

The purpose of this test is to verify that the voltage level of the test signal at tDS (DM and DQ input setup time in JEDEC specification) before the DQS midpoint is lower than the conformance lower limits of the $V_{ILDQ(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance upper limit) is set to 0.6V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals) OR
- Data Mask Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above.
- Supporting Pin - Data Strobe Signals

Test Definition Notes from the Specification

Table 73 Single-ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{ILDQ(AC)}$	AC input logic LOW	Note 2	V_{REF} - 0.220	Note 2	V_{REF} - 0.300	V	1, 2, 5

Test References

See Table 76 - Single-ended AC and DC Input Levels for DQ and DM in the *JESD209-2B*.

PASS Condition

The voltage level at tDS (DM and DQ input setup time in JEDEC specification) before the DQS midpoint for the low level voltage shall be less than or equal to the maximum $V_{ILDQ(AC)}$ value.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid falling DQ crossings that cross $V_{IL(AC)}$ in the burst.

4 For all DQ crossings found, locate all the following DQS crossings that cross midpoint. (0V is for differential DQS and V_{REF} is for single ended DQS.).

5 Calculate the time where the test result is taken. Calculation is expressed as:
$T_{TESTRESULT} = T_{DQS\ MIDPOINT} - tDS$.
(tDS – DM and DQ input setup time in JEDEC specification which is due to speed grade).

6 Take voltage level of DQ signal at $T_{TESTRESULT}$ as the test result for $V_{ILDQ(AC)}$.

7 Collect all $V_{ILDQ(AC)}$.

8 Determine the worst result from the set of $V_{ILDQ(AC)}$ measured.

$V_{ILDQ(DC)}$ - Test Method of Implementation

$V_{ILDQ(DC)}$ - DC Input Logic Low (Data, Mask).

The purpose of this test is to verify that the histogram max low level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{ILDQ(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} (which directly affects the conformance upper limit) is set to 0.6V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of V_{SSQ} (which directly affects the conformance lower limit) is set to 0V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{SSQ}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signals) OR
- Data Mask Signals (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above.
- Supporting Pin - Data Strobe Signals

Test Definition Notes from the Specification

Table 74 Single-ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{ILDQ(DC)}$	DC input logic LOW	V_{SSQ}	V_{REF} - 0.130	V_{SSQ}	V_{REF} - 0.200	V	1

Test References

See Table 76 - Single-ended AC and DC Input Levels for DQ and DM in the *JESD209-2B*.

PASS Condition

The maximum value of the test signal from tDS before the DQS midpoint to tDH after the DQS midpoint for the low level voltage shall be less than or equal to the maximum $V_{ILDQ(DC)}$ value.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IL(AC)}$ in the burst.
4 For all DQ crossings found, locate all the following DQS crossings that cross midpoint. (0V is for differential DQS and V_{REF} is for single ended DQS.)
5 Set up histogram function settings.
   - Ax: X- time position where tDS (DM and DQ input setup time in JEDEC specification) before DQS crossing midpoint.
   - Bx: X- time position where tDH (DM and DQ input hold time in JEDEC specification) after DQS crossing midpoint.
   - Ay: Top of the displaying window just to make sure it covers the maximum level of the respective signal.
   - By: Y- position at the V_{REF} voltage level.
6 Take the 'Max' value of the histogram as the test result for $V_{ILDQ(DC)}$.
7 Collect all $V_{ILDQ(DC)}$.
8 Determine the worst result from the set of $V_{ILDQ(DC)}$ measured.

7 Single-Ended Signals AC Parameters Tests for Strobe Signals

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals AC parameter tests for Strobe Signals using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

Probing for Single-Ended Signals AC parameter tests for Strobe Signals

When performing the Single-Ended Signals AC parameter tests for Strobe Signals, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections. The connection for the Single-Ended Signals AC parameter tests for Strobe Signals may look similar to the following diagram. Refer to the Connection tab in DDR2(+LP) Electrical Performance Compliance application for the exact number of probe connections.

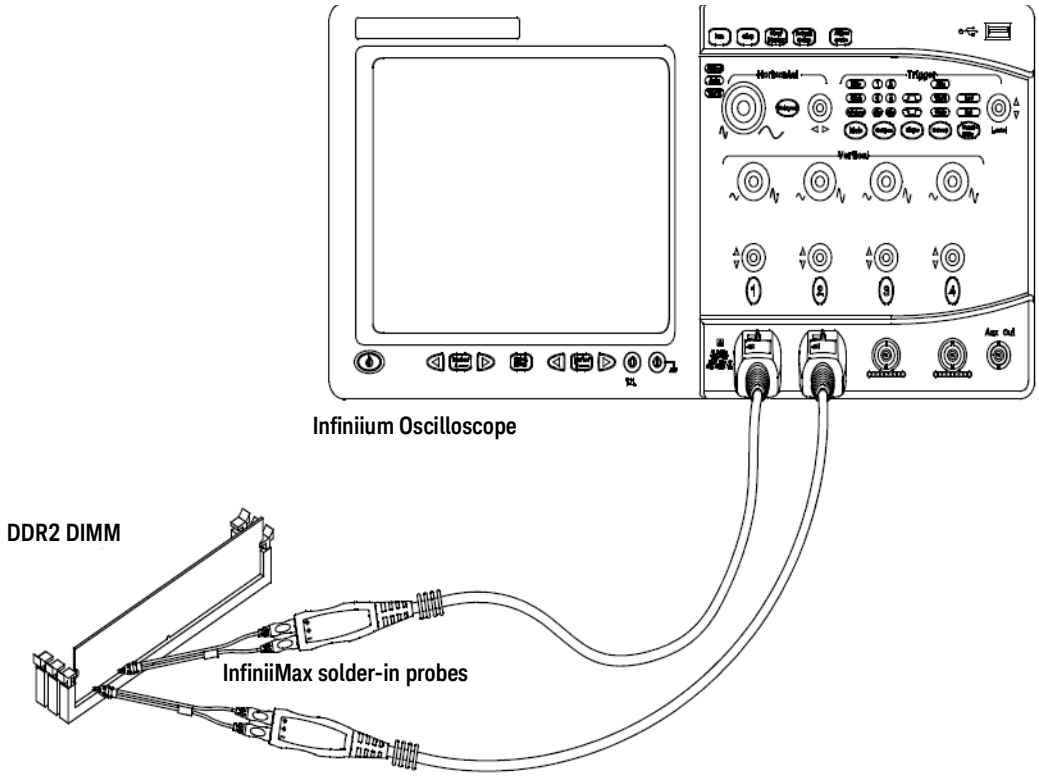


Figure 14 Probing for Single-Ended Signals AC parameter tests for Strobe Signals with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channels shown in Figure 14 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in "Starting the DDR2(+LP) Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the LPDDR2 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the LPDDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the LPDDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2(+LP) Test application, click the Set Up tab.

6 Select the Speed Grade options. For the Single-Ended Signals AC parameter tests for Strobe Signals, you can select any LPDDR2 speed grade within the selection. To see the LPDDR2 Speed Grades, check the Low Power box.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

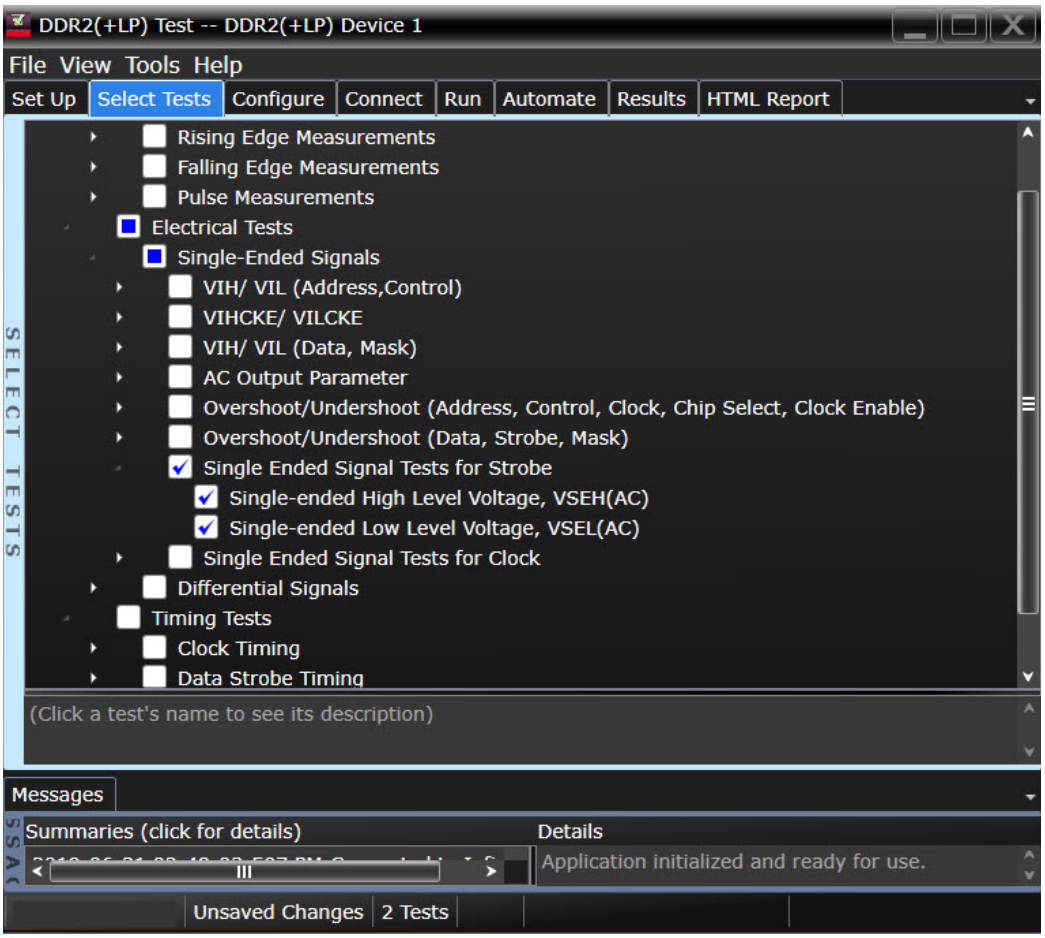


Figure 15 Selecting Single-Ended Signals AC parameter tests for Strobe Signals

9 Follow the DDR2(+LP) Test application's task flow to set up the configuration options, run the tests and view the tests results.

$V_{SEH(AC)}$ (strobe) - Test Method of Implementation

Single-ended Signal Tests for Strobe Tests can be divided into two subtests:

- $V_{SEH(AC)}$ test
- $V_{SEL(AC)}$ test

$V_{SEH(AC)}$ - Single- ended High Level Voltage.

The purpose of this test is to verify that the maximum high pulse voltage must be within the conformance limit of the $V_{SEH(AC)}$ value as specified in the JEDEC specification.

The value of V_{DDQ} (which directly affects the conformance limit) is set to 1.2V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DDQ}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 75 LPDDR2 Single-ended Levels for CK_t, DQS_t, CK_c, and DQS_c

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{SEH(AC)}$	Single-ended high level for strobes	(V_{DDQ} /2) + 0.220	Note 3	(V_{DDQ} /2) + 0.300	Note 3	V	1, 2

Test References

See Table 79 - Single-ended Levels for CK_t, DQS_t, CK_c, and DQS_c in the *JESD209-2B*.

PASS Condition

The worst measured $V_{SEH(AC)}$ shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid strobe positive pulses in this burst. A valid strobe positive pulse starts at the V_{REF} crossing on a valid strobe rising edge and ends at the V_{REF} crossing on the following valid strobe falling edge.
4 For the first valid strobe positive pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform T_{MAX}. Then perform V_{TIME} at the found T_{MAX} to get the maximum voltage of the pulse. Take the V_{TIME} measurement result as the $V_{SEH(AC)}$ value.
5 Continue the previous step for the rest of the valid strobe positive pulses that were found in the burst.
6 Determine the worst result from the set of $V_{SEH(AC)}$ measured.

$V_{SEL(AC)}$ (strobe) - Test Method of Implementation

$V_{SEL(AC)}$ - Single- ended Low Level Voltage.

The purpose of this test is to verify that the minimum low pulse voltage must be within the conformance limit of the $V_{SEL(AC)}$ value as specified in the JEDEC specification.

The value of V_{DDQ} (which directly affects the conformance limit) is set to 1.2V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DDQ}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 76 LPDDR2 Single-ended Levels for CK_t, DQS_t, CK_c, and DQS_c

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{SEL(AC)}$	Single-ended low level for strobes	Note 3	(V_{DDQ} /2) - 0.220	Note 3	(V_{DDQ} /2) - 0.300	V	1, 2

Test References

See Table 79 - Single-ended Levels for CK_t, DQS_t, CK_c, and DQS_c in the *JESD209-2B*.

PASS Condition

The worst measured $V_{SEL(AC)}$ shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid strobe negative pulses in this burst. A valid strobe negative pulse starts at the V_{REF} crossing on a valid strobe falling edge and ends at the V_{REF} crossing on the following valid strobe rising edge.

4 For the first valid strobe negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform T_{MIN}. Then perform V_{TIME} at the found T_{MIN} to get the minimum voltage of the pulse. Take the V_{TIME} measurement result as the $V_{SEL(AC)}$ value.

5 Continue the previous step for the rest of the valid strobe negative pulses that were found in the burst.

6 Determine the worst result from the set of $V_{SEL(AC)}$ measured.

8 Single-Ended Signals AC Parameters Tests for Clock

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals AC parameter tests for Clock using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

Probing for Single-Ended Signals AC parameter tests for Clock

When performing the Single-Ended Signals AC parameter tests for Clocks, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections. The connection for the Single-Ended Signals AC parameter tests for Clocks may look similar to the following diagram. Refer to the Connection tab in DDR2(+LP) Electrical Performance Compliance application for the exact number of probe connections.

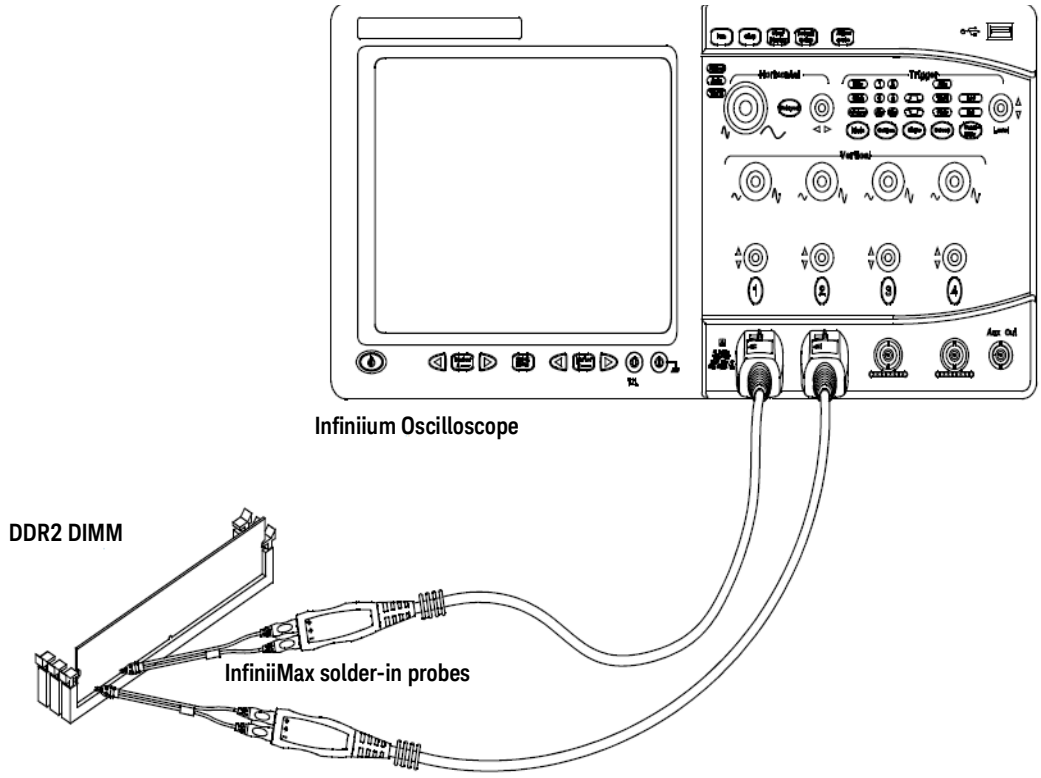


Figure 16 Probing for Single-Ended Signals AC parameter tests for Clocks with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channels shown in Figure 16 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in "Starting the DDR2(+LP) Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the LPDDR2 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the LPDDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the LPDDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2(+LP) Test application, click the Set Up tab.

6 Select the Speed Grade options. For the Single-Ended Signals AC parameter tests for Clocks, you can select any LPDDR2 speed grade within the selection. To see the LPDDR2 Speed Grades, check the Low Power box.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

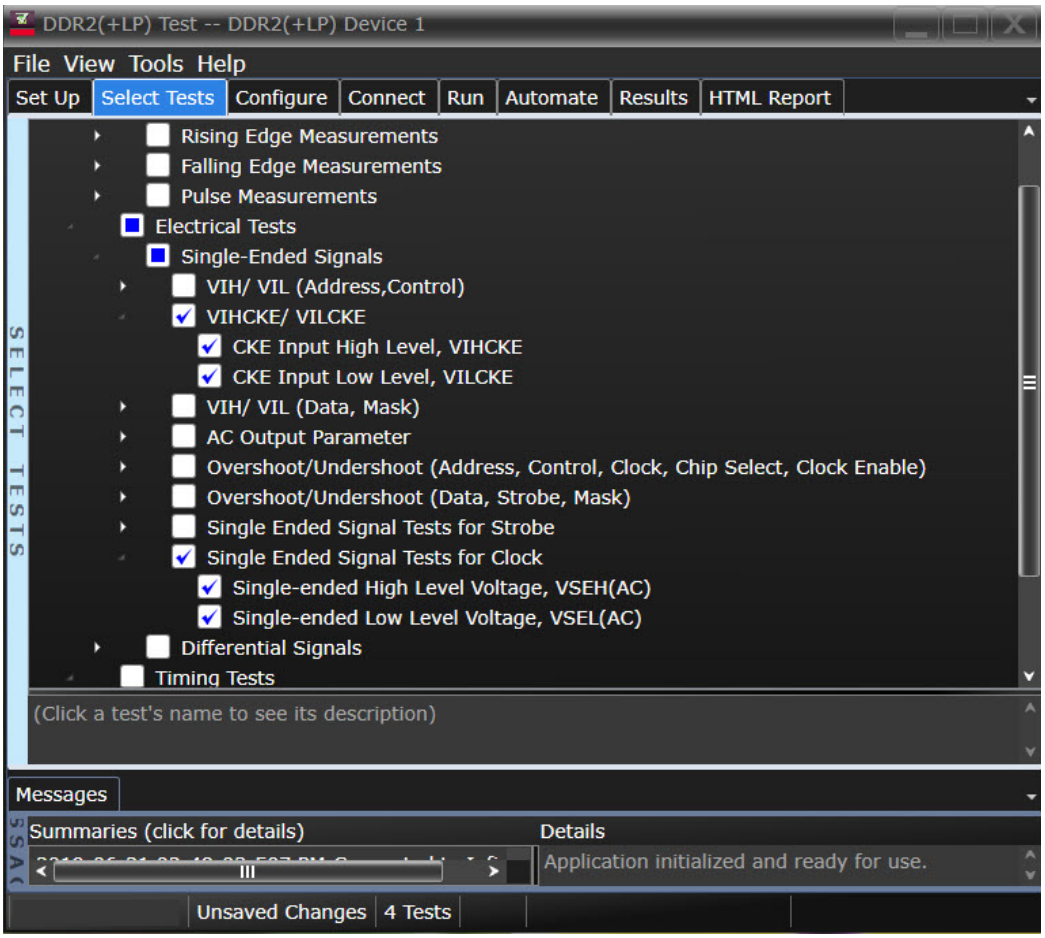


Figure 17 Selecting Single-Ended Signals AC parameter tests for Clocks

9 Follow the DDR2(+LP) Test application's task flow to set up the configuration options, run the tests and view the tests results.

$V_{SEH(AC)}$ (clock) - Test Method of Implementation

Single-ended Signal Tests for Clock Tests can be divided into two subtests:

- $V_{SEH(AC)}$ test
- $V_{SEL(AC)}$ test

$V_{SEH(AC)}$ - Single- ended High Level Voltage.

The purpose of this test is to verify that the maximum high pulse voltage must be within the conformance limit of the $V_{SEH(AC)}$ value as specified in the JEDEC specification.

The value of V_{DDCA} (which directly affects the conformance limit) is set to 1.2V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DDCA}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Clock Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Clock Signals

Test Definition Notes from the Specification

Table 77 LPDDR2 Single-ended Levels for CK_t, DQS_t, CK_c, and DQS_c

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{SEH(AC)}$	Single-ended high level for CK_t, CK_c	(V_{DDCA} /2) + 0.220	Note 3	(V_{DDCA} /2) + 0.300	Note 3	V	1, 2

Test References

See Table 79 - Single-ended Levels for CK_t, DQS_t, CK_c, and DQS_c in the *JESD209-2B*.

PASS Condition

The worst measured $V_{SEH(AC)}$ shall be within the specification limit.

Measurement Algorithm

1 Pre-condition the oscilloscope.
2 Trigger on a rising edge of the clock signal under test.
3 Find all valid Clock positive pulses in the entire waveform. A valid Clock positive pulse starts at the V_{REF} crossing on a valid Clock rising edge and ends at the V_{REF} crossing on the following valid Clock falling edge.
4 For the first valid Clock positive pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform T_{MAX}. Then perform V_{TIME} at the found T_{MAX} to get the maximum voltage of the pulse. Take the V_{TIME} measurement result as the $V_{SEH(AC)}$ value.
5 Continue the previous step for the rest of the valid Clock positive pulses that were found in the waveform.
6 Determine the worst result from the set of $V_{SEH(AC)}$ measured.

$V_{SEL(AC)}$ (clock) - Test Method of Implementation

$V_{SEL(AC)}$ - Single- ended Low Level Voltage.

The purpose of this test is to verify that the minimum low pulse voltage must be within the conformance limit of the $V_{SEL(AC)}$ value as specified in the JEDEC specification.

The value of V_{DDCA} (which directly affects the conformance limit) is set to 1.2V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DDCA}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Clock Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Clock Signals

Test Definition Notes from the Specification

Table 78 LPDDR2 Single-ended Levels for CK_t, DQS_t, CK_c, and DQS_c

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{SEL(AC)}$	Single-ended low level for CK_t, CK_c	Note 3	(V_{DDCA} /2) - 0.220	Note 3	(V_{DDCA} /2) - 0.300	V	1, 2

Test References

See Table 79 - Single-ended Levels for CK_t, DQS_t, CK_c, and DQS_c in the *JESD209-2B*.

PASS Condition

The worst measured $V_{SEL(AC)}$ shall be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope.
2. Trigger on a rising edge of the clock signal under test.
3. Find all valid Clock negative pulses in the entire waveform. A valid Clock negative pulse starts at the V_{REF} crossing on a valid Clock falling edge and ends at the V_{REF} crossing on the following valid Clock rising edge.
4. For the first valid Clock negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform T_{MIN}. Then perform V_{TIME} at the found T_{MIN} to get the minimum voltage of the pulse. Take the V_{TIME} measurement result as the $V_{SEL(AC)}$ value.
5. Continue the previous step for the rest of the valid Clock negative pulses that were found in the waveform.
6. Determine the worst result from the set of $V_{SEL(AC)}$ measured.

V_{IHCKE} Test - Input Logic High (Clock Enable) - Test Method of Implementation

The purpose of this test is to verify that the mode of histogram of the high level voltage value of the test signal within a valid sampling window is greater than the conformance lower limits of the V_{IHCKE} value specified in the JEDEC specification.

The value of V_{DDCA} which directly affect the conformance lower limit is set to 1.2V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of V_{DDCA}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: NO

Signal(s) of Interest:

- Clock Enable Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any of the signal of interest defined above

Test Definition Notes from the Specification

Table 79 LPDDR2 Single-ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Units	Notes
V_{IHCKE}	CKE Input High Level	0.8 * V_{DDCA}	Note 1	V	1

Test References

See Table 75 - Single-ended AC and DC Input Levels for CKE in the *JESD209-2B*.

PASS Condition

The mode value for the high level voltage shall be greater than or equal to the minimum V_{IHCKE} value.

Measurement Algorithm

1 Sample/acquire signal data.

2 Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at valid rising edge and end at V_{REF} crossing at the following valid falling edge (See notes on threshold).

3 Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement results as V_{IHCKE} value.

4 Continue the previous step with another 9 valid positive pulses.

5 Determine the worst result from the set of V_{IHCKE} measured.

V_{ILCKE} Test - Input Logic Low (Clock Enable) - Test Method of Implementation

The purpose of this test is to verify that the mode of histogram of the low level voltage value of the test signal within a valid sampling window is lower than the conformance maximum limits of the V_{ILCKE} value specified in the JEDEC specification.

The value of V_{DDCA} which directly affect the conformance maximum limit is set to 1.2V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of V_{DDCA}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: NO

Signal(s) of Interest:

- Clock Enable Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any of the signal of interest defined above

Test Definition Notes from the Specification

Table 80 LPDDR2 Single-ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Units	Notes
V_{ILCKE}	CKE Input Low Level	Note 1	0.2 * V_{DDCA}	V	1

Test References

See Table 75 - Single-ended AC and DC Input Levels for CKE in the *JESD209-2B*.

PASS Condition

The mode value for the low level voltage shall be less than or equal to the minimum V_{ILCKE} value.

Measurement Algorithm

1 Sample/acquire signal data.

2 Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at valid falling edge and end at V_{REF} crossing at the following rising valid edge (See notes on threshold).

3 Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement results as V_{ILCKE} value.

4 Continue the previous step with another 9 valid positive pulses.

5 Determine the worst result from the set of V_{ILCKE} measured.

9 Single-Ended Signals Overshoot/Undershoot Tests

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals Overshoot/Undershoot tests using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

Probing for Overshoot/Undershoot Tests

When performing the Single-Ended Signals Overshoot/Undershoot tests, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections as shown in the following diagram. Refer to the Connection tab in DDR2(+LP) Electrical Performance Compliance application for the exact number of probe connections.

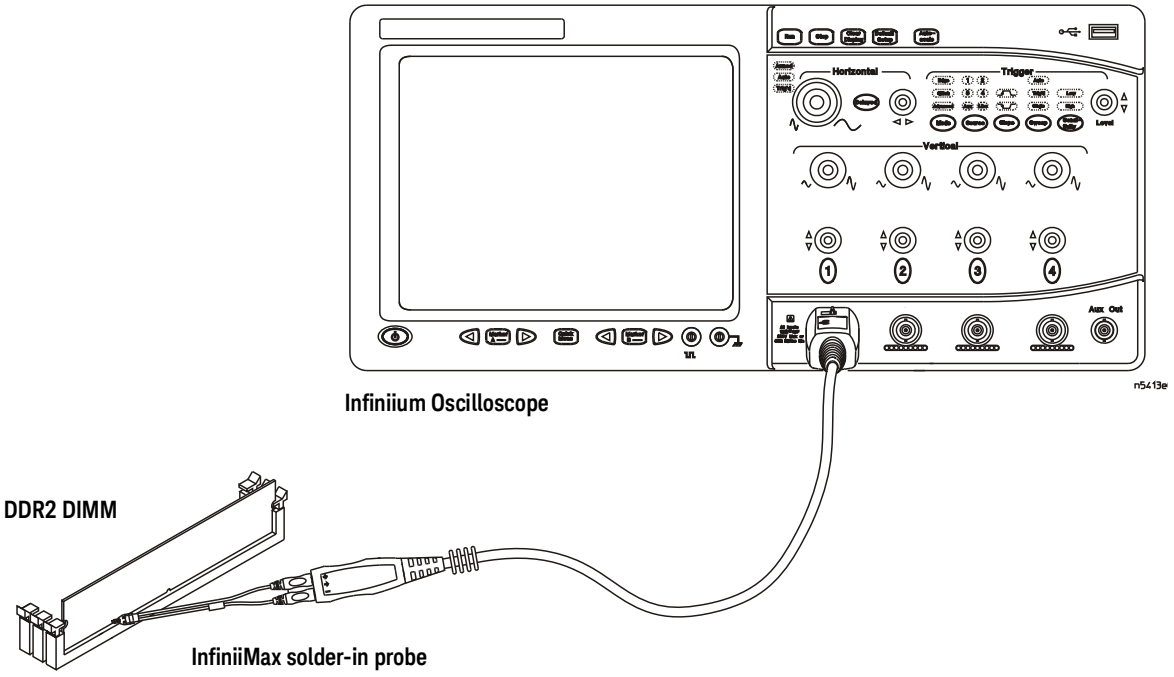


Figure 18 Probing for Single-Ended Signals Overshoot/Undershoot Tests

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channel shown in Figure 18 is just an example).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1. Start the automated test application as described in "Starting the DDR2(+LP) Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR2/LPDDR2 Device Under Test (DUT) is attached. This software will perform test on all unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2/LPDDR2 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR2/LPDDR2 devices.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR2(+LP) Test application, click the Set Up tab.
6. Select the Speed Grade options. For Single-Ended Signals Overshoot/Undershoot tests, you can select any speed grade within the selection. To select one of the LPDDR2 speed grades, check the Low Power box.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

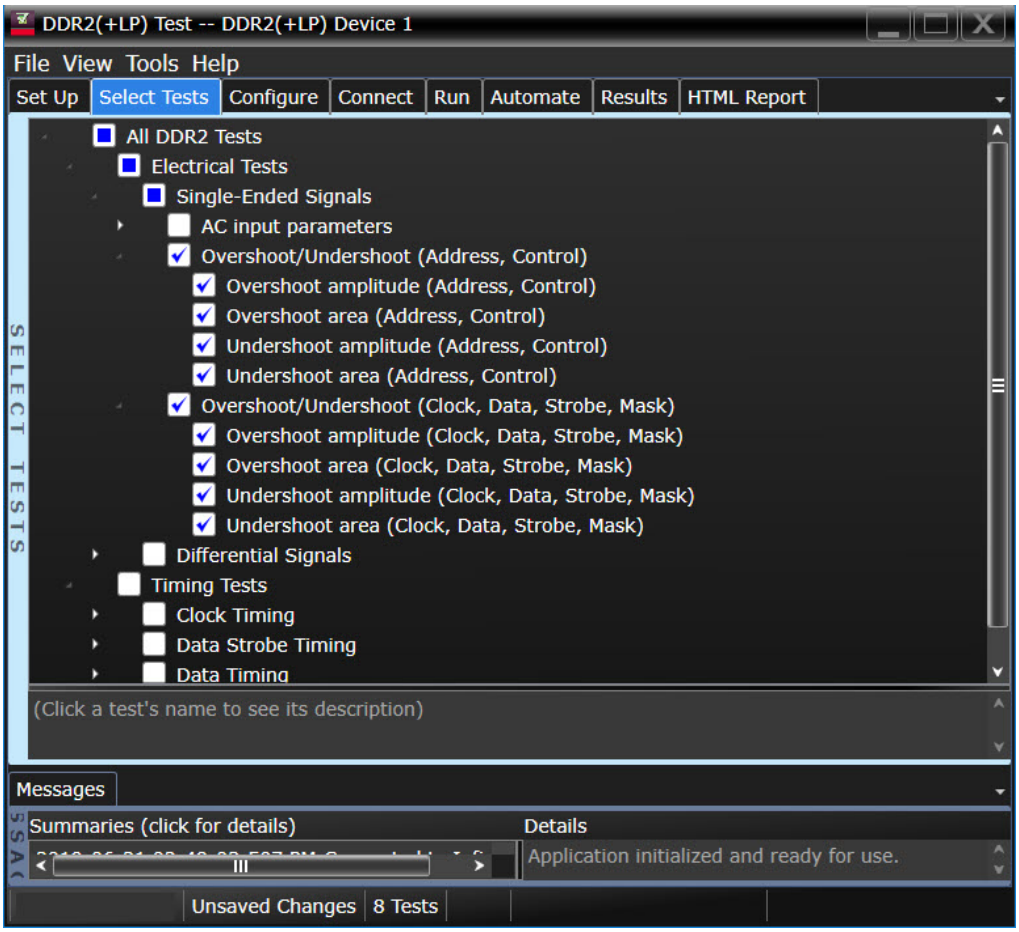


Figure 19 Selecting Single-Ended Signals Overshoot/Undershoot Tests

9 Follow the DDR2(+LP) Test application's task flow to set up the configuration options, run the tests and view the tests results.

AC Overshoot Test Method of Implementation

The Overshoot test can be divided into two sub-tests: Overshoot amplitude and overshoot area.

The purpose of this test is to verify that the overshoot value of the test signal within a user-specific region is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot test as specified in the JEDEC specification.

When there is an overshoot, the overshoot area is calculated based on the overshoot width. The overshoot area should be lower than or equal to the conformance limit of the maximum overshoot area allowed as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: READ or WRITE

Signal(s) of Interest:

- Data Signal OR
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 81 AC Overshoot Specification for Address and Control Pin

A0-A15, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for overshoot area	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V
Maximum overshoot area above V_{DD}	1.33 V-ns	1.0 V-ns	0.8 V-ns	0.66 V-ns

Table 82 AC Overshoot Specification for Clock, Data, Strobe and Mask Pins

DQ, (U/L/R)DQS, $\overline{(U/L/R)DQS}$, DM, CK, $\overline{CK}$

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for overshoot area	0.5 V	0.5 V	0.5 V	0.5 V
Maximum overshoot area above V_{DDQ}	0.38 V-ns	0.28 V-ns	0.23 V-ns	0.23 V-ns

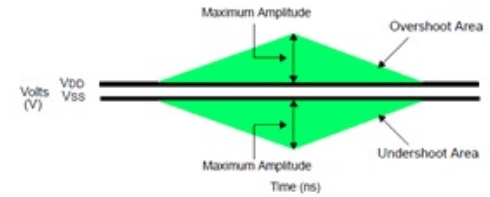


Figure 75 — AC overshoot and undershoot definition for address and control pins

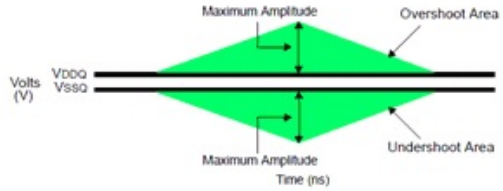


Figure 76 — AC overshoot and undershoot definition for clock, data, strobe, and mask pins

Table 83 AC Overshoot Specification for Address and Control Pins (DDR2-1066)

A0-A15, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification
	DDR2-1066
Maximum peak amplitude allowed for overshoot area	0.5(0.9)[1] V
Maximum overshoot area above V_{DD}	0.5 V-ns

Table 84 AC Overshoot Specification for Clock, Data, Strobe and Mask Pins (DDR2-1066)

DQ, (U/L/R)DQS, $\overline{(U/L/R)DQS}$, DM, CK, $\overline{CK}$

Parameter	Specification
	DDR2-1066
Maximum peak amplitude allowed for overshoot area	0.5 V
Maximum overshoot area above V_{DDQ}	0.19 V-ns

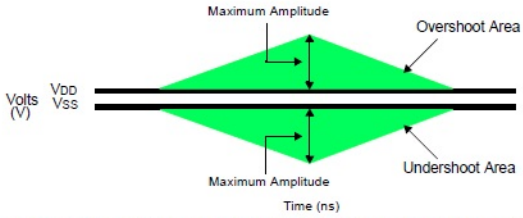


Figure 67 — AC overshoot and undershoot definition for address and control pins

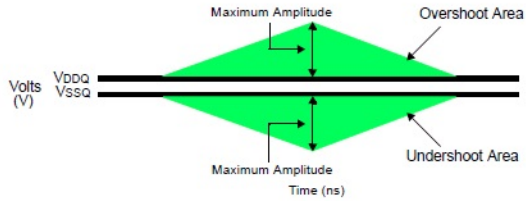


Figure 68 — AC overshoot and undershoot definition for clock, data, strobe, and mask pins

Table 85 LPDDR2 AC Overshoot/Undershoot Specification

Parameter		1066	933	800	677	533	466	400	333	266	200	Unit
Maximum peak amplitude allowed for overshoot area	Max						0.35					V
Maximum peak amplitude allowed for undershoot area	Max						0.35					V
Maximum area above V_{DD}	Max	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns
Maximum area below V_{SS}	Max	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns

Test References

See Table 24 - AC Overshoot/Undershoot Specification for Address and Control Pins and Table 25 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins in the *JEDEC Standard JESD79-2E*.

Also See Table 24 - AC Overshoot/Undershoot Specification for Address and Control Pins and Table 25 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins in the *JESD208*.

Also see Table 88 - LPDDR2 AC Overshoot/Undershoot Specification in the *JESD209-2B*.

PASS Condition

The measured maximum voltage value of the test signal should be less than or equal to the maximum overshoot value.

The calculated overshoot area value should be less than or equal to the maximum overshoot area allowed.

Measurement Algorithm

1 Set the number of sampling points to 2M samples.
2 Sample/acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3 Use T_{MAX}, V_{MAX} to get a timestamp of the maximum voltage on all regions of acquired waveform.
4 Perform manual zoom on waveform to maximize peak area.
5 Find the edges before and after the Overshoot Point at the Supply Reference Level in order to calculate the maximum overshoot length duration. The table below shows the supply reference level for each pin group.

Pin	Supply Reference Level
DDR2 Address and Control Pin	V_{DD}
DDR2 Clock, Data, Strobe, and Mask Pin	V_{DDQ}
LPDDR2 Address, Control, Clock, Chip Select and Clock Enable	V_{DDCA}
LPDDR2 Data, Strobe, Mask	V_{DDQ}

6 Calculate the overshoot amplitude.
Overshoot amplitude = V_{MAX} - supply reference level. Refer to the table above.
7 Calculate the overshoot area (V-ns)
a Area of calculation is based on the area of calculation of a triangle where the overshoot width is used as the triangle base and the overshoot amplitude is used as the triangle height.
b Area = 0.5 * base * height.
8 Compare the test results with the compliance test limits.

AC Undershoot Test Method of Implementation

The Undershoot Test can be divided into two sub-tests: Undershoot amplitude and Undershoot area.

The purpose of this test is to verify that the undershoot value of the test signal within a user-specific region is lower than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot test as specified in the JEDEC specification.

When there is an undershoot, the undershoot area is calculated based on the undershoot width. The undershoot area should be lower than or equal to the conformance limit of the maximum undershoot area allowed as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: READ or WRITE

Signal(s) of Interest:

- Data Signal OR
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above

Test Definition Notes from the Specification

Table 86 AC Undershoot Specification for Address and Control Pins

A0-A15, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for undershoot area	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V
Maximum undershoot area below V_{SS}	1.33 V-ns	1.0 V-ns	0.8 V-ns	0.66 V-ns

Table 87 AC Undershoot Specification for Clock, Data, Strobe and Mask Pins

DQ, (U/L/R)DQS, $\overline{(U/L/R)DQS}$, DM, CK, $\overline{CK}$

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for undershoot area	0.5 V	0.5 V	0.5 V	0.5 V
Maximum undershoot area below V_{SSQ}	0.38 V-ns	0.28 V-ns	0.23 V-ns	0.23 V-ns

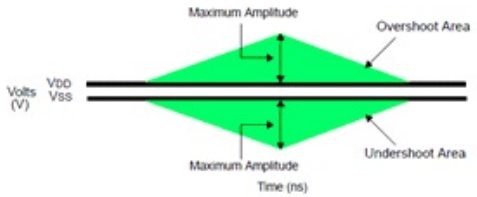


Figure 75 — AC overshoot and undershoot definition for address and control pins

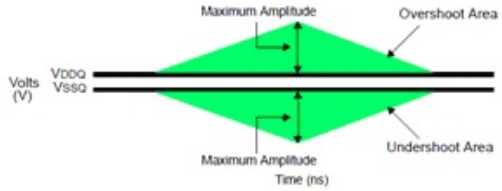


Figure 76 — AC overshoot and undershoot definition for clock, data, strobe, and mask pins

Table 88 AC Undershoot Specification for Address and Control Pins (DDR2-1066)

A0-A15, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification
	DDR2-1066
Maximum peak amplitude allowed for undershoot area	0.5(0.9)[1] V
Maximum undershoot area below V_{SS}	0.5 V-ns

Table 89 AC Undershoot Specification for Clock, Data, Strobe and Mask Pins (DDR2-1066)

DQ, (U/L/R)DQS, $\overline{(U/L/R)DQS}$, DM, CK, $\overline{CK}$

Parameter	Specification
	DDR2-1066
Maximum peak amplitude allowed for undershoot area	0.5 V
Maximum undershoot area below VSSQ	0.19 V-ns

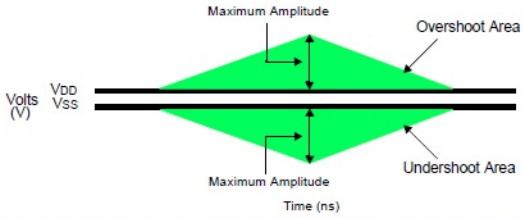


Figure 67 — AC overshoot and undershoot definition for address and control pins

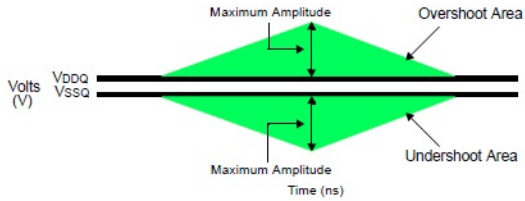


Figure 68 — AC overshoot and undershoot definition for clock, data, strobe, and mask pins

Table 90 LPDDR2 AC Overshoot/Undershoot Specification

Parameter		1066	933	800	677	533	466	400	333	266	200	Unit
Maximum peak amplitude allowed for overshoot area	Max						0.35					V
Maximum peak amplitude allowed for undershoot area	Max						0.35					V
Maximum area above V_{DD}	Max	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns
Maximum area below V_{SS}	Max	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns

Test References

See Table 24 - AC Overshoot/Undershoot Specification for Address and Control Pins and Table 25 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins, in the *JEDEC Standard JESD79-2E*.

Also See Table 24 - AC Overshoot/Undershoot Specification for Address and Control Pins and Table 25 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins in the *JESD208*.

Also see Table 88 - LPDDR2 AC Overshoot/Undershoot Specification in the *JESD209-2B*.

PASS Condition

The measured minimum voltage value for the test signal should be less than or equal to the maximum undershoot value.

The calculated undershoot area value should be less than or equal to the maximum undershoot area allowed.

Measurement Algorithm

1. Set the number of sampling points to 2M samples.
2. Sample/acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Use T_{MAX}, V_{MAX} to get a timestamp of the minimum voltage on all regions of acquired waveform.
4. Perform manual zoom on waveform to minimum peak area.
5. Find the edges before and after the Undershoot Point at the GND (~0V) Level in order to calculate the maximum undershoot length duration.
6. Calculate Undershoot amplitude.
   Undershoot amplitude = 0 - V_{MIN}.
7. Calculate the undershoot area (V-ns)
   a Area of calculation is based on the area of calculation of a triangle where the undershoot width is used as the triangle base and the undershoot amplitude is used as the triangle height.
   b Area = 0.5 * base * height.
8. Compare the test results with the compliance test limits.

10 Differential Signals AC Input Parameters Tests

This section provides the Methods of Implementation (MOIs) for Differential Signals AC Input tests using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

Probing for Differential Signals AC Input Parameters Tests

When performing the Differential Signals AC Input Parameters tests, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections. The connection for the Differential Signals AC Input Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR2(+LP) Electrical Performance Compliance application for the exact number of probe connections.

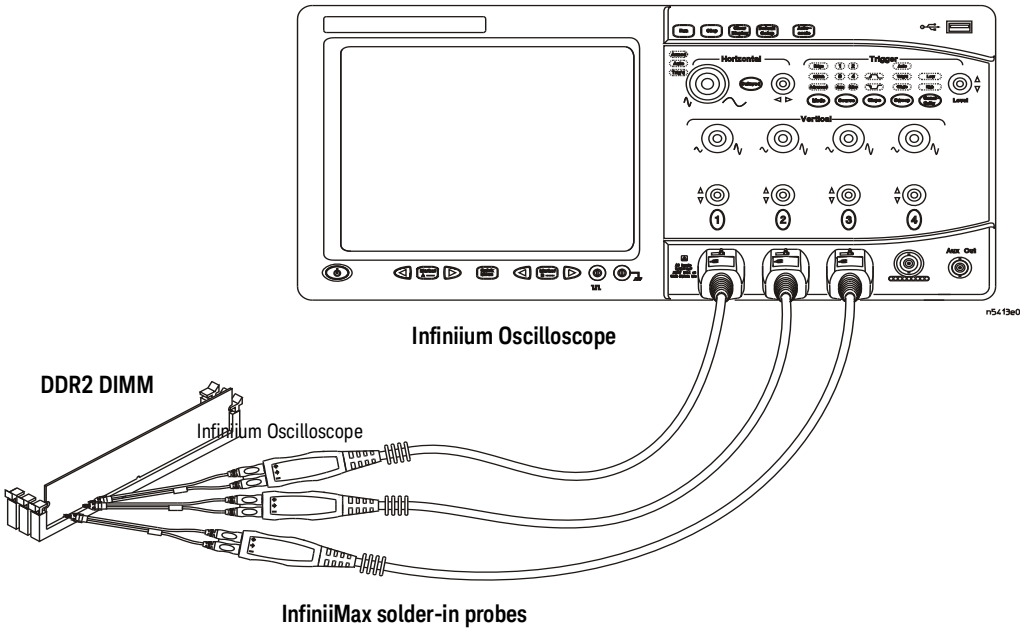


Figure 20 Probing for Differential Signals AC Input Parameters Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channels shown in Figure 20 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in "Starting the DDR2(+LP) Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR2/LPDDR2 Device Under Test (DUT) is attached. This software will perform test on all unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2/LPDDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2/LPDDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2(+LP) Test application, click the Set Up tab.

6 Select the Speed Grade options. For Differential Signals AC Input Parameters Tests that support DDR2, you can select any speed grade within the selection. To select a LPDDR2 Speed Grade (for tests that support LPDDR2), check the Low Power box.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

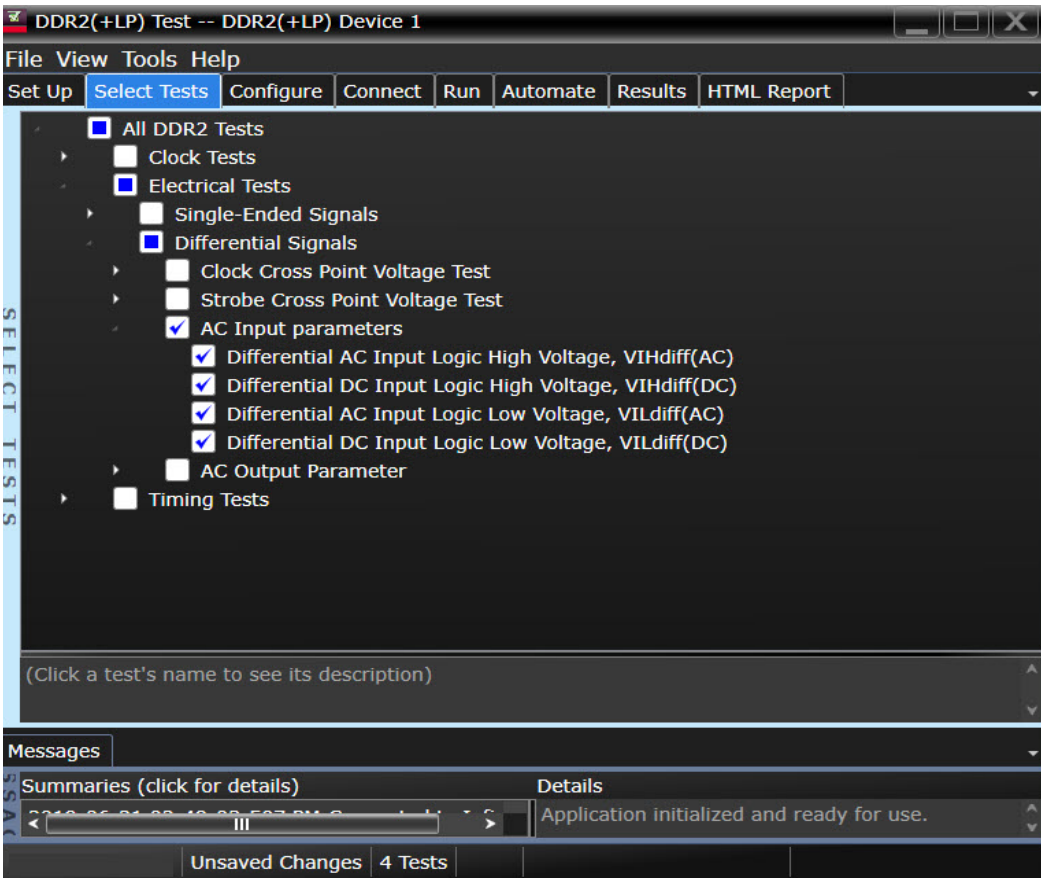


Figure 21 Selecting Differential Signals AC Input Parameters Tests

9 Follow the DDR2(+LP) Test application's task flow to set up the configuration options, run the tests and view the tests results.

$V_{ID(AC)}$, AC Differential Input Voltage Test for DQS - Test Method of Implementation

The purpose of this test is to verify that magnitude differences between the input differential signal pairs value of the test signals is within the conformance limits of the $V_{ID(AC)}$ as specified in the JEDEC specification.

The value of V_{DDQ} which directly affects the conformance lower limit is set to 1.8V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{DDQ}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 91 Differential Input AC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{ID(AC)}$	AC differential input voltage	0.5	V_{DDQ}	V	1,3

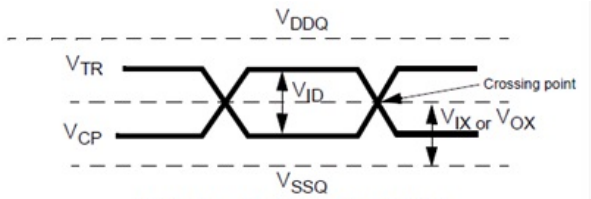
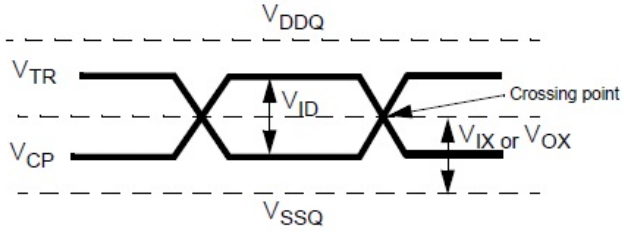


Figure 74 — Differential signal levels

Table 92 Differential Input AC Logic Level (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{ID(AC)}$	AC differential input voltage	0.5	V_{DDQ} + 0.6	V	1



Test References

See Table 22 - Differential Input AC Logic Level in the *JEDEC Standard JESD79-2E* and Table 22 - Differential Input AC Logic Level in the *JESD208*.

PASS Condition

The calculated magnitude of the differential voltage of the test signals pair should be within the conformance limits of the $V_{ID(AC)}$ value.

Measurement Algorithm

1 Sample/acquire data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the two source inputs.
3 Split read and write burst of the acquired signal.
4 Take the first valid WRITE burst found.
5 Find all differential DQS crossing that cross 0V.
6 Within the first and second DQS crossing regions, perform V_{TOP} on DQS,Gnd or /DQS,Gnd depending on which one is the positive pulse in current region. Next, perform V_{BASE} on DQS,Gnd or /DQS,Gnd depending on which one is the negative pulse in the current region. Calculate $V_{ID(AC)} = V_{TOP} - V_{BASE}$.
7 Perform the previous step on all pairs of DQS crossing.
8 Determine the worst result from the set of $V_{ID(AC)}$ measured.

$V_{ID(AC)}$, AC Differential Input Voltage Test for Clock - Test Method of Implementation

The purpose of this test is to verify that magnitude differences between the input differential signal pairs value of the test signals is within the conformance limits of the $V_{ID(AC)}$ as specified in the JEDEC specification.

The value of V_{DDQ} which directly affects the conformance lower limit is set to 1.8V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{DDQ}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Require Read/Write separation: NO

Signal(s) of Interest:

- Clock Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Clock Signals

Test Definition Notes from the Specification

Table 93 Differential Input AC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{ID(AC)}$	AC differential input voltage	0.5	V_{DDQ}	V	1,3

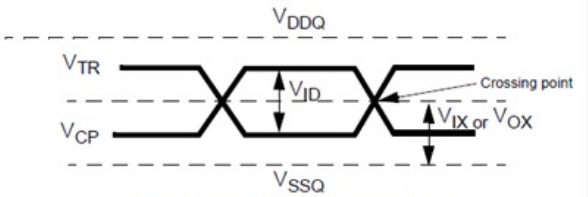
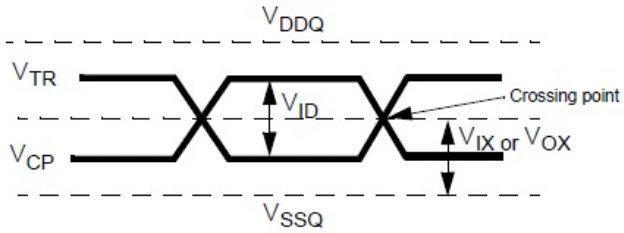


Figure 74 — Differential signal levels

Table 94 Differential Input AC Logic Level (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{ID(AC)}$	AC differential input voltage	0.5	V_{DDQ} + 0.6	V	1



Test References

See Table 22 - Differential Input AC Logic Level in the *JEDEC Standard JESD79-2E* and Table 22 - Differential Input AC Logic Level in the *JESD208*.

PASS Condition

The calculated magnitude of the differential voltage of the test signals pair should be within the conformance limits of the $V_{ID(AC)}$ value.

Measurement Algorithm

1 Sample/acquire data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the two source inputs.
3 Find the first 10 differential CLK crossing that cross 0V.
4 Within first and second CLK crossing region, perform V_{TOP} on CLK,GND OR /CLK,GND depending on which one is the positive pulse in the current region. Next, perform V_{BASE} on CLK,GND OR /CLK,GND depending on which one is the negative pulse in the current region. Calculate $V_{ID(AC)} = V_{TOP} - V_{BASE}$.
5 Perform the previous step on all pairs of CLK crossing until 10 measurement results are collected.
6 Determine the worst result from the set of $V_{ID(AC)}$ measured.

$V_{IX(AC)}$, AC Differential Input Cross Point Voltage Test for DQS -Test Method of Implementation

The purpose of this test is to verify the crossing point voltage value of the input differential test signals pair is within the conformance limits of the $V_{IX(AC)}$ as specified in the JEDEC specification.

The value of V_{DDQ} which directly affects the conformance lower limit is set to 1.8V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{DDQ}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 95 Differential Input AC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IX(AC)}$	AC differential cross point voltage	0.5 * V_{DDQ} - 0.175	0.5 * V_{DDQ} + 0.175	V	2

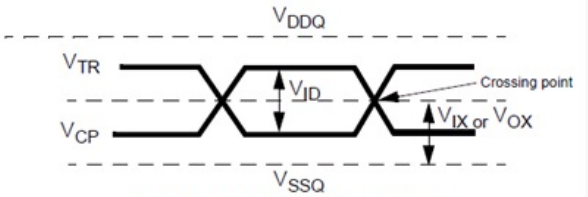
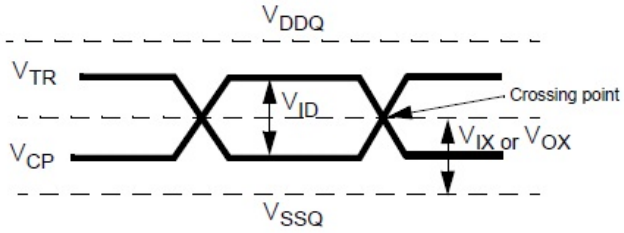


Figure 74 — Differential signal levels

Table 96 Differential Input AC Logic Level (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{IX(AC)}$	AC differential cross point voltage	0.5 * V_{DDQ} - 0.175	0.5 * V_{DDQ} + 0.175	V	2



Test References

See Table 22 - Differential Input AC Logic Level in the *JEDEC Standard JESD79-2E* and Table 22 - Differential Input AC Logic Level in the *JESD208*.

PASS Condition

The measured crossing point value for the differential test signals pair should be within the conformance limits of $V_{IX(AC)}$ value.

Measurement Algorithm

1 Sample/acquire data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the two source inputs.
3 Split read and write bursts of the acquired signal.
4 Take the first valid WRITE burst found.
5 Find all differential DQS crossing that cross 0V.
6 Use V_{Time} to get the actual crossing point voltage value using the timestamp obtained
7 Determine the worst result from the set of $V_{IX(AC)}$ measured.

$V_{IX(AC)}$, AC Differential Input Cross Point Voltage Test for Clock -Test Method of Implementation

The purpose of this test is to verify the crossing point voltage value of the input differential test signals pair is within the conformance limits of the $V_{IX(AC)}$ as specified in the JEDEC specification.

The value of V_{DDQ} which directly affects the conformance lower limit is set to 1.8V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{DDQ}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: No

Signal(s) of Interest:

- Clock Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Clock Signals

Test Definition Notes from the Specification

Table 97 Differential Input AC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IX(AC)}$	AC differential cross point voltage	0.5 * V_{DDQ} - 0.175	0.5 * V_{DDQ} + 0.175	V	2

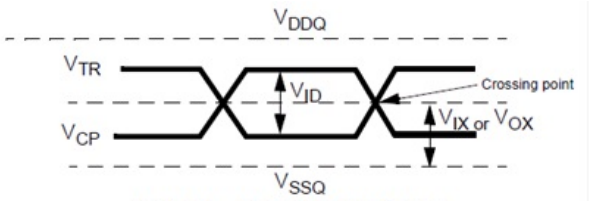
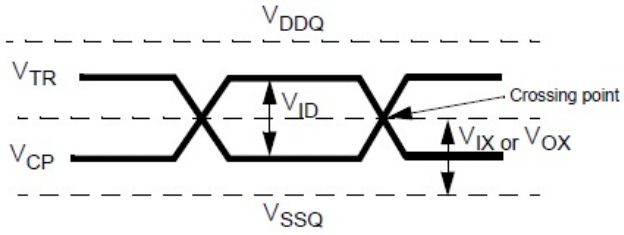


Figure 74 — Differential signal levels

Table 98 Differential Input AC Logic Level (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{IX(AC)}$	AC differential cross point voltage	0.5 * V_{DDQ} - 0.175	0.5 * V_{DDQ} + 0.175	V	2



Test References

See Table 22 - Differential Input AC Logic Level in the *JEDEC Standard JESD79-2E* and Table 22 - Differential Input AC Logic Level in the *JESD208*.

PASS Condition

The measured crossing point value for the differential test signals pair should be within the conformance limits of $V_{IX(AC)}$ value.

Measurement Algorithm

1 Sample/acquire data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the two source inputs.
3 Find the first 10 differential CLK crossing that cross 0V.
4 Use V_{Time} to get the actual crossing point voltage value by using the timestamp obtained
5 Determine the worst result from the set of $V_{IX(AC)}$ measured.

$V_{IHdiff(AC)}$ Test for DQS - Test Method of Implementation

$V_{IHdiff(AC)}$ - Differential AC Input Logic High Voltage Test for DQS.

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{IHdiff(AC)}$ value as specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance limit is set to 0.6V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IH(AC)}$ (which directly affect the conformance limit) is set to 0.9V for Speed Grades from LPDDR2- 200 to LPDDR2- 400 or 0.82V for Speed Grades from LPDDR2- 466 to LPDDR2- 1066 for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of $V_{IH(DC)}$.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 99 LPDDR2 Differential AC and DC Input Level

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{IHdiff(AC)}$	Differential input HIGH AC	2 x ($V_{IH(AC)}$ - V_{REF})	Note 3	2 x ($V_{IH(AC)}$ - V_{REF})	Note 3	V	2

Test References

See Table 77 - Differential AC and DC Input Level in the *JESD209-2B*.

PASS Condition

The worst measured $V_{IHdiff(AC)}$ shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal. (See notes on DDR read/write separation).
2 Take the first valid WRITE burst found.
3 Find all valid Strobe positive pulses in the burst. A valid Strobe positive pulse starts at 0 Volt crossing at valid Strobe rising edge (see notes on threshold) and ends at the 0V crossing on the following valid Strobe falling edge (see notes on threshold).
4 For the first valid Strobe positive pulse, zoom in on the pulse so that it appears on the oscilloscope's display, and perform the V_{TOP} measurement. Take the V_{TOP} measurement result as the $V_{IHdiff(AC)}$ value.
5 Continue the previous step for the rest of the valid Strobe positive pulses that were found in the burst.
6 Determine the worst result from the set of $V_{IHdiff(AC)}$ measured.

$V_{IHdiff(AC)}$ Test for Clock - Test Method of Implementation

$V_{IHdiff(AC)}$ - Differential AC Input Logic High Voltage Test for Clock.

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{IHdiff(AC)}$ value as specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance limit is set to 0.6V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IH(AC)}$ (which directly affect the conformance limit) is set to 0.9V for Speed Grades from LPDDR2- 200 to LPDDR2- 400 or 0.82V for Speed Grades from LPDDR2- 466 to LPDDR2- 1066 for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of $V_{IH(DC)}$.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: No

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Clock Signals

Test Definition Notes from the Specification

Table 100 LPDDR2 Differential AC and DC Input Level

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{IHdiff(AC)}$	Differential input HIGH AC	2 x ($V_{IH(AC)}$ - V_{REF})	Note 3	2 x ($V_{IH(AC)}$ - V_{REF})	Note 3	V	2

Test References

See Table 77 - Differential AC and DC Input Level in the *JESD209-2B*.

PASS Condition

The worst measured $V_{IHdiff(AC)}$ shall be within the specification limit.

Measurement Algorithm

1 Pre-condition the oscilloscope.
2 Trigger on a rising edge of the clock signal under test.
3 Find all valid Clock positive pulses in the triggered waveform. A valid Clock positive pulse starts at the 0V crossing on a valid Clock rising edge (see notes on threshold) and ends at the 0V crossing on the following valid Clock falling edge (see notes on threshold).
4 For the first valid Clock positive pulse, zoom in on the pulse so that it appears on the oscilloscope's display, and perform the V_{TOP} measurement. Take the V_{TOP} measurement result as the $V_{IHdiff(AC)}$ value.
5 Continue the previous step for the rest of the valid Clock positive pulses.
6 Determine the worst result from the set of $V_{IHdiff(AC)}$ measured.

$V_{IHdiff(DC)}$ Test for DQS - Test Method of Implementation

$V_{IHdiff(DC)}$ - Differential DC Input Logic High Voltage Test for DQS.

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{IHdiff(DC)}$ value as specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance limit is set to 0.6V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IH(DC)}$ which directly affects the conformance limit is set to 0.8V for Speed Grades from LPDDR2- 200 to LPDDR2- 400 or 0.73V for Speed Grades from LPDDR2- 466 to LPDDR2- 1066 for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of $V_{IH(DC)}$.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 101 LPDDR2 Differential AC and DC Input Level

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{IHdiff(DC)}$	Differential input HIGH DC	2 x ($V_{IH(DC)}$ - V_{REF})	Note 3	2 x ($V_{IH(DC)}$ - V_{REF})	Note 3	V	1

Test References

See Table 77 - Differential AC and DC Input Level in the *JESD209-2B*.

PASS Condition

The worst measured $V_{IHdiff(DC)}$ shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal. (See notes on DDR read/write separation).
2 Take the first valid WRITE burst found.
3 Find all valid Strobe positive pulses in the burst. A valid Strobe positive pulse starts at the 0V crossing on a valid Strobe rising edge (see notes on threshold) and ends at the 0V crossing on the following valid Strobe falling edge (see notes on threshold).
4 For the first valid Strobe positive pulse, zoom in on the pulse so that it appears on the oscilloscope's display, and perform the V_{TOP} measurement. Take the V_{TOP} measurement result as the $V_{IHdiff(DC)}$ value.
5 Continue the previous step for the rest of the valid Strobe positive pulse in the burst.
6 Determine the worst result from the set of $V_{IHdiff(DC)}$ measured.

$V_{IHdiff(DC)}$ Test for Clock - Test Method of Implementation

$V_{IHdiff(DC)}$ - Differential DC Input Logic High Voltage Test for Clock.

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{IHdiff(DC)}$ value as specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance limit is set to 0.6V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IH(DC)}$ which directly affects the conformance limit is set to 0.8V for Speed Grades from LPDDR2- 200 to LPDDR2- 400 or 0.73V for Speed Grades from LPDDR2- 466 to LPDDR2- 1066 for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of $V_{IH(DC)}$.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: No

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Clock Signals

Test Definition Notes from the Specification

Table 102 LPDDR2 Differential AC and DC Input Level

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{IHdiff(DC)}$	Differential input HIGH DC	2 x ($V_{IH(DC)}$ - V_{REF})	Note 3	2 x ($V_{IH(DC)}$ - V_{REF})	Note 3	V	1

Test References

See Table 77 - Differential AC and DC Input Level in the *JESD209-2B*.

PASS Condition

The worst measured $V_{IHdiff(DC)}$ shall be within the specification limit.

Measurement Algorithm

1 Pre-condition the oscilloscope.
2 Trigger on a rising edge of the clock signal under test.
3 Find all valid Clock positive pulses in the triggered waveform. A valid Clock positive pulse starts at the 0V crossing on a valid Clock rising edge (see notes on threshold) and ends at the 0V crossing on the following valid Clock falling edge (see notes on threshold).
4 For the first valid Clock positive pulse, zoom in on the pulse so that it appears on the oscilloscope's display, and perform the V_{TOP} measurement. Take the V_{TOP} measurement result as the $V_{IHdiff(DC)}$ value.
5 Continue the previous step for the rest of the valid Clock positive pulses.
6 Determine the worst result from the set of $V_{IHdiff(DC)}$ measured.

$V_{ILdiff(AC)}$ Test for DQS - Test Method of Implementation

$V_{ILdiff(AC)}$ - Differential AC Input Logic Low Voltage Test for DQS.

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{ILdiff(AC)}$ value as specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance limit is set to 0.6V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IL(AC)}$ which directly affects the conformance limit is set to 0.3V for Speed Grades from LPDDR2- 200 to LPDDR2- 400 or 0.38V for Speed Grades from LPDDR2- 466 to LPDDR2- 1066 for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of $V_{IH(DC)}$.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 103 LPDDR2 Differential AC and DC Input Level

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{ILdiff(AC)}$	Differential input Low AC	Note 3	$2 \times (V_{REF} - V_{IL(AC)})$	Note 3	$2 \times (V_{REF} - V_{IL(AC)})$	V	2

Test References

See Table 77 - Differential AC and DC Input Level in the *JESD209-2B*.

PASS Condition

The worst measured $V_{ILdiff(AC)}$ shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal. (See notes on DDR read/write separation).
2 Take the first valid WRITE burst found.
3 Find all valid Strobe negative pulses in this burst. A valid Strobe negative pulse starts at the 0V crossing on a valid Strobe falling edge (see notes on threshold) and ends at the 0V crossing on the following valid Strobe rising edge (see notes on threshold).
4 For the first valid Strobe negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display, and perform the V_{BASE} measurement. Take the V_{BASE} measurement result as the $V_{ILdiff(AC)}$ value.
5 Continue the previous step for the rest of the valid Strobe negative pulses in the burst.
6 Determine the worst result from the set of $V_{ILdiff(AC)}$ measured.

$V_{ILdiff(AC)}$ Test for Clock - Test Method of Implementation

$V_{ILdiff(AC)}$ - Differential AC Input Logic Low Voltage Test for Clock.

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{ILdiff(AC)}$ value as specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance limit is set to 0.6V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IL(AC)}$ which directly affects the conformance limit is set to 0.3V for Speed Grades from LPDDR2- 200 to LPDDR2- 400 or 0.38V for Speed Grades from LPDDR2- 466 to LPDDR2- 1066 for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of $V_{IH(DC)}$.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: No

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Clock Signals

Test Definition Notes from the Specification

Table 104 LPDDR2 Differential AC and DC Input Level

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{ILdiff(AC)}$	Differential input Low AC	Note 3	2 x (V_{REF} - $V_{IL(AC)}$)	Note 3	2 x (V_{REF} - $V_{IL(AC)}$)	V	2

Test References

See Table 77 - Differential AC and DC Input Level in the *JESD209-2B*.

PASS Condition

The worst measured $V_{ILdiff(AC)}$ shall be within the specification limit.

Measurement Algorithm

1 Pre-condition the oscilloscope.
2 Triggered on a rising edge of the clock signal under test.
3 Find all valid Clock negative pulses in the triggered waveform. A valid Clock negative pulse starts at the 0V crossing on a valid Clock falling edge (see notes on threshold) and ends at the 0V crossing on the following valid Clock rising edge (see notes on threshold).
4 For the first valid Clock negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display, and perform the V_{BASE} measurement. Take the V_{BASE} measurement result as the $V_{ILdiff(AC)}$ value.
5 Continue the previous step for the rest of the valid Clock negative pulses.
6 Determine the worst result from the set of $V_{ILdiff(AC)}$ measured.

$V_{ILdiff(DC)}$ Test for DQS - Test Method of Implementation

$V_{ILdiff(DC)}$ - Differential DC Input Logic Low Voltage Test for DQS.

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{ILdiff(DC)}$ value as specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance limit is set to 0.6V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IL(DC)}$ which directly affects the conformance limit is set to 0.4V for Speed Grades from LPDDR2- 200 to LPDDR2- 400 or 0.47V for Speed Grades from LPDDR2- 466 to LPDDR2- 1066 for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of $V_{IH(DC)}$.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 105 LPDDR2 Differential AC and DC Input Level

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{ILdiff(DC)}$	Differential input Low DC	Note 3	2 x (V_{REF} - $V_{IL(DC)}$)	Note 3	2 x (V_{REF} - $V_{IL(DC)}$)	V	1

Test References

See Table 77 - Differential AC and DC Input Level in the *JESD209-2B*.

PASS Condition

The worst measured $V_{ILdiff(DC)}$ shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal. (See notes on DDR read/write separation).
2 Take the first valid WRITE burst found.
3 Find all valid Strobe negative pulses in this burst. A valid Strobe negative pulse starts at the 0V crossing on a valid Strobe falling edge (see notes on threshold) and ends at the 0V crossing on the following valid Strobe rising edge (see notes on threshold).
4 For the first valid Strobe negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display, and perform the V_{BASE} measurement. Take the V_{BASE} measurement result as the $V_{ILdiff(DC)}$ value.
5 Continue the previous step for the rest of the valid Strobe negative pulses in the burst.
6 Determine the worst result from the set of $V_{ILdiff(DC)}$ measured.

$V_{ILdiff(DC)}$ Test for Clock - Test Method of Implementation

$V_{ILdiff(DC)}$ - Differential DC Input Logic Low Voltage Test for Clock.

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{ILdiff(DC)}$ value as specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance limit is set to 0.6V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of $V_{IL(DC)}$ which directly affects the conformance limit is set to 0.4V for Speed Grades from LPDDR2- 200 to LPDDR2- 400 or 0.47V for Speed Grades from LPDDR2- 466 to LPDDR2- 1066 for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of $V_{IH(DC)}$.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Required Read/Write separation: No

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Clock Signals

Test Definition Notes from the Specification

Table 106 LPDDR2 Differential AC and DC Input Level

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Units	Notes
		Min	Max	Min	Max		
$V_{ILdiff(DC)}$	Differential input Low DC	Note 3	2 x (V_{REF} - $V_{IL(DC)}$)	Note 3	2 x (V_{REF} - $V_{IL(DC)}$)	V	1

Test References

See Table 77 - Differential AC and DC Input Level in the *JESD209-2B*.

PASS Condition

The worst measured $V_{ILdiff(DC)}$ shall be within the specification limit.

Measurement Algorithm

1 Pre-condition the oscilloscope.
2 Triggered on a rising edge of the clock signal under test.
3 Find all valid Clock negative pulses in the triggered waveform. A valid Clock negative pulse starts at the 0Volt crossing on a valid Clock falling edge (see notes on threshold) and ends at the 0V crossing on the following valid Clock rising edge (see notes on threshold).
4 For the first valid Clock negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display, and perform the V_{BASE} measurement. Take the V_{BASE} measurement result as the $V_{ILdiff(DC)}$ value.
5 Continue the previous step for the rest of the valid Clock negative pulses.
6 Determine the worst result from the set of $V_{ILdiff(DC)}$ measured.

11 Differential Signal AC Output Parameters Tests

This section provides the Methods of Implementation (MOIs) for Differential Signals AC Output tests using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

Probing for Differential Signals AC Output Parameters Tests

When performing Differential Signals AC Input Parameters tests, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections. The connection for Differential Signals AC Output Parameters tests may look similar to below diagram. Refer to the Connection tab in DDR2(+LP) Electrical Performance Compliance application for the exact number of probe connections.

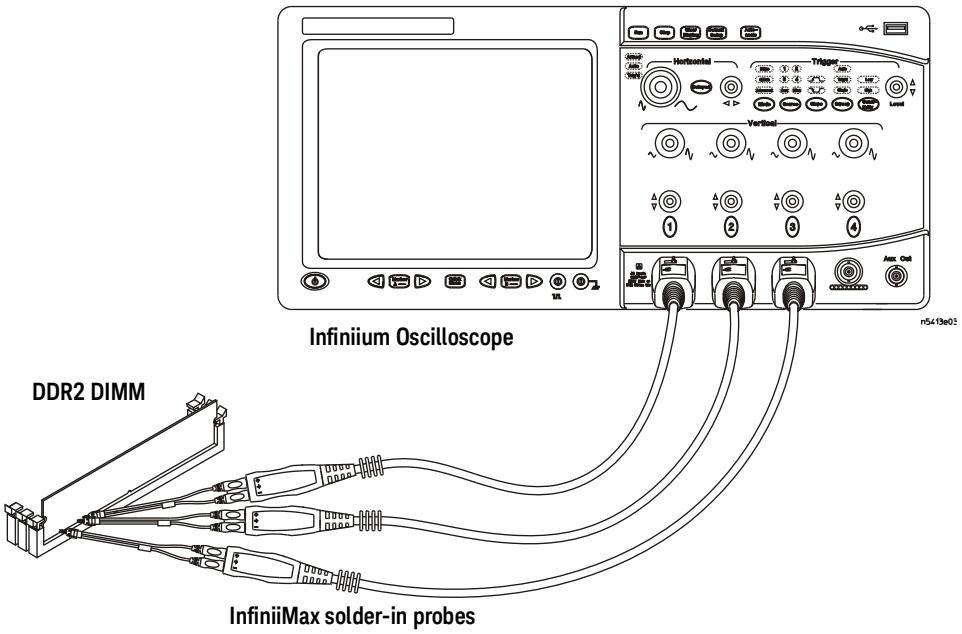


Figure 22 Probing for Differential Signals AC Output Parameters Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channels shown in Figure 22 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in “Starting the DDR2(+LP) Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR2/LPDDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2/LPDDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2/LPDDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2/LPDDR2 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Differential Signals AC Output Parameters Tests that, you can select any LPDDR2 speed grade within the selection. To see the LPDDR2 Speed Grades, check the Low Power box.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

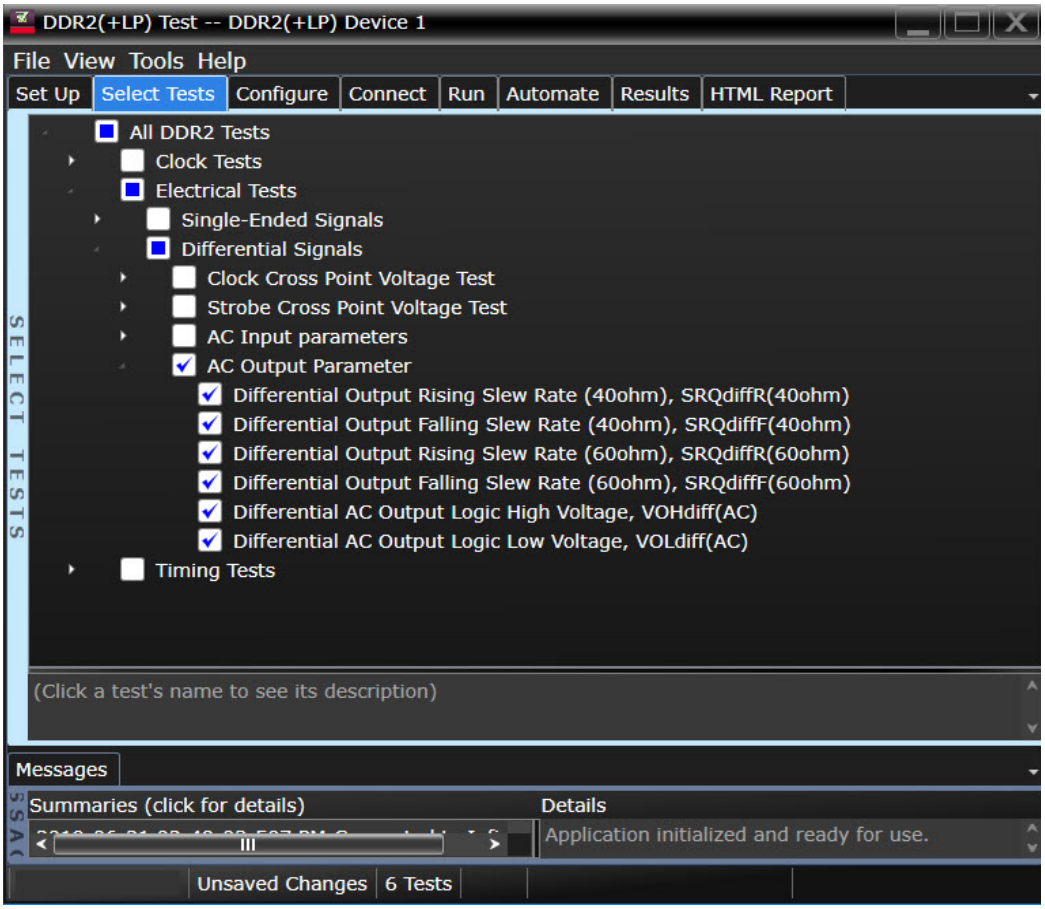


Figure 23 Selecting Differential Signals AC Output Parameters Tests

9 Follow the DDR2(+LP) Test application's task flow to set up the configuration options, run the tests and view the tests results.

V_{OX} , AC Differential Output Cross Point Voltage - Test Method of Implementation

The purpose of this test is to verify the crossing point of the output differential test signals pair is within the conformance limits of the $V_{OX(AC)}$ as specified in the JEDEC specification.

The value of V_{DDQ} which directly affects the conformance lower limit is set to 1.8V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on the different values of V_{DDQ}.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - any signal of interest, as defined above
- Supporting Pin - a corresponding DQ signal

Test Definition Notes from the Specification

Table 107 Differential AC Output Parameters

Symbol	Parameter	Min	Max	Units	Notes
$V_{OX(AC)}$	AC differential cross point voltage	0.5 * V_{DDQ} - 0.125	0.5 * V_{DDQ} + 0.125	V	1

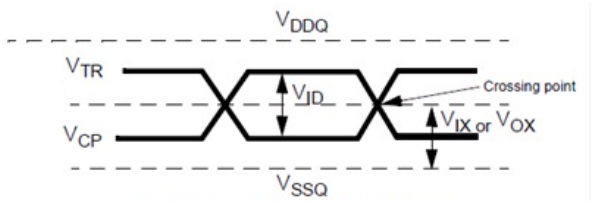
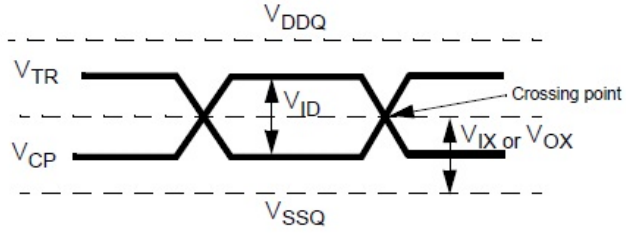


Figure 74 — Differential signal levels

Table 108 Differential AC Output Parameters (DDR2-1066)

Symbol	Parameter	Min	Max	Units	Notes
$V_{OX(AC)}$	AC differential cross point voltage	0.5 * V_{DDQ} - 0.125	0.5 * V_{DDQ} + 0.125	V	1



Test References

See Table 23 - Differential AC Output Logic Level in the *JEDEC Standard JESD79-2E* and Table 23 - Differential AC Output Logic Level in the *JESD208*.

PASS Condition

The measured crossing point value for the differential test signals pair should be within the conformance limits of $V_{OX(AC)}$ value.

Measurement Algorithm

1 Obtain sample or acquire data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the two source inputs.
3 Split read and write bursts of the acquired signal.
4 Take the first valid READ burst found.
5 Find all differential DQS crossings that cross 0V.
6 Use V_{TIME} to get the actual crossing point voltage value by using the timestamp obtained.
7 Determine the worst result from the set of $V_{OX(AC)}$ measured.

SRQdiffR (40ohm) - Test Method of Implementation

AC Output Parameter Tests can be divided into six sub tests:

- SRQdiffR(40ohm) test
- SRQdiffF(40ohm) test
- SRQdiffR(60ohm) test
- SRQdiffF(60ohm) test
- $V_{OHdiff(AC)}$ test
- $V_{OLdiff(AC)}$ test

SRQdiffR (40ohm) - Differential Output Rising Slew Rate (40ohms).

The purpose of this test is to verify that the differential rising slew rate value of the test signal must be within the conformance limit of the SRQ_{diff} value as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 109 LPDDR2 Output Slew Rate (differential)

Parameter	Symbol	LPDDR2-1066 to LPDDR2-200		Units
		Min	Max	
Differential Output Slew Rate (RON = 40ohms +/- 30%)	SRQ_{diff}	3.0	7.0	V/ns

Test References

See Table 87 - Output Slew Rate (differential) in the *JESD209-2B*.

PASS Condition

The worst measured SRQdiffR shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid Strobe rising edges in this burst. A valid Strobe rising edge starts at the $V_{OLdiff(AC)}$ crossing and ends at the following $V_{OHdiff(AC)}$ crossing.
4 For all valid Strobe rising edges, find the transition time, TR, which is the time that starts at the $V_{OLdiff(AC)}$ crossing and ends at the following $V_{OHdiff(AC)}$ crossing. Then calculate SRQdiffR = $[V_{OHdiff(AC)} - V_{OLdiff(AC)}]/TR$.
5 Determine the worst result from the set of SRQdiffR measured.

SRQdiffF (40ohm) - Test Method of Implementation

SRQdiffF (40ohm) - Differential Output Falling Slew Rate (40ohms).

The purpose of this test is to verify that the differential falling slew rate value of the test signal must be within the conformance limit of the SRQ_{diff} value as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 110 LPDDR2 Output Slew Rate (differential)

Parameter	Symbol	LPDDR2-1066 to LPDDR2-200		Units
		Min	Max	
Differential Output Slew Rate (RON = 40ohms +/- 30%)	SRQ_{diff}	3.0	7.0	V/ns

Test References

See Table 87 - Output Slew Rate (differential) in the *JESD209-2B*.

PASS Condition

The worst measured SRQdiffF shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid Strobe falling edges in this burst. A valid Strobe falling edge starts at the $V_{OHdiff(AC)}$ crossing and ends at the following $V_{OLdiff(AC)}$ crossing.

4 For all valid Strobe falling edges, find the transition time, TR, which is the time that starts at the $V_{OHdiff(AC)}$ crossing and ends at the following $V_{OLdiff(AC)}$ crossing. Then calculate SRQdiffF = $[V_{OHdiff(AC)} - V_{OLdiff(AC)}]/TR$.

5 Determine the worst result from the set of SRQdiffF measured.

SRQdiffR (60ohm) - Test Method of Implementation

SRQdiffR (60ohm) - Differential Output Rising Slew Rate (60ohms).

The purpose of this test is to verify that the differential rising slew rate value of the test signal must be within the conformance limit of the SRQ_{diff} value as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 111 LPDDR2 Output Slew Rate (differential)

Parameter	Symbol	LPDDR2-1066 to LPDDR2-200		Units
		Min	Max	
Differential Output Slew Rate (RON = 60ohms +/- 30%)	SRQ_{diff}	2.0	6.0	V/ns

Test References

See Table 87 - Output Slew Rate (differential) in the *JESD209-2B*.

PASS Condition

The worst measured SRQdiffR shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid Strobe rising edges in this burst. A valid Strobe rising edge starts at the $V_{OLdiff(AC)}$ crossing and ends at the following $V_{OHdiff(AC)}$ crossing.

4 For all valid Strobe rising edges, find the transition time, TR, which is the time that starts at the $V_{OLdiff(AC)}$ crossing and ends at the following $V_{OHdiff(AC)}$ crossing. Then calculate $SRQdiffR = [V_{OHdiff(AC)} - V_{OLdiff(AC)}]/TR$.

5 Determine the worst result from the set of SRQdiffR measured.

SRQdiffF (60ohm) - Test Method of Implementation

SRQdiffF (60ohm) - Differential Output Falling Slew Rate (60ohms).

The purpose of this test is to verify that the differential falling slew rate value of the test signal must be within the conformance limit of the SRQ_{diff} value as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 112 LPDDR2 Output Slew Rate (differential)

Parameter	Symbol	LPDDR2-1066 to LPDDR2-200		Units
		Min	Max	
Differential Output Slew Rate (RON = 60ohms +/- 30%)	SRQ_{diff}	2.0	6.0	V/ns

Test References

See Table 87 - Output Slew Rate (differential) in the *JESD209-2B*.

PASS Condition

The worst measured SRQdiffF shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write bursts of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid Strobe falling edges in this burst. A valid Strobe falling edge starts at the $V_{OHdiff(AC)}$ crossing and ends at the following $V_{OLdiff(AC)}$ crossing.

4 For all valid Strobe falling edges, find the transition time, TR, which is the time that starts at the $V_{OHdiff(AC)}$ crossing and ends at the following $V_{OLdiff(AC)}$ crossing. Then calculate SRQdiffF = $[V_{OHdiff(AC)} - V_{OLdiff(AC)}]/TR$.

5 Determine the worst result from the set of SRQdiffF measured.

$V_{OHdiff(AC)}$ - Test Method of Implementation

$V_{OHdiff(AC)}$ - Differential AC Output Logic High Voltage.

The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{OHdiff(AC)}$ value as specified in the JEDEC specification.

The value of V_{DDQ} (which directly affects the conformance limit) is set to 1.2V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DDQ}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 113 LPDDR2 Differential AC and DC Output Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200	Units	Notes
$V_{OHdiff(AC)}$	AC differential Output high measurement level (for output SR)	0.25 x V_{DDQ}	V	

Test References

See Table 83 - Differential AC and DC Output Levels in the *JESD209-2B*.

PASS Condition

The worst measured $V_{OHdiff(AC)}$ shall be within the specification limit.

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid Strobe positive pulses in this burst. A valid Strobe positive pulse starts at the 0V crossing on a valid Strobe rising edge and ends at the 0V crossing on the following valid Strobe falling edge.
4. For the first valid positive pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the V_{TOP} measurement. Take the V_{TOP} measurement result as the $V_{OHdiff(AC)}$ value.
5. Continue the previous step for the rest of the valid Strobe positive pulses that were found in the burst.
6. Determine the worst result from the set of $V_{OHdiff(AC)}$ measured.

$V_{OLdiff(AC)}$ - Test Method of Implementation

$V_{OLdiff(AC)}$ - Differential AC Output Logic Low Voltage.

The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window must be within the conformance limit of the $V_{OLdiff(AC)}$ value as specified in the JEDEC specification.

The value of V_{DDQ} (which directly affects the conformance limit) is set to 1.2V for the compliance limit set used. You may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DDQ}.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supporting Pin - Data Signals

Test Definition Notes from the Specification

Table 114 LPDDR2 Differential AC and DC Output Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200	Units	Notes
$V_{OLdiff(AC)}$	AC differential Output low measurement level (for output SR)	-0.25 x V_{DDQ}	V	

Test References

See Table 83 - Differential AC and DC Output Levels in the *JESD209-2B*.

PASS Condition

The worst measured $V_{OLdiff(AC)}$ shall be within the specification limit.

Measurement Algorithm

1. Acquire and split read and write bursts of the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid Strobe negative pulses in this burst. A valid Strobe negative pulse starts at the 0V crossing on a valid Strobe falling edge and ends at the 0V crossing on the following valid Strobe rising edge.
4. For the first valid negative pulse, zoom in on the pulse so that it appears on the oscilloscope's display and perform the V_{BASE} measurement. Take the V_{BASE} measurement result as the $V_{OLdiff(AC)}$ value.
5. Continue the previous step for the rest of the valid Strobe negative pulses that were found in the burst.
6. Determine the worst result from the set of $V_{OLdiff(AC)}$ measured.

12 Differential Signal Clock Cross Point Voltage Tests

This section provides the Methods of Implementation (MOIs) for Differential Signals Clock Cross Point Voltage tests using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

Probing for Differential Signals Clock Cross Point Voltage Tests

When performing Differential Signals Clock Cross Point Voltage tests, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections. The connection for Differential Signals Clock Cross Point Voltage tests may look similar to below diagram. Refer to the Connection tab in DDR2(+LP) Electrical Performance Compliance application for the exact number of probe connections.

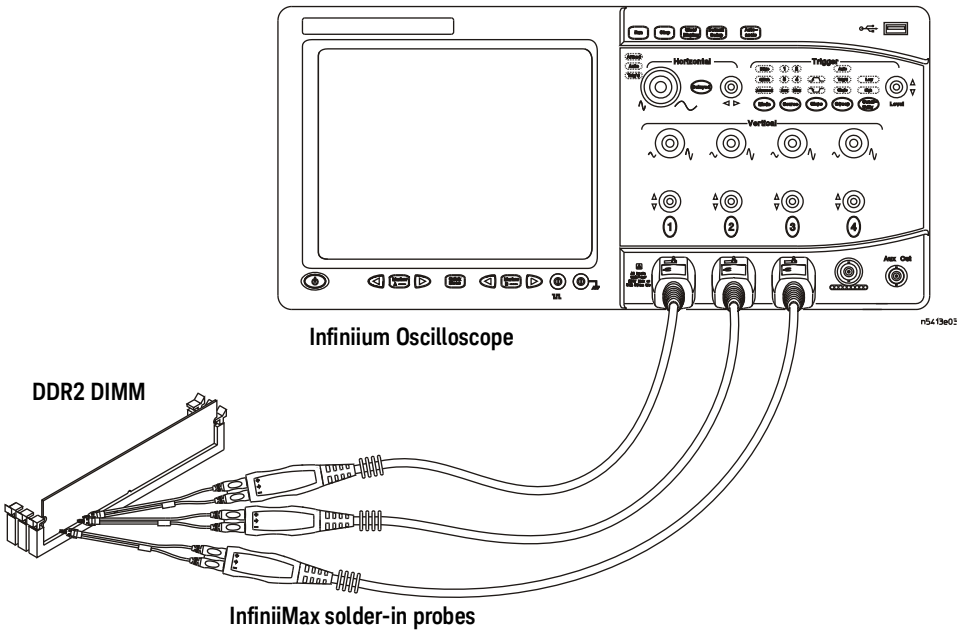


Figure 24 Probing for Differential Signals AC Output Parameters Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channels shown in Figure 24 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in “Starting the DDR2(+LP) Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR2/LPDDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2/LPDDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2/LPDDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2/LPDDR2 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Differential Signals Clock Cross Point Voltage Tests, you can select any LPDDR2 speed grade within the selection. To see the LPDDR2 Speed Grades, check the Low Power box.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

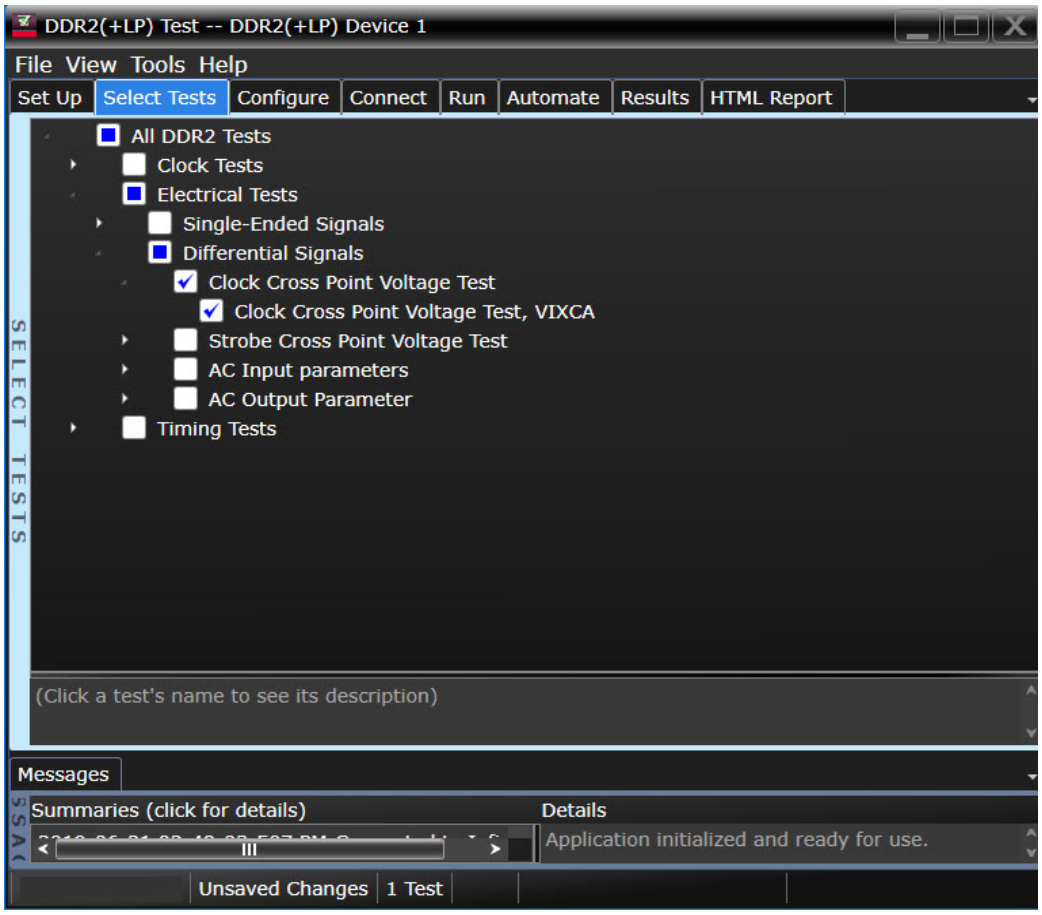


Figure 25 Selecting Differential Signals Clock Cross Point Voltage Tests

Follow the DDR2(+LP) Test application's task flow to set up the configuration options, run the tests and view the tests results.

V_{IXCA}, Clock Cross Point Voltage - Test Method of Implementation

The purpose of this test is to verify the crossing point voltage value of the input differential Clock signals pair is within the conformance limits of the V_{IXCA} as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: Write

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Clock Signals

Test Definition Notes from the Specification

Table 115 Cross Point Voltage for Differential Input Signals (CK, DQS)

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200		Units	Notes
		Min	Max		
V_{IXCA}	Differential input cross point voltage relative to V_{DDCA}/2 for CK_t, CK_c	-120	120	mV	1, 2

Test References

See Table 80 - Cross Point Voltage for Differential Input Signals (CK, DQS) in the *JESD209-2B*.

PASS Condition

The measured crossing point value for the differential Clock signals pair should be within the conformance limits of V_{IXCA} value.

Measurement Algorithm

1 Obtain sample or acquire data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the two source inputs.
3 Find the first 10 differential CLK crossing that cross 0V.
4 Use V_{TIME} to get the actual crossing point voltage value by using the timestamp obtained.
5 Determine the worst result from the set of V_{IXCA} measured.

13 Differential Signals Strobe Cross Point Voltage Tests

This section provides the Methods of Implementation (MOIs) for Differential Signals Strobe Cross Point Voltage tests using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

Probing for Differential Signals Strobe Cross Point Voltage Tests

When performing Differential Signals Strobe Cross Point Voltage tests, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections. The connection for Differential Signals Strobe Cross Point Voltage tests may look similar to below diagram. Refer to the Connection tab in DDR2(+LP) Electrical Performance Compliance application for the exact number of probe connections.

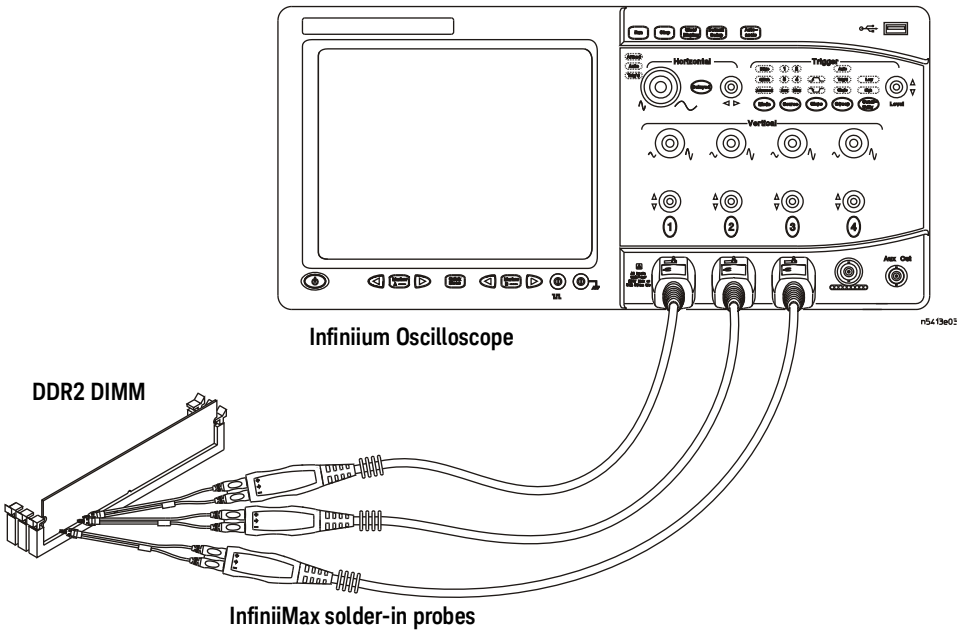


Figure 26 Probing for Differential Signals AC Output Parameters Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channels shown in Figure 26 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in “Starting the DDR2(+LP) Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR2/LPDDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2/LPDDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2/LPDDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2/LPDDR2 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Differential Signals Strobe Cross Point Voltage tests, you can select any LPDDR2 speed grade within the selection. To see the LPDDR2 Speed Grades, check the Low Power box.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

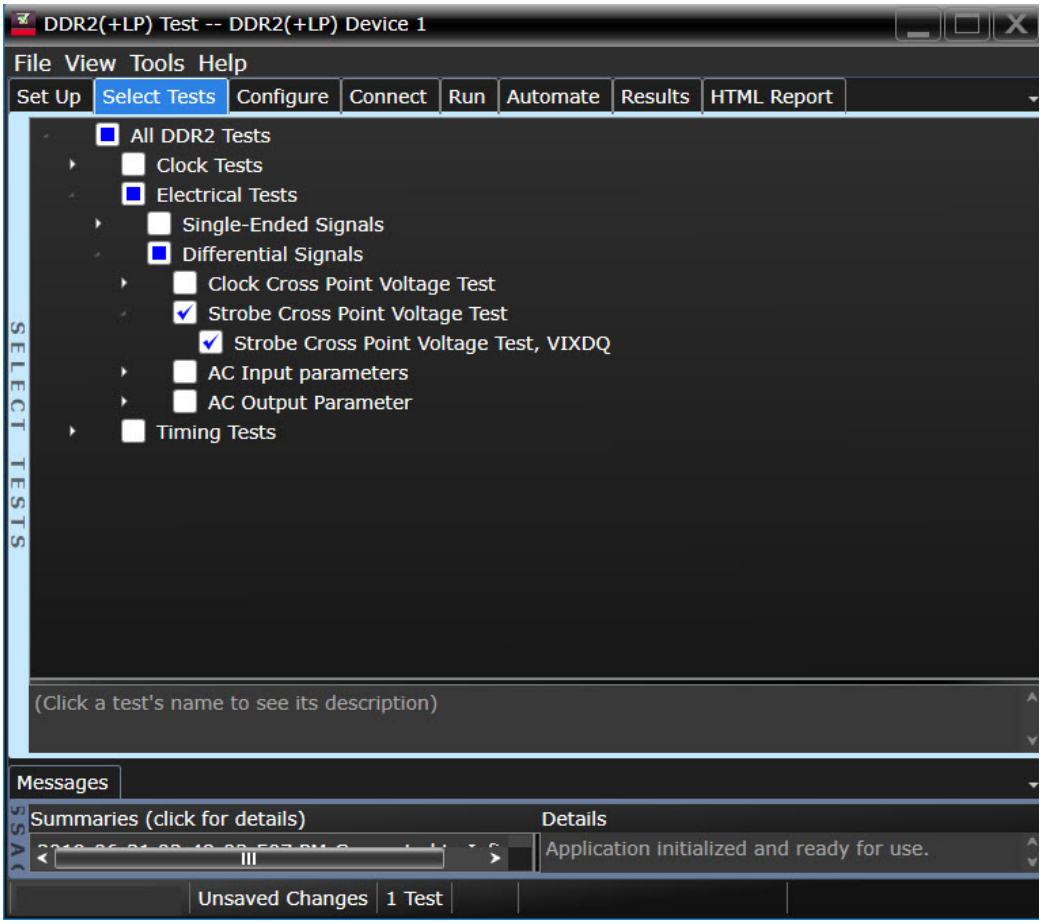


Figure 27 Selecting Differential Signals Strobe Cross Point Voltage Tests

Follow the DDR2(+LP) Test application's task flow to set up the configuration options, run the tests and view the tests results.

V_{IXDQ}, Strobe Cross Point Voltage - Test Method of Implementation

The purpose of this test is to verify the crossing point voltage value of the input differential Strobe signals pair is within the conformance limits of the V_{IXDQ} as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: Write

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - Data Strobe Signals
- Supported Pin - Data Signals

Test Definition Notes from the Specification

Table 116 Cross Point Voltage for Differential Input Signals (CK, DQS)

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200		Units	Notes
		Min	Max		
V_{IXDQ}	Differential input cross point voltage relative to $V_{DDCA}/2$ for CK_t, CK_c	-120	120	mV	1, 2

Test References

See Table 80 - Cross Point Voltage for Differential Input Signals (CK, DQS) in the *JESD209-2B*.

PASS Condition

The measured crossing point value for the differential Clock signals pair should be within the conformance limits of V_{IXDQ} value.

Measurement Algorithm

1 Obtain sample or acquire data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the two source inputs.
3 Split read and write bursts of the acquired signal.
4 Take the first valid WRITE burst found.
5 Find all differential DQS crossings that cross 0V.
6 Use V_{TIME} to get the actual crossing point voltage value by using the timestamp obtained.
7 Determine the worst result from the set of V_{IXDQ} measured.

14 Clock Timing (CT) Tests

This section provides the Methods of Implementation (MOIs) for Clock Timing tests using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Clock Timing Tests

When performing the Clock Timing tests, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections. The connection for Clock Timing tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

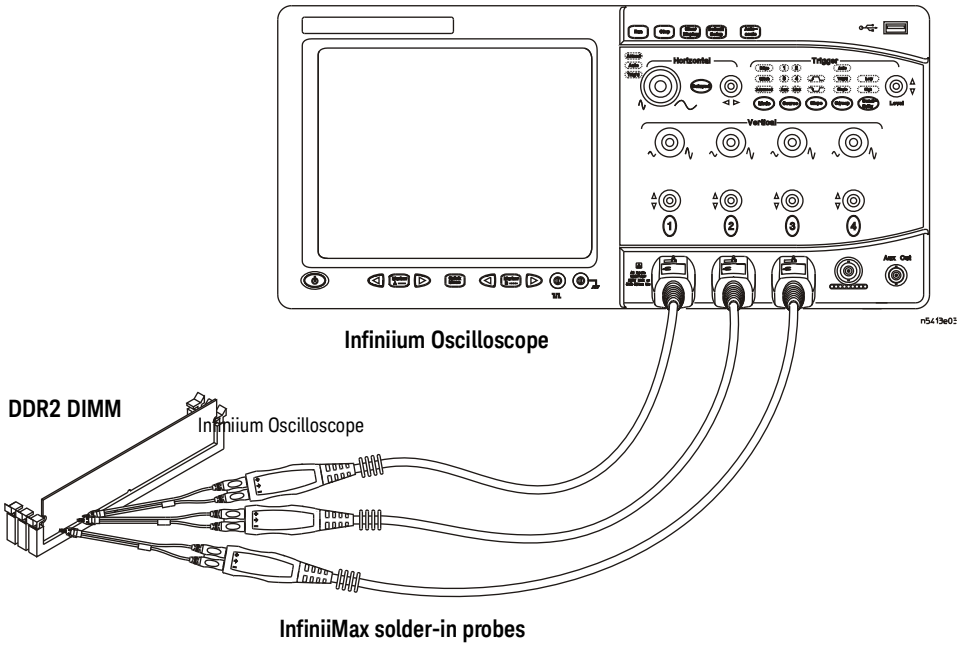


Figure 28 Probing for Clock Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channels shown in Figure 28 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in "Starting the DDR2(+LP) Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Clock Timing Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800, DDR2-1066.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

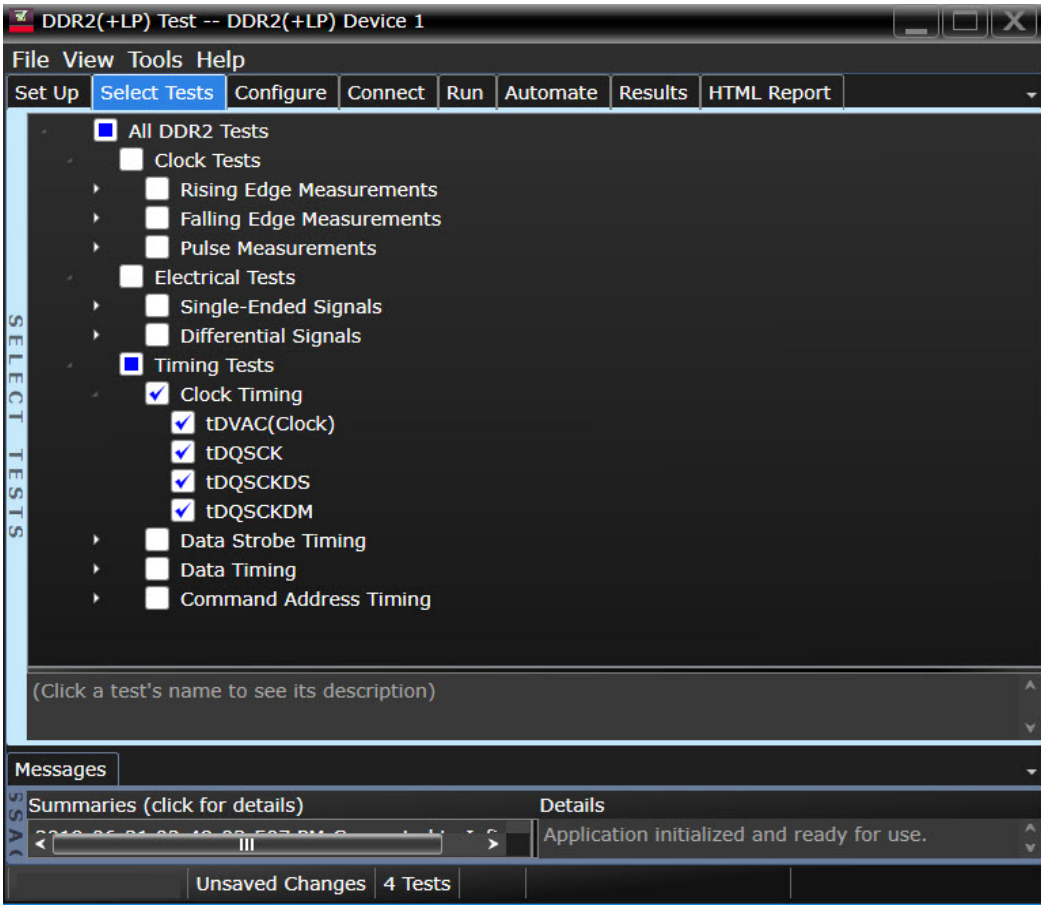


Figure 29 Selecting Clock Timing Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options, run the tests and view the tests results.

tAC, DQ Output Access Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time interval from data output (DQ rising and falling edge) access time to the nearest rising or falling edge of the clock must be within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: READ

Mode Supported: DDR2

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory.)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 117 Timing Parameters by Speed Grade (DDR2-400 and DDR-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ output access time from CK/$\overline{CK}$	tAC	-600	+600	-500	+500	ps	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ output access time from CK/$\overline{CK}$	tAC	-450	450	-400	400	ps	40

Table 118 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQ output access time from CK/$\overline{CK}$	tAC	-350	350	ps	35

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval between the data output (DQ rising and falling edge) and rising/falling edge of the clock should be within the specification limits.

Measurement Algorithm

1 Pre-condition the oscilloscope setting.
2 Acquire and split read and write burst of the acquired signal.
3 Take the first valid READ burst found.
4 Find all valid rising and falling DQ crossings at Vref in the said burst.
5 For all DQ crossings found, locate the nearest rising Clock crossing at 0V.
6 Take the time difference from DQ crossing to the corresponding Clock crossing as the tAC.
7 Determine the worst result from the set of tAC measurements.
8 Compare the test result against the compliance test limit.

tDQSCK, DQS Output Access Time from CK/CK #- Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS rising and falling edge) access time to the nearest rising or falling edge of the clock is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: READ

Mode Supported: DDR2, for LPDDR2 refer to tDQSCK Test (Low Power)

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory.)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 119 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS output access time from CK/$\overline{CK}$	tDQSCK	-500	+500	-450	+450	ps	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS output access time from CK/$\overline{CK}$	tDQSCK	-400	400	-350	350	ps	40

Table 120 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS output access time from CK/$\overline{CK}$	tDQSCK	-325	325	ps	35

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured time interval between the data strobe access output and rising edge of the clock should be within the specification limit.

Measurement Algorithm

1 Pre-condition the oscilloscope setting.
2 Acquire and split read and write burst of the acquired signal.
3 Take the first valid READ burst found.
4 Find all valid rising and falling DQS crossings at Vref in the said burst.
5 For all DQS crossings found, locate the nearest rising Clock crossing at 0V.
6 Take the time difference from DQS crossing to the corresponding Clock crossing as the tDQSCK
7 Determine the worst result from the set of tDQSCK measurements.
8 Compare the test result against the compliance test limit.

tDQSCK (Low Power), DQS Output Access Time from CK_t,CK_c - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output's (DQS rising edge) first rising edge to the rising edge of the clock that is before the nearest rising edge of the clock delayed tDQSCK Delay cycles, is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: READ

Mode Supported: LPDDR2, for DDR refer to tDQSCK Test.

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory.)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 121 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Read Parameters* [14]										
DQS output access time from CK_t/CK_c	tDQSCK	Min		2500										ps
		Max		5500										

Test References

See Table 103- LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The measured tDQSCK should be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all DQS middle cross points at V_{REF} in the burst.
4 Find all Clock middle cross points at V_{REF} in the burst.
5 Find the first DQS rising edge in the READ burst by searching for the earliest rising cross point among all the DQS middle cross points. Take the first DQS rising edge as the tDQSCK strobe point.
6 Find the closest Clock-DQS (the Clock rising middle crossing point that is closest to the first DQS rising edge).
7 Find the tDQSCK clock point. It is the Clock middle crossing point right before the closest Clock-DQS at tDQSCK Delay (cycle). By default, tDQSCK Delay is one cycle. For example, if tDQSCK Delay = 1, then the tDQSCK clock point is the Clock middle crossing point right before the closest Clock-DQS. If tDQSCK Delay = 3, then the tDQSCK clock point is the Clock middle crossing point three clock cycles before the closest Clock-DQS. tDQSCK Delay is configurable in the configuration page.
8 Compare the tDQSCK strobe point to the tDQSCK clock point as the test result. Mathematically, test result = tDQSCK strobe point - tDQSCK clock point.
9 Display the test result by going to the measurement location on the waveform and locate the marker to tDQSCK strobe point and tDQSCK clock point.
10 Compare the test result against the compliance test limit.

tDVAC (Clock), Time Above $V_{IHdiff(AC)}$/Below $V_{ILdiff(AC)}$ - Test Method of Implementation

The purpose of this test is to verify that the time the clock signal is above $V_{IHdiff(AC)}$ and below $V_{ILdiff(AC)}$ must be within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: READ or WRITE

Mode Supported: LPDDR2

Signal(s) of Interest:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal, CK

Test Definition Notes from the Specification

Table 122 Allowed time before ringback (tDVAC) for CK_t-CK_s and DQS_t-DQS_c

Slew Rate	tDVAC [ps] @ | $V_{IH/Ldiff(AC)}$ | =440mV	tDVAC [ps] @ | $V_{IH/Ldiff(AC)}$ | =600mV
	Min	Min
>4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
<1.0	150	0

Test References

See Table 78- Allowed Time Before Ringback (tDVAC) for CK_t-CK_s and DQS_t-DQS_c in the *JESD209-2B*.

PASS Condition

The worst measured tDVAC(Clock) should be within the specification limit.

Measurement Algorithm

1 Pre-condition the oscilloscope setting.
2 Trigger on rising edge of the clock signal under test.
3 Find all crossings on rising/falling edges of the signal under test that cross $V_{ILdiff(AC)}$.
4 Find all crossings on rising/falling edges of the signal under test that cross $V_{IHdiff(AC)}$.
5 tDVAC(Clock) is the time interval starting from a rising $V_{IHdiff(AC)}$ crossing point and ending at the following falling $V_{IHdiff(AC)}$ crossing point.
6 tDVAC(Clock) is also the time interval starting from a falling $V_{ILdiff(AC)}$ crossing point and ending at the following rising $V_{ILdiff(AC)}$ crossing point.
7 Collect all tDVAC(Clock) results.
8 Determine the worst result from the set of tDVAC(Clock) measured.
9 Report the worst result from the set of tDVAC(Clock) measured. No compliance limit checking is performed for this test. You need to manually check the test status (pass/fail) of this test based upon the worst tDVAC(Clock) and slew rate reported.

tQHS, Data Hold Skew Factor- Test Method of Implementation

The purpose of this test is to verify that the time interval from the data output (DQ rising and falling edge) associated with a falling clock edge access time to the nearest falling edge of the clock must be within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Signal cycle of interest: READ

Mode Supported: LPDDR2

Signal(s) of Interest:

- Data Signals (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory.)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 123 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Read Parameters* 14										
Data hold skew factor	tQHS	Max		230	260	280	340	400	450	480	600	750	1000	ps

Test References

See Table 103- LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The worst measured tQHS should be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation).
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQ crossings at V_{REF} in the said burst. (See notes on threshold).
4 For all DQ crossings found, locate the nearest DQS crossing (Rising and falling). (See notes on threshold).
5 Take the time different from DQS crossing to DQ crossing as the tQHS.
6 Determine the worst result from the set of tQHS measured.

tDQSCKDS Test - DQSCK Delta Short Test- Test Method of Implementation

The purpose of this test is to verify that the DQSCK difference within 160 ns must be within the conformance limit as specified in the JEDEC specification. Each individual DQSCK is defined as time interval from data strobe output (DQS Rising) first rising edge of sub-burst to the rising edge of the clock that before tDQSCK delay (cycle) before nearest rising edge of the clock.

Signals of Interest

Signal cycle of interest: READ

Mode Supported: LPDDR2

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS

Test Definition Notes from the Specification

Table 124 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Read Parameters* 14										
DQSCK Delta Short	tDQSCKDS	Max		330	380	450	540	670	770	900	1080	1350	1800	ps

Test References

See Table 103- LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The worst measured tDQSCKDS should be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation).
2 Gather all tDQSCKm value in all valid READ bursts found in acquisition. Here is the sub-procedure to measure tDQSCKm value.
3 Evaluate all the sub-burst in the current burst by checking with Chip Select signal.
4 Find all DQS middle cross point at V_{REF} in the said burst. (See notes on threshold).
5 Find all Clock middle cross point at V_{REF} in the said burst. (See notes on threshold).
6 For sub-burst # 1, find the first DQS rising edge by search the earliest rising cross point among all found DQS middle cross point within current sub-burst. Take the found point (first DQS rising edge) as tDQSCKm strobe point.
7 Find the closest Clock - DQS : the Clock rising middle cross point that closest to first DQS rising edge.
8 Find tDQSCKm clock point which clock middle crosspoint that before closest Clock - DQS at tDQSCK Delay (cycle). By default, tDQSCK Delay is one cycle. In example, for tDQSCK Delay = 1, tDQSCKm clock point is clock middle crosspoint that previous of closest Clock - DQS. For tDQSCK Delay = 3, tDQSCKm clock point is clock middle crosspoint that three clock before with closest Clock - DQS. tDQSCK Delay is configurable in configuration page.
9 Compare these tDQSCKm strobe point to tDQSCKm clock point as a tDQSCKm value. Mathematically, **tDQSCKm = tDQSCKm strobe point - tDQSCKm clock point**.
10 Repeat procedure (**6**) to (**9**) for the rest of sub-burst in the current burst.
11 Perform checking of tDQSCKm #1 value with tDQSCKm #2 value. If the distance of clock reference of these two measured tDQSCKm is within 160 ns, then compare tDQSCKm #1 value and tDQSCKm #2 value. Mathematically, tDQSCKDS #1 = |tDQSCKm #1 - tDQSCKm #2|. Otherwise, if the distance of clock reference of these two measured tDQSCKm is more than 160ns, disregard to perform any comparison. Perform this procedure to all possible cross check of gathered tDQSCKm.
12 The largest tDQSCKDS value found will be taken as test result.
13 Display the test result by spot to measurement location on waveform and locate the marker to tDQSCKm strobe point and tDQSCKm clock point for pair of worst tDQSCKm.
14 Compare test result to compliance test limit.

tDQSCKDM Test - DQSCK Delta Medium Test- Test Method of Implementation

The purpose of this test is to verify that the DQSCK difference within 1.6 µs must be within the conformance limit as specified in the JEDEC specification. Each individual DQSCK is defined as time interval from data strobe output (DQS Rising) first rising edge of sub-burst to the rising edge of the clock that before tDQSCK delay (cycle) before nearest rising edge of the clock.

Signals of Interest

Signal cycle of interest: READ

Mode Supported: LPDDR2

Required Read/Write separation: Yes

Signal(s) of Interest:

- Data Strobe Signals (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory.)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS

Test Definition Notes from the Specification

Table 125 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*[5]	400	333	266*[5]	200*[5]	
				Read Parameters* [14]										
DQSCK Delta Medium	tDQSCKDM	Max		680	780	900	1050	1350	1550	1800	1900	2000	2100	ps

Test References

See Table 103- LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The worst measured tDQSCKDM should be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation).
2 Gather all tDQSCKm value in all valid READ bursts found in acquisition. Here is the sub-procedure to measure tDQSCKm value.
3 Evaluate all the sub-burst in the current burst by checking with Chip Select signal.
4 Find all DQS middle cross point at V_{REF} in the said burst. (See notes on threshold).
5 Find all Clock middle cross point at V_{REF} in the said burst. (See notes on threshold).
6 For sub-burst # 1, find the first DQS rising edge by search the earliest rising cross point among all found DQS middle cross point within current sub-burst. Take the found point (first DQS rising edge) as tDQSCKm strobe point.
7 Find the closest Clock - DQS : the Clock rising middle cross point that closest to first DQS rising edge.
8 Find tDQSCKm clock point which clock middle crosspoint that before closest Clock - DQS at tDQSCK Delay (cycle). By default, tDQSCK Delay is one cycle. In example, for tDQSCK Delay = 1, tDQSCKm clock point is clock middle crosspoint that previous of closest Clock - DQS. For tDQSCK Delay = 3, tDQSCKm clock point is clock middle crosspoint that three clock before with closest Clock - DQS. tDQSCK Delay is configurable in configuration page.
9 Compare these tDQSCKm strobe point to tDQSCKm clock point as a tDQSCKm value. Mathematically, **tDQSCKm = tDQSCKm strobe point - tDQSCKm clock point**.
10 Repeat procedure (**6**) to (**9**) for the rest of sub-burst in the current burst.
11 Perform checking of tDQSCKm #1 value with tDQSCKm #2 value. If the distance of clock reference of these two measured tDQSCKm is within 1.6 µs, then compare tDQSCKm #1 value and tDQSCKm #2 value. Mathematically, tDQSCKDS #1 = |tDQSCKm #1 - tDQSCKm #2|. Otherwise, if the distance of clock reference of these two measured tDQSCKm is more than 1.6 µs, disregard to perform any comparison. Perform this procedure to all possible cross check of gathered tDQSCKm.
12 The largest tDQSCKDM value found will be taken as test result.
13 Display the test result by spot to measurement location on waveform and locate the marker to tDQSCKm strobe point and tDQSCKm clock point for pair of worst tDQSCKm.
14 Compare test result to compliance test limit.

15 Data Strobe Timing (DST) Tests

This section provides the Methods of Implementation (MOIs) for Data Strobe Timing tests using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

NOTE **Both XYZ# and $\overline{XYZ}$ are referring to compliment. Thus, CK# is the same as $\overline{CK}$.**

Probing for Data Strobe Timing Tests

When performing the Data Strobe Timing tests, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections. The connection for Data Strobe Timing tests may look similar to the following diagram. Refer to the Connection tab in DDR2(+LP) Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

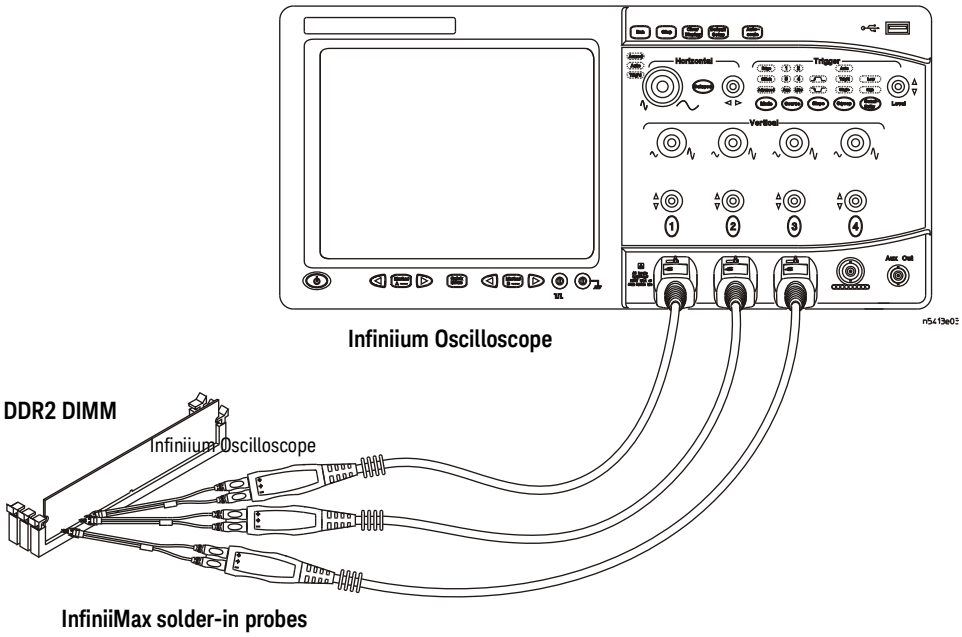


Figure 30 Probing for Data Strobe Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channels shown in Figure 30 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in “Starting the DDR2(+LP) Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR2/LPDDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2/LPDDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2(+LP) Test application, click the Set Up tab.

6 Select the Speed Grade options. For Clock Timing Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800, DDR2-1066. To access the LPDDR2 Speed Grade options (for tests that support LPDDR2), check the Low Power box.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

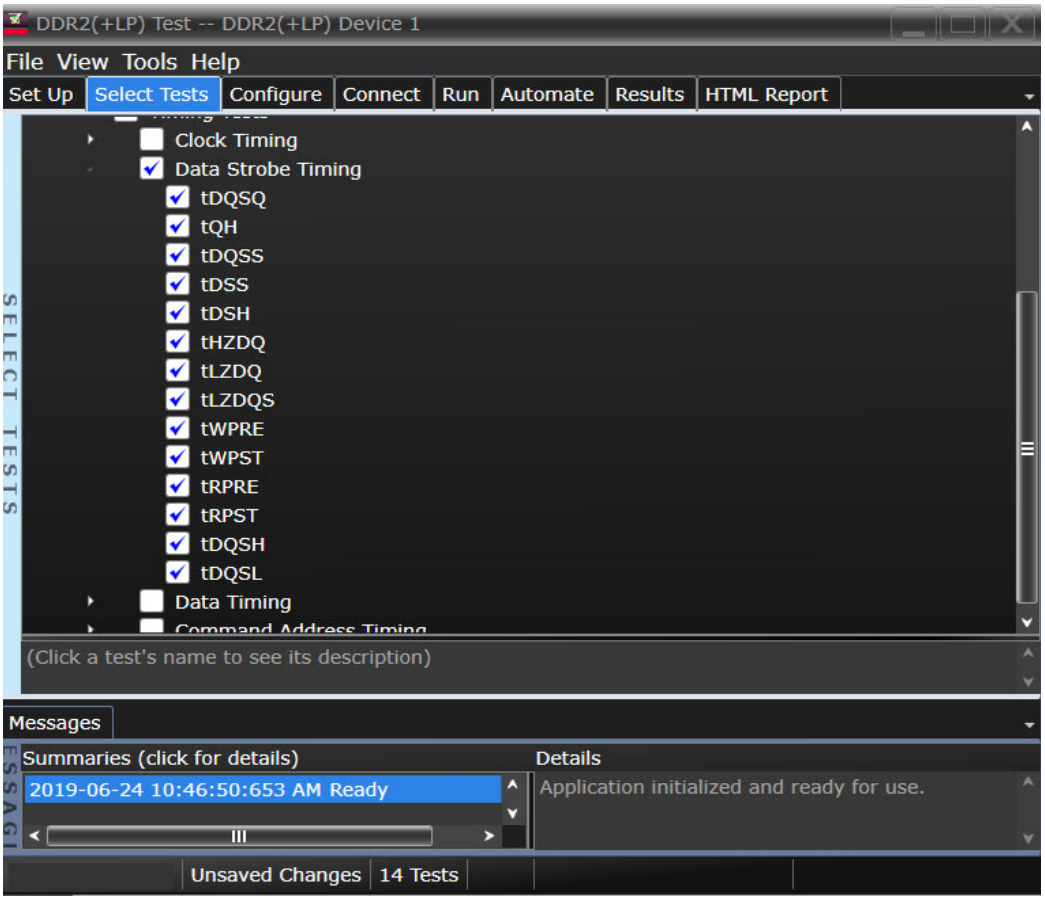


Figure 31 Selecting Data Strobe Timing Tests

9 Follow the DDR2(+LP) Test application's task flow to set up the configuration options, run the tests and view the tests results.

tHZ(DQ), DQ Out HIGH Impedance Time From CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQ is no longer driving (from HIGH state OR LOW state to the high impedance stage), to the clock signal crossing, is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, for LPDDR2 refer to the tHZ(DQ) Test (Low Power)

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 126 Timing Parameter By Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	ps	18

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	ps	18, 40

Table 127 Timing Parameter By Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	ps	15,35

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured tHZ(DQ) shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find tHZEndPoint(DQ) of the said burst.
4 Find the nearest rising Clock crossing.
5 tHZ(DQ) is the time interval of the rising Clock edge's crossing point to the tHZEndPoint.
6 Report tHZ(DQ).

NOTE Some designs do not have tri-state at V_{REF} (for example, 0.9V). This test is not guaranteed when this scenario happens, as there is no significant point of where the driver has been turned-off.

tLZ(DQS), DQS Low-Impedance Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS starts driving (from tri-state to HIGH/LOW state) to the clock signal crossing, is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, for LPDDR2 refer to tLZ(DQS) Test (Low Power)

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 128 Timing Parameter By Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS/($\overline{\text{DQS}}$) low-impedance time from CK/$\overline{\text{CK}}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	18

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS/($\overline{\text{DQS}}$) low-impedance time from CK/$\overline{\text{CK}}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	18, 40

Table 129 Timing Parameter By Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS/($\overline{\text{DQS}}$) low-impedance time from CK/$\overline{\text{CK}}$	tLZ(DQS)	tAC min	tAC max	ps	15, 35

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured tLZ(DQS) shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find tLZBeginPoint(DQS) of the said burst.
4 Find the nearest Clock rising edge.
5 tLZ(DQS) is the time interval of the rising Clock edge's crossing point to the tLZBeginPoint(DQS).
6 Report tLZ(DQS).

tLZ(DQ), DQ Low-Impedance Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQ starts driving (from high impedance state to HIGH/LOW state), to the clock signal crossing, is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, for LPDDR2 refer to tLZ(DQS) Test (Low Power)

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 130 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ LOW impedance time from CK/$\overline{CK}$	tLZ(DQ)	2 x tAC min	tAC max	2 x tAC min	tAC max	ps	18

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ LOW impedance time from CK/$\overline{CK}$	tLZ(DQ)	2 x tAC min	tAC max	2 x tAC min	tAC max	ps	18, 40

Table 131 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQ LOW impedance time from CK/$\overline{CK}$	tLZ(DQ)	2 x tAC min	tAC max	ps	15,35

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The measured tLZ(DQ) shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find tLZBeginPoint(DQ) of the said burst.
4 Find the nearest Clock rising edge.
5 tLZ(DQ) is the time interval of the rising Clock edge's crossing point to the tLZBeginPoint(DQ).
6 Report tLZ(DQ).

tDQSQ, DQS-DQ Skew for DQS and Associated DQ Signals - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS rising and falling edge) access time to the associated data (DQ rising and falling) signal is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2 and LPDDR2

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 132 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	350	x	300	ps	13

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	240	-	200	ps	13

Table 133 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	175	ps	11

Table 134 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*[5]	400	333	266*[5]	200*[5]	
				Read Parameters* [14]										
DQS-DQ skew	tDQSQ	Max		200	220	240	280	340	370	400	500	600	700	ps

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also see Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The worst measured tDQSQ shall be within the specification limit.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid rising and falling DQ crossings at V_{REF} in the said burst.
4. For all DQ crossings found, locate the nearest DQS crossing (rising and falling).
5. Take the time difference from DQ crossing to DQS crossing as the tDQSQ.
6. Determine the worst result from the set of tDQSQ measured.

tQH, DQ/DQS Output Hold Time From DQS - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data output hold time (DQ rising and falling edge) from the DQS (rising and falling edge) is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2 and LPDDR2

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 135 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	x	tHP-tQHS	x	ps	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	x	tHP-tQHS	x	ps	39

Table 136 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	x	ps	34

Table 137 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
Read Parameters* [14]														
DQ/DQS output hold time from DQS	tQH	Max		t_{QHP} - t_{QHS}										ps

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also see Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The worst measured tQH shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQ crossings at V_{REF} in the said burst.
4 For all DQ crossings found, locate the nearest DQS rising/falling crossing.
5 Using the found DQS rising/falling crossing, locate the DQS rising/falling crossing prior to it.
6 Take the time difference from DQ crossing to DQS crossing as the tQH.
7 Determine the worst result from the set of tQH measured.

tDQSS, DQS Latching Transition to Associated Clock Edge - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS falling edge) access time to the associated clock (crossing point) is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, for LPDDR2 refer to the tDQSS Test (Low Power)

Signal cycle of interest: Write

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory.)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 138 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS latching rising transitions to associated clock edges	tDQSS	-0.25	0.25	-0.25	0.25	tCK	

Parameter	Symbol	DDR2-667		DDR2-180		Units	Specific Notes
		Min	Max	Min	Max		
DQS latching rising transitions to associated clock edges	tDQSS	-0.25	0.25	-0.25	0.25	tCK(avg)	30

Table 139 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS latching rising transitions to associated clock edges	tDQSS	-0.25	0.25	tCK(avg)	25

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

Also see Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

PASS Condition

The worst measured tDQSS shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQS crossings in the said burst.
4 For all DQS crossings found, locate the nearest Clock rising crossing.
5 Take the time difference from DQS crossing to Clock crossing as the tDQSS.
6 Determine the worst result from the set of tDQSS measured.

tDQSH, DQS Input HIGH Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the high level of the data strobe signal is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory.)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 140 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK(avg)	

Table 141 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS input HIGH pulse width	tDQSH	0.35	x	tCK(avg)	

Table 142 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Write Parameters* [14]										
DQS input high level width	tDQSH	Min		0.4										t_{CK}(avg)

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The worst measured tDQSH shall be within the specification limit.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising and falling DQS crossings in the said burst.
4. tDQSH is the time interval starting from a rising edge of the DQS and ending at the following falling edge.
5. Collect all tDQSH.
6. Determine the worst result from the set of tDQSH measured.

tDQSL, DQS Input Low Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the low level of the Data Strobe signal is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 143 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK(avg)	

Table 144 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS input LOW pulse width	tDQSL	0.35	x	tCK(avg)	

Table 145 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*[5]	400	333	266*[5]	200*[5]	
				Write Parameters* [14]										
DQS input low level width	tDQSL	Min		0.4										tCK(avg)

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The worst measured tDQSL shall be within the specification limit.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising and falling DQS crossings in the said burst.
4. tDQSL is the time interval starting from a falling edge of the DQS and ending at the following rising edge.
5. Collect all tDQSL.
6. Determine the worst result from the set of tDQSL measured.

tDSS, DQS Falling Edge to CK Setup Time – Test Method of Implementation

The purpose of this test is to verify that the time interval from the falling edge of the data strobe (DQS falling edge) output access time to the clock setup time, is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 146 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK(avg)	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK(avg)	30

Table 147 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS falling edge to CK setup time	tDSS	0.2	x	tCK(avg)	25

Table 148 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Write Parameters* [14]										
DQS falling edge to CK setup time	tDSS	Min		0.2										tCK(avg)

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The worst measured tDSS shall be within the specification limit.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid falling DQS crossings in the said burst.
4. For all falling DQS crossings found, locate all nearest next rising Clock edges.
5. tDSS is the time between falling DQS crossings and the Clock rising edges found.
6. Collect all tDSS.
7. Determine the worst result from the set of tDSS measure.

tDSH, DQS Falling Edge Hold Time from CK - Test Method of Implementation

The purpose of this test is to verify that the time interval from the falling edge of the data strobe output access time to the hold time of the clock, must be within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 149 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK(avg)	30

Table 150 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQS falling edge hold time from CK	tDSH	0.2	x	tCK(avg)	25

Table 151 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Write Parameters* [14]										
DQS falling edge hold time from CK	tDSH	Min		0.2										tCK(avg)

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The worst measured tDSH shall be within the specification limit.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid falling DQS crossings in the said burst.
4. For all falling DQS crossings found, locate all nearest prior rising Clock edges.
5. tDSH is the time between falling DQS crossings and the Clock rising edges found.
6. Collect all tDSH.
7. Determine the worst result from the set of tDSH measured.

tWPST, Write Postamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS is no longer driving (from HIGH/LOW state to high impedance) from the last DQS signal crossing (last bit of the write data burst) for the Write cycle, is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 152 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
WRITE Postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
WRITE Postamble	tWPST	0.4	0.6	0.4	0.6	tCK(avg)	10

Table 153 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
WRITE Postamble	tWPST	0.4	0.6	tCK(avg)	10

Table 154 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Write Parameters* 14										
Write postamble	tWPST	Min		0.4										tCK(avg)

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The measured tWPST shall be within the specification limit.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find the tHZEndPoint(DQS) of the said burst.
4. Find the last falling edge on DQS prior to the tHZEndPoint(DQS).
5. tWPST is the time interval between the found falling DQS edge's crossing to the tHZEndPoint(DQS).
6. Report tWPST.

tWPRE, Write Preamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS starts to drive LOW (preamble behavior) to the first DQS signal crossing for the Write cycle, is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 155 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
WRITE Preamble	tWPRE	0.35	x	0.35	x	tCK	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
WRITE Preamble	tWPRE	0.35	x	0.35	x	tCK(avg)	

Table 156 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
WRITE Preamble	tWPRE	0.35	x	tCK(avg)	

Table 157 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Write Parameters* [14]										
Write Preamble	tWPRE	Min		0.35										tCK(avg)

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The measured tWPRE shall be within the specification limit.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find the tLZBeginPoint(DQS) of the said burst.
4. Find the first rising edge on DQS of the found burst.
5. tWPRE is the time interval between the found rising DQS edge's crossing to the tLZBeginPoint(DQS).
6. Report tWPRE.

tRPRE, Read Preamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS start driving LOW (*preamble behavior) to the first DQS signal crossing for the Read cycle must be within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 158 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
READ Preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	19

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
READ Preamble	tRPRE	0.9	1.1	0.9	1.1	tCK(avg)	19, 41

Table 159 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
READ Preamble	tRPRE	0.9	1.1	tCK(avg)	16,36

Table 160 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*[5]	400	333	266*[5]	200*[5]	
				Read Parameters* [14]										
READ Preamble	tRPRE	Min		0.9										tCK(avg)

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The measured tRPRE shall be within the specification limit.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid READ burst found.
3. Find the tLZBeginPoint(DQS) of the said burst.
4. Find the first rising edge on DQS of the found burst.
5. tRPRE is the time interval between the found rising DQS edge's crossing to the tLZBeginPoint(DQS).
6. Report tRPRE.

tRPST, Read Postamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS is no longer driving (from HIGH/LOW state to high-impedance) to the last DQS signal crossing (last bit of the data burst) for the Read cycle is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 161 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
READ Postamble	tRPST	0.4	0.6	0.4	0.6	tCK	19

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
READ Postamble	tRPST	0.4	0.6	0.4	0.6	tCK(avg)	19, 42

Table 162 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
READ Postamble	tRPST	0.4	0.6	tCK(avg)	16,37

Table 163 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Read Parameters* 14										
READ Postamble *15, *17	tRPST	Min		t_{CL}(abs) - 0.05										tCK(avg)

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The measured tRPST shall be within the specification limit.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid READ burst found.
3. Find the tHZEndPoint(DQS) of the said burst.
4. Find the last falling edge on DQS prior to the tHZEndPoint(DQS).
5. tRPST is the time interval between the found falling DQS edge's crossing to the tHZEndPoint(DQS).
6. Report tRPST.

tHZ(DQ) Test (Low Power), DQ Out HIGH Impedance Time From Clock - Test Method of Implementation

The purpose of this test is to verify that the time when the DQ is no longer driving (from HIGH state OR LOW state to the high impedance stage), to the reference clock signal crossing, is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2, for DDR2 refer to the tHZ(DQ) Test

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Clock Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 164 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Read Parameters* 14										
DQ high-Z from clock*15	tHZ(DQ)	Max		$t_{DQSCK}(max) + \{1.4 * t_{DQSQ}(max)\}$										ps

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The measured tHZ(DQ) shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find Data tHZEndPoint of the said burst.
4 Find RL Clock edge (tDQSCK clock edge reference).
   - Find all DQS rising middle crossing points in the burst.
   - Find the first DQS rising edge by searching for the earliest rising crossing point in all of the found DQS middle crossing points.
   - Find the closest Clock-DQS (the Clock middle crossing point that is closest to the first DQS rising edge).
   - Find the RL Clock edge (tDQSCK clock edge reference) which is the Clock middle crossing point immediately before the closest Clock-DQS to tDQSCK Delay (cycle). By default, tDQSCK Delay is one cycle. For example, if tDQSCK Delay = 1 then the tDQSCK Clock point is the Clock middle crossing point that is prior to the closest Clock-DQS. If tDQSCK Delay = 3 then the tDQSCK Clock point is the Clock middle crossing point three clock cycles before the closest Clock-DQS. tDQSCK Delay is configurable in the configuration page.
5 Define BL (bit length) to be the number of DQS middle crossing points.
6 Find “RL+BL/2” Clock edge (Clock rising middle crossing point that is BL/2 cycles after the RL Clock edge.
7 Compare the Data tHZ end point to the “RL+BL/2” Clock edge as the test result. Mathematically, the test result = Data tHZ end point - “RL+BL/2” Clock edge point.
8 Display the test result by going to the measurement location on the waveform and locate the marker to Data tHZ end point and Clock middle cross point of the test result.
9 Compare the test result against the compliance test limit.

NOTE Some designs do not have tri-state at V_{REF} (for example, 0.9V). This test is not guaranteed when this scenario happens, as there is no significant point of where the driver has been turned-off.

tHZ(DQS) Test (Low Power), DQS Out HIGH Impedance Time From Clock - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS is no longer driving (from LOW state to the high impedance stage), to the reference clock signal crossing, is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 165 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Read Parameters* 14										
DQS high-Z from clock*15	tHZ(DQS)	Max		t_{DQSCK}(max) - 100										ps

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The measured tHZ(DQS) shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find the Strobe tHZEndPoint of this burst.
4 Find RL Clock edge (tDQSCK clock edge reference).
   - Find all DQS rising middle crossing points in the burst.
   - Find the first DQS rising edge by searching for the earliest rising crossing point in all of the found DQS middle crossing points.
   - Find the closest Clock-DQS (the Clock middle crossing point that is closest to the first DQS rising edge).
   - Find the RL Clock edge (tDQSCK clock edge reference) which is the Clock middle crossing point immediately before the closest Clock-DQS to tDQSCK Delay (cycle). By default, tDQSCK Delay is one cycle. For example, if tDQSCK Delay = 1 then the tDQSCK Clock point is the Clock middle crossing point that is prior to the closest Clock-DQS. If tDQSCK Delay = 3 then the tDQSCK Clock point is the Clock middle crossing point three clock cycles before the closest Clock-DQS. tDQSCK Delay is configurable in the configuration page.
5 Define BL (bit length) to be the number of DQS middle crossing points.
6 Find “RL+BL/2” Clock edge (Clock rising middle crossing point that is BL/2 cycles after the RL Clock edge.
7 Compare the Strobe tHZ end point to the “RL+BL/2” Clock edge as the test result. Mathematically, the test result = Data tHZ end point - “RL+BL/2” Clock edge point.
8 Display the test result by going to the measurement location on the waveform and locate the marker to Strobe tHZ end point and Clock middle cross point of the test result.
9 Compare the test result against the compliance test limit.

tLZ(DQS) Test (Low Power), DQS Low Impedance Time From Clock - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS starts driving (*from tri- state to LOW state) to the reference clock signal crossing, is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2, for DDR2 refer to tLZ(DQS) Test

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 166 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Read Parameters* 14										
DQS low-Z from clock*15	tLZ(DQS)	Min		t_{DQSCK}(min) - 300										ps

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The measured tLZ(DQS) shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find the Strobe tLZBeginPoint of this burst.
4 Find RL Clock edge (tDQSCK clock edge reference).
   - Find all DQS rising middle crossing points in the burst.
   - Find the first DQS rising edge by searching for the earliest rising crossing point in all of the found DQS middle crossing points.
   - Find the closest Clock-DQS (the Clock middle crossing point that is closest to the first DQS rising edge).
   - Find the RL Clock edge (tDQSCK clock edge reference) which is the Clock middle crossing point immediately before the closest Clock-DQS to tDQSCK Delay (cycle). By default, tDQSCK Delay is one cycle. For example, if tDQSCK Delay = 1 then the tDQSCK Clock point is the Clock middle crossing point that is prior to the closest Clock-DQS. If tDQSCK Delay = 3 then the tDQSCK Clock point is the Clock middle crossing point three clock cycles before the closest Clock-DQS. tDQSCK Delay is configurable in the configuration page.
5 Find “RL-1” Clock edge (previous Clock rising middle crossing point of RL Clock edge).
6 Compare the Strobe tLZ begin point to the “RL-1” Clock edge as the test result. Mathematically, the test result = Strobe tLZ begin point - “RL-1” Clock edge point.
7 Display the test result by going to the measurement location on the waveform and locate the marker to Strobe tLZ begin point and Clock middle cross point of the test result.
8 Compare the test result against the compliance test limit.

tLZ(DQ) Test (Low Power), DQ Low Impedance Time From Clock - Test Method of Implementation

The purpose of this test is to verify that the time when the DQ starts driving (from high impedance state to HIGH/LOW state), to the reference clock signal crossing, is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2, for DDR2 refer to tLZ(DQ) Test

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 167 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Read Parameters* 14										
DQ low-Z from clock*15	tLZ(DQ)	Min		$t_{DQSCK}(min) + \{1.4 * t_{QHS}(max)\}$										ps

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The measured tLZ(DQ) shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find the Data tLZBeginPoint of this burst.
4 Find RL Clock edge (tDQSCK clock edge reference).
   - Find all DQS rising middle crossing points in the burst.
   - Find the first DQS rising edge by searching for the earliest rising crossing point in all of the found DQS middle crossing points.
   - Find the closest Clock-DQS (the Clock middle crossing point that is closest to the first DQS rising edge).
   - Find the RL Clock edge (tDQSCK clock edge reference) which is the Clock middle crossing point immediately before the closest Clock-DQS to tDQSCK Delay (cycle). By default, tDQSCK Delay is one cycle. For example, if tDQSCK Delay = 1 then the tDQSCK Clock point is the Clock middle crossing point that is prior to the closest Clock-DQS. If tDQSCK Delay = 3 then the tDQSCK Clock point is the Clock middle crossing point three clock cycles before the closest Clock-DQS. tDQSCK Delay is configurable in the configuration page.
5 Compare the Data tLZ begin point to the RL Clock edge as the test result.
Mathematically, the test result = Data tLZ begin point - RL Clock edge point.
6 Display the test result by going to the measurement location on the waveform and locate the marker to Data tLZ begin point and Clock middle cross point of the test result.
7 Compare the test result against the compliance test limit.

tQSH, DQS Output High Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the high level of the Data Strobe signal is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 168 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Read Parameters* 14										
DQS output high pulse width	tQSH	Min		t_{CH}(abs) - 0.05										t_{CK}(avg)

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The worst measured tQSH shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQS crossing in this burst.
4 tQSH is the time interval starting from a rising edge of the DQS and ending at the following falling edge.
5 Collect all tQSH.
6 Determine the worst result from the measured tQSH.

tQSL, DQS Output Low Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the low level of the Data Strobe signal is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 169 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Read Parameters* 14										
DQS output low pulse width	tQSL	Min		t_{CL}(abs) - 0.05										t_{CK}(avg)

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The worst measured tQSL shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising and falling DQS crossing in this burst.
4 tQSL is the time interval starting from a falling edge of the DQS and ending at the following rising edge.
5 Collect all tQSL.
6 Determine the worst result from the measured tQSL.

tDQSS Test (Low Power), DQS Latching Transition to Associated Clock Edge - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (first DQS rising edge) access time to the reference clock which is before the associated clock (crossing point) is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2, for DDR2 refer to the tDQSS Test

Signal cycle of interest: Write

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)
- Clock Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Clock Signal, CK
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 170 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*[5]	400	333	266*[5]	200*[5]	
				Write Parameters* [14]										
Write command to first DQS latching transition	tDQSS	Min		0.75										t_{CK}(avg)
		Max		1.25										

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JESD209-2B*.

PASS Condition

The measured tDQSS shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQS middle crossings in this burst.
4 Find the first DQS rising edge by searching for the earliest rising crossing point in all of the found DQS middle crossing points. Take the found point (first DQS rising edge) as the tDQSS strobe point.
5 Find the closest Clock-DQS (the Clock middle crossing point that is closest to the first DQS rising edge).
6 Find the tDQSS Clock point which is the rising clock middle crossing point one cycle before the closest Clock-DQS.
7 Compare the tDQSS strobe point to the tDQSS clock point as the test result.
Mathematically, the test result = tDQSS strobe point - tDQSS clock point.
8 Display the test result by going to the measurement location on the waveform and locate the marker to tDQSS strobe point and tDQSS clock point.
9 Compare the test result against the compliance test limit.

tDVAC (Strobe), Time above $V_{IHdiff(AC)}$/ below $V_{ILdiff(AC)}$ - Test Method of Implementation

The purpose of this test is to verify that the time the strobe signal is above $V_{IHdiff(AC)}$ and below $V_{ILdiff(AC)}$ is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: Write

Signal(s) of Interest:

- Data Strobe Signal (supported by Data Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 171 Allowed time before ringback (tDVAC) for CK_t-CK_s and DQS_t-DQS_c

Slew Rate	tDVAC [ps] @ $\lvert V_{IH/Ldiff(AC)} \rvert$ = 440 mV	tDVAC [ps] @ $\lvert V_{IH/Ldiff(AC)} \rvert$ = 600 mV
	Min	Min
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
< 1.0	150	0

Test References

See Table 78 - Allowed Time Before Ringback (tDVAC) for CK_t-CK_s and DQS_t- DQS_c in the *JESD209-2B*.

PASS Condition

The worst measured tDVAC(Strobe) should be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all of the rising/falling DQS crossings at the $V_{IHdiff(AC)}$ and $V_{ILdiff(AC)}$ levels in this burst.
4 tDVAC(Strobe) is the time interval starting from a DQS rising $V_{IHdiff(AC)}$ crossing point and ending at the following DQS falling $V_{IHdiff(AC)}$ crossing point.
5 tDVAC(Strobe) is also the time interval starting from a DQS falling $V_{ILdiff(AC)}$ crossing point and ending at the following DQS rising $V_{ILdiff(AC)}$ crossing point.
6 Collect all tDVAC(Strobe) results.
7 Determine the worst result from the set of tDVAC(Strobe) measured.
8 Report the worst result from the set of tDVAC(Strobe) measured. No compliance limit checking is performed for this test. You need to manually check the test status (pass/fail) of this test based on the worst tDVAC(Strobe) and the slew rate reported.

16 Data Timing Tests

This section provides the Methods of Implementation (MOIs) for Data Mask Timing tests using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

NOTE

Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Data Timing Tests

When performing the Data Timing tests, the DDR2(+LP) Compliance Test Application will prompt you to make the propser connections. The connection for Data Timing tests may look similar to the following diagrams. Refer to the Connection tab in DDR2(+LP) Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

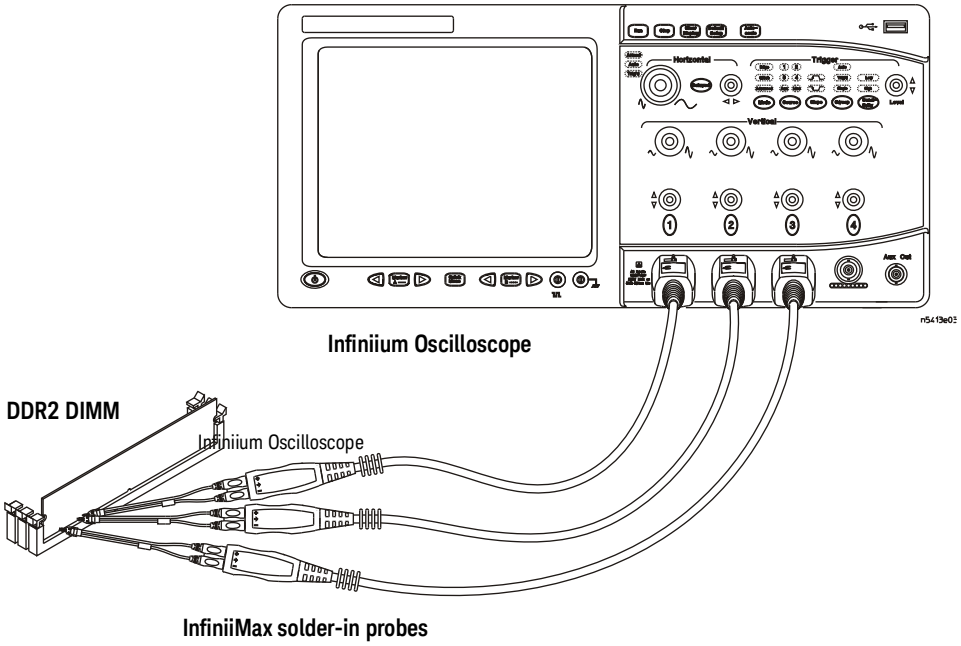


Figure 32 Probing for Data Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channels shown in Figure 32 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in "Preparing to Take Measurements" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR2/LPDDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2/LPDDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2/LPDDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2(+LP) Test application, click the Set Up tab.

6 Select the Speed Grade options. For Data Timing Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800, DDR2-1066. To select a LPDDR2 Speed Grade option (for tests that support LPDDR2), check the Low Power box.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

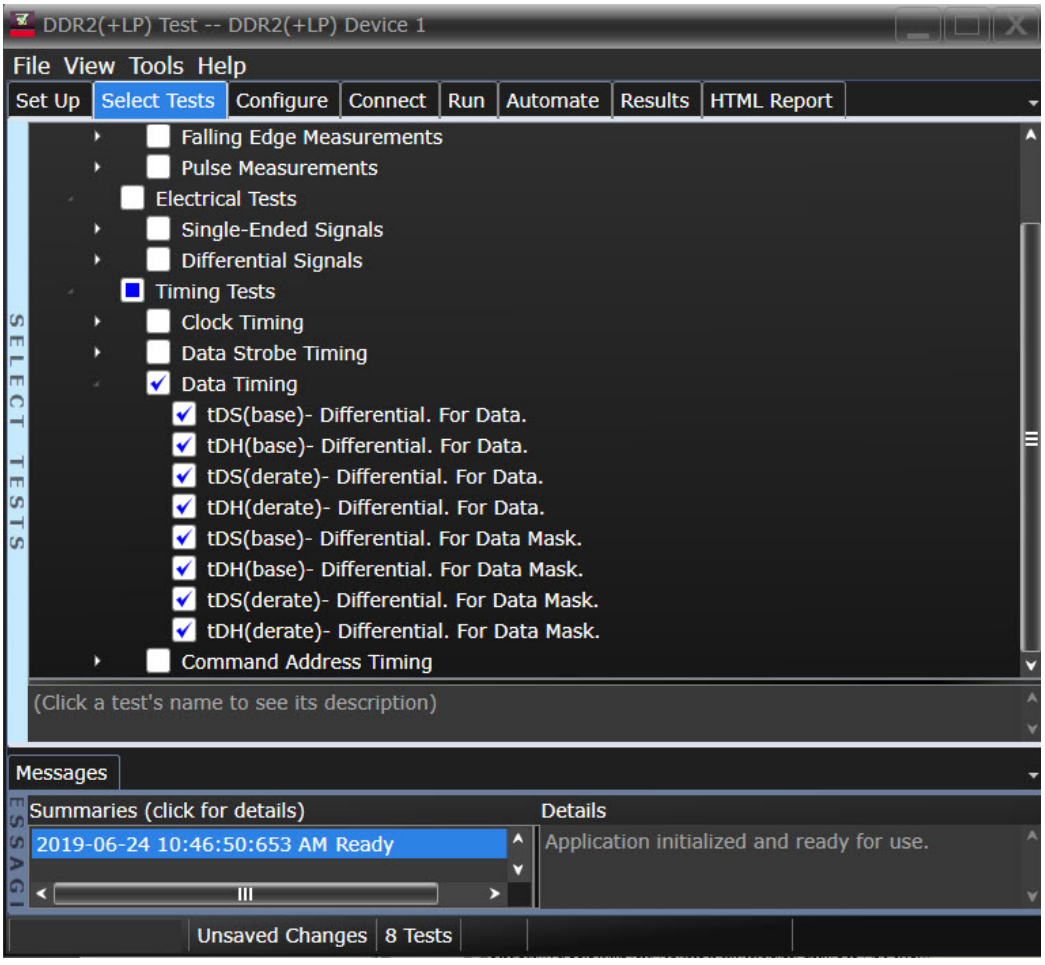


Figure 33 Selecting Data Timing Tests

9 Follow the DDR2(+LP) Test application's task flow to set up the configuration options, run the tests and view the tests results.

tDS(base), Differential DQ and DM Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Data Mask Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS (this must use a differential DQS connection)
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 172 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input setup time (differential strobe)	tDS(base)	150	x	100	x	ps	6,7,8,20,28

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input setup time	tDS(base)	100	x	50	x	ps	6,7,8,20,28,31

Table 173 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQ and DM input setup time	tDS(base)	0	x	ps	6,7,8,17,23,26

Table 174 Data Setup and Hold Base Values

Symbol	LPDDR2						Unit	Reference
	1066	933	800	677	533	466		
tDS(base)	-10	15	50	130	210	230	ps	$V_{IH/L(AC)} = V_{REF(AC)}$ +/- 220mV

Symbol	LPDDR2				Units	Specific Notes
	400	333	266	200		
tDS(base)	180	300	450	700	ps	$V_{IH/L(AC)} = V_{REF(AC)}$ +/- 300mV

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also see Table 108 - Data Setup and Hold Base- Values in the *JESD208-2B*.

PASS Condition

The worst measured tDS shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IH(AC)}$ in the burst.
4 Find all valid falling DQ crossings that cross $V_{IL(AC)}$ in the same burst.
5 For all DQ crossings found, locate all next DQS crossings that cross 0V.
6 tDS is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDS.
8 Find the worst tDS among the measured values and report the value as the test result.
9 Measure the nominal slew rate on the DQ and DQS edges where the worst tDS was found.
   - For DQ Falling, Slew Rate = (V_{REF} - $V_{IL(AC)}$) / tF
   - For DQ Rising, Slew Rate = ($V_{IH(AC)}$ - V_{REF}) / tR
     tF and tR are the transition time respectively.
   - For DQS Rising, Slew Rate = ($V_{HITHRES}$ - 0V) / tR
   - For DQS Falling, Slew Rate = (0V - $V_{LOTHRES}$) / tF
     tF and tR are the transition time respectively.
10 Report the nominal slew rate for DQ and DQS.
11 Measure the tangent slew rate on the DQ and DQS edges where the worst tDS was found. The measurement is similar to nominal slew rate, except the transition time is broken into ten parts and the slew rate is measured from a pivot point (VREF or 0V) to each of the ten points. Tangent slew rate is the maximum slew rates measured.
12 Report tangent slew rate for DQ and DQS.

tDH(base), Differential DQ and DM Input Hold Time – Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) hold time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Data Mask Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS (this must use a differential DQS connection)
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 175 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input hold time (differential strobe)	tDH(base)	275	x	275	x	ps	6,7,8,21,28

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input hold time	tDH(base)	175	x	125	x	ps	6,7,8,21,28,31

Table 176 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQ and DM input hold time	tDH(base)	75	x	ps	6,7,8,18,23,26

Table 177 Data Setup and Hold Base Values

Symbol	LPDDR2						Unit	Reference
	1066	933	800	677	533	466		
tDH(base)	80	105	140	220	300	320	ps	$V_{IH/L(AC)} = V_{REF(DC)}$ +/- 130mV

Symbol	LPDDR2				Units	Specific Notes
	400	333	266	200		
tDH(base)	280	400	550	800	ps	$V_{IH/L(DC)} = V_{REF(DC)}$ +/- 200mV

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also see Table 108 - Data Setup and Hold Base- Values in the *JESD208-2B*.

PASS Condition

The worst measured tDH shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IH(DC)}$ in the burst.
4 Find all valid falling DQ crossings that cross $V_{IL(DC)}$ in the same burst.
5 For all DQ crossings found, locate all next DQS crossings that cross 0V.
6 tDH is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDH.
8 Find the worst tDH among the measured values and report the value as the test result.
9 Measure the nominal slew rate on the DQ and DQS edges where the worst tDH was found.
   - For DQ Falling, Slew Rate = (V_{REF} - $V_{IL(DC)}$) / tF
   - For DQ Rising, Slew Rate = ($V_{IH(DC)}$ - V_{REF}) / tR
     tF and tR are the transition time respectively.
   - For DQS Rising, Slew Rate = ($V_{HITHRES}$ - 0V) / tR
   - For DQS Falling, Slew Rate = (0V - $V_{LOTHRES}$) / tF
     tF and tR are the transition time respectively.
10 Report the nominal slew rate for DQ and DQS.
11 Measure the tangent slew rate on the DQ and DQS edges where worst tDH was found. The measurement is similar to nominal slew rate, except the transition time is broken into ten parts and the slew rate is measured from a pivot point (V_{REF} or 0V) to each of the ten points. Tangent slew rate is the maximum slew rates measured.
12 Report tangent slew rate for DQ and DQS.

tDS(derate), Differential DQ and DM Input Setup Time with Derating Support - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Data Mask Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS (this must use a differential DQS connection)
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 178 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input setup time (differential strobe)	tDS(base)	150	x	100	x	ps	6,7,8,20,28

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input Setup time	tDS(base)	100	x	50	x	ps	6,7,8,20,28,31

Table 179 DDR2-400/533 tDS/tDH derating with differential data strobe

$\triangle$tDS, $\triangle$tDH derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table.)									
		DQS, $\overline{\text{DQS}}$ Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		$\triangle$tDS	$\triangle$tDH	$\triangle$tDS	$\triangle$tDH	$\triangle$tDS	$\triangle$tDH	$\triangle$tDS	$\triangle$tDH
DQ Slew Rate V/ns	2.0	125	45	125	45	125	45	-	-
	1.5	83	21	83	21	83	21	95	33
	1.0	0	0	0	0	0	0	12	12
	0.9	-	-	-11	-14	-11	-14	1	-2
	0.8	-	-	-	-	-25	-31	-13	-19

Table 179 DDR2-400/533 tDS/tDH derating with differential data strobe

△tDS, △tDH derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table.)									
		DQS, $\overline{DQS}$ Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
	0.7	-	-	-	-	-	-	-31	-42
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tDS, △tDH derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table.)											
		DQS, $\overline{DQS}$ Differential Slew Rate									
		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-	-	-
	1.0	24	24	-	-	-	-	-	-	-	-
	0.9	13	10	25	22	-	-	-	-	-	-
	0.8	-1	-7	11	5	23	17	-	-	-	-
	0.7	-19	-30	-7	-18	5	-6	17	6	-	-
	0.6	-43	-59	-31	-47	-19	-35	-7	-23	5	-11
	0.5	-	-	-74	-89	-62	-77	-50	-65	-38	-53
	0.4	-	-	-	-	-127	-140	-115	-128	-103	-116

Table 180 DDR2-667/800 tDS/tDH derating with differential data strobe

△tDS, △tDH derating values for DDR2-667, DDR2-800 (All units in 'ps'; the note applies to the entire table.)									
		DQS, $\overline{DQS}$ Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	100	45	100	45	100	45	-	-
	1.5	67	21	67	21	67	21	79	33
	1.0	0	0	0	0	0	0	12	12
	0.9	-	-	-5	-14	-5	-14	7	-2
	0.8	-	-	-	-	-13	-31	-1	-19
	0.7	-	-	-	-	-	-	-10	-42

Table 180 DDR2-667/800 tDS/tDH derating with differential data strobe

△tDS, △tDH derating values for DDR2-667, DDR2-800 (All units in 'ps'; the note applies to the entire table.)									
		DQS, $\overline{DQS}$ Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tDS, △tDH derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table.)											
		DQS, $\overline{DQS}$ Differential Slew Rate									
		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-	-	-
	1.0	24	24	-	-	-	-	-	-	-	-
	0.9	19	10	31	22	-	-	-	-	-	-
	0.8	11	-7	23	5	35	17	-	-	-	-
	0.7	2	-30	14	-18	26	-6	38	6	-	-
	0.6	-10	-59	2	-47	14	-35	26	-23	38	-11
	0.5	-	-	-24	-89	-12	-77	0	-65	12	-53
	0.4	-	-	-	-	-52	-140	-40	-128	-28	-116

Table 181 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQ and DM input setup time	tDS(base)	0	x	ps	6,7,8,17,23,26

Table 182 DDR2-1066 tDS/tDH derating with differential data strobe

△tDS, △tDH derating values for DDR2-1066 (All units in 'ps'; the note applies to the entire table.)									
		DQS, $\overline{DQS}$ Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	100	45	100	45	100	45	-	-
	1.5	67	21	67	21	67	21	79	33
	1.0	0	0	0	0	0	0	12	12

Table 182 DDR2-1066 tDS/tDH derating with differential data strobe

△tDS, △tDH derating values for DDR2-1066 (All units in 'ps'; the note applies to the entire table.)									
		DQS, $\overline{DQS}$ Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
	0.9	-	-	-5	-14	-5	-14	7	-2
	0.8	-	-	-	-	-13	-31	-1	-19
	0.7	-	-	-	-	-	-	-10	-42
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tDS, △tDH derating values for DDR2-1066 (All units in 'ps'; the note applies to the entire table.)											
		DQS, $\overline{DQS}$ Differential Slew Rate									
		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-	-	-
	1.0	24	24	-	-	-	-	-	-	-	-
	0.9	19	10	31	22	-	-	-	-	-	-
	0.8	11	-7	23	5	35	17	-	-	-	-
	0.7	2	-30	14	-18	26	-6	38	6	-	-
	0.6	-10	-59	2	-47	14	-35	26	-23	38	-11
	0.5	-	-	-24	-89	-12	-77	0	-65	12	-53
	0.4	-	-	-	-	-52	-140	-40	-128	-28	-116

Table 183 Data Setup and Hold Base-Values

Symbol	LPDDR2						Units	Reference
	1066	933	800	667	533	466		
tDS(base)	-10	15	50	130	210	230	ps	$V_{IH/L(AC)} = V_{REF(AC)}$ +/- 220mV

Symbol	LPDDR2				Units	Reference
	400	333	266	200		
tDS(base)	180	300	450	700	ps	$V_{IH/L(AC)} = V_{REF(AC)}$ +/- 300mV

Table 184 Derating Values LPDDR2 tDS/tDH - AC/DC based AC220

△tDS, △tDH derating in [ps] AC/DC based AC220 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 220mV$, $V_{IL(AC)} = V_{REF(DC)} - 220mV$ DC130 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 130mV$, $V_{IL(DC)} = V_{REF(DC)} - 130mV$									
		DQS_t, DQS_c Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	110	65	110	65	110	65	-	-
	1.5	74	43	73	43	73	43	89	59
	1.0	0	0	0	0	0	0	16	16
	0.9	-	-	-3	-5	-3	-5	13	11
	0.8	-	-	-	-	-8	-13	8	3
	0.7	-	-	-	-	-	-	2	-6
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tDS, △tDH derating in [ps] AC/DC based AC220 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 220mV$, $V_{IL(AC)} = V_{REF(DC)} - 220mV$ DC130 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 130mV$, $V_{IL(DC)} = V_{REF(DC)} - 130mV$									
		DQS_t, DQS_c Differential Slew Rate							
		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	32	32	-	-	-	-	-	-
	0.9	29	27	45	43	-	-	-	-
	0.8	24	19	40	35	56	55	-	-
	0.7	18	10	34	26	50	46	66	78
	0.6	10	-3	26	13	42	33	58	65
	0.5	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-7	2	17	34

Table 185 Derating Values LPDDR2 tDS/tDH - AC/DC based AC300

△tDS, △tDH derating in [ps] AC/DC based AC300 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 300mV$, $V_{IL(AC)} = V_{REF(DC)} - 300mV$ DC200 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 200mV$, $V_{IL(DC)} = V_{REF(DC)} - 200mV$									
		DQS_t, DQS_c Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	150	100	150	100	150	100	-	-
	1.5	100	67	100	67	100	67	116	83
	1.0	0	0	0	0	0	0	16	16
	0.9	-	-	-4	-8	-4	-8	12	8
	0.8	-	-	-	-	-12	-20	4	-4
	0.7	-	-	-	-	-	-	-3	-18
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tDS, △tDH derating in [ps] AC/DC based AC300 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 300mV$, $V_{IL(AC)} = V_{REF(DC)} - 300mV$ DC200 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 200mV$, $V_{IL(DC)} = V_{REF(DC)} - 200mV$									
		DQS_t, DQS_c Differential Slew Rate							
		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	32	32	-	-	-	-	-	-
	0.9	28	24	44	40	-	-	-	-
	0.8	20	12	36	28	52	48	-	-
	0.7	13	-2	29	14	45	34	61	66
	0.6	2	-21	18	-5	34	15	50	47
	0.5	-	-	-12	-32	4	-12	20	20
	0.4	-	-	-	-	-35	-40	-11	-8

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

See Table 43 - DDR2- 400/533 tDS/tDH Derating with Differential Data Strobe and Table 44 - DDR2- 667/800 tDS/tDH Derating with Differential Data Strobe in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2- 1066) and Table 42 - DDR2- 1066 tDS/tDH Derating with Differential Data Strobe in the *JESD208*.

Also see Table 108 - Data Setup and Hold Base-Values, Table 109 - Derating Values LPDDR2 tDS/tDH - AC/DC Based AC220 and Table 110 - Derating Values LPDDR2 tDS/tDH - AC/DC Based AC300 in the *JESD209-2B*.

PASS Condition

The worst measured tDS shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IH(AC)}$ in the burst.
4 Find all valid falling DQ crossings that cross $V_{IL(DC)}$ in the same burst.
5 For all DQ crossings found, locate all next DQS crossings that cross 0V.
6 tDS is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDS.
8 Find the worst tDS among the measured values and report the value as the test result.
9 Measure the mean slew rate for all the DQ and DQS edges.
10 Use the mean slew rate for DQ and DQS to determine the ΔtDS derating value based on the derating tables.
11 The test limit for tDS test = tDS(base) + ΔtDS.

tDH(derate), Differential DQ and DM Input Hold Time with Derating Support - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) hold time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Data Mask Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS (this must use a differential DQS connection)
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 186 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input hold time (differential strobe)	tDH(base)	275	x	225	x	ps	6,7,8,21,28

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input hold time	tDS(base)	175	x	125	x	ps	6,7,8,21,28,31

Table 187 DDR2-400/533 tDS/tDH derating with differential data strobe

$\triangle$tDS, $\triangle$tDH derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table.)									
		DQS, $\overline{\text{DQS}}$ Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		$\triangle$tDS	$\triangle$tDH	$\triangle$tDS	$\triangle$tDH	$\triangle$tDS	$\triangle$tDH	$\triangle$tDS	$\triangle$tDH
DQ Slew Rate V/ns	2.0	125	45	125	45	125	45	-	-
	1.5	83	21	83	21	83	21	95	33
	1.0	0	0	0	0	0	0	12	12
	0.9	-	-	-11	-14	-11	-14	1	-2
	0.8	-	-	-	-	-25	-31	-13	-19

Table 187 DDR2-400/533 tDS/tDH derating with differential data strobe

△tDS, △tDH derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table.)									
		DQS, $\overline{DQS}$ Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
	0.7	-	-	-	-	-	-	-31	-42
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tDS, △tDH derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table.)											
		DQS, $\overline{DQS}$ Differential Slew Rate									
		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-	-	-
	1.0	24	24	-	-	-	-	-	-	-	-
	0.9	13	10	25	22	-	-	-	-	-	-
	0.8	-1	-7	11	5	23	17	-	-	-	-
	0.7	-19	-30	-7	-18	5	-6	17	6	-	-
	0.6	-43	-59	-31	-47	-19	-35	-7	-23	5	-11
	0.5	-	-	-74	-89	-62	-77	-50	-65	-38	-53
	0.4	-	-	-	-	-127	-140	-115	-128	-103	-116

Table 188 DDR2-667/800 tDS/tDH derating with differential data strobe

△tDS, △tDH derating values for DDR2-667, DDR2-800 (All units in 'ps'; the note applies to the entire table.)									
		DQS, $\overline{DQS}$ Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	100	45	100	45	100	45	-	-
	1.5	67	21	67	21	67	21	79	33
	1.0	0	0	0	0	0	0	12	12
	0.9	-	-	-5	-14	-5	-14	7	-2
	0.8	-	-	-	-	-13	-31	-1	-19
	0.7	-	-	-	-	-	-	-10	-42

Table 188 DDR2-667/800 tDS/tDH derating with differential data strobe

△tDS, △tDH derating values for DDR2-667, DDR2-800 (All units in 'ps'; the note applies to the entire table.)									
		DQS, $\overline{DQS}$ Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tDS, △tDH derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table.)											
		DQS, $\overline{DQS}$ Differential Slew Rate									
		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-	-	-
	1.0	24	24	-	-	-	-	-	-	-	-
	0.9	19	10	31	22	-	-	-	-	-	-
	0.8	11	-7	23	5	35	17	-	-	-	-
	0.7	2	-30	14	-18	26	-6	38	6	-	-
	0.6	-10	-59	2	-47	14	-35	26	-23	38	-11
	0.5	-	-	-24	-89	-12	-77	0	-65	12	-53
	0.4	-	-	-	-	-52	-140	-40	-128	-28	-116

Table 189 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
DQ and DM input hold time	tDH(base)	75	x	ps	6,7,8,18,23,26

Table 190 DDR2-1066 tDS/tDH derating with differential data strobe

△tDS, △tDH derating values for DDR2-1066 (All units in 'ps'; the note applies to the entire table.)									
		DQS, $\overline{DQS}$ Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	100	45	100	45	100	45	-	-
	1.5	67	21	67	21	67	21	79	33
	1.0	0	0	0	0	0	0	12	12

Table 190 DDR2-1066 tDS/tDH derating with differential data strobe

△tDS, △tDH derating values for DDR2-1066 (All units in 'ps'; the note applies to the entire table.)									
		DQS, $\overline{DQS}$ Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
	0.9	-	-	-5	-14	-5	-14	7	-2
	0.8	-	-	-	-	-13	-31	-1	-19
	0.7	-	-	-	-	-	-	-10	-42
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tDS, △tDH derating values for DDR2-1066 (All units in 'ps'; the note applies to the entire table.)											
		DQS, $\overline{DQS}$ Differential Slew Rate									
		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-	-	-
	1.0	24	24	-	-	-	-	-	-	-	-
	0.9	19	10	31	22	-	-	-	-	-	-
	0.8	11	-7	23	5	35	17	-	-	-	-
	0.7	2	-30	14	-18	26	-6	38	6	-	-
	0.6	-10	-59	2	-47	14	-35	26	-23	38	-11
	0.5	-	-	-24	-89	-12	-77	0	-65	12	-53
	0.4	-	-	-	-	-52	-140	-40	-128	-28	-116

Table 191 Data Setup and Hold Base-Values

Symbol	LPDDR2						Units	Reference
	1066	933	800	667	533	466		
tDH(base)	80	105	140	220	300	320	ps	$V_{IH/L(DC)} = V_{REF(DC)}$ +/- 130mV

Symbol	LPDDR2				Units	Reference
	400	333	266	200		
tDH(base)	280	400	550	800	ps	$V_{IH/L(DC)} = V_{REF(DC)}$ +/- 200mV

Table 192 Derating Values LPDDR2 tDS/tDH - AC/DC based AC220

△tDS, △tDH derating in [ps] AC/DC based AC220 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 220mV$, $V_{IL(AC)} = V_{REF(DC)} - 220mV$ DC130 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 130mV$, $V_{IL(DC)} = V_{REF(DC)} - 130mV$									
		DQS_t, DQS_c Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	110	65	110	65	110	65	-	-
	1.5	74	43	73	43	73	43	89	59
	1.0	0	0	0	0	0	0	16	16
	0.9	-	-	-3	-5	-3	-5	13	11
	0.8	-	-	-	-	-8	-13	8	3
	0.7	-	-	-	-	-	-	2	-6
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tDS, △tDH derating in [ps] AC/DC based AC220 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 220mV$, $V_{IL(AC)} = V_{REF(DC)} - 220mV$ DC130 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 130mV$, $V_{IL(DC)} = V_{REF(DC)} - 130mV$									
		DQS_t, DQS_c Differential Slew Rate							
		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	32	32	-	-	-	-	-	-
	0.9	29	27	45	43	-	-	-	-
	0.8	24	19	40	35	56	55	-	-
	0.7	18	10	34	26	50	46	66	78
	0.6	10	-3	26	13	42	33	58	65
	0.5	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-7	2	17	34

Table 193 Derating Values LPDDR2 tDS/tDH - AC/DC based AC300

△tDS, △tDH derating in [ps] AC/DC based AC300 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 300mV$, $V_{IL(AC)} = V_{REF(DC)} - 300mV$ DC200 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 200mV$, $V_{IL(DC)} = V_{REF(DC)} - 200mV$									
		DQS_t, DQS_c Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	150	100	150	100	150	100	-	-
	1.5	100	67	100	67	100	67	116	83
	1.0	0	0	0	0	0	0	16	16
	0.9	-	-	-4	-8	-4	-8	12	8
	0.8	-	-	-	-	-12	-20	4	-4
	0.7	-	-	-	-	-	-	-3	-18
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tDS, △tDH derating in [ps] AC/DC based AC300 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 300mV$, $V_{IL(AC)} = V_{REF(DC)} - 300mV$ DC200 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 200mV$, $V_{IL(DC)} = V_{REF(DC)} - 200mV$									
		DQS_t, DQS_c Differential Slew Rate							
		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	32	32	-	-	-	-	-	-
	0.9	28	24	44	40	-	-	-	-
	0.8	20	12	36	28	52	48	-	-
	0.7	13	-2	29	14	45	34	61	66
	0.6	2	-21	18	-5	34	15	50	47
	0.5	-	-	-12	-32	4	-12	20	20
	0.4	-	-	-	-	-35	-40	-11	-8

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

See Table 43 - DDR2- 400/533 tDS/tDH Derating with Differential Data Strobe and Table 44 - DDR2- 667/800 tDS/tDH Derating with Differential Data Strobe in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2- 1066) and Table 42 - DDR2- 1066 tDS/tDH Derating with Differential Data Strobe in the *JESD208*.

Also see Table 108 - Data Setup and Hold Base-Values, Table 109 - Derating Values LPDDR2 tDS/tDH - AC/DC Based AC220 and Table 110 - Derating Values LPDDR2 tDS/tDH - AC/DC Based AC300 in the *JESD209-2B*.

PASS Condition

The worst measured tDH shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{Il(DC)}$ in the burst.
4 Find all valid falling DQ crossings that cross $V_{IH(DC)}$ in the same burst.
5 For all DQ crossings found, locate all next DQS crossings that cross 0V.
6 tDH is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDH.
8 Find the worst tDH among the measured values and report the value as the test result.
9 Measure the mean slew rate for all the DQ and DQS edges.
10 Use the mean slew rate for DQ and DQS to determine the ΔtDH derating value based on the derating tables.
11 The test limit for tDH test = tDH(base) + ΔtDH.

tDS1(base), Single-Ended DQ and DM Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Data Mask Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS (this must use a single-ended DQS connection)
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 194 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input setup time (single-ended strobe)	tDS1(base)	25	x	-25	x	ps	6,7,8,25

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) in the *JEDEC Standard JESD79-2E*.

PASS Condition

The worst measured tDS1 shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IH(AC)}$ in the burst.
4 Find all valid falling DQ crossings that cross $V_{IL(AC)}$ in the same burst.
5 For all DQ crossings found, locate all next DQS falling crossings that cross $V_{IH(AC)}$ and all next DQS rising crossing that cross $V_{IL(AC)}$.
6 tDS1 is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDS1.
8 Find the worst tDS1 among the measured values and report the value as the test result.
9 Measure the nominal slew rate on the DQ and DQS edges where worst tDS1 was found.
10 For DQ/DQS Falling, Slew Rate = (V_{REF} - $V_{IL(AC)}$) / tF
For DQ Rising, Slew Rate = ($V_{IH(AC)}$ - V_{REF}) / tR
tF and tR are the transition time respectively.
11 Report the nominal slew rate for DQ and DQS.
12 Measure the tangent slew rate on the DQ and DQS edges where worst tDS1 was found. The measurement is similar to nominal slew rate, except the transition time is broken into ten parts and the slew rate is measured from a pivot point (V_{REF} or 0V) to each of the ten points. Tangent slew rate is the maximum slew rates measured.
13 Report tangent slew rate for DQ and DQS.

tDH1(base), Single-Ended DQ and DM Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) hold time to the associated DQS edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Data Mask Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS (this must use a single-ended DQS connection)
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 195 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input hold time (single-ended strobe)	tDH1(base)	25	x	-25	x	ps	6,7,8,26

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) in the *JEDEC Standard JESD79-2E*.

PASS Condition

The worst measured tDH1 shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IL(DC)}$ in the burst.
4 Find all valid falling DQ crossings that cross $V_{IH(DC)}$ in the same burst.
5 For all DQ crossings found, locate all prior DQS rising crossings that cross $V_{IH(AC)}$ and all prior DQS falling crossings that cross $V_{IL(AC)}$.
6 tDH1 is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDH1.
8 Find the worst tDH1 among the measured values and report the value as the test result.
9 Measure the nominal slew rate on the DQ and DQS edges where worst tDH1 was found.
   - For DQ Falling, Slew Rate = (V_{REF} - $V_{IL(AC)}$) / tF
   - For DQ Rising, Slew Rate = ($V_{IH(AC)}$ - V_{REF}) / tR
     tF and tR are the transition time respectively.
   - For DQS Rising, Slew Rate = ($V_{HITHRES}$ - 0V) / tR
   - For DQS Falling, Slew Rate = (0V - $V_{LOTHRES}$) / tF
     tF and tR are the transition time respectively.
10 Report the nominal slew rate for DQ and DQS.
11 Measure the tangent slew rate on the DQ and DQS edges where worst tDH1 was found. The measurement is similar to nominal slew rate, except the transition time is broken into ten parts and the slew rate is measured from a pivot point (V_{REF} or 0V) to each of the ten points. Tangent slew rate is the maximum slew rates measured.
12 Report tangent slew rate for DQ and DQS.

tDS1(derate), Single-Ended DQ and DM Input Setup Time with Derating Support - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Data Mask Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS (this must use a differential DQS connection)
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 196 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input setup time (single-ended strobe)	tDS1(base)	25	x	-25	x	ps	6,7,8,25

Table 197 DDR2-400/533 tDS1/tDH1 derating with single-ended data strobe

△tDS1, △tDH1 derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table.)									
		DQS, Single-Ended Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	188	188	167	146	125	63	-	-
	1.5	146	167	125	125	83	42	81	43
	1.0	63	125	42	83	0	0	-2	1
	0.9	-	-	31	69	-11	-14	-13	-13
	0.8	-	-	-	-	-25	-31	-27	-30
	0.7	-	-	-	-	-	-	-45	-53
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

ΔtDS1, ΔtDH1 derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table.)											
		DQS, Single-Ended Slew Rate									
		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-	-	-
	1.0	-7	-13	-	-	-	-	-	-	-	-
	0.9	-18	-27	-29	-45	-	-	-	-	-	-
	0.8	-32	-44	-43	-62	-60	-86	-	-	-	-
	0.7	-50	-67	-61	-85	-78	-109	-108	-152	-	-
	0.6	-74	-96	-85	-114	-102	-138	-132	-181	-183	-246
	0.5	-	-	-128	-156	-145	-180	-175	-223	-226	-288
	0.4	-	-	-	-	-210	-243	-240	-286	-291	-351

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 45 - DDR2-400/533 tDS1/tDH1 Derating with Single-Ended Data Strobe in the *JEDEC Standard JESD79-2E*.

PASS Condition

The worst measured tDS1 shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IH(AC)}$ in the burst.
4 Find all valid falling DQ crossings that cross $V_{IL(AC)}$ in the same burst.
5 For all DQ crossings found, locate all prior DQS falling crossings that cross $V_{IH(DC)}$ and all prior DQS rising crossings that cross $V_{IL(DC)}$.
6 tDS1 is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDS1.
8 Find the worst tDS1 among the measured values and report the value as the test result.
9 Measure the mean slew rate for all the DQ and DQS edges.
10 Use the mean slew rate for DQ and DQS to determine the ΔtDS1 derating value based on the derating tables.
11 The test limit for tDS1 test = tDS1(base) + ΔtDS1.

tDH1(derate), Single-Ended DQ and DM Input Hold Time with Derating Support - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) hold time to the associated DQS edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)
- Data Mask Signal

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS (this must use a differential DQS connection)
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 198 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input hold time (single-ended strobe)	tDH1(base)	25	x	-25	x	ps	6,7,8,26

Table 199 DDR2-400/533 tDS1/tDH1 derating with single-ended data strobe

△tDS1, △tDH1 derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table.)									
		DQS, Single-Ended Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	188	188	167	146	125	63	-	-
	1.5	146	167	125	125	83	42	81	43
	1.0	63	125	42	83	0	0	-2	1
	0.9	-	-	31	69	-11	-14	-13	-13
	0.8	-	-	-	-	-25	-31	-27	-30
	0.7	-	-	-	-	-	-	-45	-53
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tDS1, △tDH1 derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table.)											
		DQS, Single-Ended Slew Rate									
		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-	-	-
	1.0	-7	-13	-	-	-	-	-	-	-	-
	0.9	-18	-27	-29	-45	-	-	-	-	-	-
	0.8	-32	-44	-43	-62	-60	-86	-	-	-	-
	0.7	-50	-67	-61	-85	-78	-109	-108	-152	-	-
	0.6	-74	-96	-85	-114	-102	-138	-132	-181	-183	-246
	0.5	-	-	-128	-156	-145	-180	-175	-223	-226	-288
	0.4	-	-	-	-	-210	-243	-240	-286	-291	-351

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 45 - DDR2-400/533 tDS1/tDH1 Derating with Single-Ended Data Strobe in the *JEDEC Standard JESD79-2E*.

PASS Condition

The worst measured tDH1 shall be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IL(DC)}$ in the burst.
4 Find all valid falling DQ crossings that cross $V_{IH(DC)}$ in the same burst.
5 For all DQ crossings found, locate all prior DQS rising crossings that cross $V_{IH(AC)}$ and all prior DQS falling crossings that cross $V_{IL(AC)}$.
6 tDH1 is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDH1.
8 Find the worst tDH1 among the measured values and report the value as the test result.
9 Measure the mean slew rate for all the DQ and DQS edges.
10 Use the mean slew rate for DQ and DQS to determine the ΔtDH1 derating value based on the derating tables.
11 The test limit for tDH1 test = tDH1(base) + ΔtDH1.

tVAC (Data), Time Above $V_{IH(AC)}$/Below $V_{IL(AC)}$ - Test Method of Implementation

The purpose of this test is to verify that the time the data signal is above $V_{IH(AC)}$ and below $V_{IL(AC)}$ is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 200 Required time tVAC above $V_{IH(AC)}$ {below $V_{IL(AC)}$} for valid transition

Slew Rate	tVAC @ 300 mV [ps]		tVAC @ 220 mV [ps]	
	Min	Max	Min	Max
>2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	1
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
<0.5	0	-	150	-

Test References

See Table 111 - Required time tVAC above $V_{IH(AC)}$ {below $V_{IL(AC)}$} for valid transition in the *JESD209-2B*.

PASS Condition

The worst measured tVAC(Data) should be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all of the rising/falling DQ crossings at the $V_{IH(AC)}$ and $V_{IL(AC)}$ levels in this burst.
4 tVAC(Data) is the time interval starting from a DQ rising $V_{IH(AC)}$ crossing point and ending at the following DQ falling $V_{IH(AC)}$ crossing point.
5 tVAC(Data) is also the time interval starting from a DQ falling $V_{IL(AC)}$ crossing point and ending at the following DQ rising $V_{IL(AC)}$ crossing point.
6 Collect all tVAC(Data) results.
7 Determine the worst result from the set of tVAC(Data) measured.
8 Report the worst result from the set of tVAC(Data) measured. No compliance limit checking is performed for this test. You need to manually check the test status (pass/fail) of this test based on the worst tVAC(Data) and slew rate reported.

tDIPW, DQ and DM Input Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the high or low level of the Data signal is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 201 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Write Parameters* 14										
DQ and DM input pulse width	tDIPW	Min		0.35										$t_{CK(avg)}$

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JEDEC Standard JESD209-2B*.

PASS Condition

The worst measured tDIPW should be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all of the valid rising and falling DQ crossings at V_{REF} in this burst.

4 tDIPW is the time interval starting from a rising/falling edge of the DQ and ending at the following falling/rising edge (the following edge should be in the opposite direction).

5 Collect all tDIPW.

6 Determine the worst result from the measured tDIPW.

tQHP, Data Half Period - Test Method of Implementation

The purpose of this test is to verify that the width of the high or low level of the Data signal is within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: Read

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQS signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ
- Data Strobe Signal, DQS
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 202 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*[5]	400	333	266*[5]	200*[5]	
				Read Parameters*[14]										
Data half period	tQHP	Min		$\min(t_{QSH}, t_{QSL})$										$t_{CK(avg)}$

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JEDEC Standard JESD209-2B*.

PASS Condition

The worst measured tQHP should be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all of the valid rising and falling DQ crossings at V_{REF} in this burst.
4 tQHP is the time interval starting from a rising/falling edge of the DQ and ending at the following falling/rising edge (the following edge should be in the opposite direction).
5 Collect all tQHP.
6 Determine the worst result from the measured tQHP.

tDS, DQ and DM Input Setup Time (Differential - V_{REF} based) - Test Method of Implementation

The purpose of this test is to verify that the time interval from data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge must be within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: Write

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Mask Signal (supported by Data Strobe Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS (This must use a differential DQS connection)
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 203 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Write Parameters* 14										
DQ and DM input setup time (Vref based)	tDS	Min		210	235	270	350	430	450	480	600	750	1000	ps

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JEDEC Standard JESD209-2B*.

PASS Condition

The worst measured tDS should be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation).
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IH(AC)}$ in the said burst. (See notes on threshold)
4 Find all valid falling DQ crossings that cross $V_{IL(AC)}$ in the same burst. (See notes on threshold)
5 For all DQ crossings found, locate all next DQS crossings that cross 0V. (See notes on threshold)
6 tDS is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDS.
8 Find the worst tDS among the measured value and report the value as the test result.
9 Measure nominal slew rate on the DQ and DQS edges where worst tDS is found.
   - For DQ Falling, Slew Rate = $(V_{REF} - V_{IL(AC)})/tF$
   - For DQ Rising, Slew Rate = $(V_{IH(AC)} - V_{REF})/tR$
     tF and tR are the transition time respectively.
   - For DQS Rising, Slew Rate = $(V_{HITHRES} - 0V)/tR$
   - For DQS Falling, Slew Rate = $(0V - V_{LOTHRES})/tF$
     tF and tR are the transition time respectively.
10 Report nominal slew rate for DQ and DQS.
11 Measure tangent slew rate on the DQ and DQS edges where worst tDS is found. The measurement is similar to nominal slew rate, except the transition time is break into 10 parts and slew rate is measured from a pivot point (V_{REF} or 0V) to all the 10 points. Tangent slew rate is the maximum slew rates measured.
12 Report tangent slew rate for DQ and DQS.

tDH, DQ and DM Input Hold Time (Differential - V_{REF} based) - Test Method of Implementation

The purpose of this test is to verify that the time interval from data or data mask (DQ/DM rising/falling edge) hold time to the associated DQS crossing edge must be within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: Write

Require Read/Write separation: Yes

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal) OR
- Data Mask Signal (supported by Data Strobe Signal)

Optional signal(s):

- Chip Select Signal (this signal is used to separate DQ signals from different rank of memory)

Signals required to perform the test on the oscilloscope:

- Data Signal, DQ or Data Mask Signal, DM
- Data Strobe Signal, DQS (This must use a differential DQS connection)
- Chip Select Signal, CS (optional)

Test Definition Notes from the Specification

Table 204 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Write Parameters* 14										
DQ and DM input hold time (Vref based)	tDH	Min		210	235	270	350	430	450	480	600	750	1000	ps

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JEDEC Standard JESD209-2B*.

PASS Condition

The worst measured tDH should be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal. (See notes on DDR read/write separation).
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IL(DC)}$ in the said burst. (See notes on threshold)
4 Find all valid falling DQ crossings that cross $V_{IH(DC)}$ in the same burst. (See notes on threshold)
5 For all DQ crossings found, locate all next DQS crossings that cross 0V. (See notes on threshold)
6 tDH is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDH.
8 Find the worst tDH among the measured value and report the value as the test result.
9 Measure nominal slew rate on the DQ and DQS edges where worst tDH is found.
   - For DQ Falling, Slew Rate = $(V_{REF} - V_{IL(DC)})/tF$
   - For DQ Rising, Slew Rate = $(V_{IH(DC)} - V_{REF})/tR$
     tF and tR are the transition time respectively.
   - For DQS Rising, Slew Rate = $(V_{HITHRES} - 0V)/tR$
   - For DQS Falling, Slew Rate = $(0V - V_{LOTHRES})/tF$
     tF and tR are the transition time respectively.
10 Report nominal slew rate for DQ and DQS.
11 Measure tangent slew rate on the DQ and DQS edges where worst tDH is found. The measurement is similar to nominal slew rate, except the transition time is break into 10 parts and slew rate is measured from a a pivot point (V_{REF} or 0V) to all the 10 points. Tangent slew rate is the maximum slew rates measured.
12 Report tangent slew rate for DQ and DQS.

17 Command and Address Timing (CAT) Tests

This section provides the Methods of Implementation (MOIs) for Command and Address Timing tests using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Command Address Timing Tests

When performing the Command Address Timing tests, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections. The connection for Command Address Timing tests may look similar to the following diagrams. Refer to the Connection tab in DDR2(+LP) Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

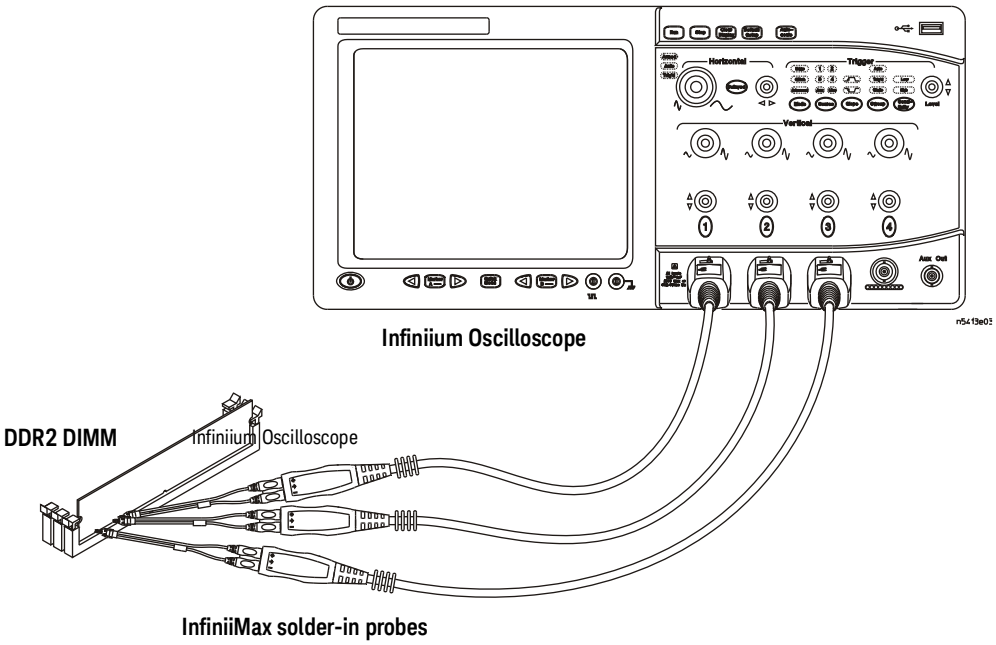


Figure 34 Probing for Command Address Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channels shown in Figure 34 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in "Starting the DDR2(+LP) Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR2/LPDDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2/LPDDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2/LPDDR2 devices.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2(+LP) Test application, click the Set Up tab.

6 Select the Speed Grade options. For Command Address Timing Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800, DDR2-1066. To select a LPDDR2 Speed Grade option (for tests that support LPDDR2), check the Low Power box.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

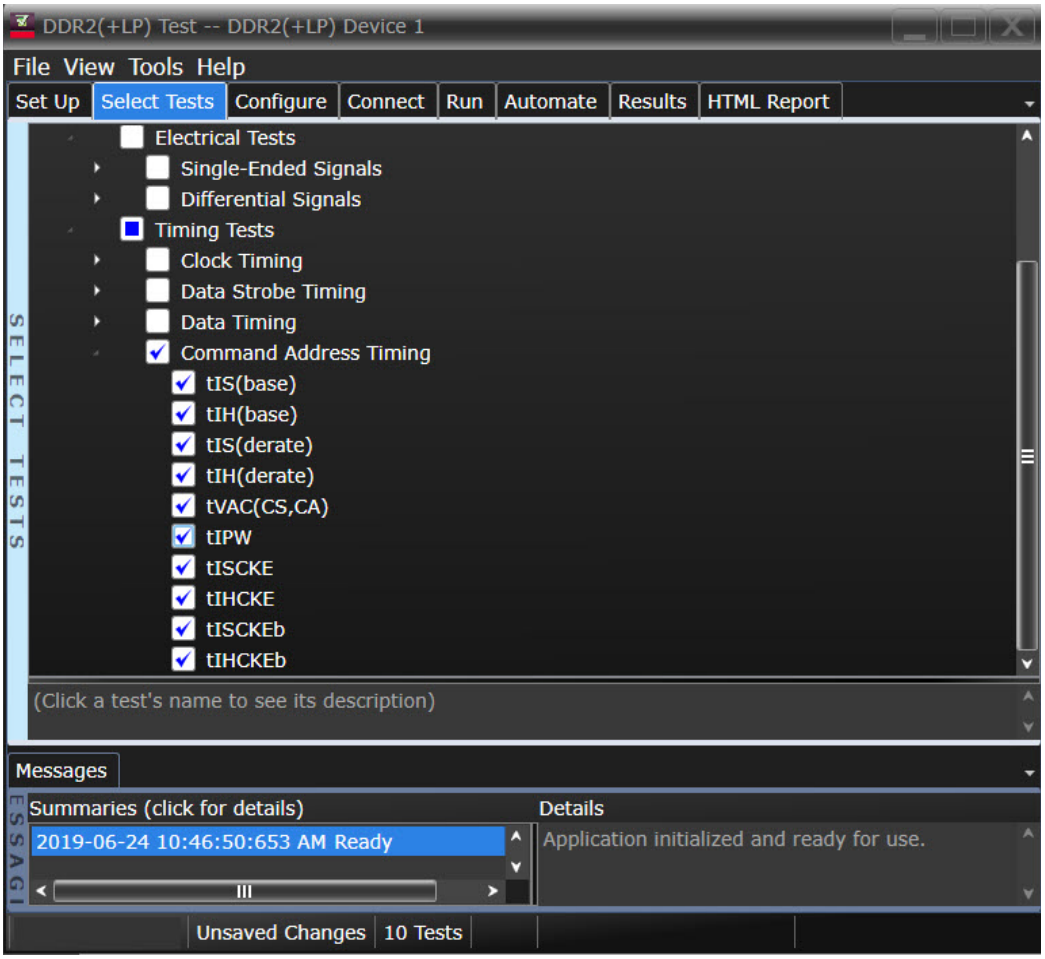


Figure 35 Selecting Command Address Timing Tests

9 Follow the DDR2(+LP) Test application's task flow to set up the configuration options, run the tests and view the tests results.

tIS(base) - Address and Control Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control or command/address (rising or falling edge) setup time to the associated clock crossing edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Address Signal OR Control Signal OR Command/Address
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Address Signal OR Control Signal OR Command/Address
- Clock Signal

Test Definition Notes from the Specification

Table 205 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input setup time	tIS(base)	350	x	250	x	ps	5,7,9,22

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input setup time	tIS(base)	200	x	175	x	ps	5,7,9,22,29

Table 206 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
Address and control input setup time	tIS(base)	125	x	ps	5,7,9,19, 24

Table 207 CA and CS_n Setup and Hold Base-Values for 1V/ns

Symbol	LPDDR2						Unit	Reference
	1066	933	800	677	533	466		
tIS(base)	0	30	70	150	240	300	ps	$V_{IH/L(AC)} = V_{REF(DC)}$ +/- 220mV

Symbol	LPDDR2				Units	Specific Notes
	400	333	266	200		
tIS(base)	300	440	600	850	ps	$V_{IH/L(AC)} = V_{REF(DC)}$ +/- 300mV

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also see Table 104 - CA and CS_n Setup and Hold Base-Values for 1V/ns in the *JESD209-2B*.

PASS Condition

The measured time interval between the address/control setup time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1 Pre-condition the oscilloscope settings.
2 Trigger on both edges (rising or falling) of the address/control signal under test.
3 Find all of the crossings on the rising edge of the signal under test that cross $V_{IH(AC)}$.
4 Find all of the crossing on the falling edge of the signal under test that cross $V_{IL(AC)}$.
5 For all crossings, locate the nearest Clock crossing that crosses 0V.
6 Take the time difference between the signal under test's crossing and the corresponding clock crossing as tIS.
7 Collect all measured tIS.
8 Report the worst tIS measured as the test result.
9 Compare the test result against the compliance test limit.

tIH(base) - Address and Control Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control or command/address (rising or falling edge) hold time to the associated clock crossing edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2. LPDDR2

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Address Signal OR Control Signal OR Command/Address
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Address Signal OR Control Signal OR Command/Address
- Clock Signal

Test Definition Notes from the Specification

Table 208 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input hold time	tIH(base)	475	x	375	x	ps	5,7,9,23

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input hold time	tIH(base)	275	x	250	x	ps	5,7,9,23,29

Table 209 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
Address and control input hold time	tIH(base)	200	x	ps	5,7,9,20,24

Table 210 CA and CS_n Setup and Hold Base-Values for 1V/ns

Symbol	LPDDR2						Unit	Reference
	1066	933	800	677	533	466		
tIH(base)	90	120	160	240	330	390	ps	$V_{IH/L(AC)} = V_{REF(DC)}$ +/- 130mV

Symbol	LPDDR2				Units	Specific Notes
	400	333	266	200		
tIH(base)	400	540	700	950	ps	$V_{IH/L(AC)} = V_{REF(DC)}$ +/- 200mV

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also see Table 104 - CA and CS_n Setup and Hold Base-Values for 1V/ns in the *JESD209-2B*.

PASS Condition

The measured time interval between the address/control hold time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Trigger on both edges (rising or falling) of the address/control signal under test.
3. Find all of the crossings on the rising edge of the signal under test that cross $V_{IL(DC)}$.
4. Find all of the crossing on the falling edge of the signal under test that cross $V_{IH(DC)}$.
5. For all crossings, locate the nearest Clock crossing that crosses 0V.
   Note: For LPDDR2 with PUT=CA option, the Clock crossing could be Clock rising or Clock falling. For other cases, the Clock crossing must be Clock rising only.
6. Take the time difference between the signal under test's crossing and the corresponding clock crossing as tIH.
7. Collect all measured tIH.
8. Report the worst tIH measured as the test result.
9. Compare the test result against the compliance test limit.

tIS(derate), Address and Control Input Setup Time with Derating Support - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control or command/address (rising or falling edge) setup time to the associated clock crossing edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Address Signal OR Control Signal OR Command/Address
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Address Signal OR Control Signal OR Command/Address
- Clock Signal

Test Definition Notes from the Specification

Table 211 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input setup time	tIS(base)	350	x	250	x	ps	5,7,9,22

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input setup time	tIS(base)	200	x	175	x	ps	5,7,9,22,29

Table 212 Derating Values for DDR2-400, DDR2-533

tIS, tIH Derating Values for DDR2-400, DDR2-533									
		CK, $\overline{CK}$ Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Units	Notes
Command/Address Slew Rate V/ns	4.0	187	94	217	124	247	154	ps	1
	3.5	179	89	200	119	239	149		
	3.0	167	83	197	113	227	143		
	2.5	150	75	180	105	210	135		
	2.0	125	45	155	75	185	105		
	1.5	83	21	113	51	143	81		
	1.0	0	0	30	30	60	60		
	0.9	-11	-14	19	16	49	46		
	0.8	-25	-31	5	-1	35	29		
	0.7	-43	-54	-13	-24	17	6		
	0.6	-67	-83	-37	-53	-7	-23		
	0.5	-110	-125	-80	-95	-50	-65		
	0.4	-175	-188	-145	-158	-115	-128		
	0.3	-285	-292	-255	-262	-225	-232		
	0.25	-350	-375	-320	-345	-290	-315		
	0.2	-525	-500	-495	-470	-455	-440		
	0.15	-800	-708	-770	-678	-740	-648		
	0.1	-1450	-1125	-1420	-1095	-1390	-1065		

Table 213 Derating Values for DDR2-667, DDR2-800

tIS, tIH Derating Values for DDR2-667, DDR2-800									
		CK, $\overline{CK}$ Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Units	Notes
Command/Address Slew Rate V/ns	4.0	150	94	180	124	210	154	ps	1
	3.5	143	89	173	119	203	149		
	3.0	133	83	163	113	193	143		
	2.5	120	75	150	105	180	135		
	2.0	100	45	130	75	160	105		
	1.5	67	21	97	51	127	81		
	1.0	0	0	30	30	60	60		
	0.9	-5	-14	25	16	55	46		
	0.8	-13	-31	17	-1	47	29		
	0.7	-22	-54	8	-24	38	6		
	0.6	-34	-83	-4	-53	26	-23		
	0.5	-60	-125	-30	-95	0	-65		
	0.4	-100	-188	-70	-158	-40	-128		
	0.3	-168	-292	-138	-262	-108	-232		
	0.25	-200	-375	-170	-345	-140	-315		
	0.2	-325	-500	-295	-470	-265	-440		
	0.15	-517	-708	-487	-678	-457	-648		
	0.1	-1000	-1125	-970	-1095	-940	-1065		

Table 214 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
Address and control input setup time	tIS(base)	125	x	ps	5,7,9,19,24

Table 215 Derating Values for DDR2-1066

tIS, tIH Derating Values for DDR2-1066									
		CK, $\overline{CK}$ Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Units	Notes
Command/Address Slew Rate V/ns	4.0	150	94	180	124	210	154	ps	1
	3.5	143	89	173	119	203	149		
	3.0	133	83	163	113	193	143		
	2.5	120	75	150	105	180	135		
	2.0	100	45	130	75	160	105		
	1.5	67	21	97	51	127	81		
	1.0	0	0	30	30	60	60		
	0.9	-5	-14	25	16	55	46		
	0.8	-13	-31	17	-1	47	29		
	0.7	-22	-54	8	-24	38	6		
	0.6	-34	-83	-4	-53	26	-23		
	0.5	-60	-125	-30	-95	0	-65		
	0.4	-100	-188	-70	-158	-40	-128		
	0.3	-168	-292	-138	-262	-108	-232		
	0.25	-200	-375	-170	-345	-140	-315		
	0.2	-325	-500	-295	-470	-265	-440		
	0.15	-517	-708	-487	-678	-457	-648		
	0.1	-1000	-1125	-970	-1095	-940	-1065		

Table 216 CA and CS_n Setup and Hold Base-Values for 1V/ns

Symbol	LPDDR2						Units	Reference
	1066	933	800	667	533	466		
tIS(base)	0	30	70	150	240	300	ps	$V_{IH/L(AC)} = V_{REF(DC)}$ +/- 220mV

Symbol	LPDDR2				Units	Reference
	400	333	266	200		
tIS(base)	300	440	600	850	ps	$V_{IH/L(AC)} = V_{REF(DC)}$ +/- 300mV

Table 217 Derating Values LPDDR2 tIS/tIH - AC/DC based AC220

△tIS, △tIH derating in [ps] AC/DC based AC220 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 220mV$, $V_{IL(AC)} = V_{REF(DC)} - 220mV$ DC130 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 130mV$, $V_{IL(DC)} = V_{REF(DC)} - 130mV$									
		CK_t, CK_c Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CA, CS_n Slew Rate V/ns	2.0	110	65	110	65	110	65	-	-
	1.5	74	43	73	43	73	43	89	59
	1.0	0	0	0	0	0	0	16	16
	0.9	-	-	-3	-5	-3	-5	13	11
	0.8	-	-	-	-	-8	-13	8	3
	0.7	-	-	-	-	-	-	2	-6
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tIS, △tIH derating in [ps] AC/DC based AC220 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 220mV$, $V_{IL(AC)} = V_{REF(DC)} - 220mV$ DC130 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 130mV$, $V_{IL(DC)} = V_{REF(DC)} - 130mV$									
		CK_t, CK_c Differential Slew Rate							
		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CA, CS_n Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	32	32	-	-	-	-	-	-
	0.9	29	27	45	43	-	-	-	-
	0.8	24	19	40	35	56	55	-	-
	0.7	18	10	34	26	50	46	66	78
	0.6	10	-3	26	13	42	33	58	65
	0.5	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-7	2	17	34

Table 218 Derating Values LPDDR2 tDS/tDH - AC/DC based AC300

△tDS, △tDH derating in [ps] AC/DC based AC300 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 300mV$, $V_{IL(AC)} = V_{REF(DC)} - 300mV$ DC200 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 200mV$, $V_{IL(DC)} = V_{REF(DC)} - 200mV$									
		DQS_t, DQS_c Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CA, CS_n Slew Rate V/ns	2.0	150	100	150	100	150	100	-	-
	1.5	100	67	100	67	100	67	116	83
	1.0	0	0	0	0	0	0	16	16
	0.9	-	-	-4	-8	-4	-8	12	8
	0.8	-	-	-	-	-12	-20	4	-4
	0.7	-	-	-	-	-	-	-3	-18
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tDS, △tDH derating in [ps] AC/DC based AC300 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 300mV$, $V_{IL(AC)} = V_{REF(DC)} - 300mV$ DC200 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 200mV$, $V_{IL(DC)} = V_{REF(DC)} - 200mV$									
		DQS_t, DQS_c Differential Slew Rate							
		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CA, CS_n Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	32	32	-	-	-	-	-	-
	0.9	28	24	44	40	-	-	-	-
	0.8	20	12	36	28	52	48	-	-
	0.7	13	-2	29	14	45	34	61	66
	0.6	2	-21	18	-5	34	15	50	47
	0.5	-	-	-12	-32	4	-12	20	20
	0.4	-	-	-	-	-35	-40	-11	-8

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

See Table 46 - Derating Values for DDR2- 400, DDR2- 533 and Table 47 - Derating Values for DDR2- 667, DDR2- 800 in the in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2- 1066) and Table 43 - Derating Values for DDR2- 1066 in thee *JESD208*.

Also see Table 104 - CA and CS_n Setup and Hold Base-Values for 1V/ns, Table 105 - Derating Values LPDDR2 tIS/tIH - AC/DC Based AC220 and Table 106 - Derating Values LPDDR2 tIS/tIH - AC/DC Based AC300 in the *JESD209-2B*.

PASS Condition

The measured time interval between the address/control setup time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1 Pre-condition the oscilloscope.
2 Trigger on either rising or falling edge of the address/control signal under test.
3 Find all crossings on rising edge of the signal under test that cross $V_{IH(AC)}$.
4 Find all crossings on falling edge of the signal under test that cross $V_{IL(AC)}$.
5 For all the crossings found, locate the nearest Clock crossings that cross 0V.

   Note: For LPDDR2 with PUT=CA option, the Clock crossing could be Clock rising or Clock falling. For other cases, the Clock crossing must be Clock rising only.
6 Take the time different of the signal under test's crossings to the corresponding clock crossing as tIS.
7 Collect all measured tIS.
8 Report the worst tIS measured as test result.
9 Measure the mean slew rate for all the ADD/CMD and CK edges.
10 Use the mean slew rate for ADD/CMD and CK to determine the ΔtIS derating value based on the derating tables.
11 The test limit for tIS test = tIS(base) + ΔtIS.

tIH(derate), Address and Control Input Hold Time with Derating Support - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control or command/address (rising or falling edge) hold time to the associated clock crossing edge is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2, LPDDR2

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Address Signal OR Control Signal OR Command/Address
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Address Signal OR Control Signal OR Command/Address
- Clock Signal

Test Definition Notes from the Specification

Table 219 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input hold time	tIH(base)	475	x	375	x	ps	5,7,9,23

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input hold time	tIS(base)	275	x	250	x	ps	5,7,9,23,29

Table 220 Derating Values for DDR2-400, DDR2-533

tIS, tIH Derating Values for DDR2-400, DDR2-533									
		CK, $\overline{CK}$ Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Units	Notes
Command/Address Slew Rate V/ns	4.0	187	94	217	124	247	154	ps	1
	3.5	179	89	200	119	239	149		
	3.0	167	83	197	113	227	143		
	2.5	150	75	180	105	210	135		
	2.0	125	45	155	75	185	105		
	1.5	83	21	113	51	143	81		
	1.0	0	0	30	30	60	60		
	0.9	-11	-14	19	16	49	46		
	0.8	-25	-31	5	-1	35	29		
	0.7	-43	-54	-13	-24	17	6		
	0.6	-67	-83	-37	-53	-7	-23		
	0.5	-110	-125	-80	-95	-50	-65		
	0.4	-175	-188	-145	-158	-115	-128		
	0.3	-285	-292	-255	-262	-225	-232		
	0.25	-350	-375	-320	-345	-290	-315		
	0.2	-525	-500	-495	-470	-455	-440		
	0.15	-800	-708	-770	-678	-740	-648		
	0.1	-1450	-1125	-1420	-1095	-1390	-1065		

Table 221 Derating Values for DDR2-667, DDR2-800

tIS, tIH Derating Values for DDR2-667, DDR2-800									
		CK, $\overline{CK}$ Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Units	Notes
Command/Address Slew Rate V/ns	4.0	150	94	180	124	210	154	ps	1
	3.5	143	89	173	119	203	149		
	3.0	133	83	163	113	193	143		
	2.5	120	75	150	105	180	135		
	2.0	100	45	130	75	160	105		
	1.5	67	21	97	51	127	81		
	1.0	0	0	30	30	60	60		
	0.9	-5	-14	25	16	55	46		
	0.8	-13	-31	17	-1	47	29		
	0.7	-22	-54	8	-24	38	6		
	0.6	-34	-83	-4	-53	26	-23		
	0.5	-60	-125	-30	-95	0	-65		
	0.4	-100	-188	-70	-158	-40	-128		
	0.3	-168	-292	-138	-262	-108	-232		
	0.25	-200	-375	-170	-345	-140	-315		
	0.2	-325	-500	-295	-470	-265	-440		
	0.15	-517	-708	-487	-678	-457	-648		
	0.1	-1000	-1125	-970	-1095	-940	-1065		

Table 222 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units	Specific Notes
		Min	Max		
Address and control input setup time	tIH(base)	200	x	ps	5,7,9,19,24

Table 223 Derating Values for DDR2-1066

tIS, tIH Derating Values for DDR2-1066									
		CK, $\overline{CK}$ Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Units	Notes
Command/Address Slew Rate V/ns	4.0	150	94	180	124	210	154	ps	1
	3.5	143	89	173	119	203	149		
	3.0	133	83	163	113	193	143		
	2.5	120	75	150	105	180	135		
	2.0	100	45	130	75	160	105		
	1.5	67	21	97	51	127	81		
	1.0	0	0	30	30	60	60		
	0.9	-5	-14	25	16	55	46		
	0.8	-13	-31	17	-1	47	29		
	0.7	-22	-54	8	-24	38	6		
	0.6	-34	-83	-4	-53	26	-23		
	0.5	-60	-125	-30	-95	0	-65		
	0.4	-100	-188	-70	-158	-40	-128		
	0.3	-168	-292	-138	-262	-108	-232		
	0.25	-200	-375	-170	-345	-140	-315		
	0.2	-325	-500	-295	-470	-265	-440		
	0.15	-517	-708	-487	-678	-457	-648		
	0.1	-1000	-1125	-970	-1095	-940	-1065		

Table 224 CA and CS_n Setup and Hold Base-Values for 1V/ns

Symbol	LPDDR2						Units	Reference
	1066	933	800	667	533	466		
tIH(base)	90	120	160	240	330	390	ps	$V_{IH/L(AC)} = V_{REF(DC)}$ +/- 130mV

Symbol	LPDDR2				Units	Reference
	400	333	266	200		
tIH(base)	400	540	700	950	ps	$V_{IH/L(AC)} = V_{REF(DC)}$ +/- 200mV

Table 225 Derating Values LPDDR2 tIS/tIH - AC/DC based AC220

△tIS, △tIH derating in [ps] AC/DC based AC220 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 220mV$, $V_{IL(AC)} = V_{REF(DC)} - 220mV$ DC130 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 130mV$, $V_{IL(DC)} = V_{REF(DC)} - 130mV$									
		CK_t, CK_c Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CA, CS_n Slew Rate V/ns	2.0	110	65	110	65	110	65	-	-
	1.5	74	43	73	43	73	43	89	59
	1.0	0	0	0	0	0	0	16	16
	0.9	-	-	-3	-5	-3	-5	13	11
	0.8	-	-	-	-	-8	-13	8	3
	0.7	-	-	-	-	-	-	2	-6
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tIS, △tIH derating in [ps] AC/DC based AC220 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 220mV$, $V_{IL(AC)} = V_{REF(DC)} - 220mV$ DC130 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 130mV$, $V_{IL(DC)} = V_{REF(DC)} - 130mV$									
		CK_t, CK_c Differential Slew Rate							
		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CA, CS_n Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	32	32	-	-	-	-	-	-
	0.9	29	27	45	43	-	-	-	-
	0.8	24	19	40	35	56	55	-	-
	0.7	18	10	34	26	50	46	66	78
	0.6	10	-3	26	13	42	33	58	65
	0.5	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-7	2	17	34

Table 226 Derating Values LPDDR2 tDS/tDH - AC/DC based AC300

△tDS, △tDH derating in [ps] AC/DC based AC300 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 300mV$, $V_{IL(AC)} = V_{REF(DC)} - 300mV$ DC200 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 200mV$, $V_{IL(DC)} = V_{REF(DC)} - 200mV$									
		CK_t, CK_c Differential Slew Rate							
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CA, CS_n Slew Rate V/ns	2.0	150	100	150	100	150	100	-	-
	1.5	100	67	100	67	100	67	116	83
	1.0	0	0	0	0	0	0	16	16
	0.9	-	-	-4	-8	-4	-8	12	8
	0.8	-	-	-	-	-12	-20	4	-4
	0.7	-	-	-	-	-	-	-3	-18
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-

△tDS, △tDH derating in [ps] AC/DC based AC300 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 300mV$, $V_{IL(AC)} = V_{REF(DC)} - 300mV$ DC200 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 200mV$, $V_{IL(DC)} = V_{REF(DC)} - 200mV$									
		CK_t, CK_c Differential Slew Rate							
		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CA, CS_n Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	32	32	-	-	-	-	-	-
	0.9	28	24	44	40	-	-	-	-
	0.8	20	12	36	28	52	48	-	-
	0.7	13	-2	29	14	45	34	61	66
	0.6	2	-21	18	-5	34	15	50	47
	0.5	-	-	-12	-32	4	-12	20	20
	0.4	-	-	-	-	-35	-40	-11	-8

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

See Table 46 - Derating Values for DDR2- 400, DDR2- 533 and Table 47 - Derating Values for DDR2- 667, DDR2- 800 in the in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2- 1066) and Table 43 - Derating Values for DDR2- 1066 in thee *JESD208*.

Also see Table 104 - CA and CS_n Setup and Hold Base-Values for 1V/ns, Table 105 - Derating Values LPDDR2 tIS/tIH - AC/DC Based AC220 and Table 106 - Derating Values LPDDR2 tIS/tIH - AC/DC Based AC300 in the *JESD209-2B*.

PASS Condition

The measured time interval between the address/control hold time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope.
2. Trigger on either rising or falling edge of the address/control signal under test.
3. Find all crossings on rising edge of the signal under test that cross $V_{IL(DC)}$.
4. Find all crossings on falling edge of the signal under test that cross $V_{IH(DC)}$.
5. For all the crossings found, locate the nearest Clock crossings that cross 0V.

   Note: For LPDDR2 with PUT=CA option, the Clock crossing could be Clock rising or Clock falling. For other cases, the Clock crossing must be Clock rising only.
6. Take the time different of the signal under test's crossings to the corresponding clock crossing as tIH.
7. Collect all measured tIH.
8. Report the worst tIH measured as test result.
9. Measure the mean slew rate for all the ADD/CMD and CK edges.
10. Use the mean slew rate for ADD/CMD and CK to determine the ΔtIH derating value based on the derating tables.
11. The test limit for tIH test = tIH(base) + ΔtIH.

tVAC (CS, CA), Time Above $V_{IH(AC)}$/Below $V_{IL(AC)}$ - Test Method of Implementation

The purpose of this test is to verify that the time the command/address signal is above $V_{IH(AC)}$ and below $V_{IL(AC)}$ is within the conformance limits as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Command/Address Signal (LPDDR2 only) OR
- Control Signal

Signals required to perform the test on the oscilloscope:

- Command/Address Signal OR
- Control Signal

Test Definition Notes from the Specification

Table 227 Required time tVAC above $V_{IH(AC)}$ {below $V_{IL(AC)}$} for valid transition

Slew Rate	tVAC @ 300 mV [ps]		tVAC @ 220 mV [ps]	
	Min	Max	Min	Max
>2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	1
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
<0.5	0	-	150	-

Test References

See Table 107 - Required time tVAC above $V_{IH(AC)}$ {below $V_{IL(AC)}$} for valid transition in the *JESD209-2B*.

PASS Condition

The worst measured tVAC(CS, CA) should be within the specification limit.

Measurement Algorithm

1 Pre-condition the oscilloscope setting.
2 Trigger on either a rising or falling edge of the command/address/control signal under test.
3 Find all of the rising/falling edges of the signal under tests that cross $V_{IL(AC)}$.
4 Find all of the rising/falling edges of the signal under tests that cross $V_{IH(AC)}$.
5 tVAC(CS,CA) is the time interval starting from a rising $V_{IH(AC)}$ crossing point and ending at the following falling $V_{IH(AC)}$ crossing point.
6 tVAC(CS,CA) is also the time interval starting from a falling $V_{IL(AC)}$ crossing point and ending at the following rising $V_{IL(AC)}$ crossing point.
7 Collect all tVAC(CS,CA) results.
8 Determine the worst result from the set of tVAC(CS,CA) measured.
9 Report the worst result from the set of tVAC(CS,CA) measured. No compliance limit checking is performed for this test. You need to manually check the test status (pass/fail) of this test based on the worst tVAC(CS,CA) and slew rate reported.

tIPW, Address and Control Input Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the high or low level of address or control or command/address signal must be within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: DDR2. LPDDR2

Signal cycle of interest: WRITE

Require Read/Write separation: No

Signal(s) of Interest:

- Address Signal (DDR2 only) OR Command/Address Signal (LPDDR2 only) OR Control Signal

Signals required to perform the test on the oscilloscope:

- Address Signal (DDR2 only) OR Command/Address Signal (LPDDR2 only) OR Control Signal

Test Definition Notes from the Specification

Table 228 Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) & (DDR2-667 and DDR2-800)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK	

Parameter	Symbol	DDR2-667		DDR2-800		Units[34]	Specific Notes
		Min	Max	Min	Max		
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK(avg)	

Table 229 Timing Parameters by Speed Grade (DDR2-1066)

Parameter	Symbol	DDR2-1066		Units[29]	Specific Notes
		Min	Max		
Control & Address input pulse width for each input	tIPW	0.6	x	tCK(avg)	

Table 230 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*[5]	400	333	266*[5]	200*[5]	
Command Address Input Parameters*[14]														
Address and control input pulse width	tIPW	Min							0.40					$t_{CK(avg)}$

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800) in the *JEDEC Standard JESD79-2E*.

See Table 41 - Timing Parameters by Speed Grade (DDR2-1066) in the *JESD208*.

Also see Table 103 - LPDDR2 AC Timing Table in the *JEDEC Standard JESD209-2B*.

PASS Condition

The worst measured tIPW shall be within the specification limit.

Measurement Algorithm

1. Pre-condition the oscilloscope settings.
2. Triggered on either rising or falling edge of the command/address/control signal under test.
3. Find all crossings on rising/falling edge of the signal under test that cross V_{REF}.
4. tIPW is time started from a rising/falling edge of the signal under test and ended at the following falling/rising (following edge should not same direction) edge.
5. Collect all tIPW.
6. Determine the worst result from the set of tIPW measured.

tISCKE, CKE Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from Clock Enable signal (CKE rising/falling edge) setup time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Require Read/Write Separation: No

Signal(s) of Interest:

- Clock Enable Signal

Signals required to perform the test on the oscilloscope:

- Clock Enable Signal
- Clock Signal

Test Definition Notes from the Specification

Table 231 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				CKE Input Parameters* 14										
CKE input setup time	tISCKE	Min		0.25										$t_{CK(avg)}$

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JEDEC Standard JESD209-2B*.

PASS Condition

The measured time interval between Clock Enable (CKE) setup time to respective clock crossing point shall be within the specification limit.

Measurement Algorithm

1 Pre-condition the oscilloscope.
2 Triggered on either rising or falling edge of the Clock Enable signal under test.
3 Find all crossings on rising edge of the signal under test that cross $V_{IH(AC)}$.
4 Find all crossings on falling edge of the signal under test that cross $V_{IL(AC)}$.
5 For all the crossings found, locate the nearest rising Clock crossings on the right that cross 0V.
6 Take the time difference of the signal under test's crossings to the corresponding clock crossing as tISCKE.
7 Collect all measured tISCKE.
8 Report the worst tISCKE measured as test result.
9 Compare the test result to the compliance test limit.

tIHCKE, CKE Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from Clock Enable signal (CKE rising/falling edge) hold time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Require Read/Write Separation: No

Signal(s) of Interest:

- Clock Enable Signal

Signals required to perform the test on the oscilloscope:

- Clock Enable Signal
- Clock Signal

Test Definition Notes from the Specification

Table 232 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				CKE Input Parameters* 14										
CKE input hold time	tIHCKE	Min		0.25										$t_{CK(avg)}$

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JEDEC Standard JESD209-2B*.

PASS Condition

The measured time interval between Clock Enable (CKE) hold time to respective clock crossing point shall be within the specification limit.

Measurement Algorithm

1 Pre-condition the oscilloscope.
2 Triggered on either rising or falling edge of the Clock Enable signal under test.
3 Find all crossings on rising edge of the signal under test that cross $V_{IL(DC)}$.
4 Find all crossings on falling edge of the signal under test that cross $V_{IH(DC)}$.
5 For all the crossings found, locate the nearest rising Clock crossings on the right that cross 0V.
6 Take the time difference of the signal under test's crossings to the corresponding clock crossing as tIHCKE.
7 Collect all measured tIHCKE.
8 Report the worst tIHCKE measured as test result.
9 Compare the test result to the compliance test limit.

tISCKEb, CKE Input Setup Time (Boot Parameter) - Test Method of Implementation

The purpose of this test is to verify that the time interval from Clock Enable signal (CKE rising/falling edge) setup time to the associated clock crossing edge for boot parameter must be within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Require Read/Write Separation: No

Signal(s) of Interest:

- Clock Enable Signal

Signals required to perform the test on the oscilloscope:

- Clock Enable Signal
- Clock Signal

Test Definition Notes from the Specification

Table 233 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Boot Parameters (10 MHz - 55 MHz))* 8,10,11										
CKE input setup time	tISCKEb	Min		2.5										ns

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JEDEC Standard JESD209-2B*.

PASS Condition

The measured time interval between Clock Enable (CKE) setup time to respective clock crossing point shall be within the specification limit.

Measurement Algorithm

1 Pre-condition the oscilloscope.
2 Triggered on either rising or falling edge of the Clock Enable signal under test.
3 Find all crossings on rising edge of the signal under test that cross $V_{IH(AC)}$.
4 Find all crossings on falling edge of the signal under test that cross $V_{IL(AC)}$.
5 For all the crossings found, locate the nearest rising Clock crossings on the right that cross 0V.
6 Take the time difference of the signal under test's crossings to the corresponding clock crossing as tIHCKE.
7 Collect all measured tISCKEb.
8 Report the worst tISCKEb measured as test result.
9 Compare the test result to the compliance test limit.

tIHCKEb, CKE Input Hold Time (Boot Parameter) - Test Method of Implementation

The purpose of this test is to verify that the time interval from Clock Enable signal (CKE rising/falling edge) hold time to the associated clock crossing edge for boot parameter must be within the conformance limit as specified in the JEDEC specification.

Signals of Interest

Mode Supported: LPDDR2 only

Signal cycle of interest: WRITE

Require Read/Write Separation: No

Signal(s) of Interest:

- Clock Enable Signal

Signals required to perform the test on the oscilloscope:

- Clock Enable Signal
- Clock Signal

Test Definition Notes from the Specification

Table 234 LPDDR2 AC Timing Table

Parameter	Symbol	Min Max	Min t_{CK}	LPDDR2										Unit
				1066	933	800	677	533	466*5	400	333	266*5	200*5	
				Boot Parameters (10 MHz - 55 MHz))* 8,10,11										
CKE input hold time	tIHCKEb	Min		2.5										ns

Test References

See Table 103 - LPDDR2 AC Timing Table in the *JEDEC Standard JESD209-2B*.

PASS Condition

The measured time interval between Clock Enable (CKE) hold time to respective clock crossing point shall be within the specification limit.

Measurement Algorithm

1 Pre-condition the oscilloscope.
2 Triggered on either rising or falling edge of the Clock Enable signal under test.
3 Find all crossings on rising edge of the signal under test that cross $V_{IL(DC)}$.
4 Find all crossings on falling edge of the signal under test that cross $V_{IH(DC)}$.
5 For all the crossings found, locate the nearest rising Clock crossings on the right that cross 0V.
6 Take the time difference of the signal under test's crossings to the corresponding clock crossing as tIHCKEb.
7 Collect all measured tIHCKEb.
8 Report the worst tIHCKEb measured as test result.
9 Compare the test result to the compliance test limit.

18 Custom Mode Read-Write Eye-Diagram Tests

This section provides the Methods of Implementation (MOIs) for Advanced Debug Mode Read-Write Eye-Diagram tests using a Keysight 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, differential solder-in probe head and the DDR2(+LP) Compliance Test Application.

Probing for Custom Mode Read-Write Eye Diagram Tests

When performing the Custom Mode Read-Write Eye Diagram tests, the DDR2(+LP) Compliance Test Application will prompt you to make the proper connections as shown in Figure 36.

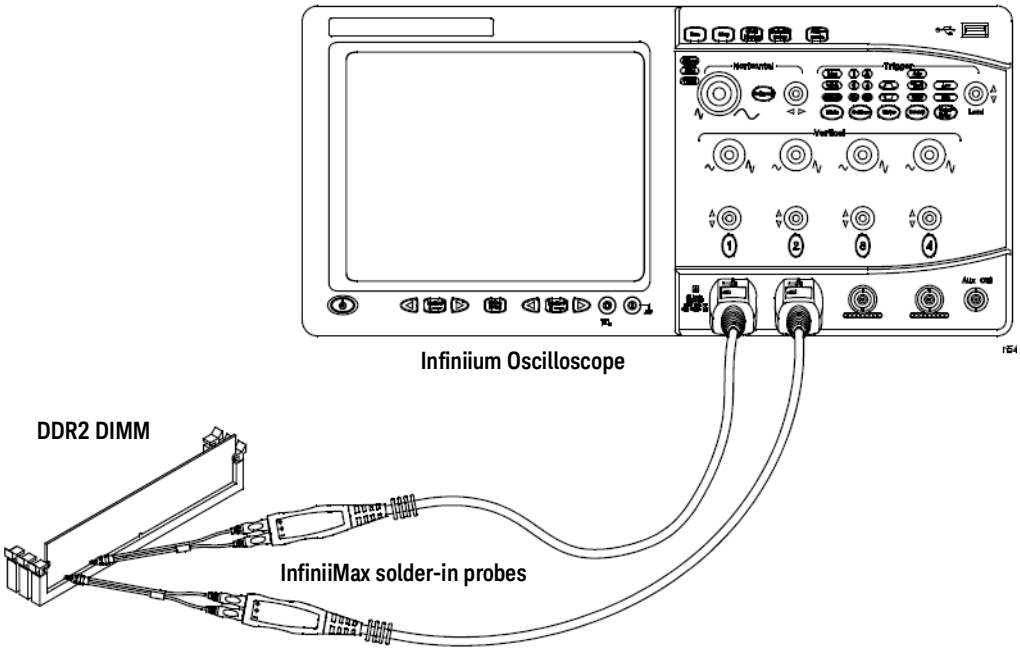


Figure 36 Probing for Custom Mode Read-Write Eye Diagram Tests

You can use any of the oscilloscope channels as the Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2(+LP) Compliance Test Application. (The channels shown in Figure 36 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 20, “InfiniiMax Probing,” starting on page 349.

Test Procedure

1 Start the automated test application as described in "Starting the DDR2(+LP) Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer systems where the DDR2 Device Under Test (DUT) is attached. This software will perform a test on all the unused RAM on the system by producing repetitive bursts of read-write data signals to the DDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2 devices.

4 Connect the oscilloscope probes to any of the oscilloscope channels.

5 In the DDR2 Test application, click the Set Up tab.

6 Select Custom as the Test Mode option. This selection shows an additional command button - Set Mask File.

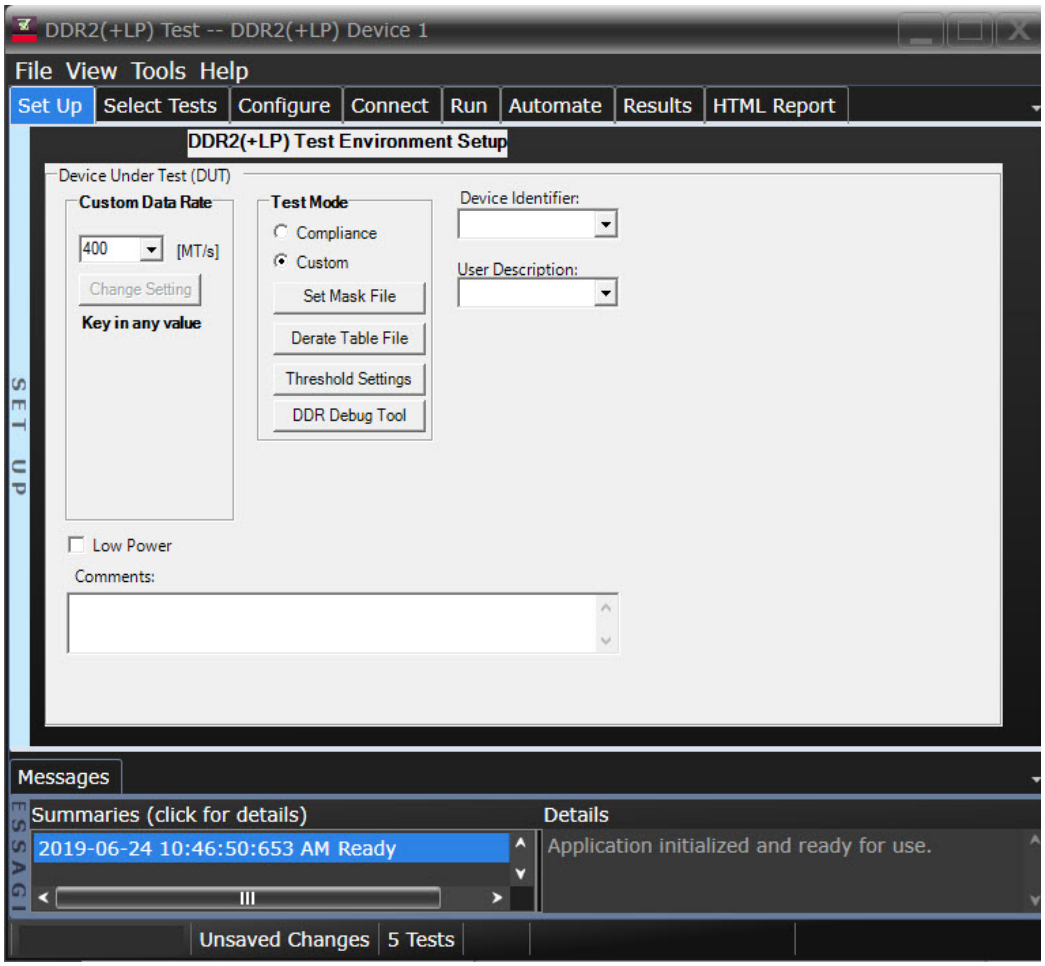


Figure 37 Selecting Custom Test Mode

7 Click this button to view or select test mask files for eye diagram tests.

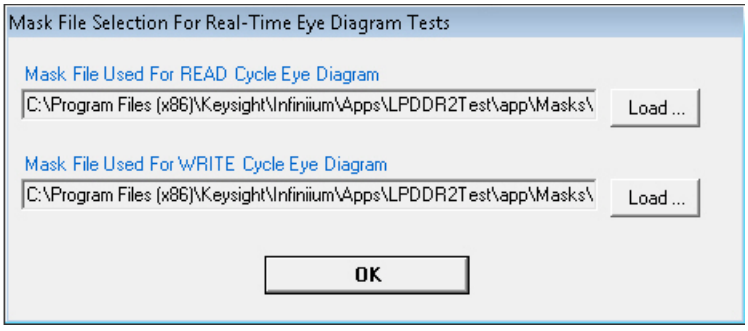


Figure 38 Selecting Test Mask for Eye Diagram Tests

8 Advanced Debug Mode also allows you to type in the data rate of the DUT signal.

9 Type in or select the Device Identifier as well as the User Description from the drop-down list. Enter your comments in the Comments text box.

10 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group

.

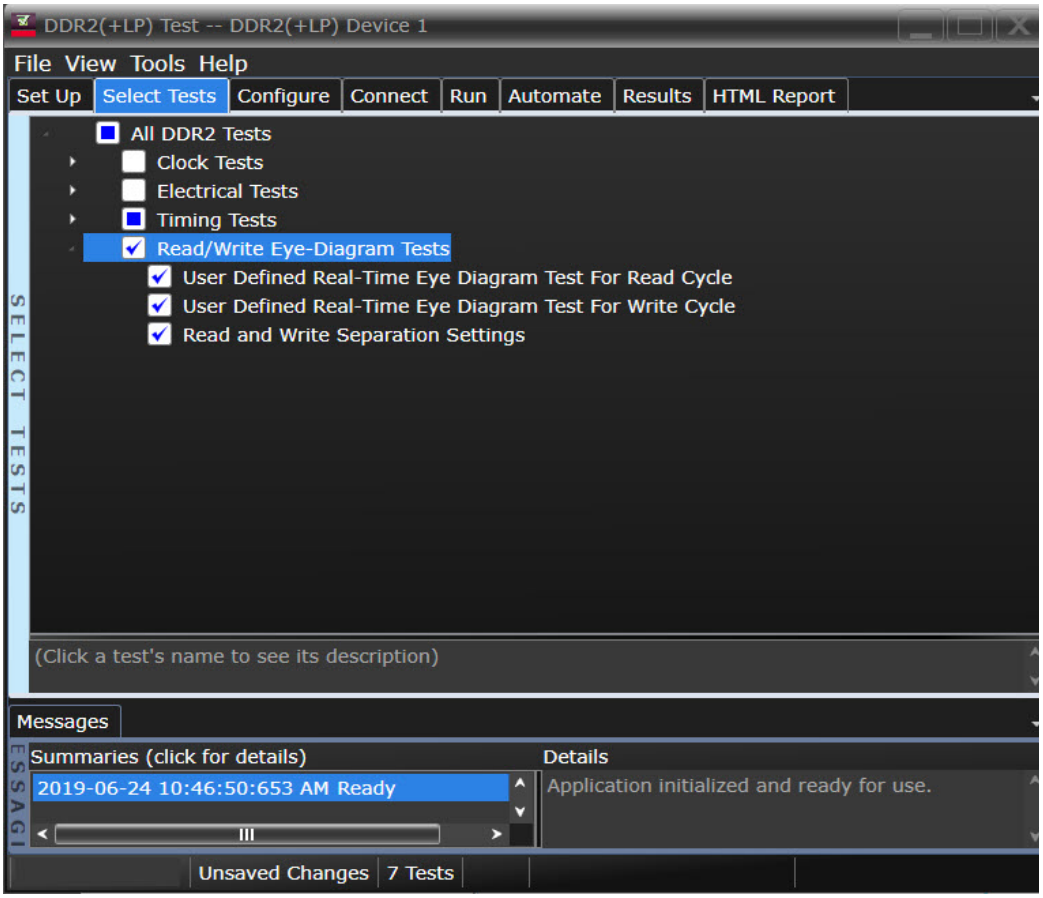


Figure 39 Selecting Advanced Debug Read-Write Eye-Diagram Tests

11 Follow the DDR2 Test application's task flow to set up the configuration options, run the tests and view the tests results.

User Defined Real-Time Eye Diagram Test for Read Cycle Method of Implementation

The Advanced Debug Mode Read-Write Eye Diagram test can be divided into two sub-tests. One of them is the User Defined Real-Time Eye Diagram Test for Read Cycle. There is no available specification on the eye test in JEDEC specifications. Mask testing is definable by the customers for their evaluation tests purpose. The purpose of this test is to automate all the required setup procedures in order to generate an eye diagram for the DDR2 data READ cycle. This additional feature of mask test allows you to perform evaluation and debugging on the created eye diagram. The test will show a fail status if the total failed waveforms is greater than 0.

Signals of Interest

Signal cycle of interest: READ

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - DQ Signal
- Supporting Pin - DQS Signal

Measurement Algorithm

1. Use the Setup time and Hold time to find and capture the Read cycle.
2. Setup the oscilloscope to generate eye diagram.
3. Start the mask test.
4. Loop until the number of required waveforms is acquired.
5. Obtain and display the total failed waveforms as the test result.

User Defined Real-Time Eye Diagram Test for Write Cycle Method of Implementation

Just as in the previous test, there is no available specification on the eye diagram test in the JEDEC specifications for User Defined Real-Time Eye Diagram Test for Write Cycle. Mask testing is definable by the customers for their evaluation tests purpose. The purpose of this test is to automate all the required setup procedures in order to generate an eye diagram for the DDR2 data WRITE cycle. This additional feature of mask test allows you to perform evaluation and debugging on the created eye diagram. The test will show a fail status if the total failed waveforms is greater than 0.

Signals of Interest

Signal cycle of interest: WRITE

Signal(s) of Interest:

- Data Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test, PUT - DQ Signal
- Supporting Pin - DQS Signal

Measurement Algorithm

1. Use the Setup time and Hold time to find and capture the Write cycle.
2. Setup the oscilloscope to generate eye diagram.
3. Start the mask test.
4. Loop until the number of required waveforms is acquired.
5. Return the total failed waveforms as the test result.

19 Calibrating the Infiniium Oscilloscope and Probe

This section describes the Keysight Infiniium digital storage oscilloscope calibration procedures.

Required Equipment for Oscilloscope Calibration

To calibrate the Infiniium oscilloscope in preparation for running the DDR2 automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Keysight p/n 54855-67604, qty = 2 (provided with the Keysight Infiniium oscilloscope).
- Calibration cable (provided with the 80000B and 90000A series Infiniium oscilloscopes). Use a good quality 50 Ω BNC cable.
- BNC shorting cap.

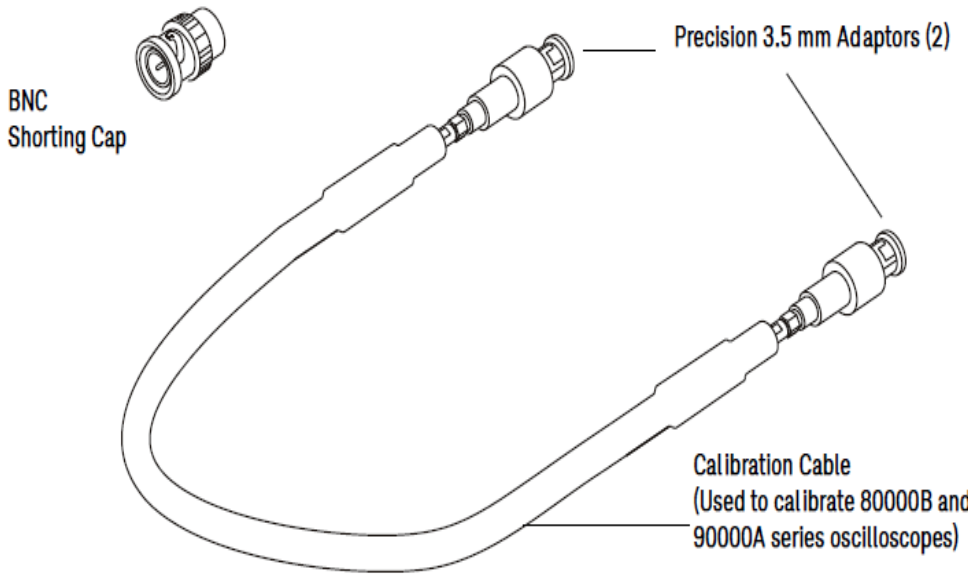


Figure 40 Accessories Provided with the Keysight Infiniium Oscilloscope

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Keysight oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:
   a Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.
   b Plug in the power cord.
   c Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.
   d Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:
   a Locate the BNC shorting cap.
   b Locate the calibration cable.
   c Locate the two Keysight precision SMA/BNC adapters.
   d Attach one SMA adapter to the other end of the calibration cable - hand tighten snugly.
   e Attach another SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 41 below, perform the following steps:
   a Click on the Utilities>Calibration menu to open the Calibration dialog box.

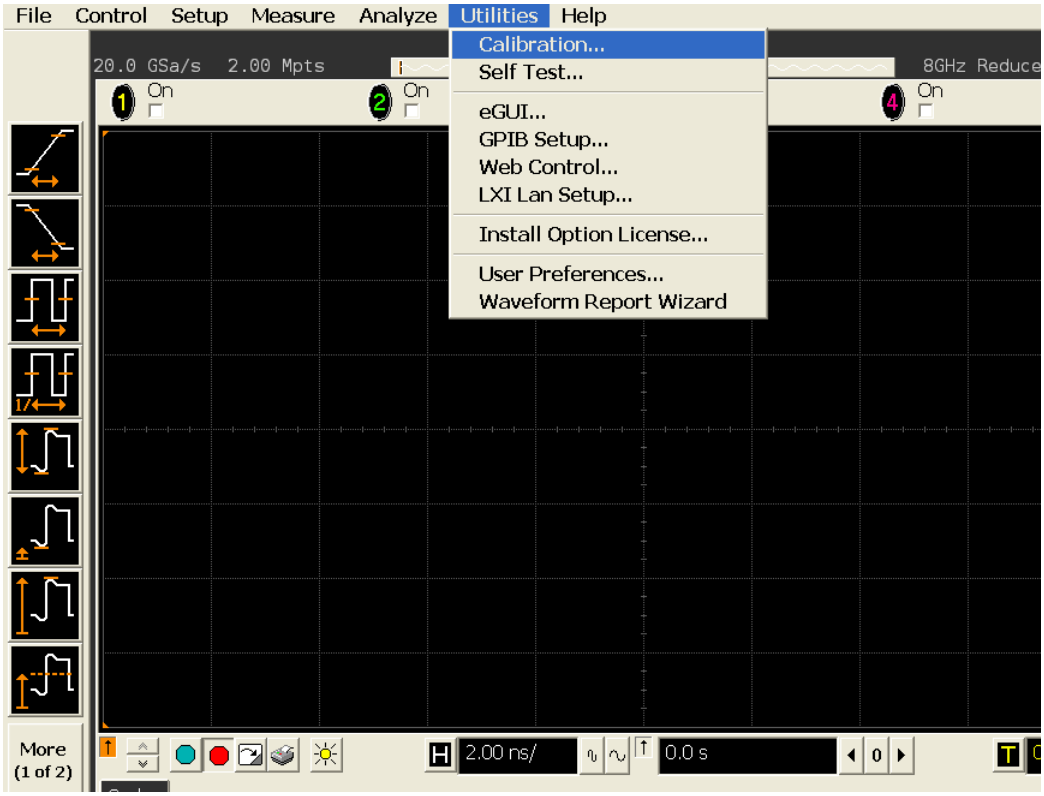


Figure 41 Accessing the Calibration Menu

4 Referring to Figure 42 below, perform the following steps to start the calibration:

b Uncheck the Cal Memory Protect checkbox.

c Click the Start button to begin the calibration.

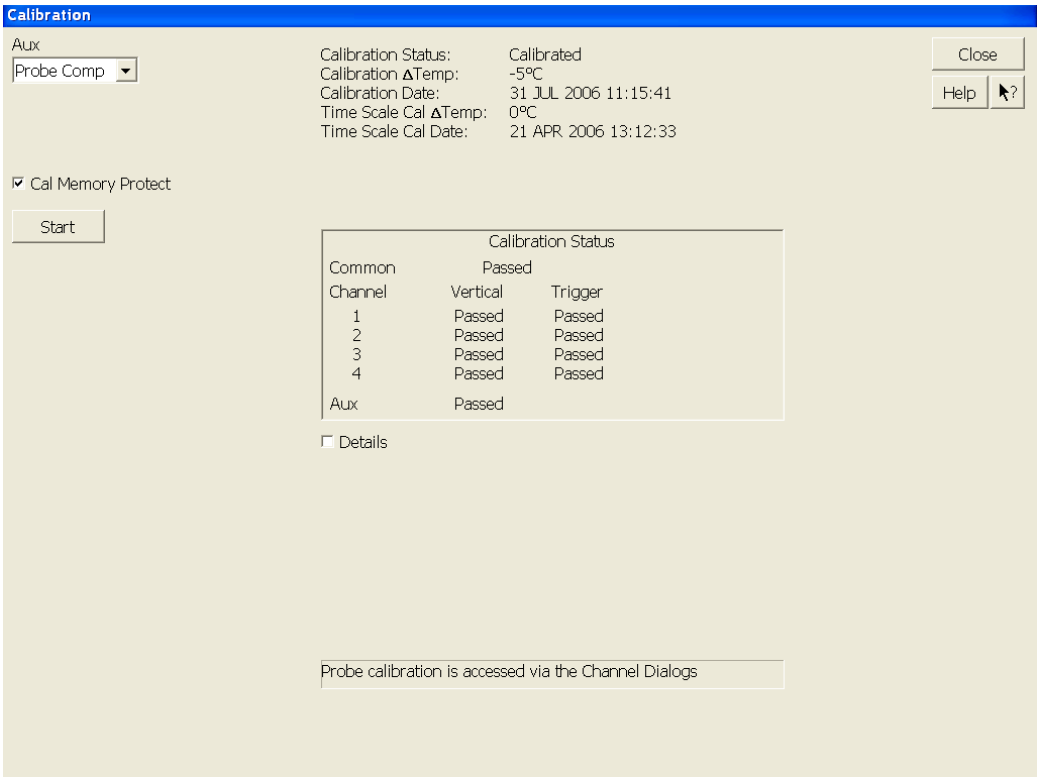


Figure 42 Oscilloscope Calibration Window

d During the calibration of channel 1, if you are prompted to perform a Time Scale Calibration, as shown in Figure 43 below.

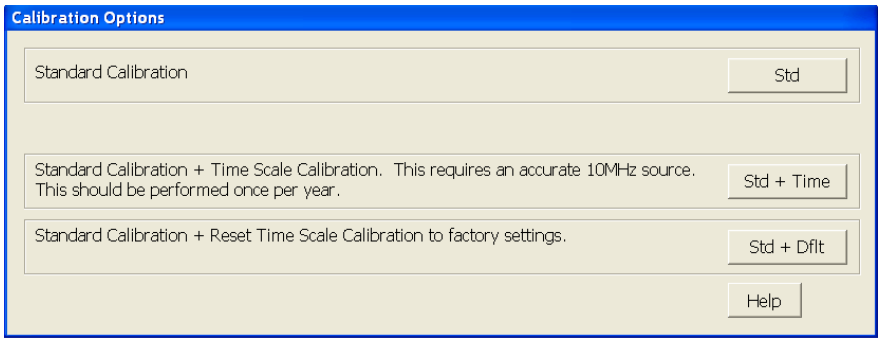


Figure 43 Time Scale Calibration Dialog box

e Click on the Std+Dflt button to continue the calibration, using the Factory default calibration factors.

f When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

g Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

h Click the Close button to close the calibration window.

i The internal calibration is completed.

j Read NOTE below.

NOTE

These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Required Equipment for Probe Calibration

Before performing DDR2 tests you should calibrate the probes. Calibration of the solder-in probe heads consist of a vertical calibration and a skew calibration. The vertical calibration should be performed before the skew calibration. Both calibrations should be performed for best probe measurement performance.

The calibration procedure requires the following parts.

- BNC (male) to SMA (male) adaptor
- Deskew fixture
- 50 Ω SMA terminator

Probe Calibration

Connecting the Probe for Calibration

For the following procedure, refer to Figure 44 below.

1 Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.

2 Connect the 50 Ω SMA terminator to the connector farthest from yellow pincher.

3 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.

4 Connect the probe to an oscilloscope channel.

5 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.

6 Push down the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.

7 Release the yellow pincher.

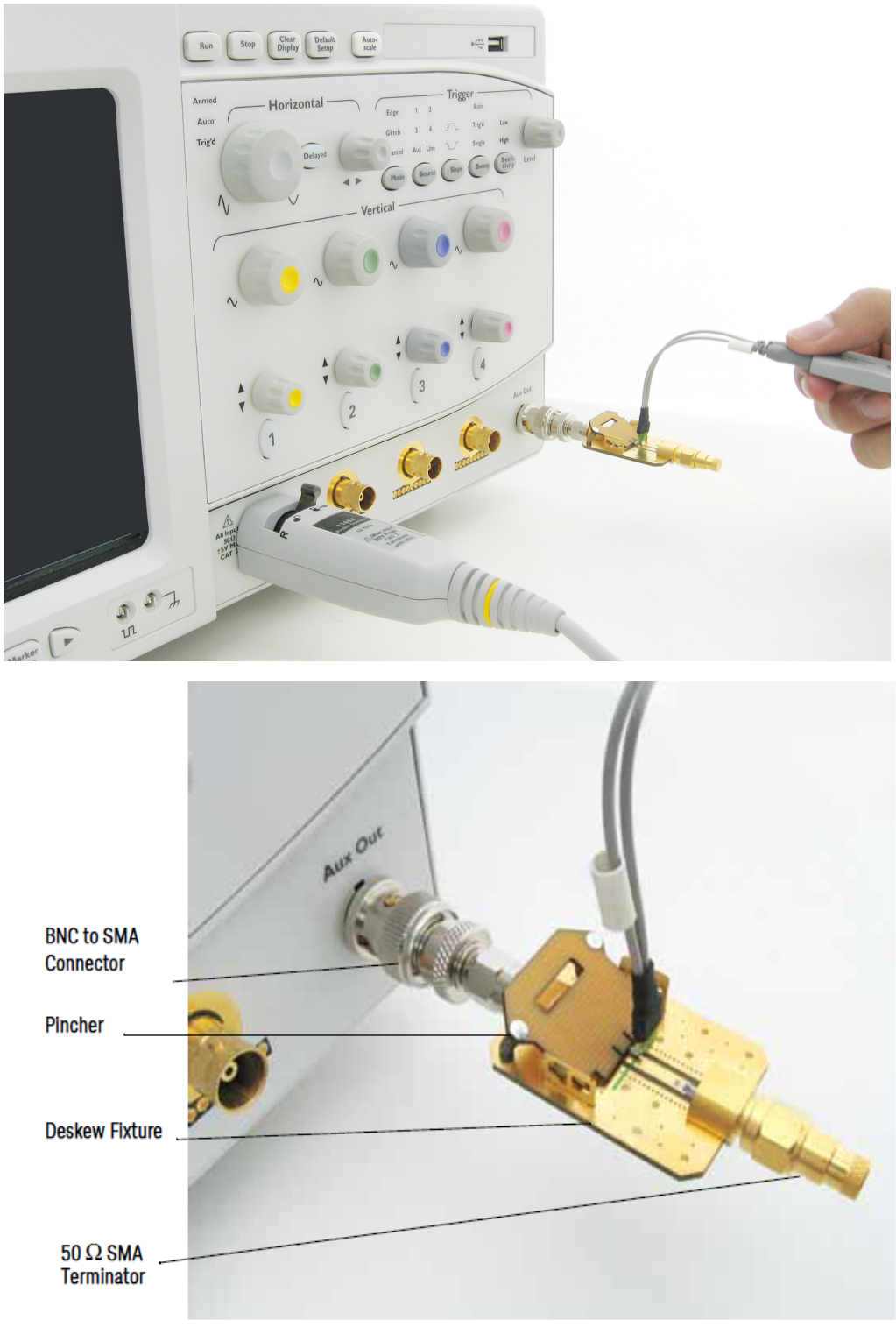


Figure 44 Solder-in Probe Head Calibration Connection Example

Verifying the Connection

1 On the Infiniium oscilloscope, press the autoscale button on the front panel.
2 Set the volts per division to 100 mV/div.
3 Set the horizontal scale to 1.00 ns/div.
4 Set the horizontal position to approximately 3 ns. You should see a waveform similar to that in Figure 45 below.

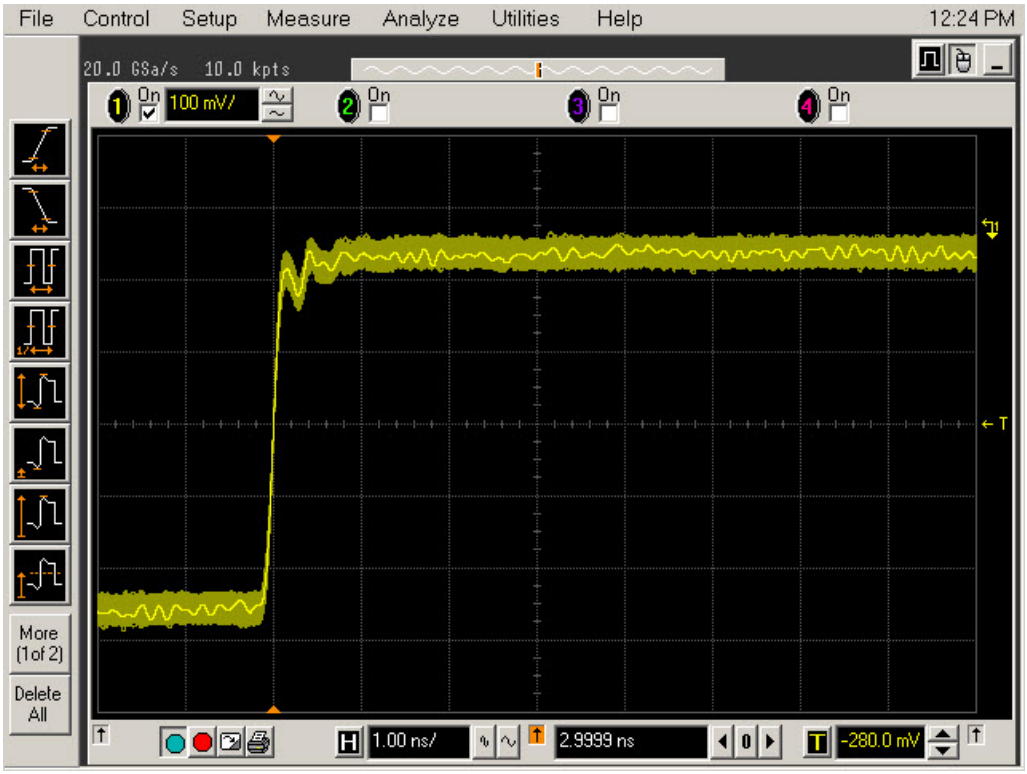


Figure 45 Good Connection Waveform Example

If you see a waveform similar to that of Figure 46 below, then you have a bad connection and should check all of your probe connections.

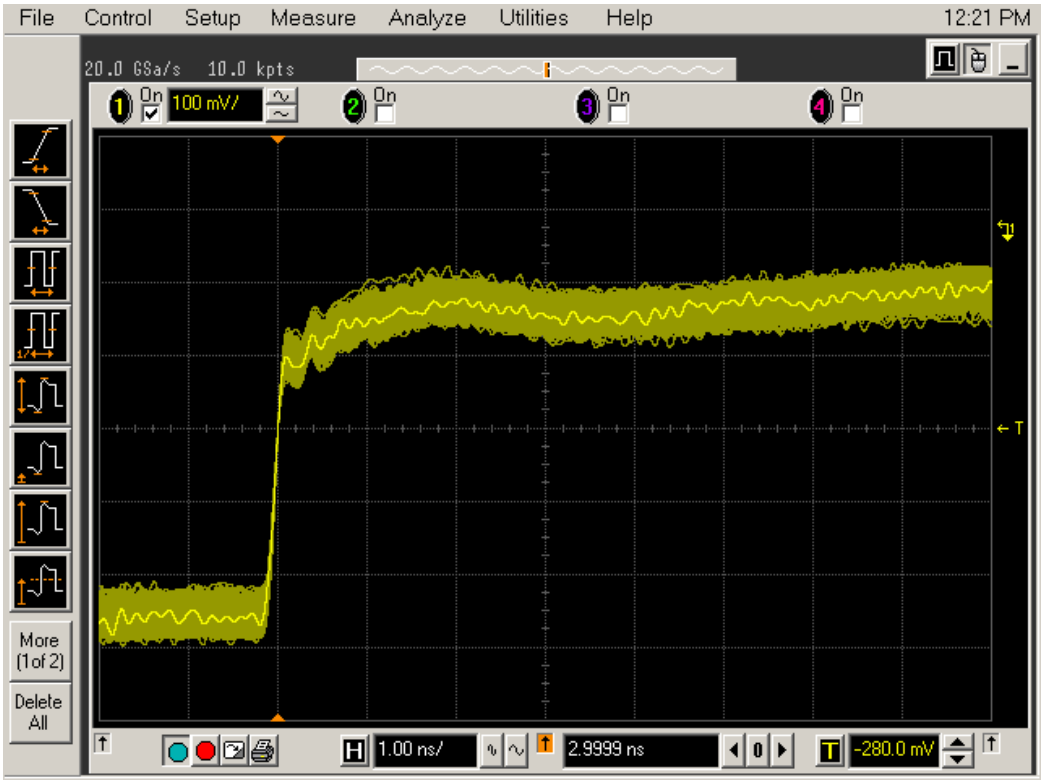


Figure 46 Bad Connection Waveform Example

Running the Probe Calibration and Deskew

1 On the Infiniium oscilloscope in the Setup menu, select the channel connected to the probe, as shown in Figure 47.

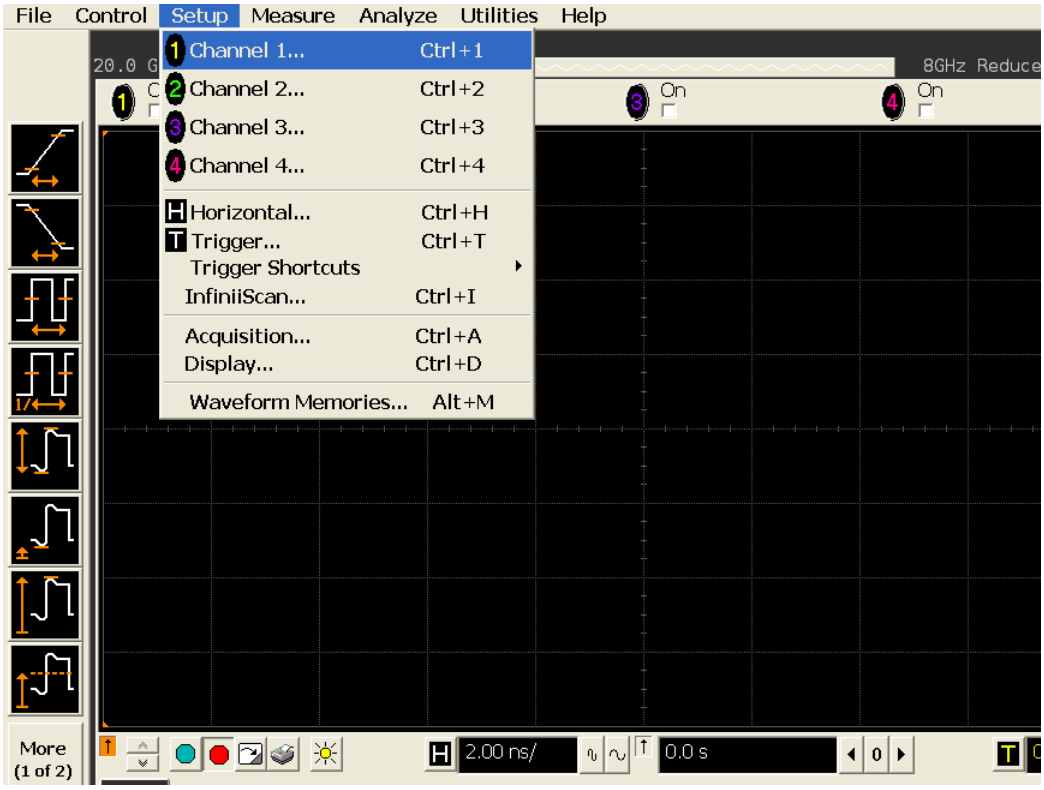


Figure 47 Channel Setup Window.

2 In the Channel Setup dialog box, select the Probes... button, as shown in Figure 48.

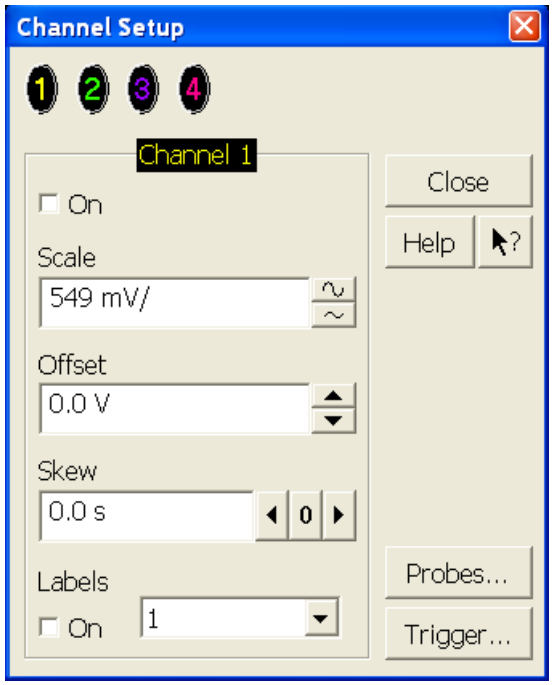


Figure 48 Channel Dialog Box

3 In the Probe Setup dialog box, select the Calibrate Probe... button.

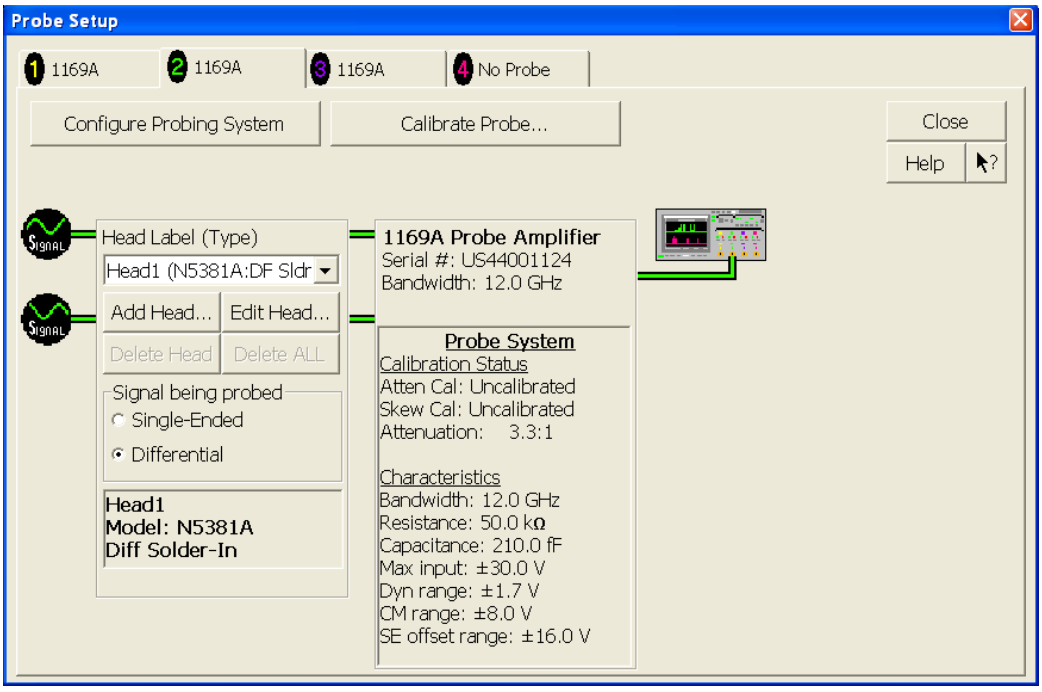


Figure 49 Probe Setup Window.

4 In the Probe Calibration dialog box, select the Calibrated Atten/Offset radio button.

5 Select the Start Atten/Offset Calibration... button and follow the on-screen instructions for the vertical calibration procedure.

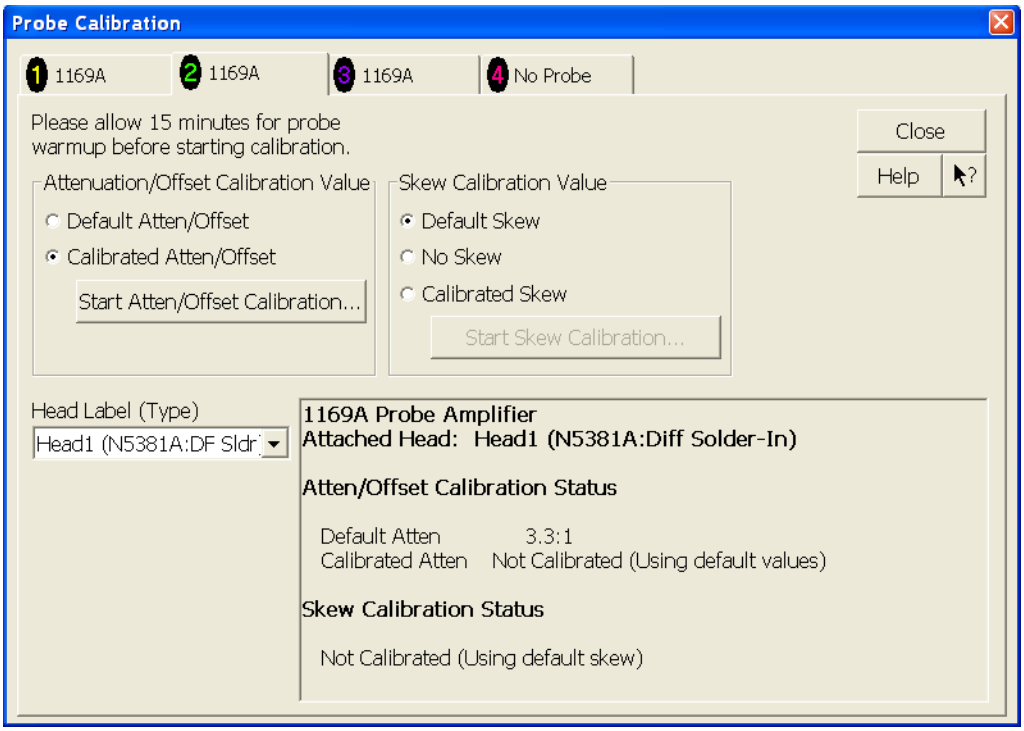


Figure 50 Probe Calibration Window.

6 Once the vertical calibration has successfully completed, select the Calibrated Skew... button.

7 Select the Start Skew Calibration... button and follow the on-screen instructions for the skew calibration.

At the end of each calibration, the oscilloscope will prompt you if the calibration was or was not successful.

Verifying the Probe Calibration

If you have successfully calibrated the probe, it is not necessary to perform this verification. However, if you want to verify that the probe was properly calibrated, the following procedure will help you verify the calibration.

The calibration procedure requires the following parts:

- BNC (male) to SMA (male) adaptor
- SMA (male) to BNC (female) adaptor
- BNC (male) to BNC (male) 12 inch cable such as the Keysight 8120-1838
- Keysight 54855-61620 calibration cable (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Keysight 54855-67604 precision 3.5 mm adaptors (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Deskew fixture

For the following procedure, refer to Figure 51.

1 Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.
2 Connect the SMA (male) to BNC (female) to the connector farthest from the yellow pincher.
3 Connect the BNC (male) to BNC (male) cable to the BNC connector on the deskew fixture to one of the unused oscilloscope channels. For infiniium oscilloscopes with bandwidths of 6 GHz and greater, use the 54855-61620 calibration cable and the two 54855-64604 precision 3.5 mm adaptors.
4 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.
5 Connect the probe to an oscilloscope channel.
6 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.
7 Push down on the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.
8 Release the yellow pincher.
9 On the oscilloscope, press the autoscale button on the front panel.
10 Select Setup menu and choose the channel connected to the BNC cable from the pull-down menu.
11 Select the Probes... button.
12 Select the Configure Probe System button.
13 Select User Defined Probe from the pull-down menu.
14 Select the Calibrate Probe... button.
15 Select the Calibrated Skew radio button.
16 Once the skew calibration is completed, close all dialog boxes.

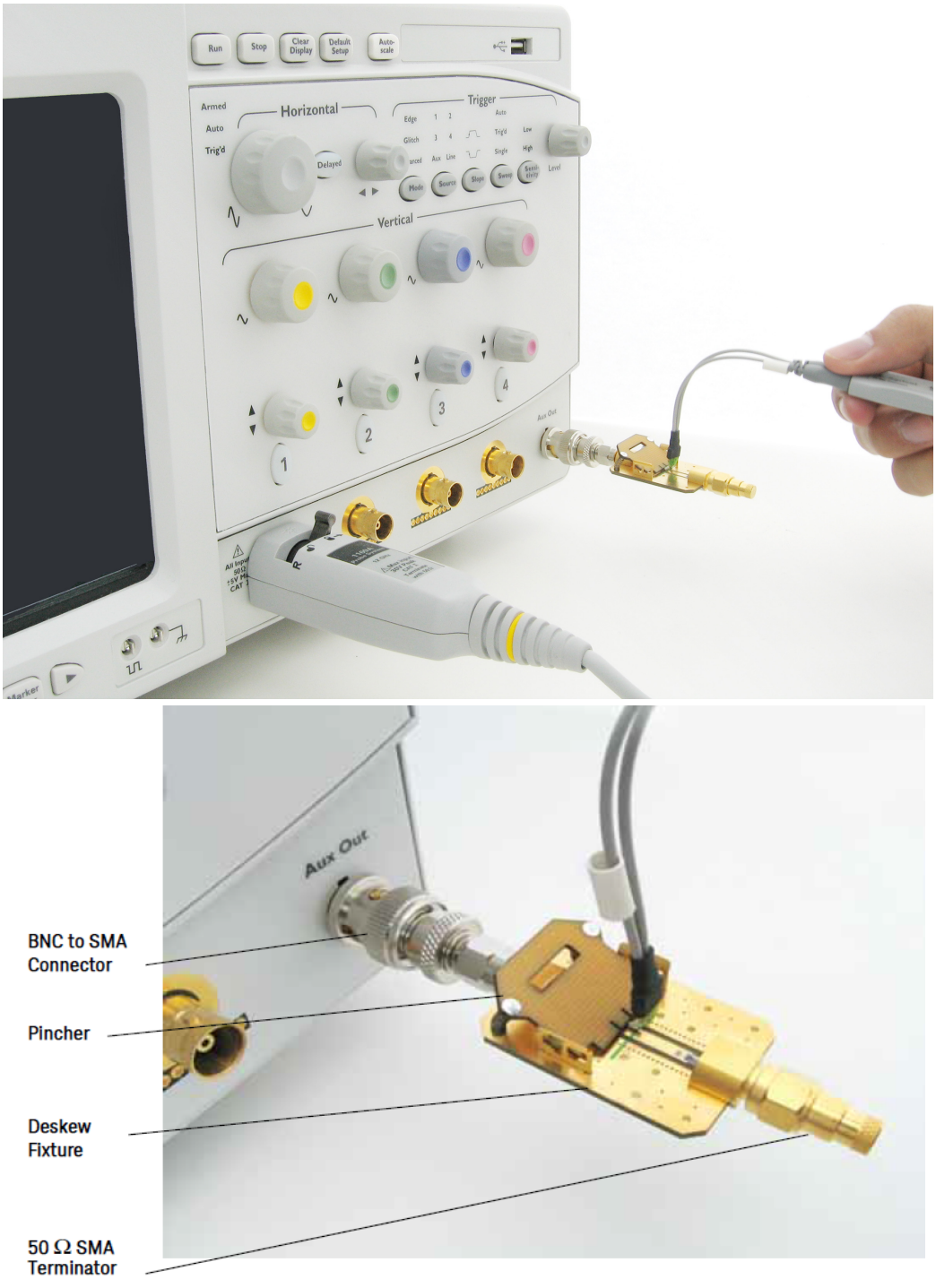


Figure 51 Probe Calibration Verification Connection Example

17 Select the Start Skew Calibration... button and follow the on-screen instructions.
18 Set the vertical scale for the displayed channels to 100 mV/div.
19 Set the horizontal range to 1.00 ns/div.
20 Set the horizontal position to approximately 3 ns.
21 Change the vertical position knobs of both channels until the waveforms overlap each other.
22 Select the Setup menu choose Acquisition... from the pull-down menu.
23 In the Acquisition Setup dialog box enable averaging. When you close the dialog box, you should see waveforms similar to that in Figure 52.

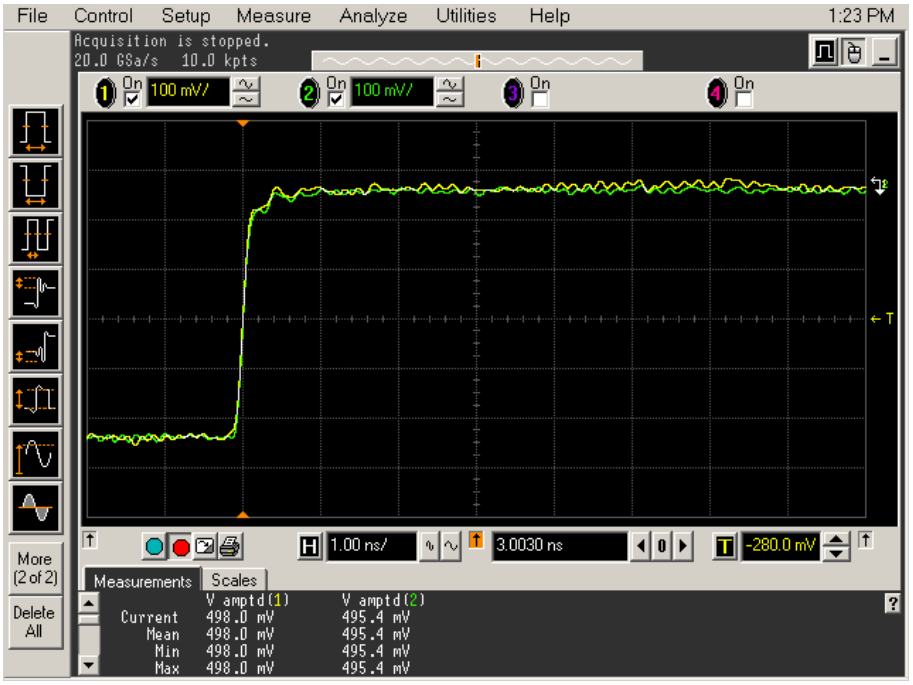


Figure 52 Calibration Probe Waveform Example

NOTE

Each probe is calibrated with the oscilloscope channel to which it is connected. Do not switch probes between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the probes be labeled with the channel on which they were calibrated.

20 InfiniiMax Probing

Figure 53 1134A InfiniiMax Probe Amplifier

Keysight recommends 116xA or 113xA probe amplifiers, which range from 3.5 GHz to 12 GHz.

Keysight also recommends the E2677A differential solder-in probe head. Other probe head options include N5381A InfiniiMax II 12 GHz differential solder-in probe head, N5382A InfiniiMax II 12 GHz differential browser, E2675A InfiniiMax differential browser probe head, N5425A InfiniiMax ZIF probe head and N5426A ZIF Tips.

Figure 54 E2677A / N5381A Differential Solder-in Probe Head

Table 235 Probe Head Characteristics (with 1134A probe amplifier)

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential Solder-in	E2677A	7 GHz, 0.27 pF, 50 kOhm	7 GHz, 0.44 pF, 25 kOhm

Used with 1168A or 1169A probe amplifier, the E2677A differential solder-in probe head provides 10 GHz and 12 GHz bandwidth respectively.

U

V

W

Z