Boundary-scan Technology, Justification, and Test Implementation For Designers

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Abstract:
This paper provides practical insight for designers on the merits, design, and test implementation of Boundary-scan technology. The information here is written from a Manufacturing Test and Test Equipment Applications Engineering perspective. The inclusion of Boundary-scan impacts all areas of product development and support including device and circuit design, manufacturing, and field service. There is a wealth of information available that addresses both the methodology of how to integrate boundary-scan into devices **and** the proper implementation for the test of boards containing boundary-scan devices. This paper focuses on the glue that binds these two processes together. The rewards of taking the necessary steps to include boundary-scan in the product design cycle and the value provided to the product manufacturing process are addressed. Designers and test engineers must work together to successfully define a strategy that balances product development and the attainment of product shipment requirements driven by the ever increasing time-to-volume pressures. A product is designed once, but manufactured over and over at some level of volume. It is key that a corporate strategy be defined to optimize the entire product development and product deployment endeavor. The payback of increased fault coverage is maintained throughout the entire product lifecycle. Manufacturing can not be reactionary to the challenges of a design, rather a strategy must be forged where the successful deployment of electronic products is optimized.

Boundary-scan Test Technology Overview:
Boundary-scan technology was created to address the verification of increasingly complex devices **and** circuits and to allow testing where limited test access is dictated. Devices are increasing in complexity at a staggering rate. The inclusion of boundary-scan circuitry into a device can make the test development process generic and easy to automate. In order to meet volume-manufacturing demands, a methodology must exist to be able to verify that a product does not have any manufacturing defects. In order to approach 100% fault coverage, all device pins need to be exercised and if a pin fault exists (e.g. open pin/trace), an accurate diagnostic must be provided to facilitate repair. A methodology must exist to not only determine if a device/circuit functions, but also provide a diagnosis to allow repairs to be performed in a timely fashion. Diagnostics to the pin level are supported, something conventional digital testing can not always provide. Accomplishing this task will go a long way towards reducing work-in-process (WIP) and meeting time-to-volume (TTV) demands. Repair operations are often invisible to design and test engineers. What we jointly supply to the manufacturing floor will greatly impact the profitability of the entire organization.

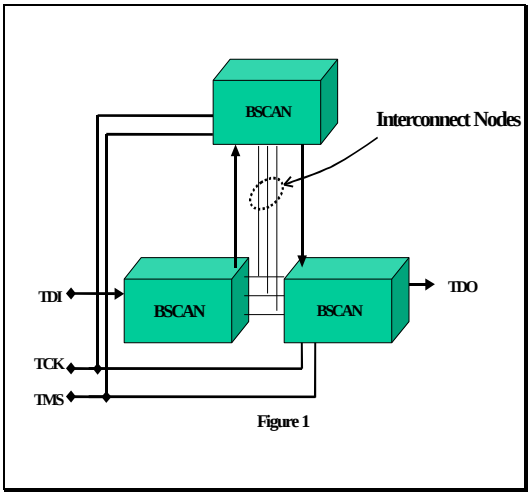

Figure 1

The workhorse of manufacturing test is the "in-circuit test" approach. This is where a board is exercised via a bed-of-nails fixture containing spring-loaded probes where access to every electrical trace is maintained. As designs become more complex, device integration explodes and device pinout escalates. Providing access to every electrical trace hits a practical limit. The routing of signals between high pin-count fine-pitch devices becomes a challenge. Guaranteeing access by adding test

points is constrained by the lack of real estate. Today, some discrete devices are approaching the size of test points. Devices and test points now compete for real estate. Boundary-scan supports the test of device interconnects (figure 1) without providing direct access to each electrical trace [3]. Through boundary-scan, the same level of fault coverage and diagnostics can be attained even though full access is not provided. The use of boundary-scan extends the current test development methodology. Manufacturing faults are easily identified: solder joint integrity, shorts, wrong/missing devices, device orientation, stuck pins (due to electrostatic discharge [ESD] and heat [solder process]), and bond wire failures.

If the test of conventional logic (non-boundary scan equipped) connected to boundary-scan devices is desired, this can be performed through the scan chain (figure 2). Patterns are simply scanned into the TAP (boundary-scan test access port) serially, shifted to the inputs of the device or cluster, and the response captured and shifted out to verify proper operation. Control and visibility of the conventional logic is provided through the 'serial' scan chain. Pattern rate is significantly derated due to the serial shift operation, therefore 'at-speed' testing can not be performed and complex timing can not be emulated. Tests of complex devices or clusters will require very large pattern sets. The complexity of the conventional logic may dictate the feasibility of performing this type of testing. Consider the capability of the target boundary-scan test platform to determine whether the large pattern sets can be applied.

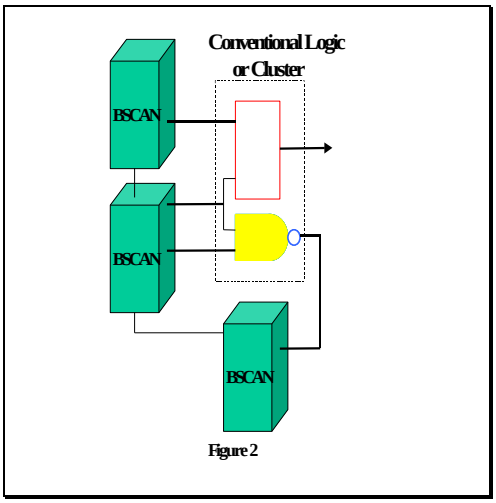

Figure 2

As soon as the boundary-scan test development process is instilled as a common occurrence, the process to implement boundary-scan tests can be made routine. This is aided by the fact that every facet of device compliance is defined by the IEEE 1149.1 [6] standard. Other standards are on the horizon that focus on other test opportunities such as analog/linear component test and system test (1149.4 and 1149.5). The 1149.1 standard provides a rigid structure that allows flexibility for designers to accommodate unique requirements. By adopting boundary-scan technology, both test development time and the expertise required to develop comprehensive tests can be reduced both for existing and future designs, guaranteeing high quality and product reliability. Most merchant devices supplied by IC vendors have incorporated boundary-scan due to market demands. We can now capitalize on this fact and exploit the benefits offered. A manufacturing/test cost reduction will result that will be enjoyed over the entire product life-cycle.

There is also a potential to increase the reliability of fixture probe access and fixture fabrication time by reducing the number of access points. For low volume products, boundary-scan can be used to perform circuit verification via lower-cost benchtop testers where the development of a fixture, a test, and the utilization of capital intensive large scale ATE (automatic Test Equipment) can not be justified.

Boundary-scan Cost Drivers:

Manufacturing faults are the dominant players in the fault pareto, however the test of core logic functions can optionally be implemented if this functionality is designed into the boundary-scan infrastructure. Boundary-scan can increase fault coverage significantly. Faults do not escape to later process steps where diagnostics are limited and repair tasks are much more expensive. A 25% increase in test coverage can provide a 50% repair cost savings [5]. Boundary-scan impacts a wide array of cost drivers including reduction in test development time, reduced manufacturing costs, improved product quality, scrap reduction, and reduced field returns. If a supplier off-loads manufacturing and test to a contract manufacturer, test development or test support is more easily accomplished via boundary- scan.

In the past there was some resistance to integrating boundary-scan technology into a device. The impact of the small incremental increase in gate and pin count is eclipsed by a significant increase in fault coverage attained and by the reduction in test development time. Also, the impact on the design cycle has been lessened. Tools now exist to automate the

inclusion of boundary-scan structures into ICs. In addition, careful selection of cell types can reduce or eliminate the impact on device performance. Note that cell representations are not logic diagrams and that logic functions can be merged into the existing core logic, reducing adverse parasitics or gate delays.

Boundary-scan Device Architecture Considerations:

The adoption of a limited access test approach dictates that a number of factors be considered. Rather than being able to rely on traditional unpowered shorts testing to find destructive faults, these potentially destructive faults must be detected with power applied to the board. The test platform utilized (large commercial ATE or benchtop rig) determines the stress devices are subjected to when faults are found while power is applied to the board. The battery of tests used must not jeopardize long-term circuit reliability. The test suite dictated by the test platform defines the level of safety. Devices must be robust enough to withstand the short-term stress imposed by the test technique. Device designers must be cognizant of this fact. The faster the test is performed, the less designers must consider the resiliency of their devices to sustain these short duration clashes.

Designers have the choice of including some optional functionality into the boundary-scan device infrastructure. One optional boundary-scan capability called ID-Code exists to allow verification of proper device placement. This functionality allows the validation that the proper revision and correct speed/technology part has been inserted and soldered to the board. A functional equivalent but incorrect technology part could be placed on the board and possibly function in an unreliable manner. Implementing ID-Code in a device will allow reading the ID-code to verify that the correct part or correct revision part has been inserted on the board. It is possible (rare) that two fine pitch devices using identical packaging could be swapped on a board. If the power/ground pin mapping is identical for these two different parts (same pin-out, cell structure), then only ID-Code can differentiate between these devices.

During the "Capture Instruction Register" state of a boundary-scan device the two least significant bits (01) are defined so they can be shifted out to verify device and scan chain integrity. Rather than waste the most significant bits, they can be utilized to work like ID-Code bits allowing an alternate means to determine what has been actually placed on the board.

The actual operation of a boundary-scan pin is defined by the boundary-scan cell type inserted between the device pin and core logic. It is recommended for output pins and bi-directional pins that a self-monitoring cell (figure 3) be chosen (e.g. IEEE cell BC_7). This additional capability will have limited impact on increasing device complexity and gate count, but will provide increased flexibility and improved fault coverage. For example, if access is not provided for a node containing a boundary-scan device driving a non-boundary-scan device, faults on this node can be verified by driving and reading back data on the pin by using the readback capability of a self-monitoring cell. In addition, if a device pin is isolated (unused dangling pin), a fault (short to adjacent pin) that could impact long-term device reliability could be verified.

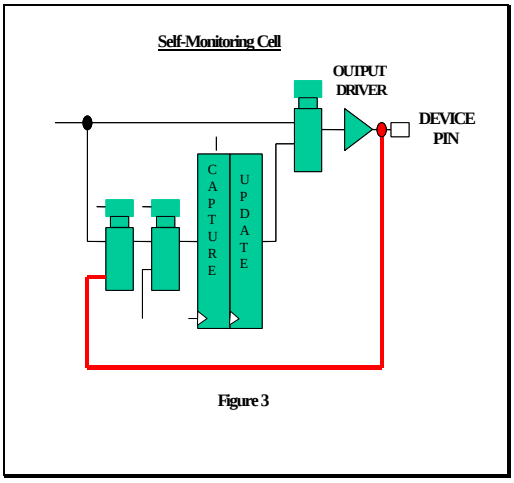

Figure 3

Board Design Guidelines:

How boundary-scan devices are deployed and connected on a board depends on the test strategy defined by the partnership of design, test, and field repair. If full access is provided, connecting all boundary-scan devices together in a scan chain is not required for manufacturing test, but may be a requirement for a burn-in process step or product self-test/diagnostics. If there are nodal (electrical trace) access constraints (limited access), then connecting all devices together in a scan chain is required to support manufacturing test. To simplify the test development process, it probably makes sense in this case to connect all devices together in a single chain. Test development may be better automated if all the devices are connected together in a single scan chain. If a low cost bench-top tester can **not** handle the volume of data required by long scan chains, multiple chains could be configured. If

multiple chains are warranted for some particular test or verification step, then the board could be designed so that all the devices can be linked together into one chain. Fixture wiring would provide the linkage to support a more comprehensive manufacturing test activity supplied by large scale ATE.

The entire test infrastructure (design through field repair) needs to be considered when configuring scan chains. Unusual chain configurations should be avoided (e.g. parallel chains where the TDI [test data in] pins of each chain are tied together and the TDO [test data out] chain outputs are tied in common). Devices having questionable compliance adherence should be grouped at the end or beginning of a chain so that they can be bypassed if they do not operate as expected.

Unstable tests could result if a ground bounce (ground shift) occurs while testing a device. This is something that can occur if all outputs switch at the same time. The chip designer needs to supply a robust internal grounding scheme to avoid internal device ground shifts. The board designer needs to insure that there is a robust grounding scheme. In addition, enough ground/power probe access needs to be provided to insure test stability. Also, signal quality on the TAP test clock (TCK) line is most important. Proper buffering and terminations may be required to guarantee clean signals.

Access does not need to be provided to determine the existence of series termination resistors on interconnect nodes (common on high-speed busses). These can be verified by testing the interconnects via boundary-scan test techniques and associating any nodal faults with a specific resistor. Access to a couple of series resistors could be provided in order to determine if the proper 'reel' containing the correct resistance value was loaded.

Impact of Boundary-scan at Other Process Steps:

Boundary-scan has been successfully used in other product verification arenas. Where environmental stress screening (ESS) or burn-in is justified, boundary-scan can be used as the vehicle to exercise and monitor the board. The board can be dynamically exercised and tested through the 1149.1 JTAG Test Access Port. Some board designs include self-test hardware where the board is exercised by an embedded control mechanism that controls and verifies board functionality through the boundary-scan chain while undergoing temperature cycling.

Boundary-scan can also be utilized for design prototype verification, reducing the time to eliminate process defects and clear the way to focus on the intended design verification task. Prototype verification could be performed by commercial ATE or via a PC driven benchtop exerciser. This can have a major impact on design verification time. With today's dense and complex boards, the use of logic analyzers and scopes may be impractical.

In addition, boundary-scan can be used to support field service needs or remote diagnostics. Boundary-scan can be utilized by field service organizations to diagnose faults at a customer's site or at a depot repair facility. The boundary-scan diagnostic tools could be controlled through an 1149.1 port built into the design or through embedded self-test hardware/firmware that exercises the board through a boundary-scan channel. Remote diagnostics via dial-up capability can be used to perform remote diagnostics via boundary-scan.

Tests developed for one test function can be used across all product development, verification, and field repair steps. Effort expended in one area can be leveraged across many process steps and used throughout the corporate domain. .

Successful Boundary-scan Test Development:

Currently the biggest obstacle to automating and successfully implementing boundary-scan tests is in the accuracy of a BSDL (boundary-scan description language) file and whether a part is fully compliant. The BSDL file is a description of how the device behaves when placed into the boundary-scan test mode. It is this file that defines the tests that will be generated (figure 4). If a custom part is designed, compliant behavior as defined by the 1149.1 standard should be verified. This can be performed by using a BSDL verification tool that generates a pattern set to verify a device's adherence to the standard. Optimally, the vector set can be applied to a new silicon design before being committed to a board. An alternative would be to take the pattern set and run it against a software design simulator to verify that the silicon matches the BSDL description. If steps such as these are not taken, non-compliant behavior found too late in the product development cycle could negatively impact test development. BSDL semantics and syntax errors should also be identified since they could indicate an even deeper and more severe problem with the silicon. Common problems encountered include pinout errors,

incorrect cell definition, incorrect cell order, wrong cell length, wrong opcodes, wrong control cell definitions and disable values, and wrong ID-Code (rev change).

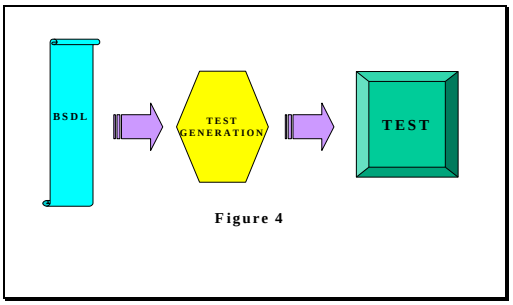

Figure 4

If programmable devices such as Logic Cell Arrays (LCAs) exist in a design, the BSDL for each instantiation will need to be modified. In general since LCAs are programmable, the personality of the pin (input, output, bi-directional) is defined by the board design. Care must be taken to modify the BSDL file so that it matches the board topology. In general, all design-for-test (DFT) analysis should be performed up front as part of the design cycle. Corporate design/test guidelines should be addressed long before the design enters the manufacturing stage [2].

In-System-Programmable Devices:

The Boundary-scan port is also being used to allow the programming of PLDs (Programmable Logic Devices) and Flash Memory devices at the board level [1]. These In-System-Programmable (ISP) devices are sometimes called In-System-Re-programmable (ISR) parts. There are a number of reasons to perform this task at the board level. It would be very difficult to make electrical contact with these devices without being soldered to the target printed circuit board. Manufacturers are either performing this task on a dedicated off-line programming station or to reduce the number of process steps and handling, programming is performed via a piece of ATE which is also being used to perform tests of other board functions. Many opt to perform this task by ATE at the board level since after the device is programmed the functionality can then be immediately verified. However, programming these devices takes time, and throughput requirements may dictate that programming occur on a standalone benchtop programmer.

The board may need to be designed to allow upstream parts to be tri-stated to support the relatively long programming sequence[4]. Most device loading algorithms allow mixing PLDs or Flash together in the same scan chain. If the outputs of a device are not disabled during the initial power-up, this could cause a bus clash and the shortening of its life expectancy. It is suggested that devices qualified do not exhibit this behavior, or the board be designed to avoid this pitfall.

Summary:

Complex devices can be tested in a generic fashion if boundary-scan capability is provided. Designers, layout engineers, and test engineers need to strive to provide full access. Where access is **truly** not feasible on some nets (routing constraints, performance), boundary-scan interconnect test offers a test solution. Attaining the goals of cost, quality, and time-to-market requires a lot of cross-departmental cooperation. Excellent fault coverage is important so that defects are not discovered at later stages of test in manufacturing or even worse, at the customer's premises. By lowering WIP, fewer goods need to be produced to meet product demand. The test strategy needs to be optimized to reflect the specific requirements dictated by a particular design. If a company can not meet production schedules and keep its manufacturing costs down, the competitive edge will be lost. The proper design and test implementation of boundary-scan will contribute significantly to meeting these goals.

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