



# Why Boundary Scan is Coming of Age

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**Agilent's Boundary Scan Online Users Group**

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# About the Speaker



**Louis Y. Ungar**

**Position** - President of A.T.E. Solutions, Inc., the leading independent testability consulting and educational firm.

**Professional Associations** - President of the Testability Management Action Group (TMAG), Consultant to the American Society of Test Engineer (ASTE), SMTA Testability Chair, Member of IEEE.

**Major Accomplishments** – Educated more than 7,000 test professionals from 2 dozen countries, consulted for more than 100 organizations, created BestTest information source for test professionals, patents for Built-In Self Test, Elected to ASTE Board, founded TMAG.

**Education** - BS in Electronics Engineering and in Computer Sciences from UCLA, completed course work for MA in Management.

**Professional Goal** – Convince engineers and managers that product quality through better test is not only noble, but also cost effective.





# What Is Covered

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- **Boundary Scan and Why We Need It**
- **Historical Perspective**
- **How and Why Boundary Scan Caught On**
- **Economically Justified**
- **Tapping into Seldom Used Features**
- **Summary and Conclusion**



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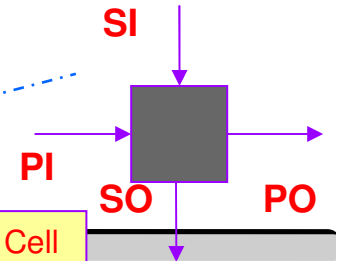


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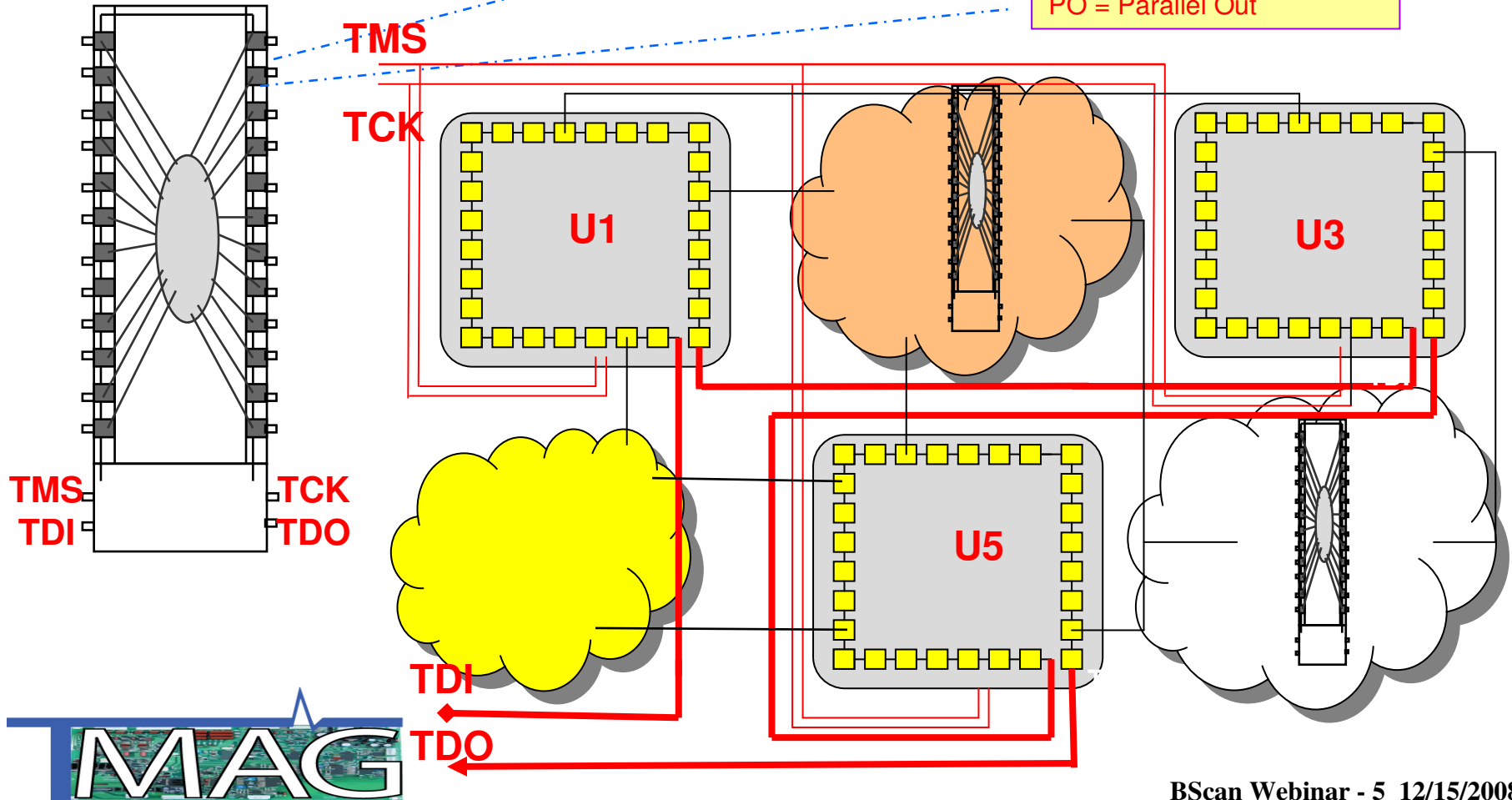
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# What is Boundary Scan?



Typical Boundary-Scan Cell  
SI = Scan In SO = Scan Out  
PI = Parallel In  
PO = Parallel Out





# Why We Need Boundary Scan



- To Meet Design for Testability (DFT) Goals
- To Provide Access to Circuit Nodes
- To Deal with Increasing Circuit Complexity
- To Provide Built-In Self Test (BIST)
- To Reap Economic Benefits





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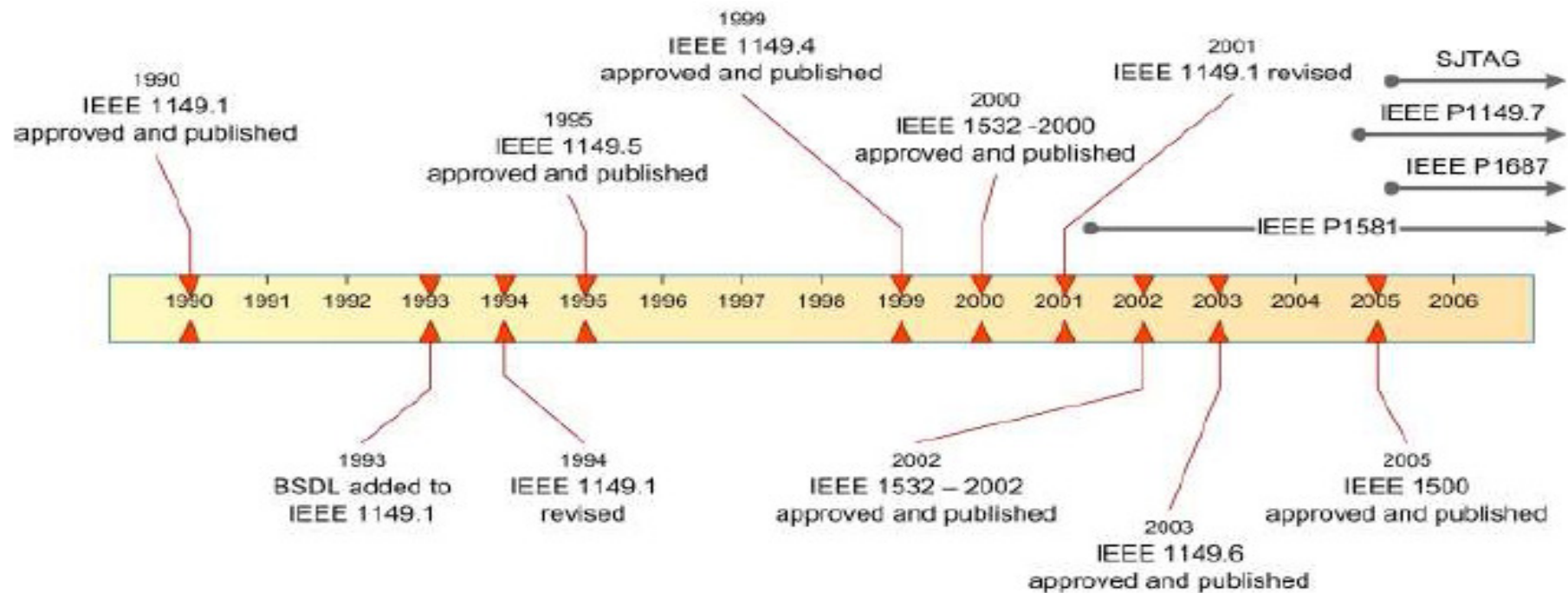
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# Historical Development

Source: Heiko Ehrenberg Goepel USA [http://www.ieee.li/pdf/viewgraphs\\_jtag\\_boundary\\_scan.pdf](http://www.ieee.li/pdf/viewgraphs_jtag_boundary_scan.pdf)



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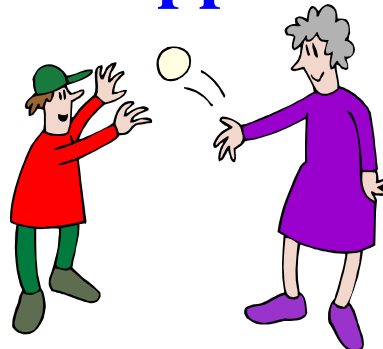
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# How and Why Boundary Scan Caught On



- IC Manufacturers make boundary scanned chips
- Tool Makers provide software, including Automatic Test Program Generation (ATPG)
- In-Circuit Board Testers support boundary scan
- Low-Cost Functional Board Testers available
- Lower-Cost Field Support available



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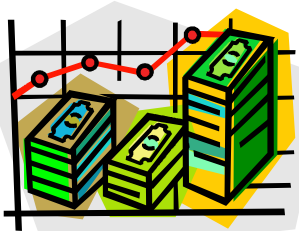


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# Economic Justification



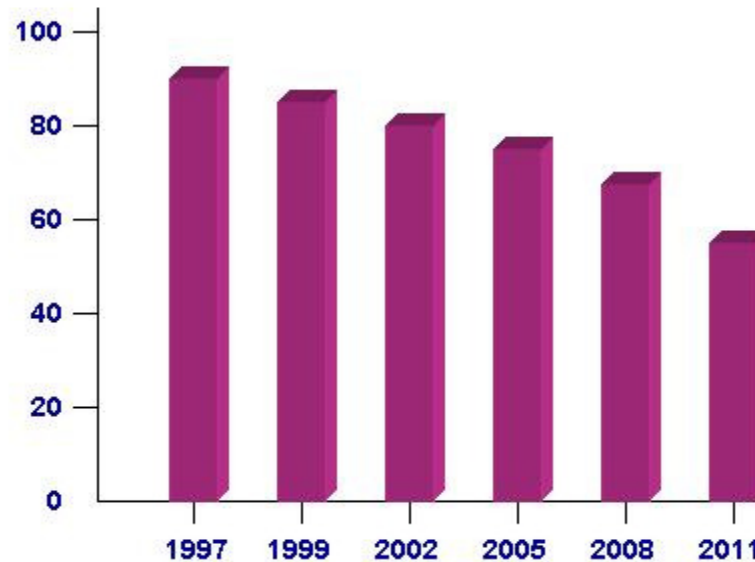
- **Faults Found in the Factory are Less Costly Than Escaped Faults**
- **Testable Circuits are Less Costly to Test and Repair**
- **More Boundary Scan Cells Available Create More Scannable Nodes**
- **Reduce manufacturing test and field support costs**





# Faults Escaping Tests

## Lower Yield Due to Tester Inaccuracy



Source: Yervant Zorian, *Testing the Monster Chip*, IEEE Spectrum, July 1999

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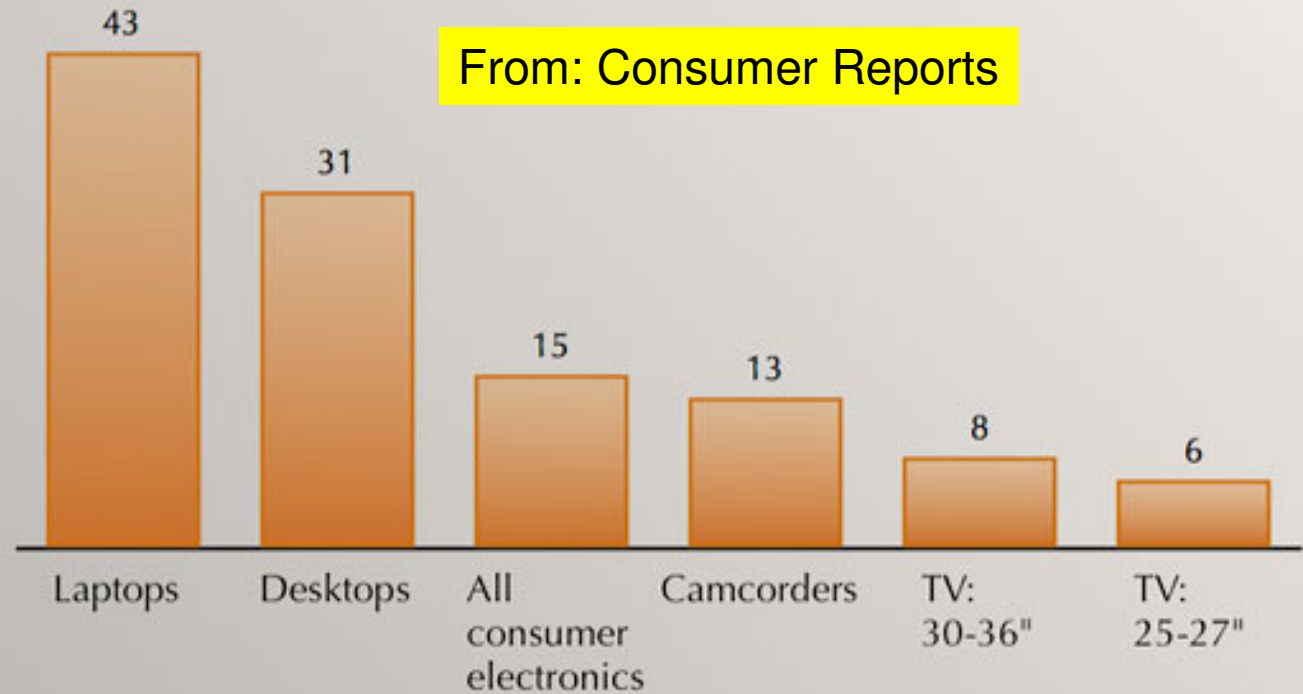


# Repair Rates Expected

Repair rates for 3- to 4-year old products—2006  
Percent



From: Consumer Reports



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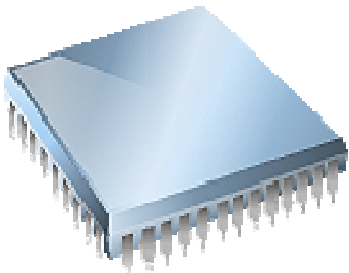


# Boundary Scan Availability

## ■ More Boundary Scan Covered Nodes

More boundary scanned chips

Large chips such as Microprocessors with boundary scan cover 1,000+ nodes



Ball Grid Array (BGA) devices tend to have boundary scan and large number of nodes

Field Programmable Gate Arrays (FPGAs) have “JTAG test access port” (even if they don’t have boundary scan)

» FPGAs can have I/O pins programmed as boundary scan cells





# Traditional DFT Economic Metrics

## ■ Economics of DFT is measured by

**Benefit = Total Cost with DFT - Total Cost without DFT**

## ■ Total Cost includes

Design Costs



Parts Costs



Manufacturing Costs



Test Costs



Penalty Costs



Support Costs



**Benefit**

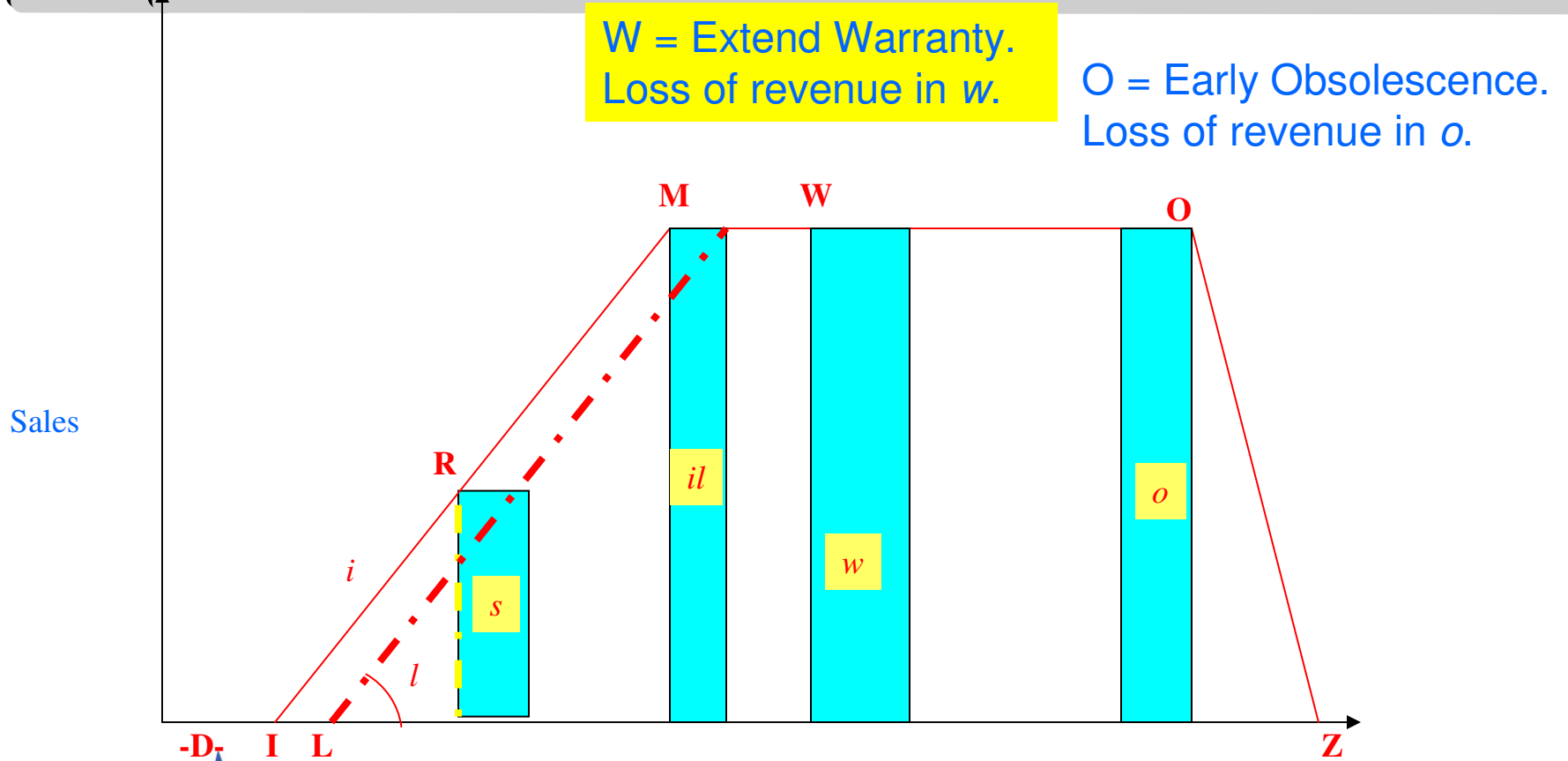






# Revenue Generation Model

From: Louis Y. Ungar, "The Economics of Harm Prevention through Design for Testability", AutoTestCon 2008



W = Extend Warranty.  
Loss of revenue in *w*.

O = Early Obsolescence.  
Loss of revenue in *o*.

R = Rework. Loss of revenue in *s*.

Time

L = Late Delivery. Loss of revenue in *il*. [bestTest.com](http://bestTest.com)



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# Features We Seldom Use

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- **SAMPLE Instruction Provides On-Board Logic Analysis**
- **RUNBIST Instruction Provides Chip Test in Manufacturing and Support**
- **Boundary-Scan Cells Configured as Linear Feedback Shift Registers (LFSRs) to Provide Board-Level Built-In Self Test (BIST)**
- **Board-Edge Boundary-Scan to Improve Isolation at System Test Levels**





# Expansions Already Started

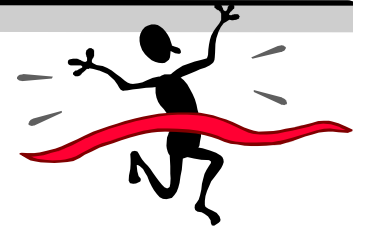
- Mixed-Signal Boundary Scan using 1149.4
- High Speed Applications using 1149.6
- Integration with Microprocessor Emulation
- Interrogation tool for internal BIST structures
- Use with Bit Error Ratio (BER) jitter measurements
- Integrating Hierarchical BIST across systems, boards and ICs





# Summary and Conclusions

- Boundary Scan, introduced in 1990 may have taken its time – but it *has* “Caught On.”
- IC Manufacturers make them and with only a few boundary scanned devices the entire circuit is testable.
- Tools are available to generate some tests automatically, others easily.
- Boundary scan supports manufacturing tests for in-circuit and functional tests as well as for diagnoses in the field.
- Boundary scan is growing in its scope, incorporating BIST, high speed transmission, analog and microprocessor emulation.





## More Information Available



- Courses from A.T.E. Solutions, Inc. teach engineers the mechanics and managers the value of boundary scan. Bring course to your facility.
- Find vendors of Boundary Scan tools and thousands of articles at [www.BestTest.com](http://www.BestTest.com)
- Acquire the SMTA/TMAG Testability Guidelines from [www.TMAG4DFT.org](http://www.TMAG4DFT.org) or [www.SMTA.org](http://www.SMTA.org)
- Share your concerns, questions and experiences with testability professionals at TMAG.



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# Questions?





**It Pays to Play!!!!**

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**The winners of the giftcards given throughout this session will hear their name and will receive their giftcard via email within a few days.**



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