PCIe standard updates and 3.0 testing challenges

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Agenda

1:00pm – 2:30pm – PCIe standard updates and 3.0 testing challenges

- What is PCI Express and how does the PCI-SIG establish the new standards
- PCIe 3.0 customer challenges and needs
  - Transaction and Data Link Layers
    - What is Link Training and how does it work?
    - Probing and Debugging PCIe 3.0
  - Physical Layer Transmitter Test challenges
  - Physical Layer Receiver Test challenges

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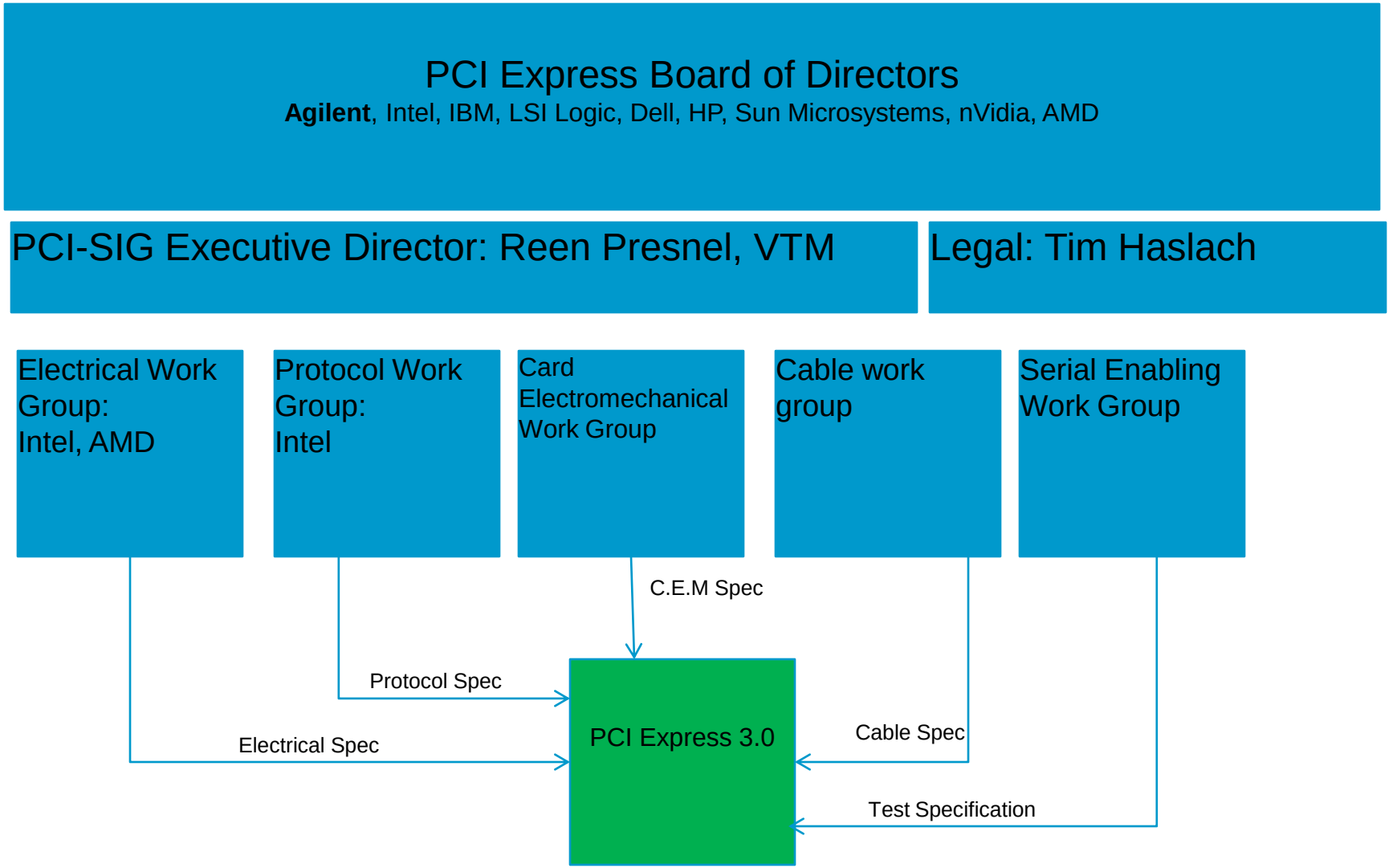
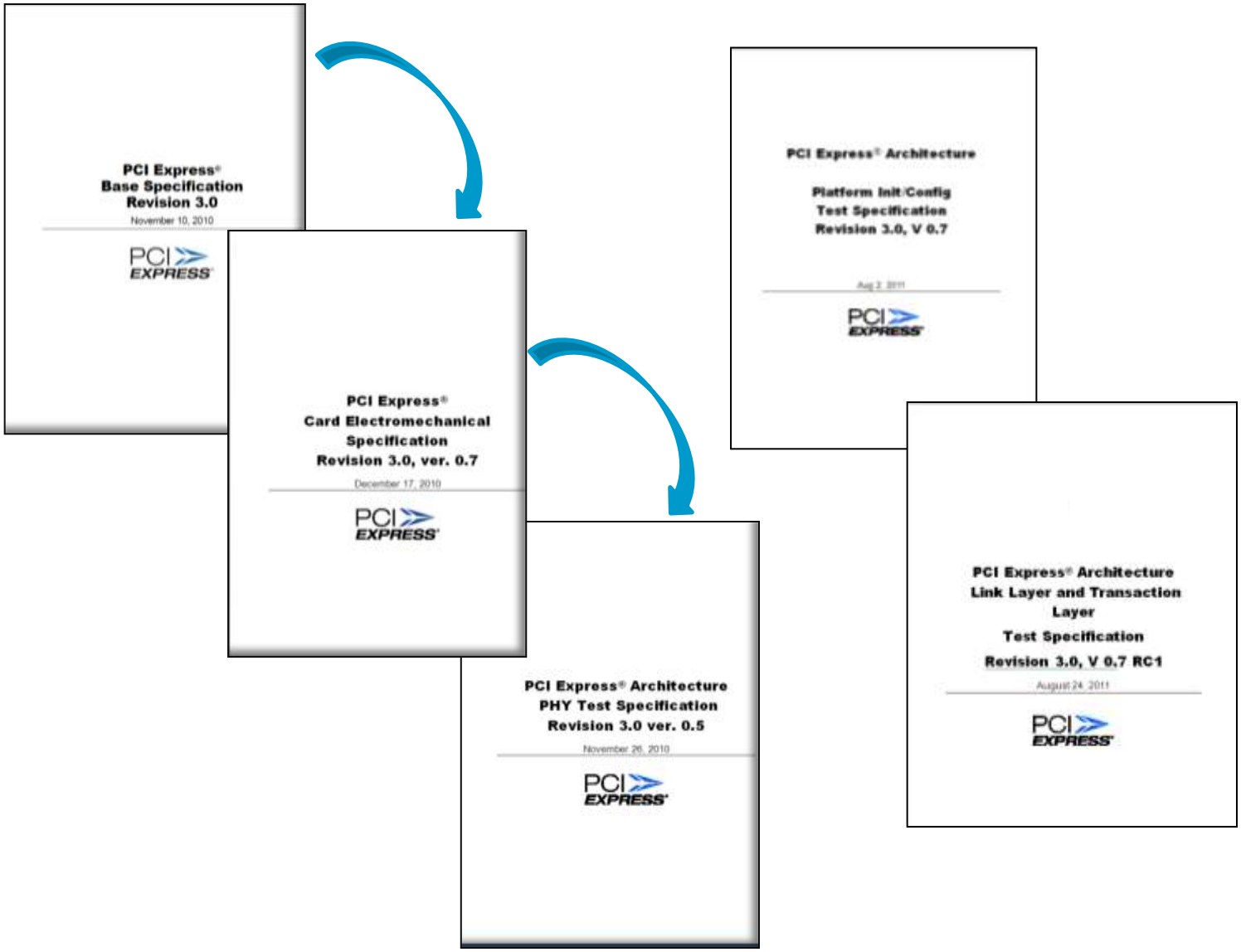
What is PCI Express?

- A serial high speed interconnect
- Operates more like a network than a bus
- Point-to-point (not multi-drop)
- Device enumeration uses the same protocol as PCI
- Operates at 2.5GT/s, 5GT/s, & 8GT/s vs 33-66MHz for PCI
- PCI Express and PCI can co-exist

PCI-SIG PCI Express Standards Organization



PCI-SIG Specifications



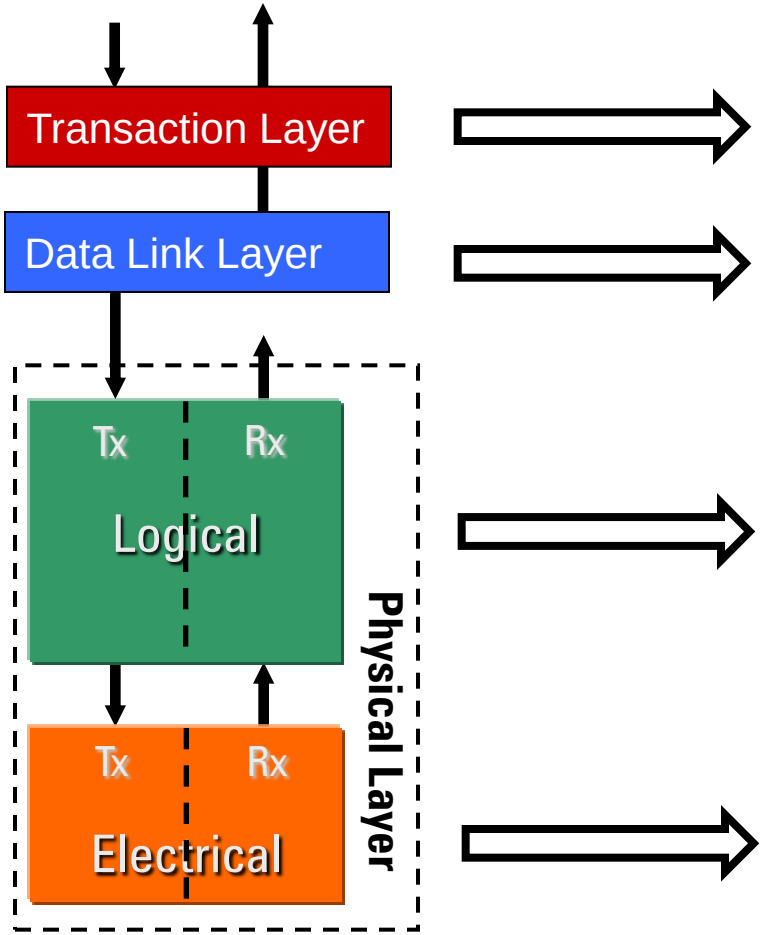
PCI Express Overview

PCIe Standard	Raw Bit Rate	Interconnect Bandwidth	Bandwidth/Lane *(in each direction)*	Total Bandwidth for x16 link *(in each direction)*
PCIe 1.1	2.5 GT/s	2 Gb/s	~250 MB/s	~4 GT/s
PCIe 2.0	5.0 GT/s	4 Gb/s	~500 MB/s	~8 GT/s
PCIe 3.0	8.0 GT/s	8 Gb/s	~1,000 MB/s	~16 GT/s

PCIe 3.0 Major Specification Changes

- New 12GHz oscilloscope *maximum* bandwidth specification
- De-embedding required
- CTLE + DFE (1 tap) Reference Receiver
- New jitter measurements for TX
- CEM tests to require convolution of channel and package losses
- TX equalization space greatly expanded
- TX⇔RX back channel established for tuning TX EQ settings maximizing RX EQ performance
- Updated Reference Clock phase jitter requirements
- Calibration of RX jitter stress signal must account for calibration instrument noise floor.
- New Compliance Patterns

PCI Express Architecture



Protocol Analyzer

Oscilloscope

BERT

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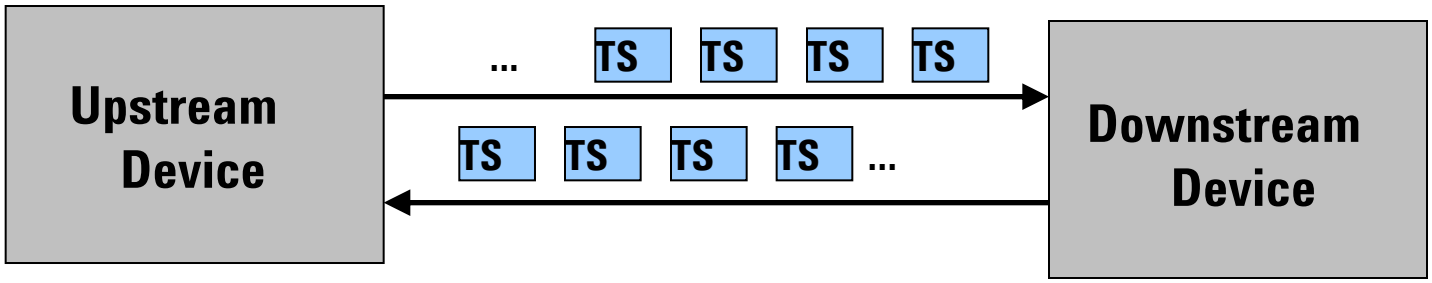
How does link training work?



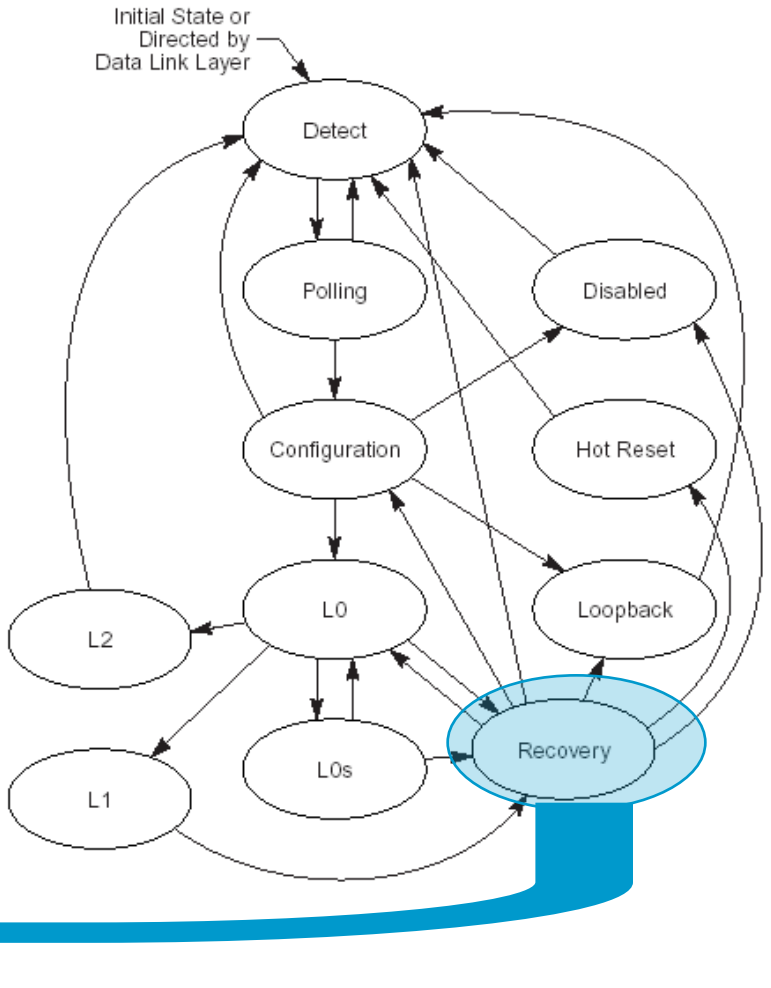
Two PCI Express devices exchange Training Sequences to negotiate link parameters like

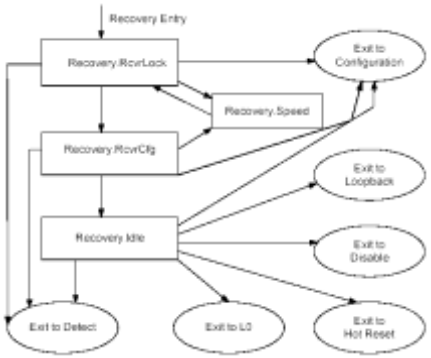
- lane polarity
- link number/lane numbers
- set of lanes that belong to the link
- link equalization
- scrambler enabled or disabled
- link speed
- number of fast training sequences required

Training Sequences are also used to switch the link to low power states.

How does Link Training Work - Logical Physical Layer

- Each of the devices implements a so called LTSSM that controls the link training.
- LTSSM stands for “Link Training and Status State Machine”
- Link training starts in state Detect.
- An active link that can transport transaction layer packets is in state “L0”.





Debugging Equalization Problems

Which phase of equalization does the link get to?

Does the link get to 8G with equalization disabled

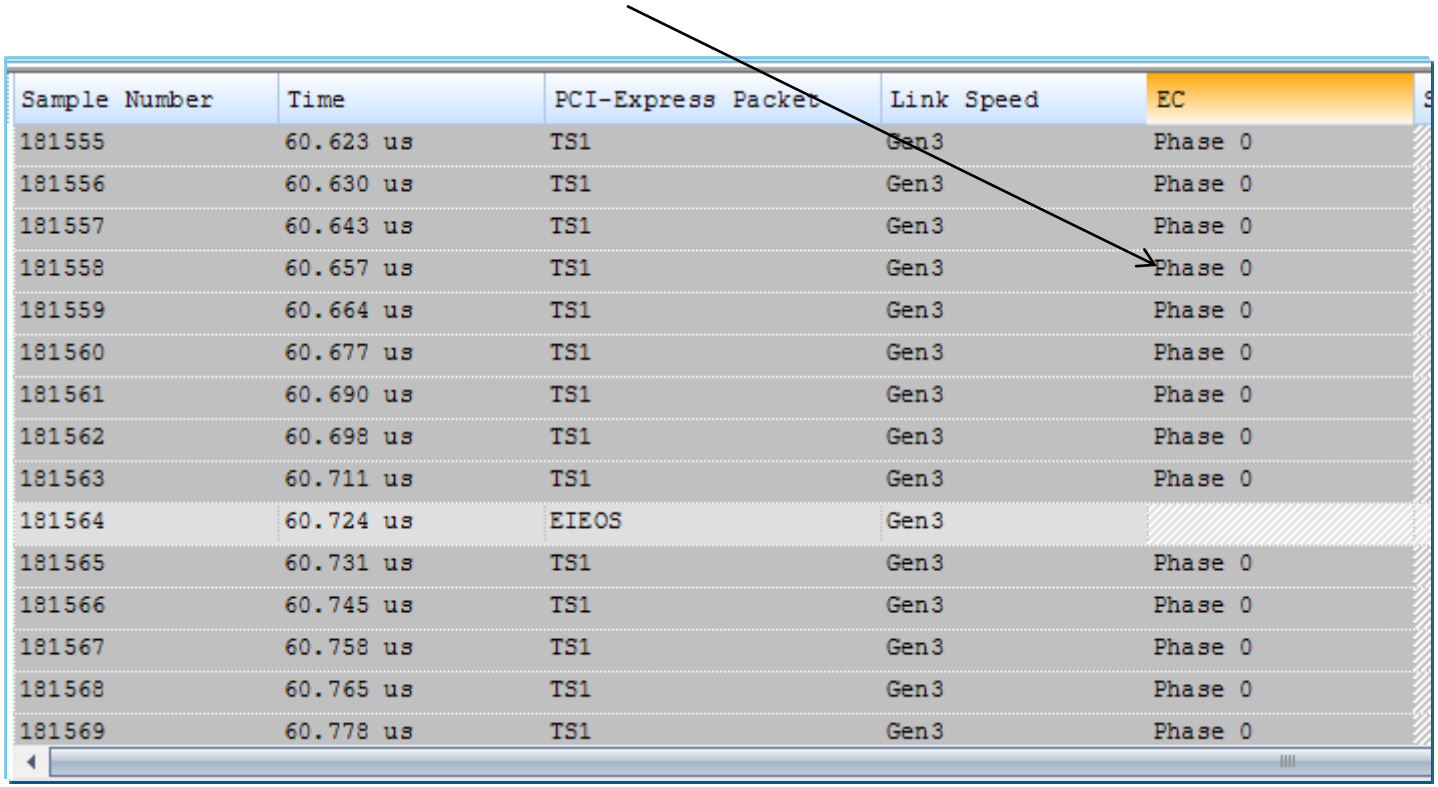
Change the presets and coefficients that are being used

Check BIOS settings on platform

Monitoring the rate of Recovery state transitions in L0 may give an indicator if frame errors are happening

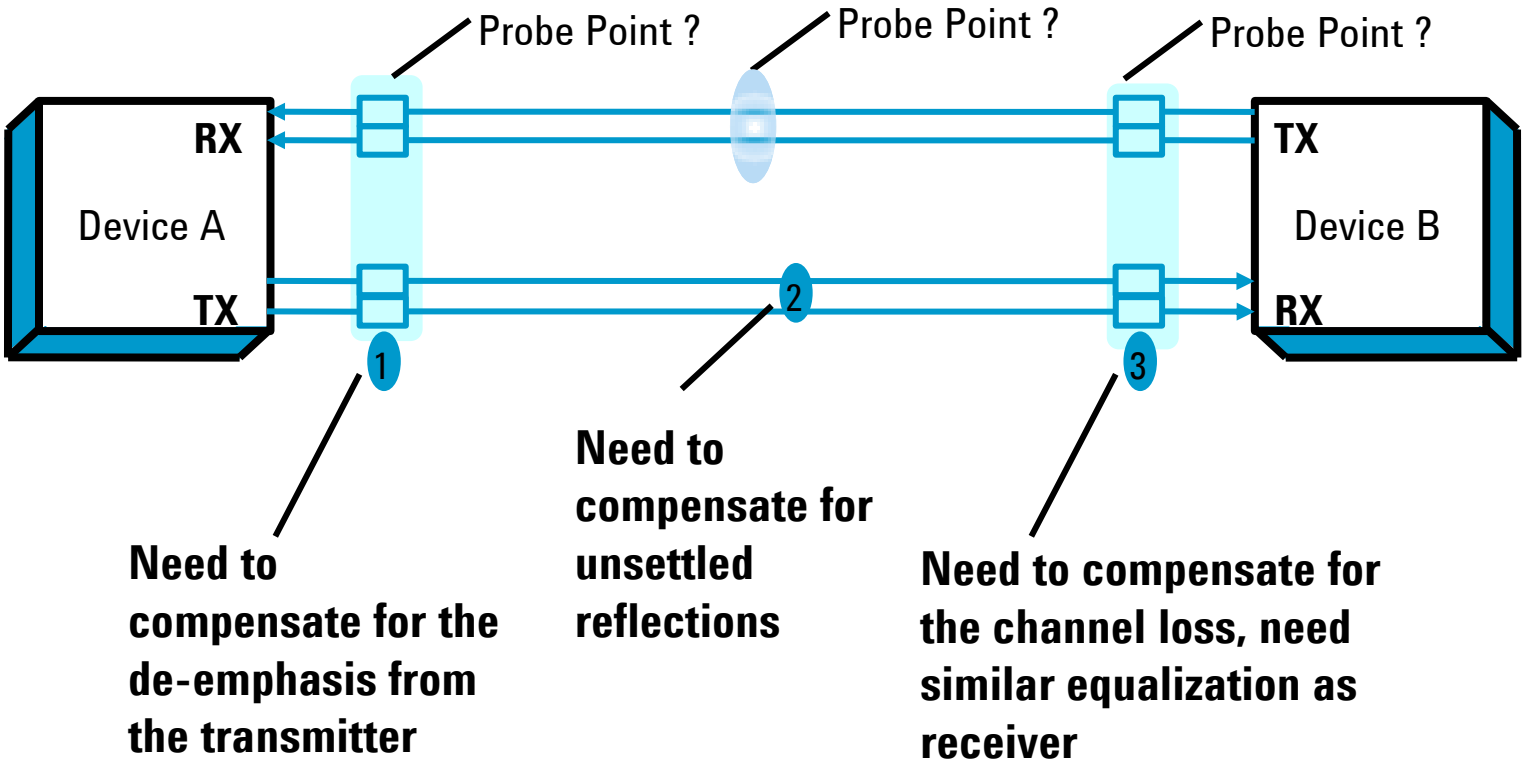
Recovery.equalization

Check the EC Field in the TS Ordered Sets to see which phase of equalization the link is in.

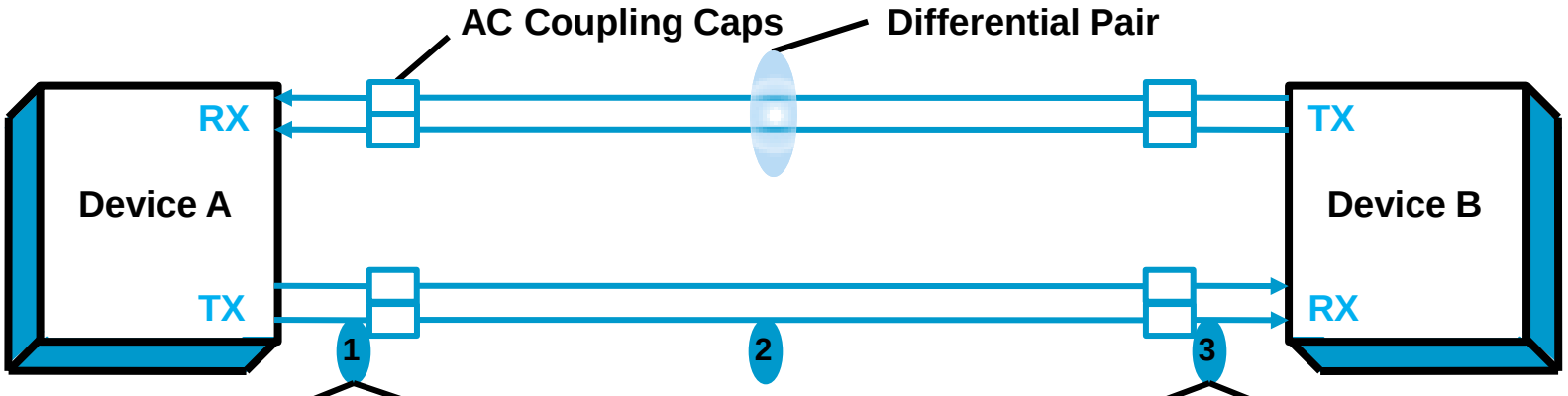


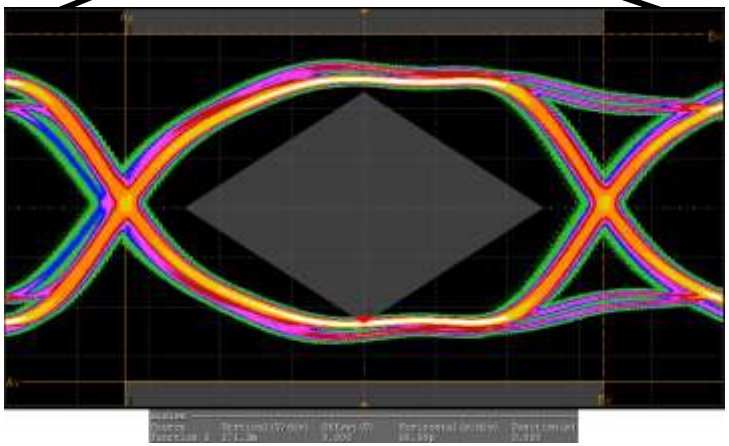
Sample Number	Time	PCI-Express Packet	Link Speed	EC
181555	60.623 us	TS1	Gen3	Phase 0
181556	60.630 us	TS1	Gen3	Phase 0
181557	60.643 us	TS1	Gen3	Phase 0
181558	60.657 us	TS1	Gen3	Phase 0
181559	60.664 us	TS1	Gen3	Phase 0
181560	60.677 us	TS1	Gen3	Phase 0
181561	60.690 us	TS1	Gen3	Phase 0
181562	60.698 us	TS1	Gen3	Phase 0
181563	60.711 us	TS1	Gen3	Phase 0
181564	60.724 us	EIEOS	Gen3	
181565	60.731 us	TS1	Gen3	Phase 0
181566	60.745 us	TS1	Gen3	Phase 0
181567	60.758 us	TS1	Gen3	Phase 0
181568	60.765 us	TS1	Gen3	Phase 0
181569	60.778 us	TS1	Gen3	Phase 0

PCI Express 3.0
Probing at 8GT/s

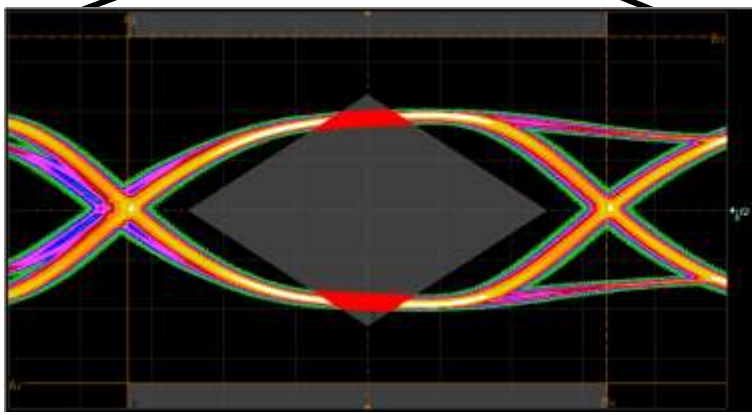


Comparison of Probing Point Extremes





Probe at Measurement Point 1
(at TX with TX Mask)



Probe at Measurement Point 3(at RX with TX Mask)

Probing Point	Location	Recommended?	Comments
1	TX side of coupling capacitor	It depends	Depends on what you want to measure. Will show more TX characteristics.
3	RX side of coupling capacitor	Yes	Closest point to RX. Decoupled from transmission line. Best option

Tools required for debugging

- Debugging PCI Express 3.0 designs is complex
- Isolate the layer that the problem occurs
- Thorough validation of the physical layer will prevent physical layer problems causing Link Training and Transaction Layer problems
- Using the correct tool will ease debug

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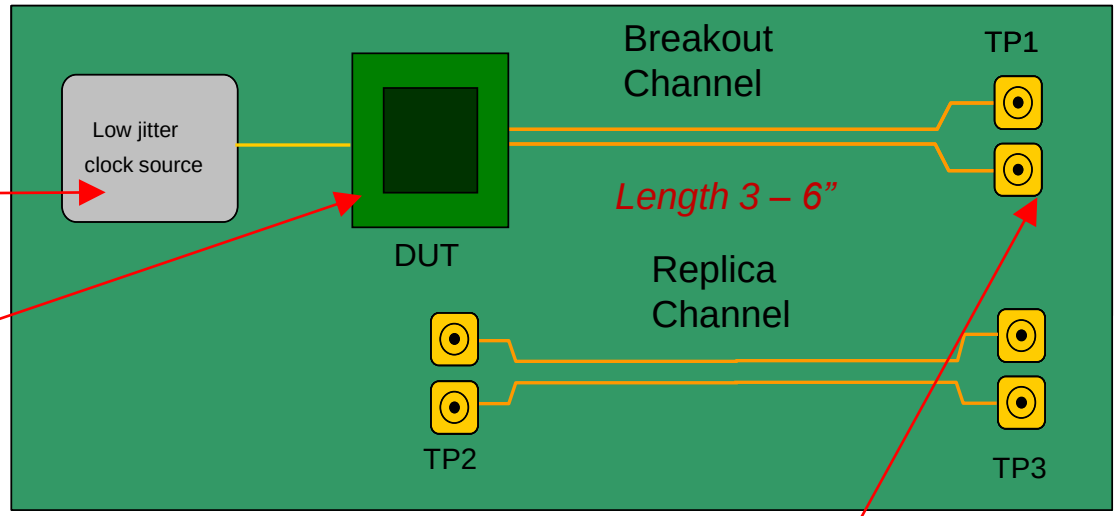
TX Measurement Challenges for PCIe 3.0

4.3.3.1.2. Measurement Setup for 8.0 GT/s Transmitters

- The PCIe electrical specification references all measurements to the device's pin. However, the pin of a device under test (DUT) **is not generally accessible**, and the closest accessible point is usually a pair of microwave-type coaxial connectors separated from the DUT pins by several inches of PCB trace, called the breakout channel.

External Generator. Can be a pulse Generator (Agilent 81134A, 81150A) or sinusoidal source (Agilent E8663D PSG or N5181A MXG)

Specification Reference Point is at the pin

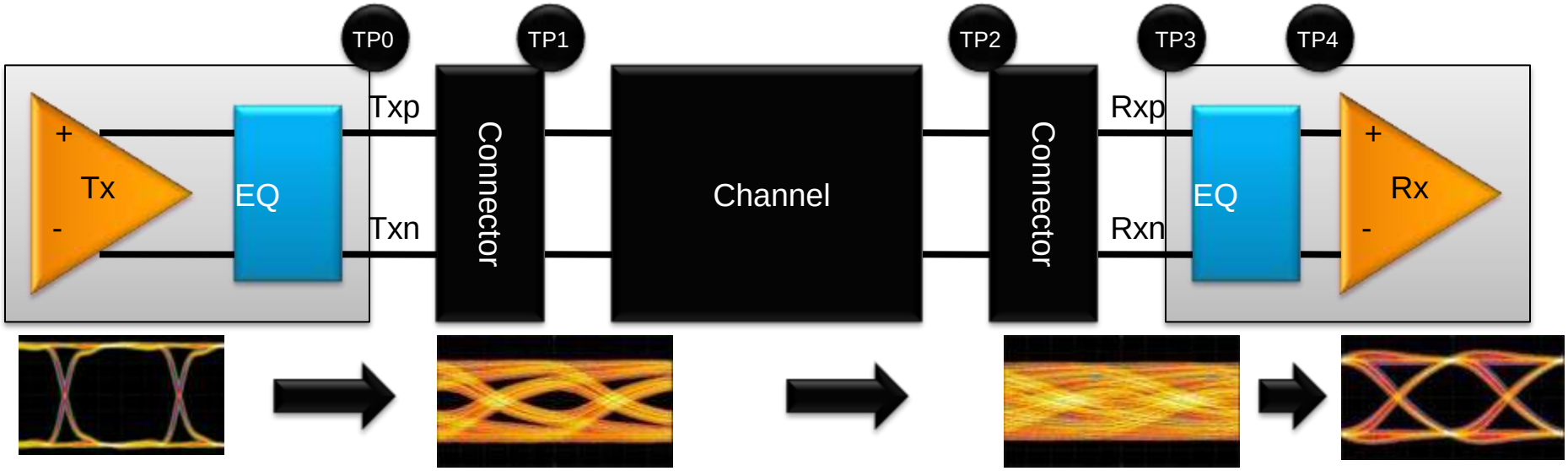


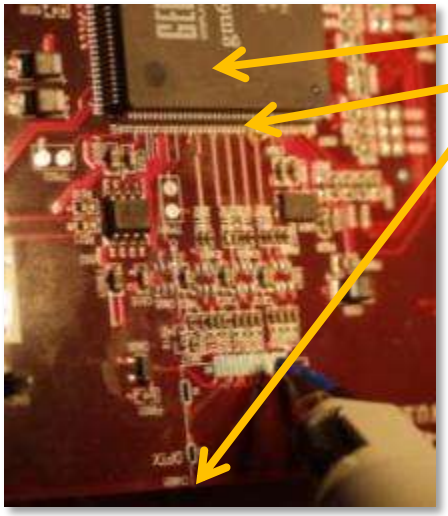
Measurement point is at TP1

TX Measurement Challenges for PCIe 3.0

- Signal path flow
- Obtaining S-21
- S-Parameters
- Measurement of 8 GT/s signal
- De-embedded waveform measurements

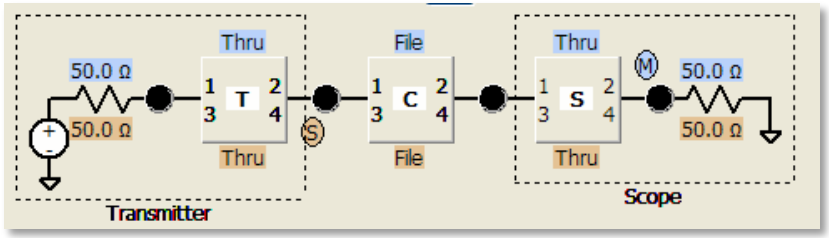
Signal Path Flow





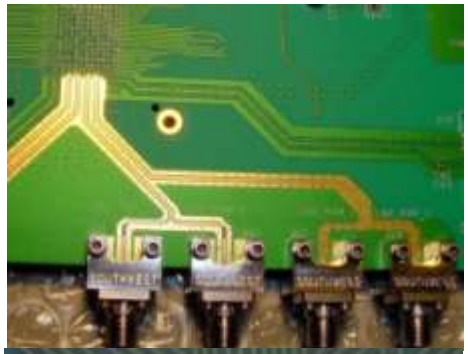
Signal generated here
Exits IC here
Exits board here

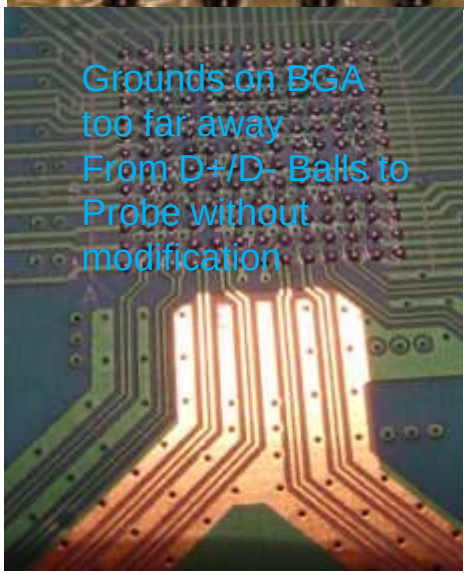
Combine measurements and transmission line models to view simulated scope measurements at any location in your design

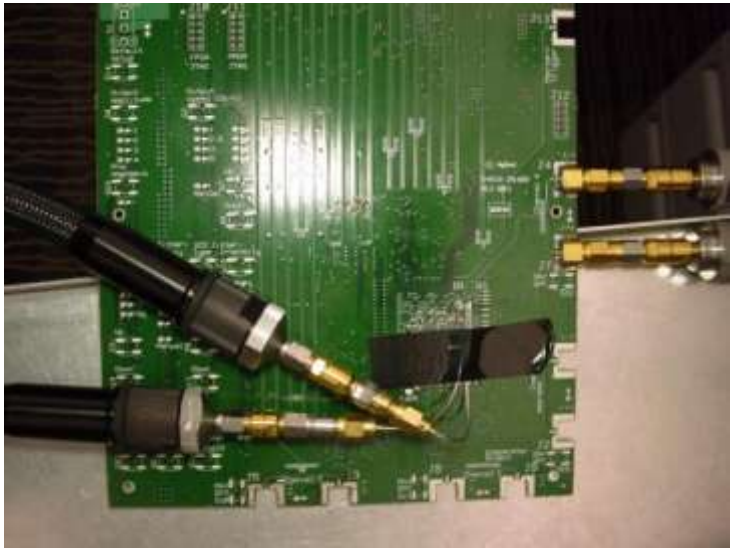


Load S-Parameters into Signal Path

Obtaining S-21

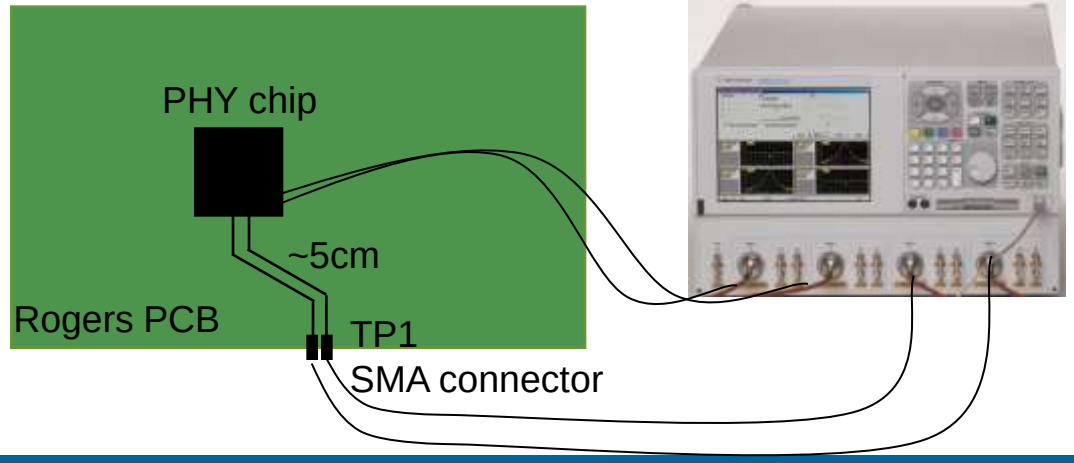






Use SMA's when Available
May require special probing
and board modifications if not.

Agilent N5230B-245 20GHz
Vector Network Analyzer



S-Parameters

m100223a_DemBd54916_26408v5sn450_A_p1J16p2J17.s2p - Notepad

File Edit Format View Help

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!Agilent Technologies,N5245A,MY49151035,A.08.60.09
!Agilent N5245A: A.08.60.09
!Date: Tuesday, February 23, 2010 18:18:08
!Correction: S11(Full 2 Port(1,2))
!S21(Full 2 Port(1,2))
!S12(Full 2 Port(1,2))
!S22(Full 2 Port(1,2))
!S2P File: Measurements: S11, S21, S12, S22:
# Hz S  dB   R 50
10000000 -1.224343e+001 -1.772934e+002 -4.689444e+000 -4.055600e+000
20000000 -1.221624e+001 1.791212e+002 -4.735650e+000 -5.167600e+000
30000000 -1.223820e+001 1.770460e+002 -4.753351e+000 -6.887907e+000
40000000 -1.224887e+001 1.752930e+002 -4.758249e+000 -8.748381e+000
50000000 -1.225741e+001 1.736047e+002 -4.773274e+000 -1.065208e+001
60000000 -1.229180e+001 1.720742e+002 -4.772188e+000 -1.257893e+001
70000000 -1.232777e+001 1.705868e+002 -4.775970e+000 -1.455881e+001
80000000 -1.235762e+001 1.691501e+002 -4.780704e+000 -1.653611e+001
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100000000 -1.243223e+001 1.662739e+002 -4.794525e+000 -2.045283e+001
110000000 -1.247415e+001 1.648788e+002 -4.802291e+000 -2.244328e+001
120000000 -1.251828e+001 1.634819e+002 -4.808766e+000 -2.442240e+001
130000000 -1.256693e+001 1.620814e+002 -4.814651e+000 -2.640366e+001
140000000 -1.262438e+001 1.607373e+002 -4.820703e+000 -2.839193e+001
150000000 -1.268803e+001 1.594424e+002 -4.828022e+000 -3.037498e+001
160000000 -1.274603e+001 1.581215e+002 -4.833044e+000 -3.234686e+001
170000000 -1.280791e+001 1.567978e+002 -4.840835e+000 -3.432754e+001
180000000 -1.287825e+001 1.554966e+002 -4.847504e+000 -3.631363e+001
190000000 -1.295092e+001 1.541922e+002 -4.852639e+000 -3.828690e+001
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250000000 -1.346412e+001 1.468278e+002 -4.896165e+000 -5.012396e+001
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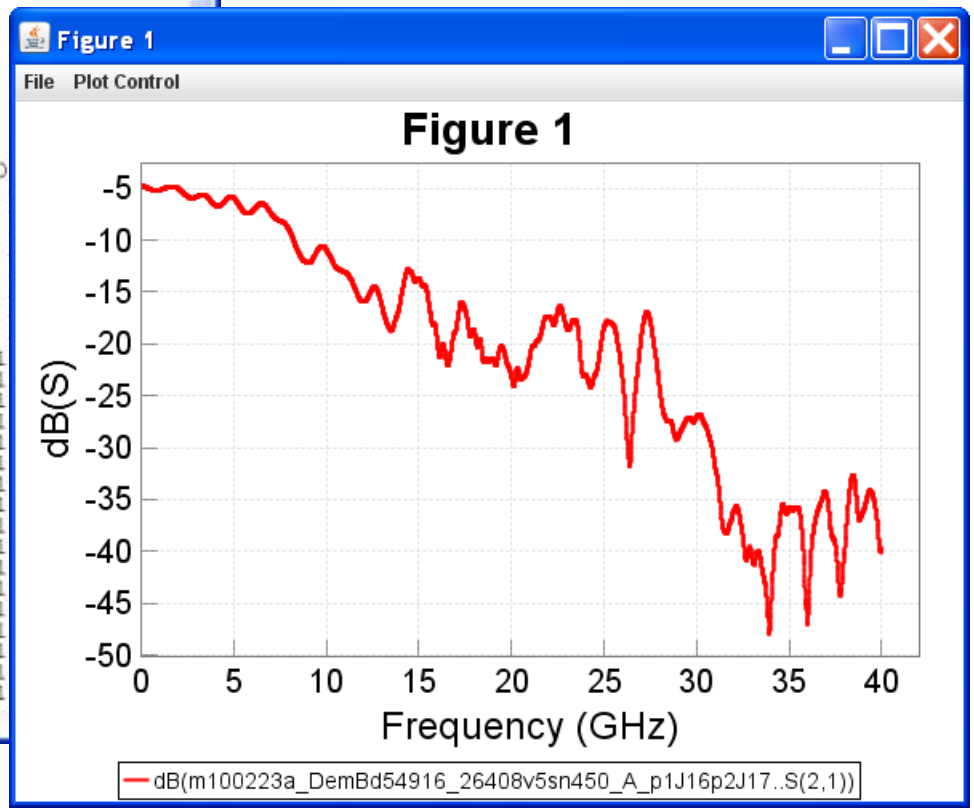
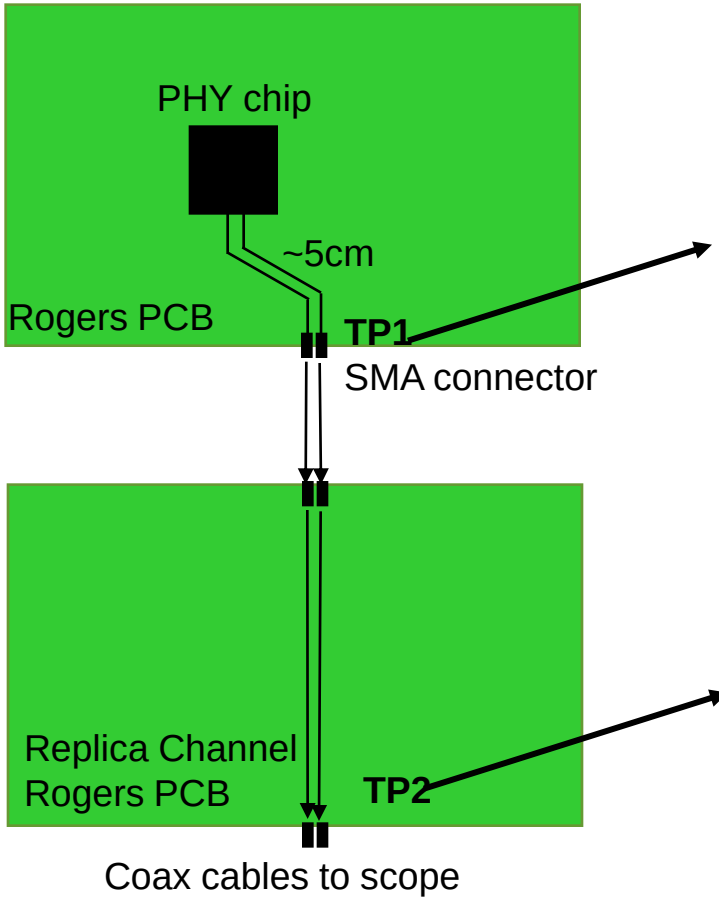
```

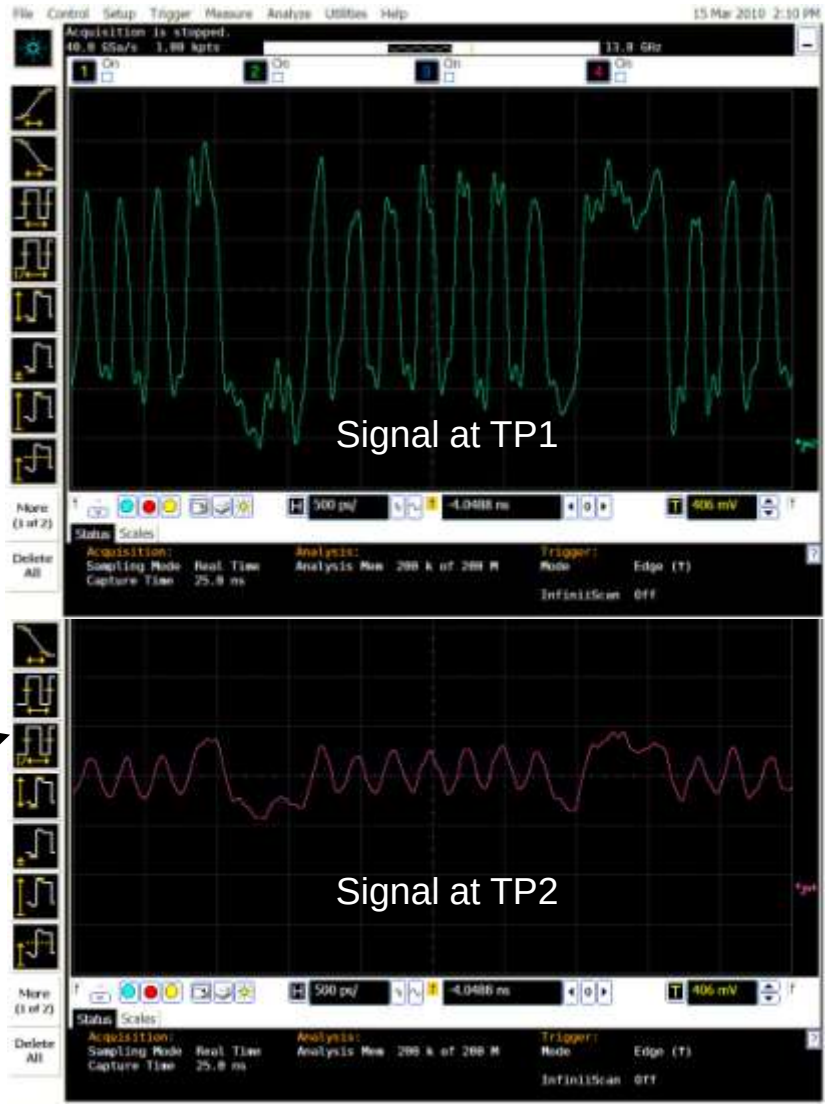
S2P File



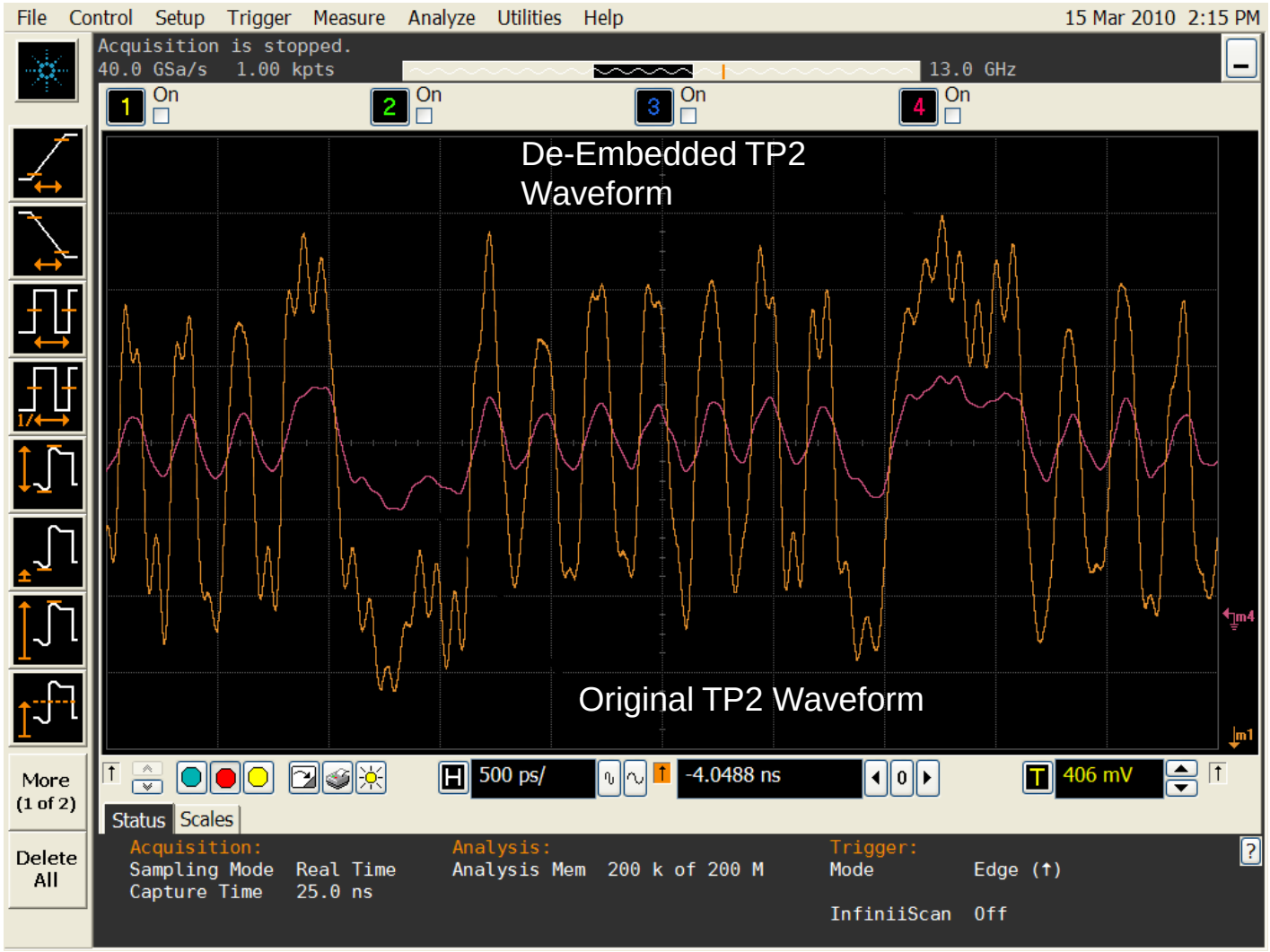
S21 Insertion Loss

Measurement of 8GT/s Signal





De-embedded Waveform Measurements



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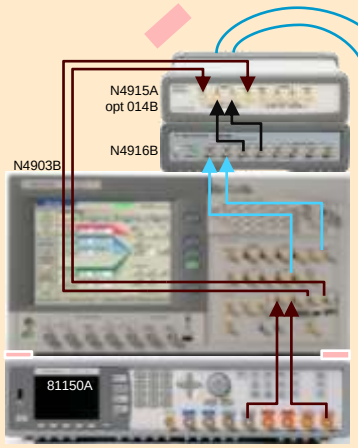
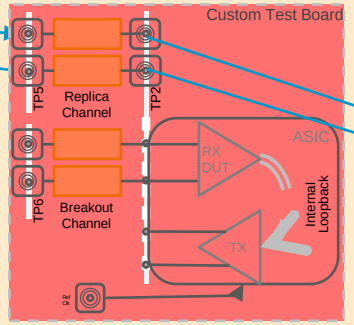
Why is Phy-layer of PCIe3 so Different from PCIe1&2? Goals and Consequences

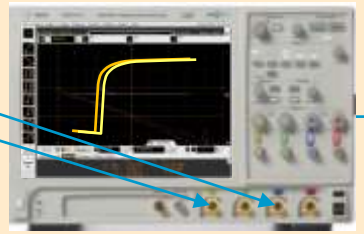
- Effective data rate shall be doubled
- Existing infrastructure of PCs and servers shall be reusable, which means:
  all PCIe2-compliant channels shall also be compliant with PCIe3
  simulations showed: TX-de-emphasis not sufficient to achieve desired eye opening

⇨ **RX equalization is necessary**

Comparison of Calibration Methods Base vs CEM

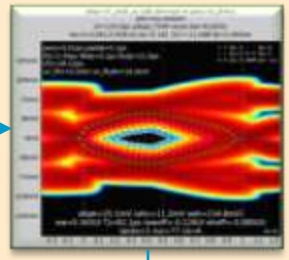


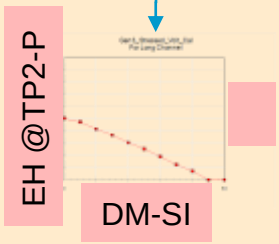




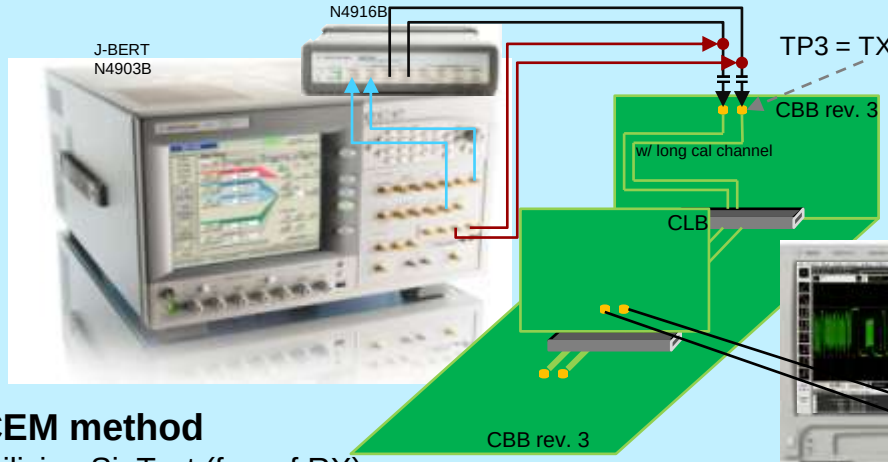
input parameters:
RJ = 2ps,rms
SJ = 0.1UIpp
DM-SI =14mVpp

SEASIM





Base-Spec method utilizing Seasim :
averaged step response,
simulated pattern & impairments & ref RX



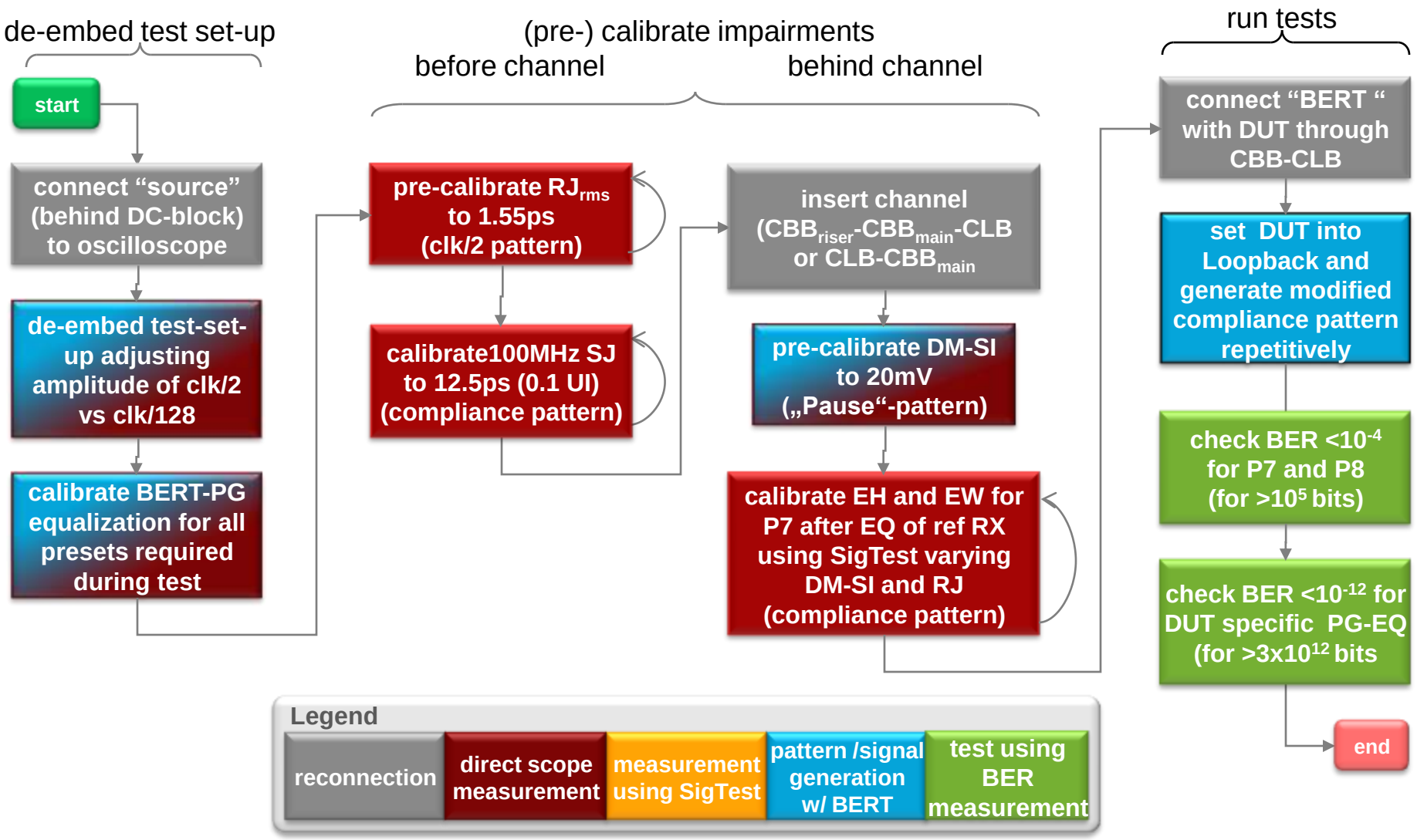
TP6/TP2 = RX-pin

SigTest SW

TP2-P = RX behind EQ

CEM method
utilizing SigTest (for ref RX):
compliance pattern w/ impairments „on“ w/o scope averaging

Calibration and Test Flow Chart



Calibration of Jitter Value or Eye Opening using SigTest-SW

The calibration procedure for any jitter value RJ, SJ (TJ) or eye opening (EH & EW) always consists of the following steps:

1. Set start value on J-BERT
2. Save waveform on DSA in bin format
3. Upload waveform to SigTest and calculate signal parameters using appropriate “Technology“ and “Template“ pressing <Test> button
4. If relevant result is out of target window adjust parameter on J-BERT accordingly and repeat procedure from 2.
5. Otherwise record value for later use

Note: DM-SI is determined w/o SigTest-SW by direct scope measurement

Typical Values on J-BERT
Achieving a Calibrated Stress Signal

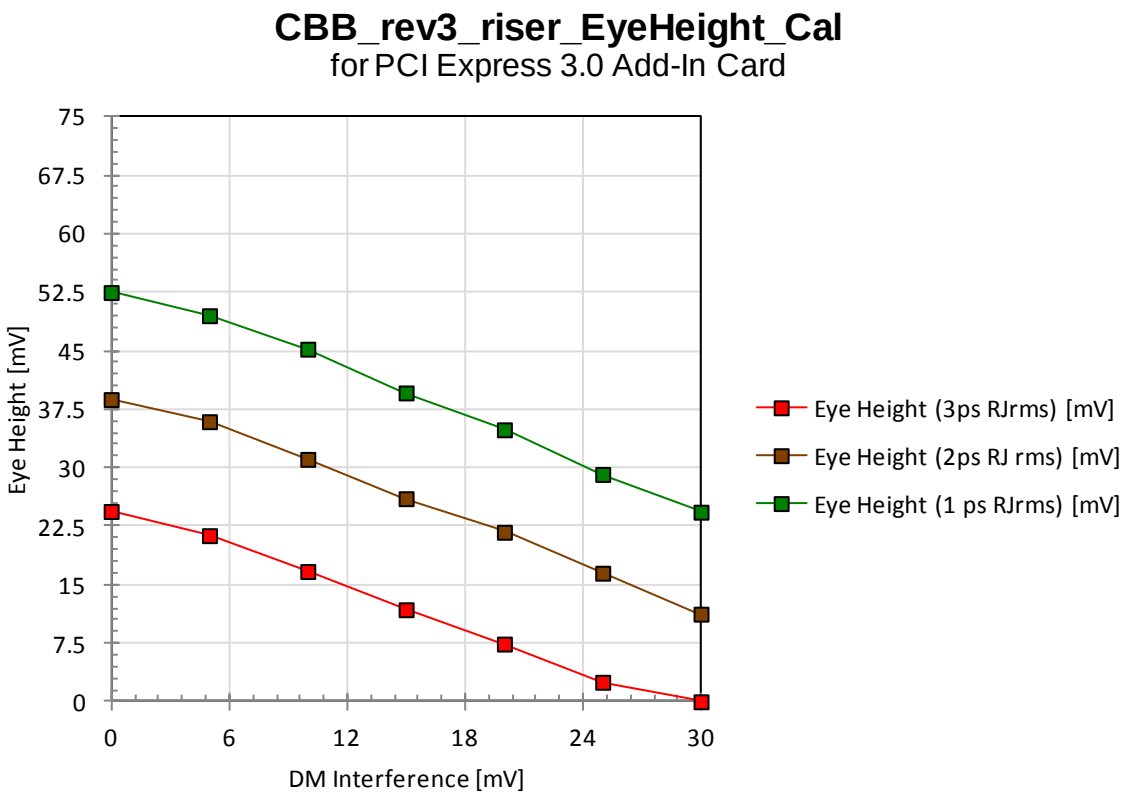
	de-embed	P7	P8
Vampt / mV	604	604	604
Pre-Curs / dB	0	4.1	4.1
Post-Cur1 / dB	-0.7	-4.5	-7.1
	pre-adjust	final adjust (EW/ EH)	
RJ / mUI (ps) RMS	11.5 (1.44)	11.5 (1.44)	
PJ2 / mUI (ps)	110 (13.8)	110 (13.8)	
DM-SI /mV	45	110	

Actual values may differ because they depend on parameters of individual units in use, as well instrumentation, accessories or SIG-boards

N5990A Automation SW option 101, PCIe
Calibration of Eye Opening of Stress-test Signal

Eye opening (EH and EW) is calibrated over a wide range of impairments

Not only the compliance point can be tested but the DUT‘s margin can be determined as well



Conclusions

1. Probing at pins of device not practical at PCIe 3.0 speeds of 8GT/s.
2. De-embedding may remove fixture effects and recover some jitter margin.
3. Voltage measurements more impacted by de-embedding noise compared to jitter.
4. Calibration of the stressed eye for receiver test should minimize effect of instrument noise.
5. Stressed eye for RX testing is referenced to the die pad for the receiver. TX voltage and jitter parameters are generally referenced to the pin of the device.
6. Calibration Channel is crucial for ensuring RX signal amplitudes are at the proper level at the RX Die pad.
7. CEM RX Test Calibration still TBD but should be ready by April workshop in Milpitas
8. Tools for full PCIe 3.0 TX and RX testing are available today.

Thank you!
Questions?