A NEW TEST STRATEGY FOR COMPLEX PRINTED CIRCUIT BOARD ASSEMBLIES

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Introduction

The trend in Printed Circuit Board Assembly (PCBA) technology is towards higher complexity. Many boards have significantly more components and solder joints today than just a few years ago. More components and more solder joints means more defect opportunities and lower yields. A higher number of components typically means higher cost for each PCBA, resulting in higher WIP cost (work in process) and scrap costs. The higher WIP costs and scrap costs are also because higher complexity typically means lower yields and more difficulty in diagnosing when failures occur. Today's smaller components are also increasing the challenge to place them correctly on the PCB. Components such as 20 mil and 16 mil QFP's and 0402 and 0201 chip components are examples in this same category. At the same time, we are loosing the 100% electrical access that we have relied so heavily on for the success of In-Circuit Test (ICT). We are also losing visual access of solder joints, such as the joints under a BGA. The decrease in electrical and visual access makes it more difficult for effective test and inspection techniques.

To place even more fuel on the fire, Time to Market pressures and requirements to ramp up volume faster with less resources is placing the manufacturer in a no-win situation. To stay competitive you need a test and inspection strategy that addresses all these trends. We have come to a cross-road and it is time to think about the test/inspection problem from a new point of view.

The common test strategy

The most common test/inspection strategy today is Manual Visual Inspection (MVI), followed by In-Circuit Test, and then some form of Functional Test (FT), as seen in Figure 1.

The grid patterns indicates fault coverage and each test method has significant fault coverage. However most test engineers have spent little time analyzing overlapping fault coverage as well as missed fault coverage, resulting in both overlapping fault coverage and for some fault

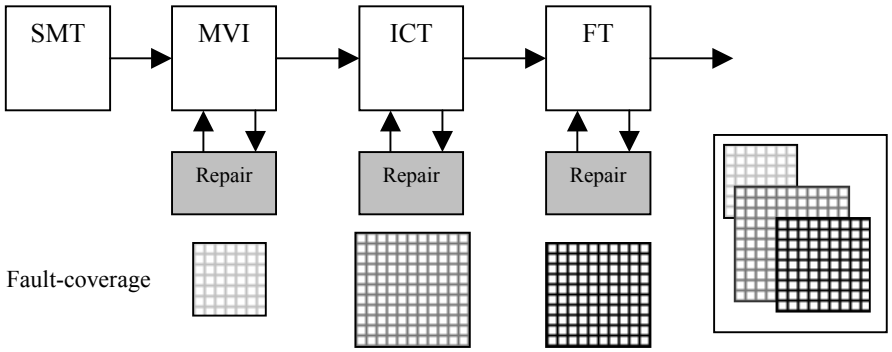


Figure 1

types, missed coverage. This is indicated in figure 1 with the three overlapping grids in the white square to the right. The white area in the square indicates missed fault coverage. Overlapping fault coverage indicates potential for lowering total test cost and missed fault coverage means lower quality of shipped products and more field failures.

Complexity index.

Since this paper proposes a new test strategy for complex boards it is important to define complexity in this context. Listening to many in the industry you hear that everybody believes that they have very complex boards. However you can clearly see that some boards are significantly more complex than others. So the phrase "high complexity boards" is very subjective. To have a good understanding of complexity it would be an advantage if we speak the same language. To be more objective, this paper will introduce a Complexity Index (Ci) so we can better understand what we are discussing. This complexity index is from a manufacturing point of view, not from a testing point of view. The basic idea is that, the higher the complexity, the more difficult it is to achieve high yields without any test and inspections.

- The more components that are placed on a PCB and the more solder joints that needs to be soldered correctly— the higher the complexity it is to make it correct.

- Also in a high mix – low volume environment it is more complex to make the PCBA without any defects. You don't have the luxury to fine-tune your manufacturing process, as you can in a high volume environment.

- It is also more difficult to have high yields for a double-sided SMT board, than for a single-sided board. For a double-sided board there are more manufacturing steps and the boards go through the reflow process twice (or reflow /wave).

All of the factors indicated above adds to the complexity to build it without any failures and therefore the Complexity Index used in this paper have the following formula:

$$Ci = ((\#C + \#J)/100)) * D * M$$

Where:

Ci = Complexity Index
#C = Number components
#J = Number of joints
D = Double sided D = 1 and Single sided D = 0.5
M = High Mix M = 1 for high mix and M = 0.5 for low mix.

We could also include number of fine-pitch components and number of 0402's and 0201's but for the objective to make the Complexity index as simple as possible, they are not included.

Complexity type	Complexity index
Low complexity	< 25
Medium complexity	>= 25 and < 75
High complexity	>= 75

Table 1

In Table 1, low complexity PCBA's, medium complexity PCBA's, and high complexity PCBA's has been defined. The test/inspection strategy proposed in this paper is targeted mainly for high complexity boards. It may also make economic sense in some cases for medium complexity boards, but are unlikely to be a good economic decision for low complexity boards.

The question arises if the difficulty to test should impact the Complexity Index. It could be argued that the difficulty of test is mainly a function of what test techniques you are using and what faults you are looking for. If you are looking for solder opens on a very complex ASIC, without Boundary-Scan, and are using traditional ICT vector techniques, everybody would agree that it would be very difficult and time consuming to do. However, if we are using X-ray instead to find the solder opens on the same complex ASIC, it becomes trivial. We do not even need to know which pins are inputs or outputs. Since the complexity from a testing point of view is significantly dependent on test methods used, it is not included it in this formula.

Board Complexity and test economics

The bottom line of all testing is the economics. Let us look at three different boards, a low complexity, a medium complexity, and a high complexity board and see the economics for these three cases.

- The low complexity board has 75 components and 425 solder joints. It has between 75 to 150 electrical nodes.
- The medium complexity board has 550 components and 4,450 solder joints. It has between 700 to 1,500 electrical nodes.
- The high complexity board has 2,500 components and 17,500 solder joints. It typically has between 3,000 to 4,000 electrical nodes.

First, what kind of yields should we expect for these three board types? Let's assume that we have a manufacturing process with a defect level of 200 DPMO (Defects Per Million Opportunities) for both components and for solder joints. If we use the formula that the yield is

$$\text{Yield} = [1 - (\text{DPMO}/1{,}000{,}000)]^{N}$$

Where DPMO is Defects Per Million Opportunities
N = Defect Opportunities

- For the low complexity board we have 500 defect opportunities (75 components + 425 solder joints),
- the medium complexity board has 5,000 defect opportunities (550 + 4,450), and
- the high complexity board has 20,000 defect opportunities (2,500 + 17,500).

The formula above results in a yield out of our SMT process of
- 90% for the low complexity,
- 37% for the medium complexity and
- 2% for the high complexity board.

This means that almost all of our low complexity boards will be good, while almost all of high complex boards will have at least one failure per board.

Let's assume that for each board type we have one dedicated SMT line, running 24 hr/day, 5 days a week and 50 weeks per year. For the low complexity board we will produce 1,600,000 boards per year, 160,000 boards for the medium complexity and 40,000 boards of the high complexity type. Let's also assume that the manufacturing cost for the low complexity board is $20, for the medium complexity $400 and $4,000 for the high complexity board.

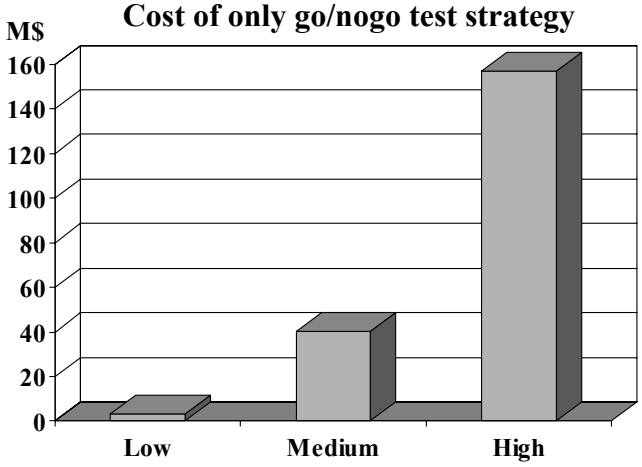
"Test provides no value added"

You hear this statement now and then, and if that was true, then one strategy we could select is to do a very simple go / no-go test. We ship the boards that work. We do not do any repairs on the boards that fails, we just throw them away, or scrap them.

The yearly cost of this less than perfect strategy is for the low complexity board $3.2M. 1,600,000 board * 10% (scrap rate) * $20 (board cost). The cost for the medium complexity board is $40.3M and for the high complexity board $156.8M. With this strategy we can see significant differences in costs for the three different cases even if the total number of defect opportunities per year is the same. If our test and repair costs are lower than these numbers, then test will add value to the bottom line. A summary of this example can be seen in Table 2 and Figure 2.

	Low complexity	Medium complexity	High complexity
Complexity Index	5	50	200
Number components	75	550	2,500
Number solder joints	425	4,450	17,500
Defect opportunities	500	5,000	20,000
Nodes	75-150	700 – 1,500	3,000-4,000
Yield out of SMT (no test)	90%	37%	2%
Number boards / year	1,600,000	160,000	40,000
Cost per board	$20	$400	$4,000
Value scrapped boards	$3,200,000	$40,320,000	$156,800,000
Yearly defect opportunities	800,000,000	800,000,000	800,000,000

Table 2



Note that all three cases have the same number of defect opportunities per year.

Figure 2

From Table 2 and Figure 2, we can see that an effective test strategy is important in all cases, however we can clearly see that it is most important for the high complexity board. A key point in the example above is that all three cases have the same amount of defect opportunities per year. So even with a given defect level and quality requirement different, test strategies should be selected depending on the board complexity.

Today's fault spectrum and defect levels

In selecting an optimal test strategy it is important to have a very good understanding of the current fault spectrum. It is important to stress current fault spectrum because it is changing over time. For example, component failures are significantly lower today and I quote *"Component quality levels within the semiconductor industry have improved significantly over the last 2 decades. As we approach silicon defect rates in the magnitude of parts per billion, we believe there is a reduced need for electrical verification of components when performing structural test"* (1). Today with fine-pitch components and double-sided SMT boards, the solder joint defects are a higher percentage of total number of faults. In addition to having a very good picture of the fault spectrum, it is important to also have a good measure of defect levels.

Below is a study done on four different major companies that are using 3D Automatic X-ray Inspection (AXI) as a complement to traditional test strategies. All these four companies have a high mix, low volume manufacturing process. Data has been gathered on an inspection of a large number of solder joints, 139,837,570 on 85,594 boards. Only those failures detected by the AXI equipment and repaired have been entered into the database. In this study a total of 335,895 faults were detected and repaired. If we count each solder joint inspected as one Defect Opportunity, than this results in a defect level of 2,402 DPMOsj (Defects per Million Solder Joint Opportunities). This number is significantly higher than the typical "party line" used in the industry. Figure 3 shows the DPMOsj levels for the different board types included in this study.

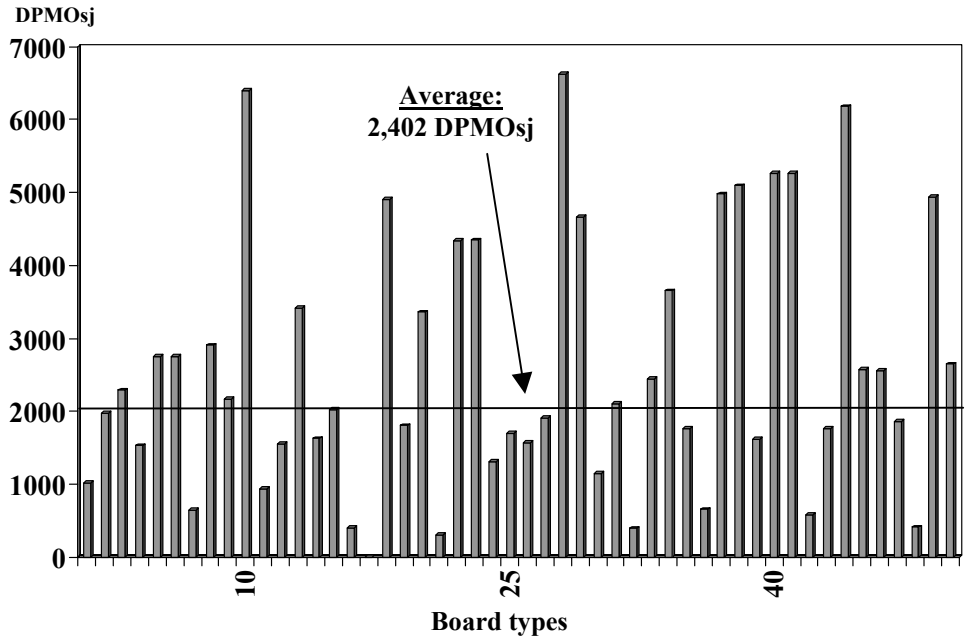


Figure 3

The fault spectrum of the 335,895 faults can be seen in figure 4. The most dominant fault type in this study was opens, followed by shorts and insufficient solder.

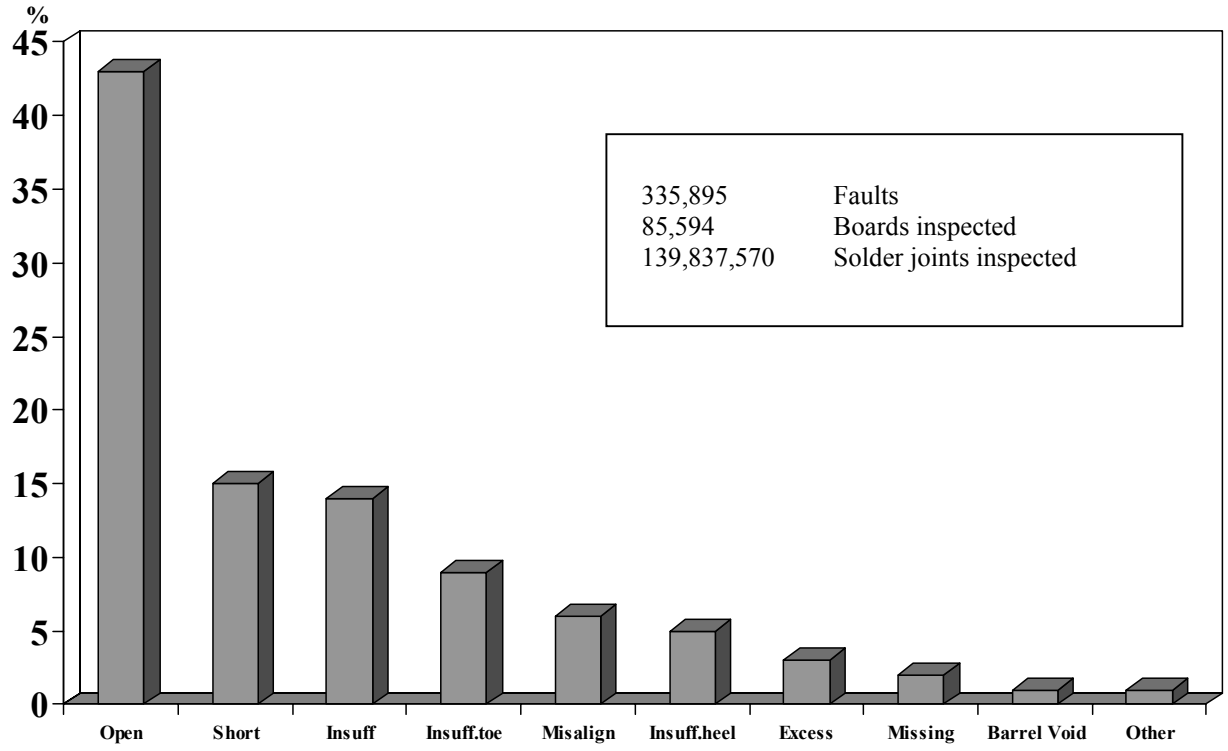


Figure4

Note that in this study only repaired solder defects has been included. However, if manufacturing component failures such as misoriented components, wrong value components, and functional faults would be included, they would not typically be part of the three highest bars in the fault spectrum.

A key point in this study is that defect levels for high mix – low volume boards are significantly higher than what typically is said in the industry.

The problem of testing high complexity PCB's

We have addressed the economic case for testing high complexity boards and talked about fault spectrum and defect levels. However, there are other issues when testing high complexity boards that are important when selecting a test strategy.

It is common knowledge that it is a cost advantage to find defects as early as possible. Therefore it is important to try to have a high fault coverage as early in the manufacturing process as possible. Manual Visual Inspection on complex boards, with fine pitch components and many hidden solder joints, is not adequate. AOI could be considered, but since the majority of defects are solder related, we should select the test method with the highest possible fault coverage of solder defects. The recommended inspection tool is AXI, which has the highest fault coverage for this type of failures. Also, as will be seen later, significant reduction in test overlap can be achieved if very high fault coverage of shorts, opens, and missing components can be achieved before electrical test is done.

If we turn are attention to the ICT test for high complexity boards, we can see some short comings. If a high fault coverage is desired, very long programming time is most often needed. In addition, turn around time for the fixture build can be significantly longer when the probe count is over 3,000 to 3,500 probes. Both of these characteristics will have a negative impact on the manufacturer's important Time-to-Market issue.

In addition, there are other difficulties with the traditional ICT test strategy for the most complex boards. The fixture cost is expensive, the probability of fixture contact problems increase with more test probes that need to hit shrinking test targets. This results in numerous re-tests and difficulties in differentiating between real faults and fixture induced faults. The mechanical forces put on the PCBA is significant and vacuum fixtures are not always enough. To overcome those forces often pneumatic fixtures are needed, increasing the cost and weight of the fixtures. Several manufacturers have tried the traditional ICT approach with less than optimal results for this type of boards. They have begun searching for alternatives to this traditional test strategy, (ICT) for high complexity boards. It is clear that it would be an advantage if the new strategy:

- has a very high fault coverage of solder defects as early as possible,
- uses simpler, more reliable fixtures,
- has higher yields into functional test, and
- provides solutions to limited electrical and visual access

New recommended test strategy

The new recommended test strategy for complex PCBA's is to replace manual visual inspection with Automatic X-ray Inspection (AXI). After the PCBA's have been x-ray inspected they are ICT and Functionally tested. The new test strategy is shown in Figure 5

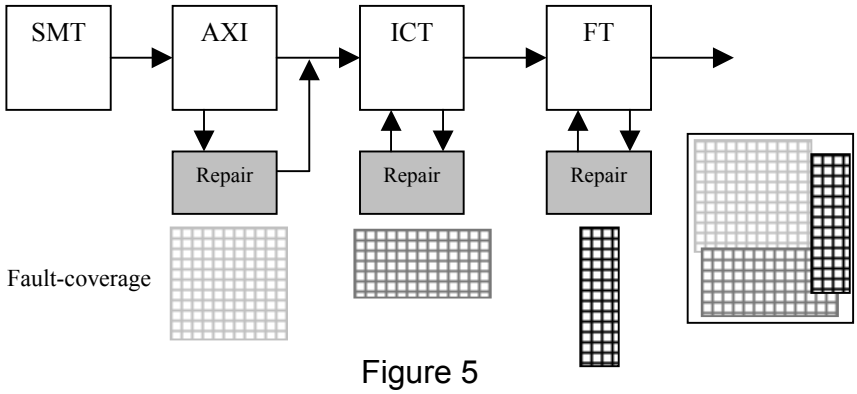


Figure 5

Note that we have higher fault coverage and less overlapping test coverage in this case. We can achieve the less overlapping test by simplifying the ICT test. But before we talk about how we can simplify the ICT test, let's first see how AXI and ICT compliment each other before we discuss how we can simplify the ICT test and the ICT fixture.

There are many users of this AXI-ICT-FT strategy today. The following two quotes are from two of those AXI-ICT-FT users and are taken from published articles.

"The biggest single impact is yield at ICT; we saw this rise from an average of about 75% up to 95%". "It was literally a step change" (2)

"Neither the AXI or ICT system alone could have achieved the net effect of the complementary test strategies. Incorporating both systems has increased manufacturing defect coverage on products to 97%; lowered field failures, warranty and repair costs; and allowed greater design flexibility. Products move to market faster, costs are lower and quality is higher. A complementary approach is key." (3)

Also a study done by an Hewlett-Packard division shows higher yields into Functional Test, fewer field returns and lower overall costs if an approach of AXI and ICT is used to find manufacturing faults. The following is data gathered within HP that shows the effectiveness of the combination of AXI and ICT before Functional Test. This HP division is using a Contract Manufacturer (CM) for their board manufacturing. The CM can provide MVI, AXI, and ICT test, while the HP division does its own Functional Test. Each PCBA has a unique serial number and field failures are also tracked, using these unique serial numbers.

This data is not an experiment, it is data gathered from normal production and field failures over a significant amount off time. The 6,928 boards in this study are of the type high mix – low volume.

Six different board types are included in this data. For one board type no AXI or ICT were performed, only minimal MVI, due to lower anticipated lifetime volume and lower complexity. For five board types ICT was used. However very good experience with the combination of AXI and ICT made them add AXI to all of these five board types. Table 3 shows how many boards we have in each group.

Capability to detect solder defects. In Table 3, you can see each major test strategy's effectiveness of detecting solder related defects. The DPMOc levels reported are defects detected at Functional Test. DPMOc is Defects Per Million Component Opportunities. If only Manual Visual Inspection was used, Functional Test saw 419 DPMOc solder defects. If ICT was added this number was reduced to 195 DPMOc, and if a combination of AXI and ICT were used this number was reduced to 23 DPMOc. In this study no data is available of the effectiveness of AXI alone, but experience and earlier mentioned references indicate that AXI is extremely effective in finding solder related defects.

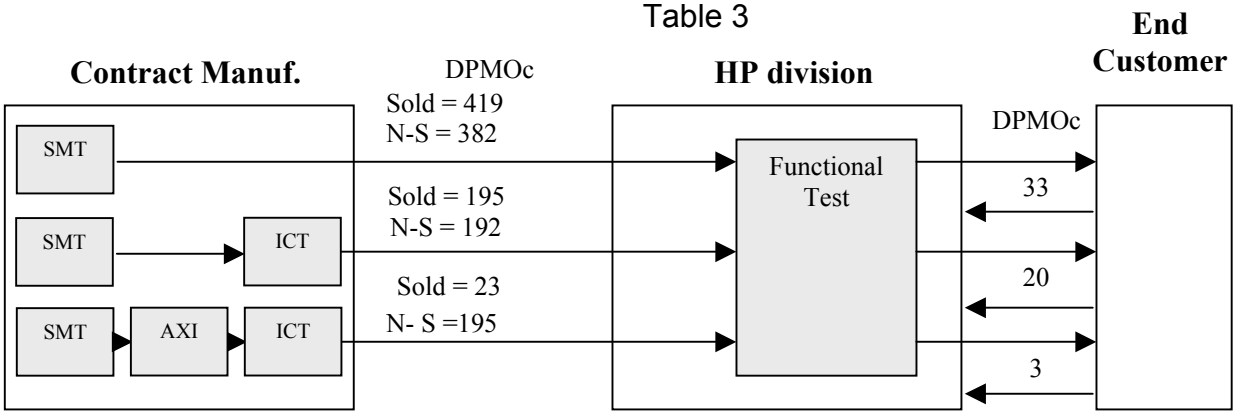
Capability to detect Non-Solder related defects. Table 3 indicates the different strategy's effectiveness in detecting non-solder related defects. If only Manual Visual Inspection is used 382 DPMOc is detected at Functional Test. If ICT is added the defect level decreases to 192 DPMOc. If both AXI and ICT is used the defect level basically stays the same at 195 DPMOc. This is not to surprisingly since AXI is not well suited to detect non-solder related defects.

Capability to reduce Field failures. In Table 3 the field failures can be seen for boards that have gone through the different test strategies. The boards that have only been visually inspected and functionally tested have a field failure rate of 33 DPMOc. If ICT has been added—this decreases to 20 DPMOc. For boards with both AXI, ICT, and Functional Test, the field failure rate is down to 3 DPMOc for this sample of boards. Figure 6 is an overview of the

different test steps and their effectiveness. Figure 7 is a graphical illustration of the different strategies effectiveness.

Activities prior to Functional Test	Number of boards	Faults found at Functional Test			Field failures DPMOc
		Solder defect DPMOc	Non-Solder DPMOc	Total DPMOc	
SMT+ mvi	3,147	419	382	801	33
SMT+mvi +ICT	2,642	195	192	387	20
SMT+AXI+ICT	1,139	23	195	218	3

Table 3



Total of 6,928 boards in the study. Sold = Solder defects. N- S = Non solder defects.

Figure 6

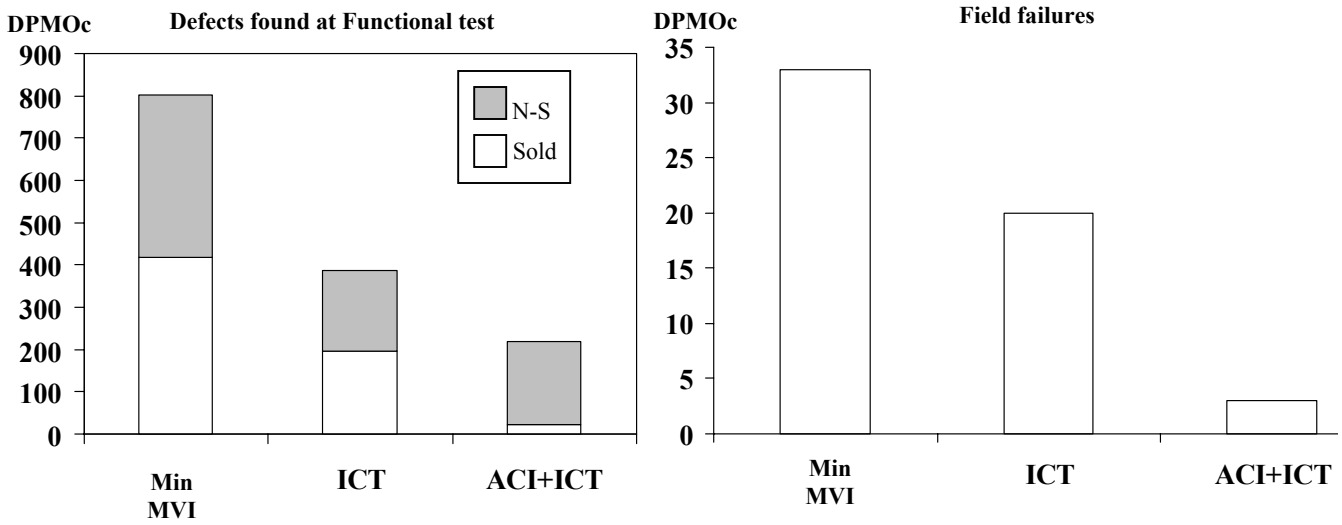


Figure 7

This study shows that a combination of AXI and ICT in front of Functional Test is very effective of finding manufacturing type defects. AXI is very effective at finding solder related defects and ICT is very effective at finding non-solder related manufacturing defects. It is also interesting to note that field returns are significantly reduced when both AXI and ICT are used. The reduction in field returns when ICT is used is due mainly to a more effective test of safety circuits that normally is very difficult to find in Functional Test. The field failures are reduced

when AXI is used because AXI is very effective at finding marginal solder joints. Marginal solder joints are electrically correct during test, but are likely to fail during thermo cycling and mechanical stress. Note that adding ICT cuts field failures by up to half and adding AXI reduces field failures close to an order of magnitude, a very significant number! For high complexity boards, with many defect opportunities, this is even more significant.

Divide and conquer

The previous data illustrates significant benefits in using a combined test strategy. However additional benefits can be achieved if the test problem is looked upon with new perspective.

A very old strategy, to simplify test, is to “divide and conquer”. Let us look back in time to the late sixties and early seventies. At that time Functional Test was the dominant test strategy. PCBA’s were very simple compared to today’s technologies. Program development simpler and fault diagnosis for a faulty board was in most cases straightforward. However, as complexity increased—a complementary test strategy was needed and the birth of the in-circuit tester occurred. The idea with ICT was the classical test approach of “divide and conquer”. Instead of testing functions of the PC board assembly, the ICT tested individual components, simplifying program development and improving diagnostic resolution. As we saw with the addition of ICT in the mid-seventies, we have come to a similar case today were we need a new way to “divide and conquer” for the most complex boards. The suggested way to “divide and conquer” today’s most complex boards is to separate solder joint testing from component testing.

AXI has an extremely high fault coverage of solder joint defects, such as opens, shorts, insufficient solder and other marginal solder joints. The key to this new strategy is to recognize the strength of AXI and take advantage of it during ICT test development. Let us think about what we can do during ICT test development if we have already removed all shorts, opens and identified all missing components.

Simplified ICT test and simplified ICT fixtures

The result if all shorts, opens and missing components have been removed is a much simpler ICT test. The manufacturing faults that remain are of the type: wrong value component, wrong component, misoriented component, damaged component, etc. If we only are trying to test, that the right component is placed, its basic functionality, and that it is oriented correctly, we can simplify the ICT test. As an example you can consider the circuit in Figure 8. This circuit is an octal buffer and it has series resistors on all inputs. The series resistors are in one resistor pack. The traditional ICT strategy for a circuit like this is to first test for shorts, second to test all resistors to make sure they have the right value and that we do not have any opens on the resistor pack pins. Last we test all pins on the octal buffer, to verify that we have the right component and that all pins are soldered correctly. To test the circuit in this way needs 25 test probes.

If we use the new strategy and are only testing for, right component, basic functionality, and right orientation, then we only need to test one resistor in the resistor pack and only one of the eight buffers. Note that number of test probes in this case is reduced to four.

Since AXI has a very high fault coverage of solder defects and ICT has a very good fault coverage of component failures the overall fault coverage is significantly higher than the traditional test strategy. In addition, this strategy has less overlapping fault coverage. As an example, if you test for opens using both AXI and ICT you have an overlapping fault coverage. When trying to minimize test cost without reducing fault coverage, you should try to eliminate as much overlapping tests as possible.

"With improved component quality, we can rely on methods like AXI to detect solder shorts and opens, and do not require an ICT probe on every component I/O to check for component shorts and opens" (1)

It should be noted that some component failures and silicon failures, could go undetected from the AXI and ICT test steps. However remember that some sort of Functional Test is part of the entire test strategy. Overall impact will be higher yields into Functional Test, however a few faults that could have been detected at ICT will now be detected at Functional Test.

In addition early indications also shows that total test development time for this new test strategy is shorter than the conventional test strategy.

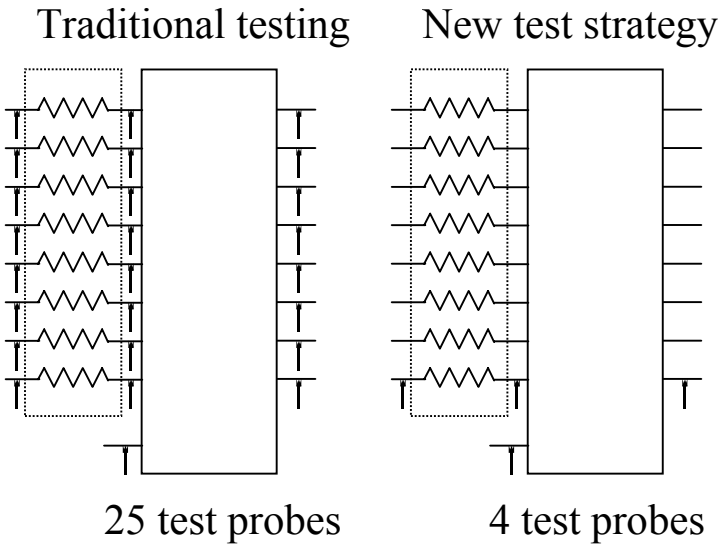


Figure 8

Result on probe reduction techniques

The probe reduction techniques that was just described has been tested on several real boards. At the deadline of this paper four boards have been analyzed with this strategy in mind. The result of this study can be seen in Table 4. The second column indicates board complexity, board A was only single-sided therefore it was classed as low complexity. The next column indicates number of nodes (or test probes) if all nodes were probed. The next column is when "all" components are tested, however using the technique of only testing one resistor in a resistor pack and if possible only a few pins on an IC. The following column indicates percentages of probes that could be removed if that strategy was selected. The second to last column is showing how many test probes were needed if, in addition to the strategy in the "all"

test, the strategy of doing “reel” test were implemented. “Reel” test is when we only measure the first and last mounted components that are coming from the same reel of the pick and place machine. We call this “Reel” test. “Reel” test applies mainly to resistors. The last column shows probe reduction as a percentage if all probe reduction techniques have been used.

Board ID	Complexity	# nodes 100% access	# probes needed “all” test	% probe reduction “all” test	# probes needed “reel” test	% probe reduction “reel” test
Board A	Low	790	577	27.0%	360	54.4%
Board B	Medium	773	453	41.4%	345	55.4%
Board C	High	2,880	2,055	28.6%	1,910	33.7%
Board D	High	5,644	2,603	53.9%	1,921	66.0%

Table 4

As can be seen in Table 4 significant simplifications of the test fixture can be achieved if this strategy is implemented. Early indications also shows easier debug when this strategy is used.

Note that the probe reduction technique does not need to be applied to all components. For instance a Flash-ram or a very critical component can be 100% probed as usual. The probe reduction technique gives more flexibility and a Design-For-Test tool when you are forced to reduce electrical access and also when you would like to lower overall test costs.

Future work

In this paper data has been presented that clearly supports the superior fault coverage when a combined AXI – ICT strategy is used before Functional Test and result of probe reductions techniques has been shown. The next step that we are planning to do is to verify that the probe reduction technique does not result in lower yields when used in real production situations. Based on the experience, the data gathered to date and the typical fault spectrum that exists in the industry, we have high confidence that no significant reduction in fault coverage will result in the use of this strategy. We will continue to study actual manufacturing test results, using this test strategy, to substantiate this theory.

Also studies will be performed to see the amount of reduction in test development time that this strategy is capable of delivering.

Conclusion

This paper has presented a new test strategy for high complexity printed circuit board assemblies. The strategy is based on complementary use of AXI, ICT, and Functional Test. The key benefits are higher fault coverage, resulting in higher yields into functional test and lower field failures. Less overlapping tests are also resulting in simplified in-circuit test and simplified in-circuit fixtures. It also provides a good solution when electrical and visual access is reduced. In almost all cases it also have significant economic advantages.

Also note that it is outside the scope of this paper to talk about the most optimal test strategy for low complexity boards, and medium complexity boards.

References

(1) Effective Structural Test Strategies for High Complexity Boards, Amit Verma, The Test ’98 Conference

(2) X-ray Vision Improves Yield, David Evans, TEST November/December 1996

(3) No Single Test Strategy, Steve Bonham and Wayne Singbeil, Circuits Assembley November 1997.