

Agilent N4880A Reference Clock Multiplier

Data Sheet

Preliminary Version 0.91

Accurate and simplified receiver test for PCI Express ®,

SD UHS-II host and MIPI M-PHY devices:

- Multiplies 19.2 to 100 MHz reference clocks to an external clock signal for J-BERT or ParBERT pattern generators
- Transparent to 33 kHz SSC on the reference clock because N4880A uses a multiplying PLL with 2 or 5 MHz loop bandwidth
- Tolerates small input signals with an input sensitivity of 100 mVpp differential
- Stand-alone graphical user interface and remote control interface via rear panel USB 2.0 connection



Agilent N4880A Specifications

Table 1: Specifications for N4880A	
Reference clock input	50 Ω differential, DC coupled, unused input has to be terminated with 50 Ω
Clock input frequency range	PCIe™: 100 MHz , UHS-II: 26 to 52 MHz , MIPI M-PHY: 19.2 MHz, 26 MHz, 38.4 MHz, 52 MHz
Clock input voltage range	100 mVpp to 2 Vpp differential
Clock input transition times	< 7.7 ns (20 %/80 %)
Loop bandwidth	PCIe: typ. 5 MHz , UHS-II: typ.2 MHz , MIPI M-PHY: typ.2 MHz (see also table 2)
Clock input duty cycle	45 % to 55 %
Max. input voltage level	-3.0 V to +3.0 V
SSC	Reference clock input tolerates up to 3% SSC down-spread modulated with 33 kHz for 26 MHz reference clocks
Clock output	50 Ω single ended, DC coupled. Can drive J-BERT or ParBERT 7G/13 G pattern generator modules
Clock multiplier factors	See table 2
Clock output range	6.240 GHz to 12.480 GHz
Clock output voltage	Typical 300 to 600 mVpp, not adjustable
Output jitter	Typical 1.9 ps rms RJ additional intrinsic jitter@ ref clock 2 ns (20 %/80 %) transition time, 100 mVpp Typical 2.1 ps rms RJ additional intrinsic jitter@ ref clock 7.7 ns (20 %/80 %) transition time, 100 mVpp.
Output transition time	Typical < 25 ps (20% /80%), not adjustable
Output duty cycle	Typical 50% \pm 5%, not adjustable
Connectors front panel	SMA 3.5 mm, female
Connectors rear panel	USB, IEC power connector

Agilent N4880A Specifications

Table 2: Multiplier factors for N4880A

Digital Bus Standard	Reference Clock Input	Target Bit Rate	N4880A Output Clock*	PLL Loop Bandwidth	N4880A Multiplier	Recommended CLK IN Divider in Pattern Generator to achieve Target Bit Rate ⁽¹⁾
PCI Express 3	100 MHz	8 GHz	8 GHz	5 MHz	80	1
PCI Express 2	100 MHz	5 GHz	10 GHz	5 MHz	100	2
PCI Express 1	100 MHz	2.5 GHz	10 GHz	5 MHz	100	4
MIPI M-PHY	19.2 MHz	1.248 GHz	9.984 GHz	2 MHz	520	8
MIPI M-PHY	19.2 MHz	1.4592 GHz	11.6736 GHz	2 MHz	608	8
MIPI M-PHY	19.2 MHz	2.496 GHz	9.984 GHz	2 MHz	520	4
MIPI M-PHY	19.2 MHz	2.9184 GHz	11.6736 GHz	2 MHz	608	4
MIPI M-PHY	19.2 MHz	4.992 GHz	9.984 GHz	2 MHz	520	2
MIPI M-PHY	19.2 MHz	5.8368 GHz	11.6736 GHz	2 MHz	608	2
MIPI M-PHY	26 MHz	1.248 GHz	9.984 GHz	2 MHz	384	8
MIPI M-PHY	26 MHz	1.456 GHz	11.648 GHz	2 MHz	448	8
MIPI M-PHY	26 MHz	2.496 GHz	9.984 GHz	2 MHz	384	4
MIPI M-PHY	26 MHz	2.912 GHz	11.648 GHz	2 MHz	448	4
MIPI M-PHY	26 MHz	4.992 GHz	9.984 GHz	2 MHz	384	2
MIPI M-PHY	26 MHz	5.824GHz	11.648 GHz	2 MHz	448	2
MIPI M-PHY	38.4 MHz	1.248 GHz	9.984 GHz	2 MHz	260	8
MIPI M-PHY	38.4 MHz	1.4592 GHz	11.6736 GHz	2 MHz	304	8
MIPI M-PHY	38.4 MHz	2.496 GHz	9.984 GHz	2 MHz	260	4
MIPI M-PHY	38.4 MHz	2.9184 GHz	11.6736 GHz	2 MHz	304	4
MIPI M-PHY	38.4 MHz	4.992 GHz	9.984 GHz	2 MHz	260	2
MIPI M-PHY	38.4 MHz	5.8368 GHz	11.6736 GHz	2 MHz	304	2

Agilent N4880A Specifications

Digital Bus Standard	Reference Clock Input	Target Bit Rate	N4880A Output Clock*	PLL Loop Bandwidth	N4880A Multiplier	Recommended CLK IN Divider in Pattern Generator to achieve Target Bit Rate ⁽¹⁾
MIPI M-PHY	52 MHz	1.248 GHz	9.984 GHz	2 MHz	192	8
MIPI M-PHY	52 MHz	1.456 GHz	11.648 GHz	2 MHz	24	8
MIPI M-PHY	52 MHz	2.496 GHz	9.984 GHz	2 MHz	192	4
MIPI M-PHY	52 MHz	2.912 GHz	11.648 GHz	2 MHz	192	4
MIPI M-PHY	52 MHz	5.824 GHz	11.648 GHz	2 MHz	224	2
MIPI M-PHY	52 MHz	5.824 GHz	11.648 GHz	2 MHz	224	2
SD UHS-II ⁽²⁾	26 MHz to 52 MHz	0.780 GHz to 1.560 GHz	6.24 GHz to 12.48 GHz	2 MHz	240	8
SD UHS-II ⁽²⁾	26 MHz to 52 MHz	0.390 GHz to 0.780 GHz	6.24 GHz to 12.48 GHz	2 MHz	240	16

⁽¹⁾ 7G versions of J-BERT N4903B and ParBERT 81250 can be used, even if N4880A output clock rate is higher than 7 GHz.

⁽²⁾ In case of a reference clock between 26 MHz and < 28.125 MHz and the need for sinusoidal jitter injection a N4916B-001 clock doubler has to be applied between the reference clock multiplier output and the J-BERT external clock input. In addition, the pattern generator bits need to be doubled (e.g. 01 -> 0011) to compensate for the clock doubling.

Table 3. General characteristics for N4880A

Power consumption	100 – 240 V ~50/60 Hz, 80 VA max.
Operating temperature	5 °C to 40 °C (–23 °F to 104 °F)
Storage temperature	–40 °C to 70 °C
Operating humidity	95% relative humidity non-condensing
Storage humidity	50% relative humidity
Physical dimensions (WxHxD)	Bench top with bumper and connectors: 228 x 59 x 240 mm (9.0 x 2.3 x 9.74 in)
Rackmount without bumper	1/2 x 19" width, 1U height
Weight net	1.9 kg (4.2 lb)
Weight shipping	~4.5 kg (10 lb)
Warranty period	1 year
Regulatory standards:	
Safety	IEC61010-1:2001, EN61010-1:2001, CAN/CSA-C22 No. 61010-04, UL 61010-1:2004
EMC	IEC61326-1:1997+A1:1998, EN61326-1:1997+A1:1998
Quality management	ISO 9004, ISO 14000
Remote control interface:	
Connectivity	USB 2.0, rear panel
Programming language	Command line programming interface, SCPI extension on J-BERT N4903B SW 7.2 or higher
Stand-alone user interface	Graphical, color user interface
System requirements	OS: Microsoft Windows® XP, SP3 (32 bit), or Vista SP2 (32 and 64 bit), or Windows 7 SP1 (32 and 64 bit); Microsoft .NET 2.0 SP2 For using the J-BERT SCPI remote extension N4903B SW 7.2 or higher is needed

Ordering Information

Table 4: Ordering Instructions

Reference clock multiplier	N4880A
Accessories included in N4880A	1 x 50 Ω termination 3.5 mm, USB cable, USB-stick with software and user documentation, functional test report, ROHS addendum
Recommended accessories:	
Four SMA-SMA cables, unmatched (for clock in and out)	15442A
SMP-to-SMA cable pair (for PCIe CEM test)	N4235-61602
Rack-mount kit	E5810A-100
Warranty and services:	
Warranty and calibration services	R1280
Productivity assistance	R1380-N49xx

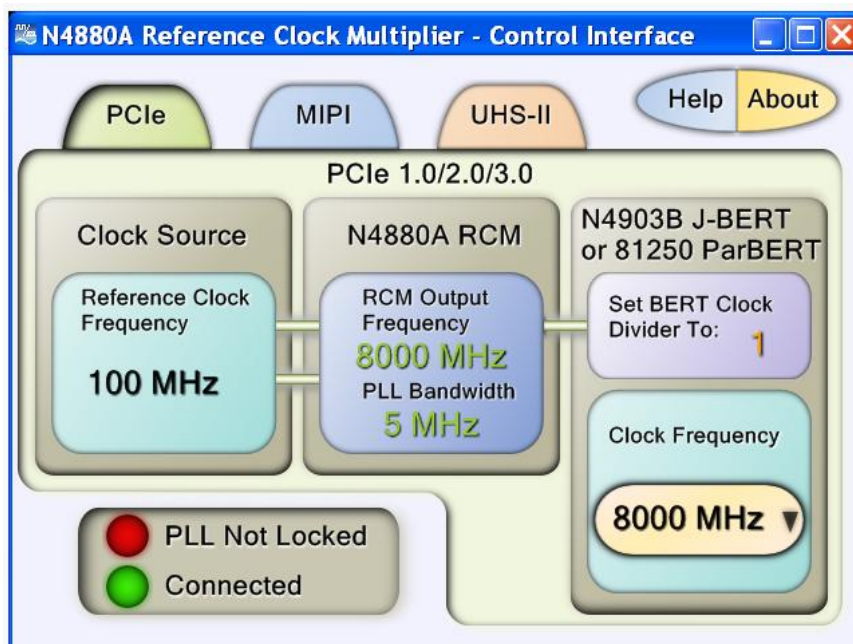


Figure 1: Choose settings for the N4880A with the stand-alone graphical user interface. The example shows a setting for a PCI Express 3.0 motherboard test at 8 Gb/s

Related Literature

Title	Publication Number
J-BERT N4903B high performance serial BERT Data Sheet	5990-3217EN
PCI Express 3.0 calibration channels Data Sheet	5990-7659EN
N4916B 4-tap de-emphasis signal converter Data Sheet	5990-4630EN
Infiniium 90000 X-series oscilloscopes 16-32 GHz true analogue bandwidth Data Sheet	5990-5271EN
Infiniium DSO90000 series high-performance oscilloscopes Data Sheet	5989-7819EN
N5990A Test automation software platform Data Sheet	5989-5483EN
How to pass receiver test according to PCI Express 3.0 CEM specification Application Note	5990-9208EN
Accurate calibration of PCIe 3.0 receiver stress signals (base spec) Application Note	5990-6599EN
PCIe 2.0 receiver testing with J-BERT N4903B Application Note	5990-3233EN


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