Detecting open signal pins becomes more challenging as packages get smaller and denser. There are access issues and time-to-market pressures in getting traditional libraries ready for production tests. As such, a growing number of manufacturers prefer vectorless test solutions to maintain maximum coverage in the most efficient way.

A recent breakthrough in vectorless test technology reduces test dependency on lead frames, enabling reliable measurements of ultra small geometry packages, flip chips, devices with minimal or no lead frames and devices under heat spreaders. This column provides background on the emergence of vectorless test and details on the benefits of this technique.

Powered, digital ICT in-circuit testing has long been used to verify a device is operating properly and free of defects like solder opens and shorts. This type of testing, however, requires an expensive digital ICT tester and time-consuming test development and debug. Because of these cost and time pressures, ICT engineers have turned to unpowered vectorless testing to find common manufacturing faults like opens.

During the past decade, vectorless test has become a popular method for detecting opens on ICs at ICT test. The device under test (DUT) is not powered up; thus, there is no need for expensive digital tester resources, and test development and debug is fast and automatic.

Vectorless test has two broad categories: parasitic diode and capacitively coupled lead-frame. The former measures current flow through the parasitic diode junctions in a device (clamping diodes, substrate junctions). If a solder is open, current will not flow. While simple in principle, there are practical concerns. The parasitic junction characteristics can vary from device to device. Parallel diode junctions may be present when multiple devices are connected to the tested node. Setting the thresholds to catch real defects while minimizing false calls can be challenging in a production environment. Therefore, parasitic diode testing for IC opens is a limited vectorless solution.

The second technique relies on a fixture-mounted plate that forms a capacitor with the IC’s lead-frame metal during the test (Figure 1). The target pin is stimulated with an AC voltage source, while the device’s remaining pins are connected to ground. The signal capacitively couples to the sensor plate mounted in the fixture. To minimize measurement noise and increase the signal amplitude, an amplifier is mounted directly on the plate. The tester’s detector then measures this amplified signal.

The value of the capacitance can be approximated by a parallel plate model, where:

\[ C = \varepsilon \frac{A}{d} \]

\[ A = \text{area of the lead-frame metal.} \]

\[ d = \text{distance between lead frame and fixture-mounted sensor plate.} \]

\[ \varepsilon = \text{combined } Dk \text{ of the package material and protective insulator on the sensor plate.} \]

These parameters are highly controlled and result in a stable capacitance value for a given device across multiple boards and fixtures. Typically, this value is around 100 fF for correctly soldered joints. It is near zero for opens. This wide difference between good and bad measurements ensures a stable production test. And, because a sensor plate is over each IC tested, multiple devices connected to the same node present no problem.

As IC packaging technologies have advanced, however, lead-frame geometries have shrunk. This has reduced the amount of metal forming the capacitor’s bottom half (Figure 1). This reduces the measured value of a good solder joint. Furthermore, increasing power requirements of modern ICs have led to the widespread use of heatsinks and heat spreaders. These act as an additional series-coupled capacitance in the measurement path. This also reduces the measured value of a good solder joint. For many modern BGAs, good solder joints can measure less than 20 fF, and in some cases, less than 5 fF!

Most ICT vendors have thus introduced advanced vectorless test techniques. These rely on the capacitive coupling technique, but use advanced measurement hardware and noise reduction software to improve the signal-to-noise ratio (SNR) for low-valued measurements. Many ICT platforms have high SNR vectorless test.

Ever-smaller BGAs and emerging packaging such as flip chips and µBGAs, which have almost no available metal for capacitive coupling, challenge even these techniques. Test OEMs continue to innovate in ICT and vectorless test techniques to meet requirements of next-generation devices.