Practical Digital Pre-Distortion Techniques for PA Linearization in 3GPP LTE

Jinbiao Xu
Agilent Technologies
Master System Engineer
Agenda

• Digital PreDistortion—Principle
• Crest Factor Reduction
• Digital PreDistortion Simulation
• Digital PreDistortion Hardware Verification
Digital Pre-Distortion----- Principle

Output Power

- $P_{sat}$
- $P_{\text{out-pd}}$
- $P_{\text{out}}$

Linear Response

Saturation

Operating region with predistortion

Operating region without predistortion

Input Power

Output Phase

- $\theta_{o-pd} = k \theta_{out}$
- Desired Output

Linear Output

Input Power

$P_i$, $P_{i-pd}$
Digital Pre-Distortion----- Principle

The DPD-PA cascade attempts to combine two nonlinear systems into one linear result which allows the PA to operate closer to saturation.

The objective of digital predistorter is to have $y(t) \approx Cx(t)$, where $C$ is a constant.

The most important step is to extract PA nonlinear behavior accurately and efficiently.
Memory Polynomial Algorithm

- As the signal (such as 3GPP LTE) bandwidth gets wider, power amplifiers begin to exhibit memory effects. Memoryless (LUT) pre-distortion can achieve only very limited linearization performance.
- Volterra series is a general nonlinear model with memory. It is unattractive for practical applications because of its large number of coefficients.
- Memory polynomial reduces Volterra’s model complexity. It is interpreted as a special case of a generalized Hammerstein model. Its equation is as follows:

\[
z(n) = \sum_{k=1}^{K} \sum_{q=0}^{Q} a_{kq} y(n-q) |y(n-q)|^{k-1}
\]

\(K\) is Nonlinearity order and \(Q\) is Memory order.
Signal Training to derive the Memory Polynomial

1. Pre-distorter training:
   Nonlinear coefficients are extracted from the PA input and PA output waveforms (i.e., on real physical behavior)

2. Copy of PA: The DPD model accurately captures the nonlinearity with memory effects

Memory Polynomial Coefficients

\[ \hat{a} = (U^H U)^{-1} U^H z \]

\[ \hat{a} = [\hat{a}_{10}, \ldots, \hat{a}_{K0}, \ldots, \hat{a}_{1Q}, \ldots, \hat{a}_{KQ}]^T \]

\[ z = [z(0), z(1), \ldots, z(N-1)]^T \]
Crest Factor Reduction (CFR) Concepts

- Spectrally efficient wideband RF signals may have PAPR >13dB.
- CFR preconditions the signal to reduce signal peaks without significant signal distortion
- CFR allows the PA to operate more efficiently – it is not a linearization technique
- CFR supplements DPD and improves DPD effectiveness
- Without CFR and DPD, a basestation PA must operate at significant back-off from saturated power to maintain linearity. The back-off reduces efficiency

Benefits of CFR
1. PAs can operate closer to saturation, for improved efficiency (PAE).
2. Output signal still complies with spectral mask and EVM specifications
Crest Factor Reduction (CFR) Concepts

If you can reduce the Peak-to-Average Ratio of the signal, then for a given amplitude Peak, you can raise the Average power (up & to the right, above) with no loss in signal quality.

Thus, CFR enables higher PA efficiency by reducing the back-off, often by 6dB.
Crest Factor Reduction for Multiple-Carrier Signals

- Multiple-Carrier Signals (such as GSM, WCDMA, WiMAX) already have high PAPR.
- In the future, they will also include multiple waveforms (ie - LTE with 3G WCDMA).
- Therefore CFR will increase in importance for Multi-Carrier PA (MCPA) linearization.

CFR algorithm for multiple carrier signals
- PW (Peak Windowing)-CFR
- NS (Noise-Shaping) -CFR
- PI (Pulse Injection)-CFR
- PC (Peak Cancellation)-CFR
CFR for 3GPP LTE DL OFDM Signal

- Controls EVM and band limits in the frequency domain.
  - Constrains constellation errors, to avoid bit errors.
  - Constrains the degradation on individual sub-carriers.
- Allows QPSK sub-carriers to be degraded more than 64 QAM sub-carriers.
- Does not degrade reference signals, P-SS and S-SS.
- All control channels (PDCCH, PBCH, PCFICH and PHICH) adopts QPSK threshold.
LTE CFR (Crest Factor Reduction)

Simulation Results

LTE Downlink 10MHz, Sampling Rate 61.44MHz, QPSK, EVM threshold 10%

<table>
<thead>
<tr>
<th>Origin_PAPR</th>
<th>CFR_PAPR</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.05</td>
<td>6.685</td>
</tr>
</tbody>
</table>

Copyright Agilent Technologies 2010

SystemVue DPD
Jinbiao Xu
May 26, 2010
DPD Simulation Workspace

- **Step 1**: Create DPD Stimulus
  - CCDF Measurement
  - CreateDPDStimulus (Schematic)
  - CreateDPDStimulus Analysis (CreateDPDStimulus)
  - CreateDPDStimulus Analysis_Data (CreateDPDStimulus Analysis)
  - PAPR

- **Step 3**: DUT Model Extraction
  - DPD_NMSE
  - DPD_PowerAlignment
  - DUTModelExtraction_AM_AM
  - DUTModelExtraction_Spectrum
  - DUTModelExtraction (Schematic)
  - DUTModelExtraction Analysis (DUTModelExtraction)
  - DUTModelExtraction Analysis_Data (DUTModelExtraction Analysis)
  - PA_AM_AM

- **Step 4**: DPD Response
  - DPD_AM_AM
  - DPD_Spectrum
  - DPDResponse (Schematic)
  - DPDResponse Analysis (DPDResponse)
  - DPDResponse Analysis_Data (DPDResponse Analysis)
  - PA_DPD_Spectrum
  - EVM
  - EVMMeasurements (Schematic)
  - EVMMeasurements Analysis (EVMMeasurements)
  - EVMMeasurements Analysis_Data (EVMMeasurements Analysis)

- **Step 5**: ACLR Measurements
  - ACLRMeasurements (Schematic)
  - ACLRMeasurements Analysis (ACLRMeasurements)
  - ACLRMeasurements Analysis_Data (ACLRMeasurements Analysis)
  - After_PA_ACLR
  - AfterDPD_PA_ACLR
  - Original_ACLR

**Step 1 is to Generate Waveform for DPD**

**Step 3 is for DUT Model Extraction**

**Step 4 is for DPD Response**

Compared with hardware verification tool, simulation tool does not include Step 2 and Step 5.

**Hardware verification tool will be introduced later.**
LTE DPD simulation for a memoryless nonlinear PA

**EVM (dB)**

<table>
<thead>
<tr>
<th>Index</th>
<th>AfterDPD_PA</th>
<th>Original</th>
<th>After_PA</th>
</tr>
</thead>
</table>

**ACLR (dB)**

<table>
<thead>
<tr>
<th></th>
<th>Original_ACLR_L_2BW</th>
<th>Original_ACLR_L_BW</th>
<th>Original_ACLR_U_BW</th>
<th>Original_ACLR_U_2BW</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA_ACLR_L_2BW</td>
<td>72.036</td>
<td>64.23</td>
<td>63.542</td>
<td>71.869</td>
</tr>
<tr>
<td>PA_ACLR_L_BW</td>
<td>51.075</td>
<td>36.899</td>
<td>38.963</td>
<td>51.151</td>
</tr>
<tr>
<td>DPD_PA_ACLR_L_2BW</td>
<td>71.651</td>
<td>64.067</td>
<td>63.404</td>
<td>71.497</td>
</tr>
</tbody>
</table>
LTE DPD simulation for a nonlinear PA with memory
DPD Hardware Verification Flowchart consists of 5 steps:

- **Step 1 (Create DPD Stimulus)** is to download waveform (LTE or User defined) into ESG/MXG.
- **Step 2 (Capture DUT Response)** is to capture both waveforms before power amplifier and after power amplifier from PSA/MXA/PXA by using VSA89600 software.
- **Step 3 (DUT Model Extraction)** is to extract PA nonlinear coefficients based on both captured PA input and PA output waveforms and then to verify DPD by using PA nonlinear coefficients.
- **Step 4 (DPD Response)** is to show the performance improvement after DPD.
DPD Hardware Verification Platform

1. PA input signal capture

Signal source: LTE 10MHz

Agilent MXG/ESG

10MHz Reference

External Trigger

PSA/MXA/PXA

2. PA output signal capture

MXG/ESG

10MHz Reference

External Trigger

PSA/MXA/PXA

Attenuator
DPD Hardware Verification – LTE (Step 1)

The CFR must be enabled in LTE source. LTE parameters (such as bandwidth, Resource Block allocation and etc) can be set.

The download waveform transmit power, length also can be set.
DPD Hardware Verification – LTE (Step 2)

Firstly, connect the ESG directly with the PSA/PXA and click the “Capture Waveform” button in the “Capture PA Input” panel in the GUI. The captured signal is the input of the PA DUT.

Then, connect the ESG with the DUT, and then connect the DUT with the PSA/PXA and click the “Capture Waveform” button in the “Capture PA Output” panel in the GUI. The captured signal is the output of the PA DUT.

These I/Q files are stored for further usage.
This step is to extract PA nonlinear coefficient from the PA input and PA output waveform and get the coefficients of the DPD model.
This step is to apply the DPD model extracted in Step 3. The generated LTE downlink signal is firstly pre-distorted by the extracted model, and then downloaded into the ESG.
DPD Hardware Verification – LTE (Step 5)

Step 5: Verify DUT Response

Spectrum
EVM
ACLR

This step is to verify the performances of the DPD (including spectrums of the DUT output signal w/ and w/o DPD, EVM and ACLR).

![Spectrum Diagram]

**EVM (dB)**

<table>
<thead>
<tr>
<th>Index</th>
<th>AfterDPD_PA</th>
<th>Original</th>
<th>After_PA</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-19.443</td>
<td>-19.382</td>
<td>-18.577</td>
</tr>
<tr>
<td>2</td>
<td>-18.84</td>
<td>-18.844</td>
<td>-18.071</td>
</tr>
</tbody>
</table>

**ACLR (dB)**

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Original_ACLR_L_2BW</td>
<td>53.179</td>
</tr>
<tr>
<td>PA_ACLR_L_2BW</td>
<td>50.653</td>
</tr>
<tr>
<td>PA_ACLR_U_2BW</td>
<td>51.252</td>
</tr>
<tr>
<td>Original_ACLR_U_2BW</td>
<td>53.363</td>
</tr>
<tr>
<td>DPD_PA_ACLR_L_2BW</td>
<td>51.307</td>
</tr>
<tr>
<td>DPD_PA_ACLR_U_2BW</td>
<td>51.23</td>
</tr>
<tr>
<td>DPD_PA_ACLR_L_2BW</td>
<td>52.437</td>
</tr>
<tr>
<td>DPD_PA_ACLR_U_2BW</td>
<td>52.825</td>
</tr>
</tbody>
</table>
Hardware Verification Results of Doherty PA

EVM (dB)

<table>
<thead>
<tr>
<th>Index</th>
<th>AfterDPD_PA</th>
<th>Original</th>
<th>After_PA</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-19.531</td>
<td>-19.384</td>
<td>-18.625</td>
</tr>
<tr>
<td>2</td>
<td>-18.438</td>
<td>-18.392</td>
<td>-18.616</td>
</tr>
</tbody>
</table>

ACLR (dB)

<table>
<thead>
<tr>
<th>ACPAPower</th>
<th>AfterDPD_PA</th>
<th>Original</th>
<th>After_PA</th>
</tr>
</thead>
<tbody>
<tr>
<td>51.614</td>
<td>43.585</td>
<td>50.147</td>
<td>50.005</td>
</tr>
<tr>
<td>50.992</td>
<td>27.643</td>
<td>42.426</td>
<td>42.082</td>
</tr>
<tr>
<td>50.005</td>
<td>27.422</td>
<td>42.426</td>
<td>47.779</td>
</tr>
</tbody>
</table>

Copyright Agilent Technologies 2010

Jinbiao XU
May 26, 2010
References

10. Amplifier Pre-Distortion Linearization and Modeling Using X-Parameters, Agilent EEsof EDA