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Channel Design, Simulation and Measurement

SandForce TRUSTED

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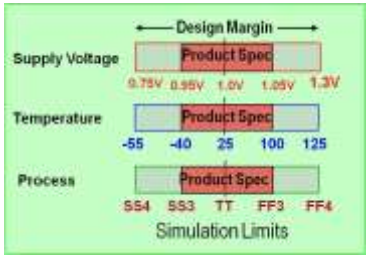
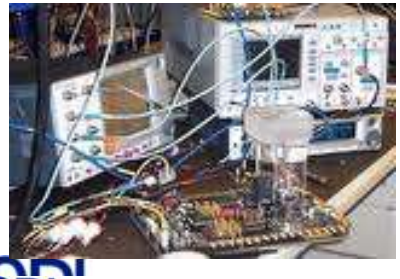
GRL's multi-disciplinary capabilities help customers adopt high speed interfaces



THUNDERBOLT™

DisplayPort



Characterization & Stress Testing

SI Modeling & Simulation

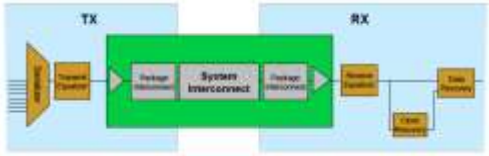
Model Validation Testing & Refinement

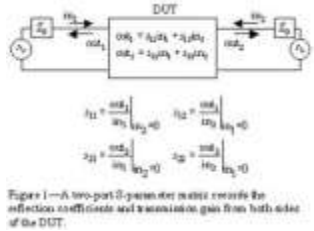
Board Characterization & Probing

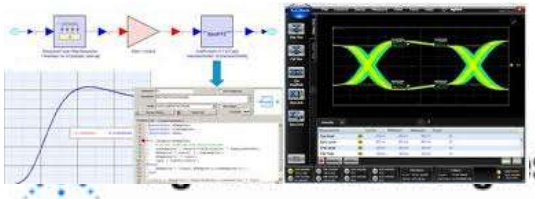
IC Bring-Up, Debug Testing, & SERDES tuning

Test Equipment Methodology development

Standards Compliance Testing







GRL Company Confidential

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Connectivity Standards Covered

Authorized Test Lab (ATC)

- First ATC selected by Intel/Apple
- Now Testing DP 1.2
- SandForce Preferred ATC

ATC Expected in Early 2012

- USB 2.0/3.0
- Now Testing MHL
- HDMI 1.3/1.4

Independent Lab Validation

- Now Testing PCIe Gen3
- Turnkey DDR2/DDR3 Testing
- SandForce Preferred ATC
- 10G Ethernet XAUI, SGMII, XFI,
- SDI, 3G-SDI, HD-SDI, 6G SDI
- D-PHY M-PHY
- SRIO T1/T2/T3 2.1
- CPRI-1/2/3/4
- OBSAI-1/2/3
- 3.75 Gbs
- CEI 6G LR/SR
- OC 12/48 OTU-1

Agenda

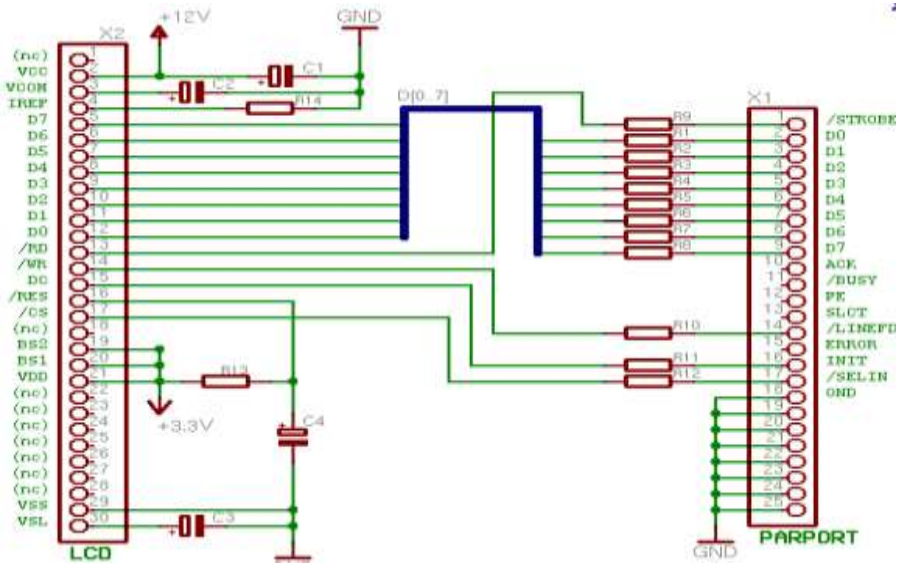
- Introduction
- Challenges at High Speed
- Addressing SI in Early Design
- S-parameters Basics
- Simulations and Measurements
- Conclusions

Introduction

- With the shift from parallel bus interfaces to serial links, high data rate signals have not only changed chip designs but also board designs. The impact of the physical channel on Signal Integrity has to be taken into consideration at a very early stage of design.
- Simulation accuracy heavily depends on model accuracy. The correlation between simulation and measurement is a key to a successful design.
- This presentation will address the entire simulation flow including extraction of channel S-parameters, simulation with the extracted S-parameter model using Agilent's ADS transient simulator, and validation of the simulation through measurement.

Problem: The High Speed Challenge

- Traditional wide parallel buses are no longer suitable for high speed designs. Why?
  - Difficult to maintain comparable skew between the individual parallel-signal lines
  - More power consumed by a faster-switching parallel bus
  - Difficult to route the individual parallel-signal lines



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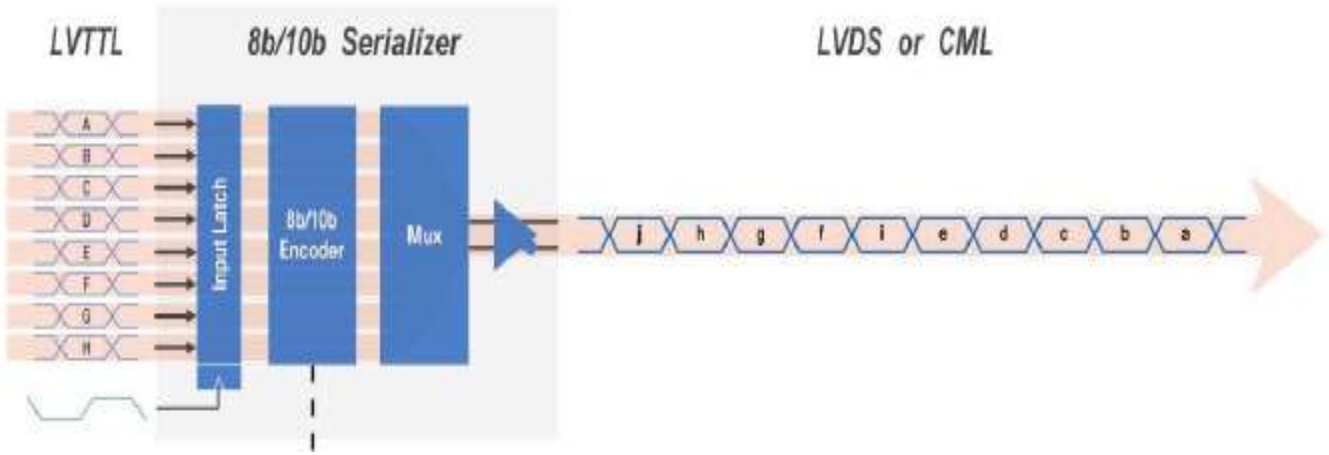
The High Speed Challenge

- Serial Links are better for high speed designs. Why?
  - Ability to move a large amount of data over a differential pair
  - Reduces the complexity, cost, power and board space
  - Enables data rates higher than 10Gbps not feasible with parallel links



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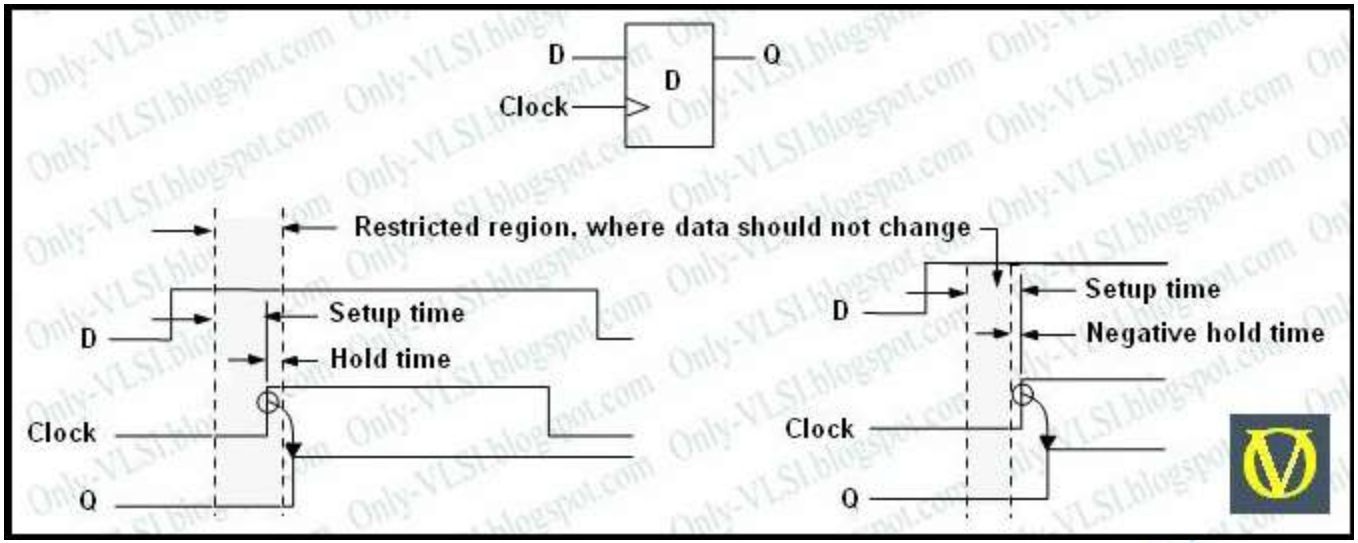
The High Speed Challenge

- At High Speed, things get tricky…
  - Digital signals must be handled like microwave signals (rise/fall edge in 50ps range)
  - Less margin for timing errors
  - Timing errors can violate the digital circuit setup and hold time, as well as propagation delay time, leading to logic function failures



The High Speed Challenge

- At higher speed, Signal Integrity issues become more problematic:
  - **Transmission Line Effects** – Losses and reflections in interconnecting traces including package leads, vias, connectors and impedance mismatch
  - **Coupling Effects** – Cross talk between signal lines or between signal and clock lines
  - **Ground Bounce Noise** – Faster switching times cause higher transient current in outputs as they discharge load capacitance. As the current flows through package inductance, it causes ground bounce noise
  - **Power Integrity** – DC supply distribution and decoupling, unwanted signal and clock propagation through power distribution circuit
  - **Electromagnetic Interference (EMI)** – External noise ingress, self-interference and control of radiated emissions

Solution: Address SI at an Early Stage of Design

The key to accurate simulation early in the design is to properly understand and model the impact of the physical channel on the signal as it travels from the transmitter to the receiver.

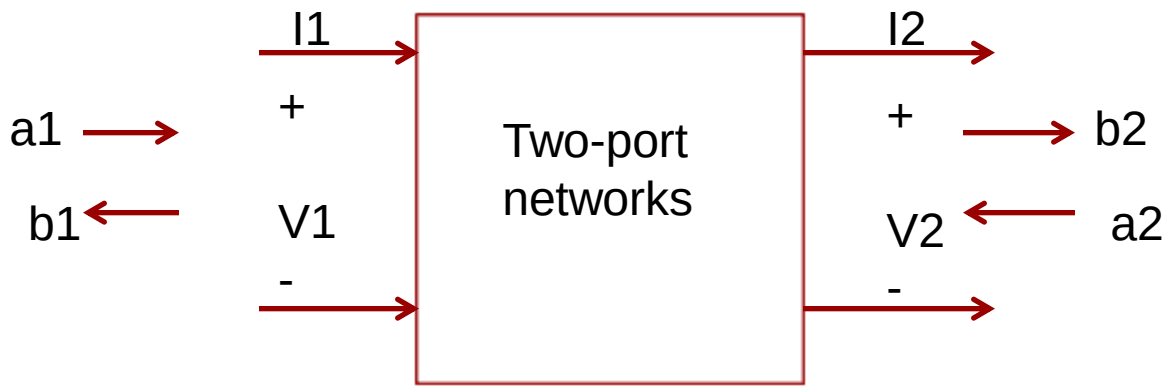
Effective design simulation follows these basic steps:

1. Model the Physical Channel using S-parameters
2. Simulate the Model (using Agilent's ADS suite)
3. Validate the Model through Measurements

1. Model the Physical Channel Using S-parameters

What are S-parameters, anyway?

- How can we describe linear two-port (and multi-port) networks?
  - I1 and I2 are current flow in and out of the net work



  - V1 and V2 are voltages on the input port and output port
  - a1, b1 and a2, b2 are normalized forward and backward traveling waves

S-parameter Basics

- The network can be described as T-parameters and Z-parameters

$$\begin{bmatrix} V1 \\ I1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V2 \\ I2 \end{bmatrix}$$

Transfer matrix (T-parameter)

$$\begin{bmatrix} V1 \\ V2 \end{bmatrix} = \begin{bmatrix} Z11 & Z12 \\ Z21 & Z22 \end{bmatrix} \begin{bmatrix} I1 \\ -I2 \end{bmatrix}$$

Impedance matrix (Z-parameter)

S-parameter Basics

- It can be described as Y-parameters and…

$$\begin{bmatrix} I1 \\ -I2 \end{bmatrix} = \begin{bmatrix} Y11 & Y12 \\ Y21 & Y22 \end{bmatrix} \begin{bmatrix} V1 \\ V2 \end{bmatrix}$$

Admittance matrix (Y-parameter)

S-parameter Basics

$$\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} S11 & S12 \\ S21 & S22 \end{bmatrix} \begin{bmatrix} a1 \\ a2 \end{bmatrix}$$

Scattering matrix (S-parameter)

- S-parameter meanings
  - S11 and S22 are reflection coefficients
  - S21 and S12 are transmission coefficients
- Travelling wave variables a1, b1, a2 and b2 defined in terms of V1, I1, V2 and I2 and a characteristics Z0 (=50Ω)

$$a1 = \frac{V1 + Z0I1}{2\sqrt{Z0}} \quad b1 = \frac{V1 - Z0I1}{2\sqrt{Z0}}$$
$$a2 = \frac{V2 - Z0I2}{2\sqrt{Z0}} \quad b2 = \frac{V2 + Z0I2}{2\sqrt{Z0}}$$

- At low frequency transfer and impedance matrices are commonly used, at microwave frequency scattering matrix is used

4-port Single-ended S-parameter Matrix

Stimulus

Response				
	S_{11}	S_{12}	S_{13}	S_{14}
	S_{21}	S_{22}	S_{23}	S_{24}
	S_{31}	S_{32}	S_{33}	S_{34}
	S_{41}	S_{42}	S_{43}	S_{44}

Interpreting single ended measurements:

S_{11} : return loss, single ended

$S_{21} = S_{12}$: insertion loss, single ended

$S_{31} = S_{13}$: near end cross talk

$S_{41} = S_{14}$: far end cross talk

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4-port Differential S-parameter Matrix

			Stimulus			
			Differential signal		Common signal	
			port 1	port 2	port 1	port 2
Response	Differential signal	port 1	SDD11	SDD12	SDC11	SDC12
		port 2	SDD21	SDD22	SDC21	SDC22
	Common signal	port 1	SCD11	SCD12	SCC11	SCC12
		port 2	SCD21	SCD22	SCC21	SCC22

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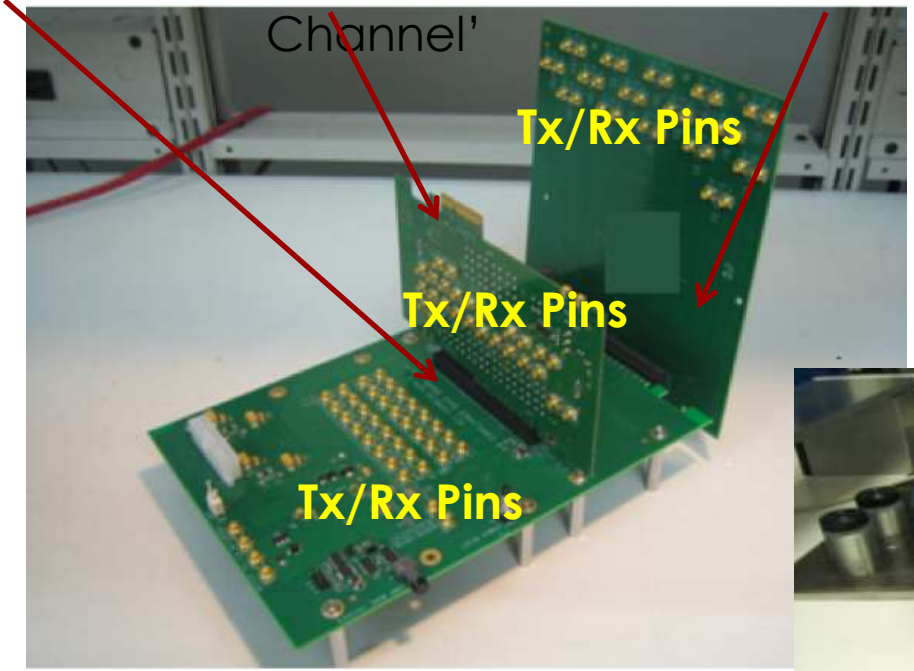
Example: PCIe3 & PCIe2 Compliance Boards

Gen3 System 'Short Channel'

Gen3 Add-In Card 'Short Channel'

Gen3 System 'Long Channel'



Gen2 System

What do the S-parameters look like?

What S-parameters look like…
on a ENA/PNA

What S-parameters look like…
in Touchstone format

```
!Agilent Technologies,E5071C,MY46110800,A.10.05
!Date: Mon Oct 31 17:32:18 2011
!Data & Calibration Information:
!Freq S11:SOLT4(ON)    S12:SOLT4(ON)    S13:SOLT4(ON)    S14:SOLT4
(ON)
!     S21:SOLT4(ON)    S22:SOLT4(ON)    S23:SOLT4(ON)    S24:SOLT4
(ON)
!     S31:SOLT4(ON)    S32:SOLT4(ON)    S33:SOLT4(ON)    S34:SOLT4
(ON)
!     S41:SOLT4(ON)    S42:SOLT4(ON)    S43:SOLT4(ON)    S44:SOLT4
(ON)
!PortZ  Port1:50+j0     Port2:50+j0     Port3:50+j0     Port4:50+j0
!Above PortZ is port z conversion or system Z0 setting when
saving the data.
!When reading, reference impedance value at option line is always
used.
# Hz S dB R 50
300000     -3.710275e+001  5.016047e+001    -6.321117e+001
      8.894588e+001    -7.374141e-002  -4.920827e-001   -
5.448646e+001    1.750432e+002
      -6.156123e+001  -1.455568e+002  -3.909540e+001  3.194251e+
001   -5.830857e+001  -7.659711e+001  -6.399278e-002   -
9.781381e-002
      -1.109173e-001  -4.248510e-001  -6.087116e+001  2.287436e+
001   -3.656398e+001  3.362571e+001    -5.763790e+001   -
1.143456e+002
      -5.867332e+001  -1.042585e+002  -8.806616e-002   -
2.812778e-001    -7.118126e+001  1.067795e+002    -4.241316e+001
```

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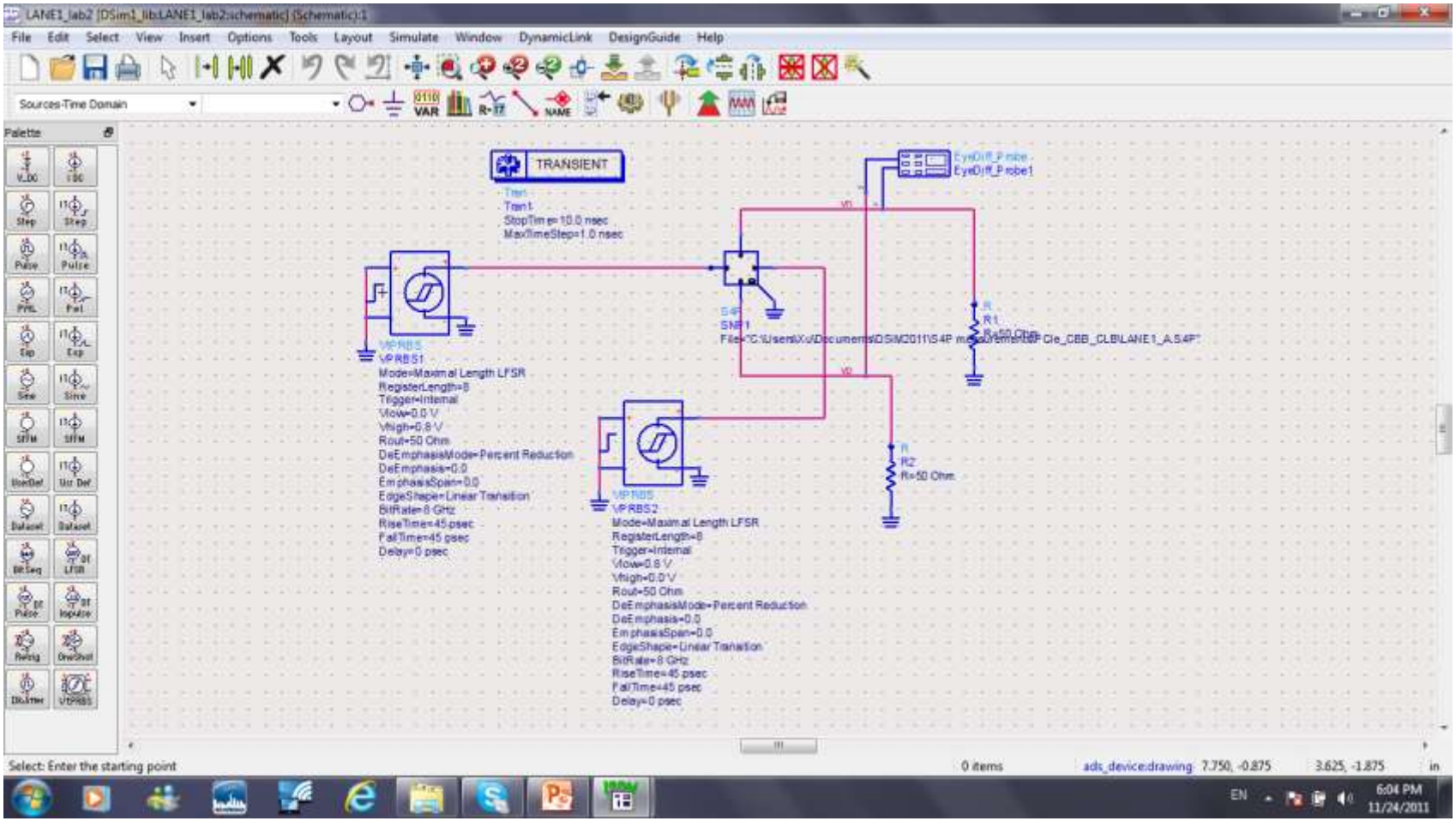
2. Simulate with the Channel S-parameters in ADS

- Create schematics in ADS
- Run ADS transient simulation with the measured channel S-parameters
- Simulate eye diagram of the channel

Schematics of the measured channel s4p file and the transient simulation controller



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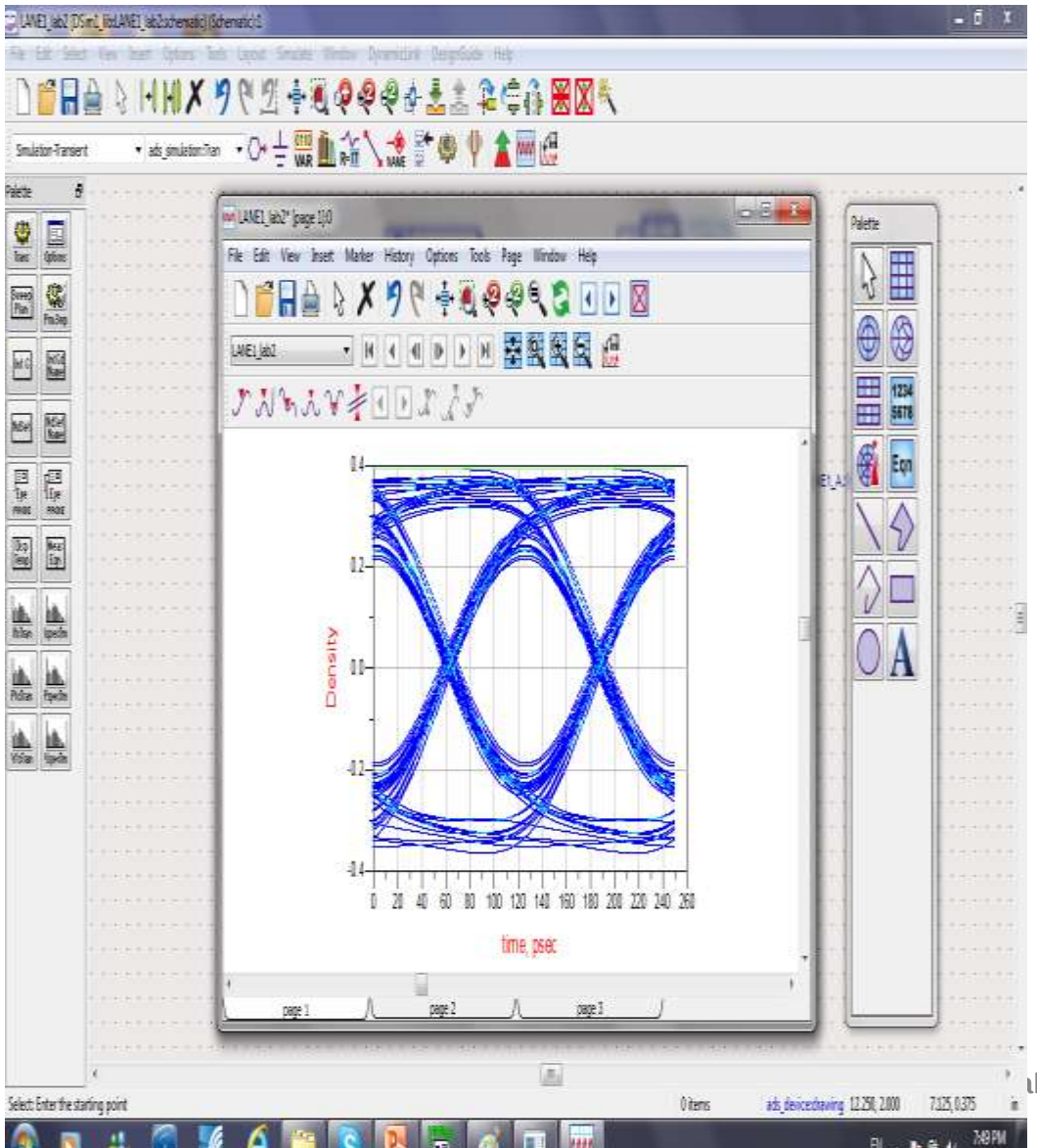
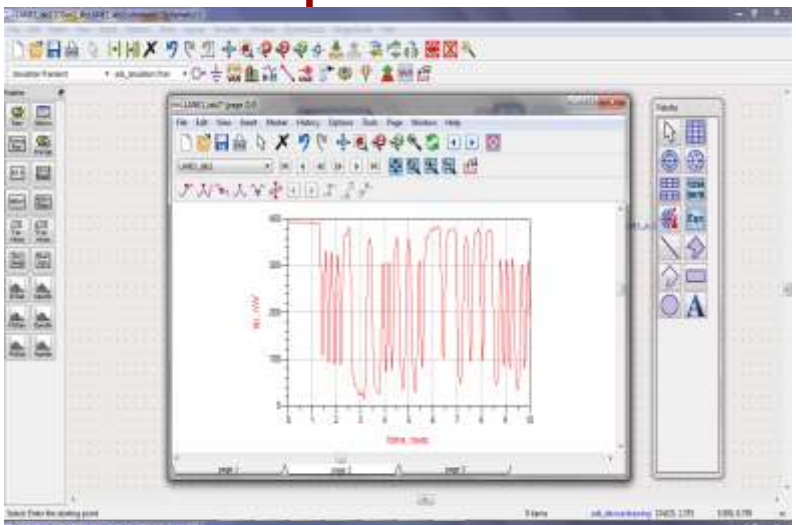
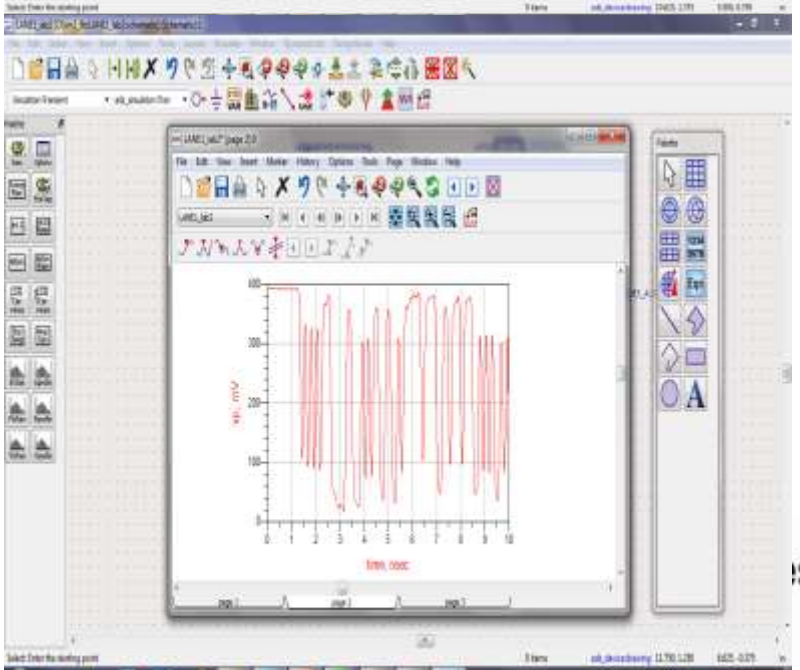
Simulated eye diagram and waveforms of a differential pair

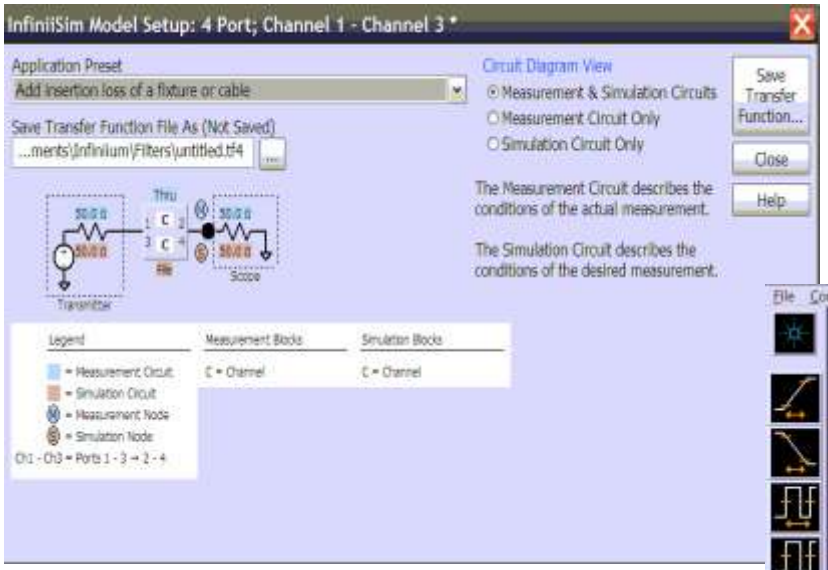


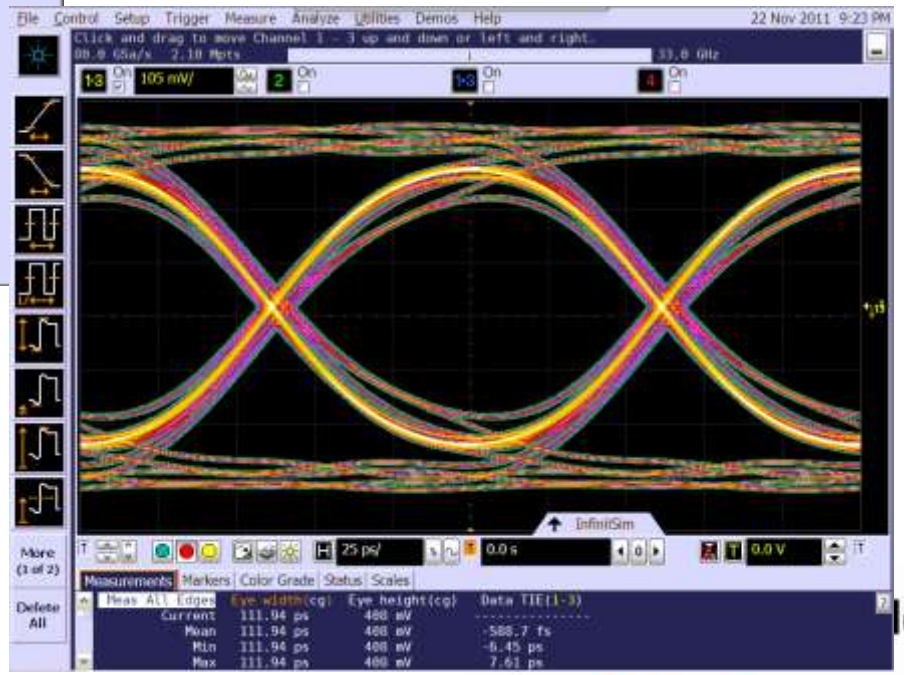




3. Verify the Model Through Measurement

- Make ‘Embedded Channel’ Measurements using S-parameters





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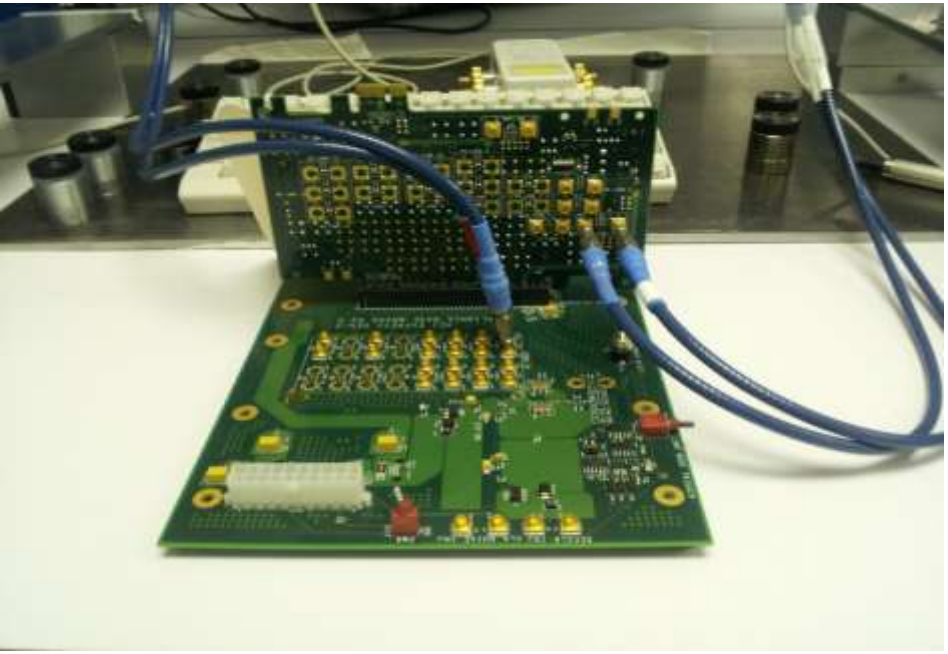
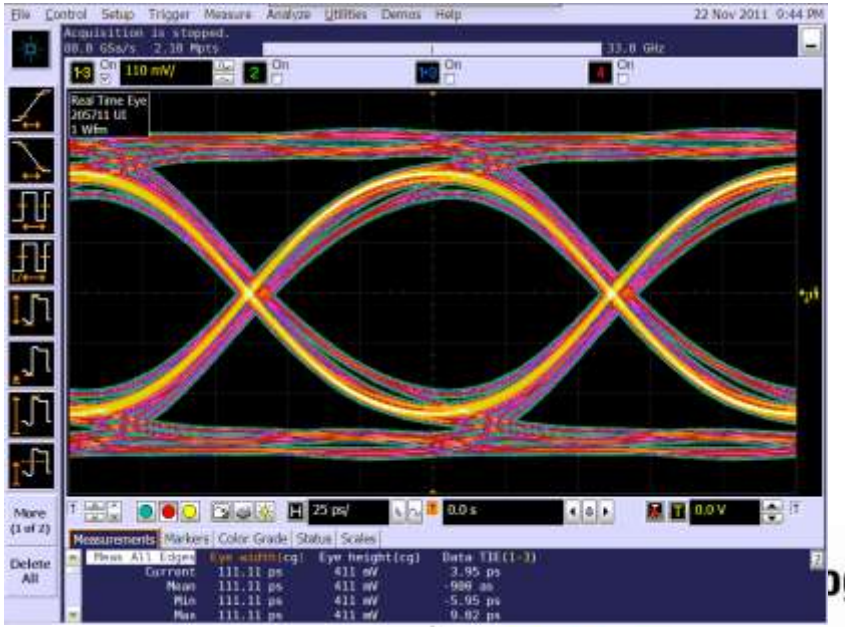
Model Verification Through Measurement

- Make ‘Physical Channel’ Measurements using PCIe Compliance Load Board/Compliance Base Board (CLB/CBB)





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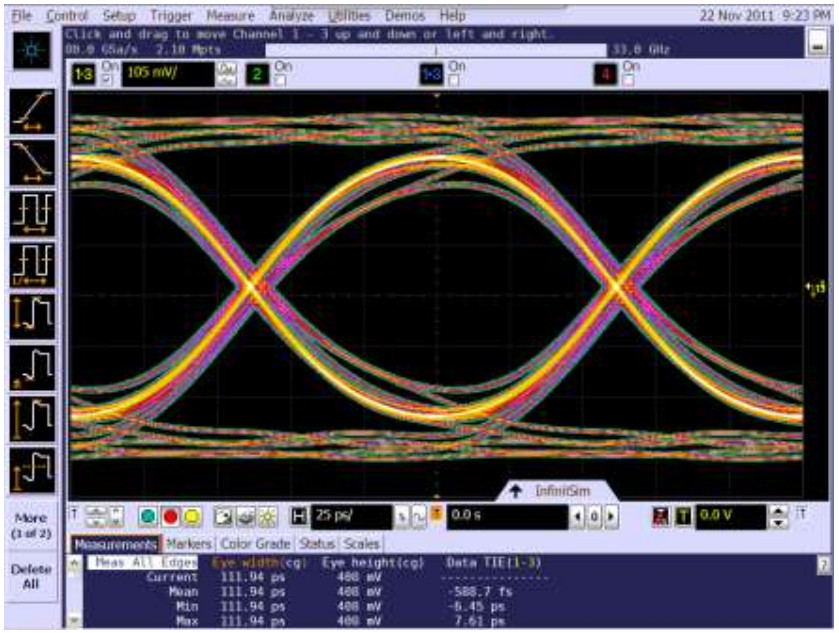
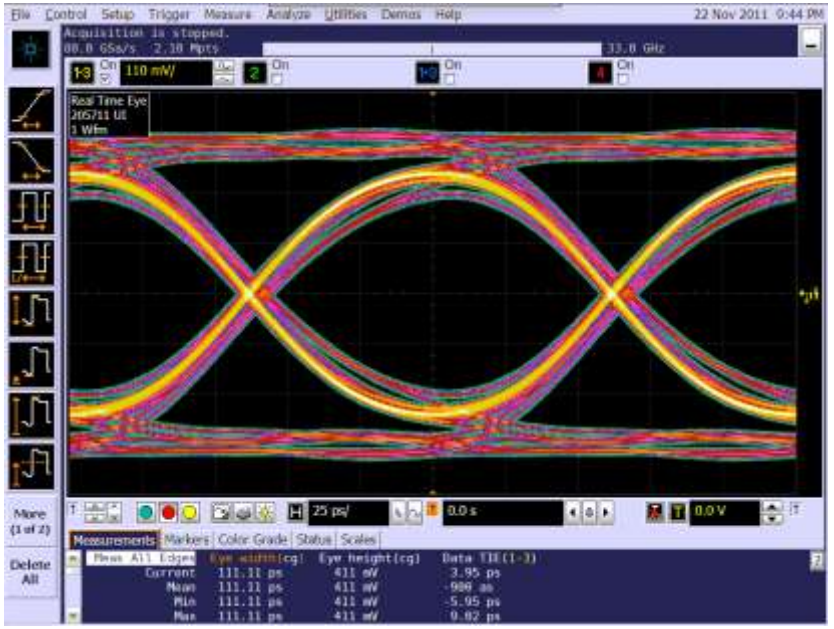
Instrument SW and HW eyes

- Compare Embedded and Physical Measurements for Correlation.





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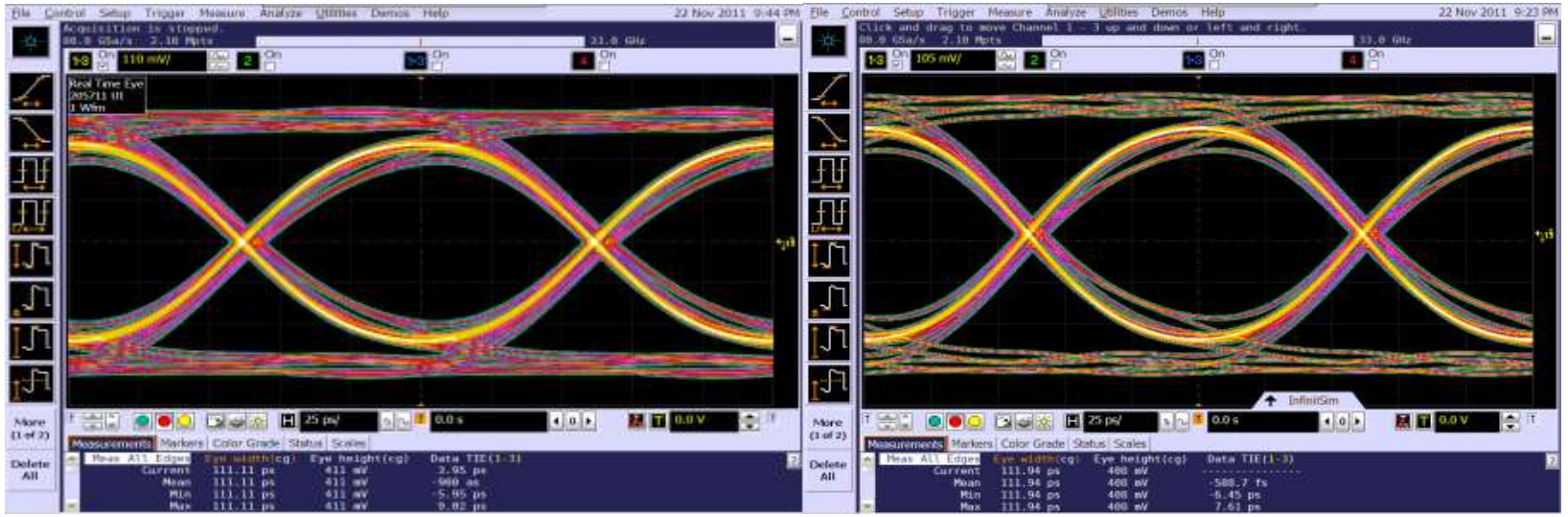
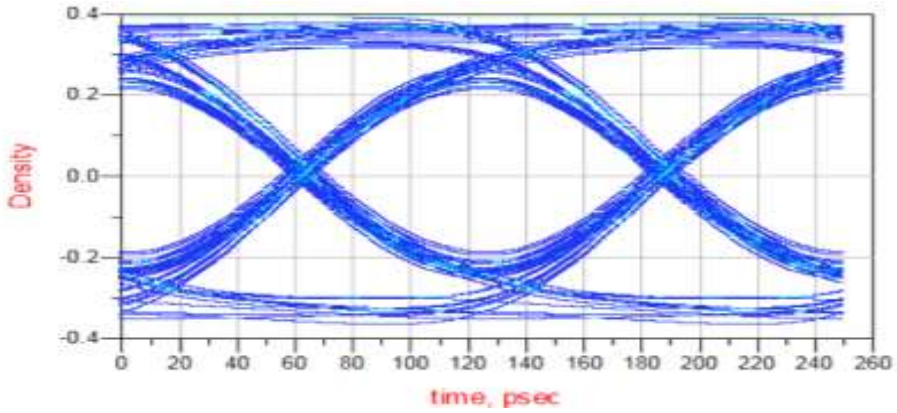
PCIe Compliance boards S-parameters validated by Instrument SW/HW eyes and ADS simulated eye





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Conclusion

1. Approach Board Design and IC Design together
2. Take Signal Integrity issues into consideration early using S-parameters of the physical channel and media in simulations
3. A basic understanding of S-parameters is key to properly integrate your Channel Model into your Design
4. Channel Model validation is critical for simulation accuracy

This approach can help you in several ways…

- Better timing margin
- Avoid re-spin of the design
- Get product to market faster and more cost-effectively.

Q&A

THANK YOU!

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