Design for Testability – Test for Designability

Bob Neal
Manufacturing Test Division
Agilent Technologies
Loveland, Colorado

Abstract:

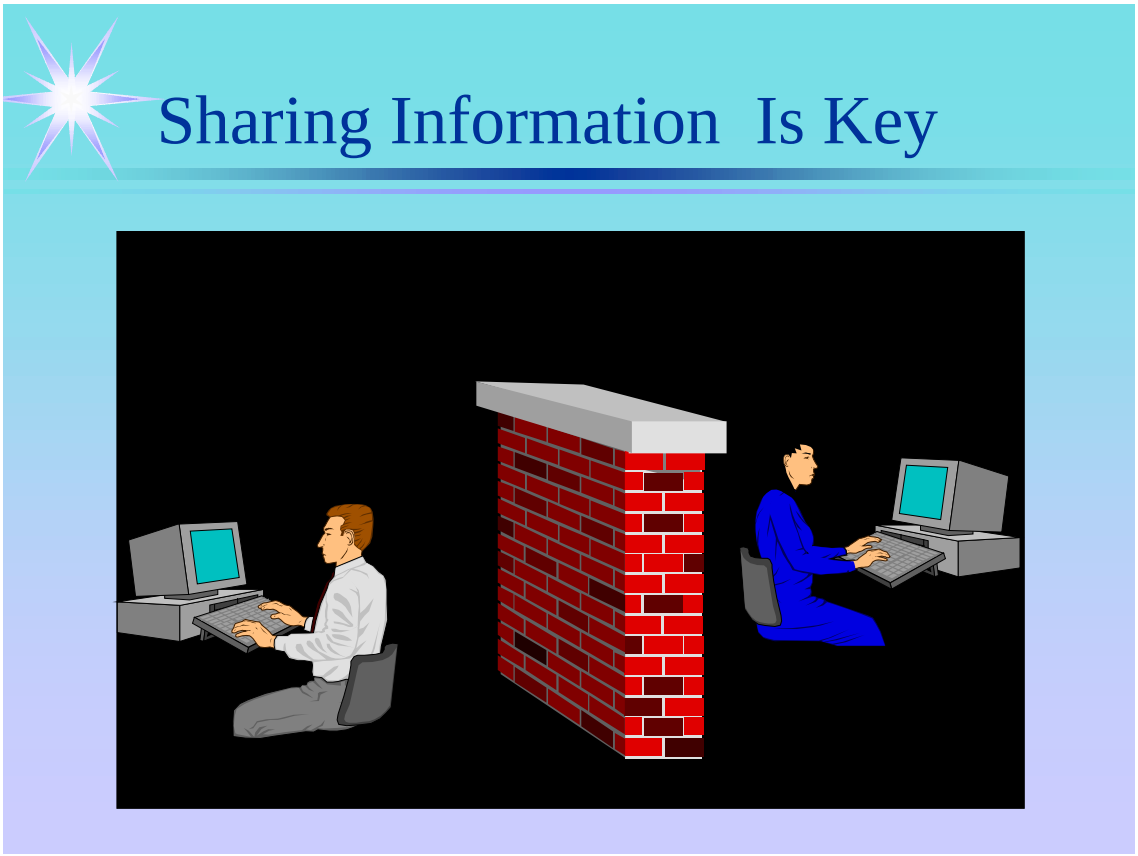
Designing for manufacturability and testability has been addressed by numerous publications and papers in the past. Some of the proposed guidelines have become obsolete because of technology and test system advances. Others have been difficult to justify and enforce by the manufacturing/test organizations of the enterprise. This paper addresses the essential testability considerations, both physical and logical, and focuses on both the new constraints and the new freedoms of modern manufacturing test in the ever-changing challenge.

Introduction:

The cost to produce a printed circuit assembly comes primarily from the cost of components, the cost of manufacturing and the cost of test. Test can comprise as much as 30% of the cost of building a product. If a product is manufactured with defects, a large penalty is paid in testing and repair. Thus, the concept of *designing for profitability* logically includes design for manufacturability (DFM) – manufacturing at the lowest feasible cost and lowest rate of defect introduction – and design for testability (DFT). In fact by increasing test coverage and defect isolation and diagnosis, DFT becomes a key ingredient in designing profitability into a product.

Test is no longer being viewed as a *no value added* or *hard to justify* expense, but rather as an integral part of the manufacturing process. The effort put into designing for testability can be the difference between a smooth manufacturing operation and a room full of dog boards. The sophistication of the testing/screening methods employed should be a direct reflection of the sophistication of the printed circuit board (PCB) under test and its technologies. Key to this effort is fault detection and isolation. As isolation can be increased, diagnosis can be faster and more deterministic. Accurate diagnosis can be used to indict not only the product failure, but also the process failure. Correcting the process failure leads to less rework and waste and increased throughput and yields, leading to higher profits.

The focus of this paper is to balance the freedom of the designers with the need to achieve optimal fault coverage of potential manufacturing defects. The most common method of coverage is electrical in-circuit test because it continues to provide the most cost-effective approach to detecting and diagnosing failures. But traditional electrical in-circuit testing has its own shortcomings. Some of these are being addressed by new innovations in electrical in-circuit test and also by functional test, manual visual inspection, automated optical inspection (AOI), and x-ray laminography (AXI). But before we delve into the technology, let us first understand the environment and the goal. This leads to the first key point.

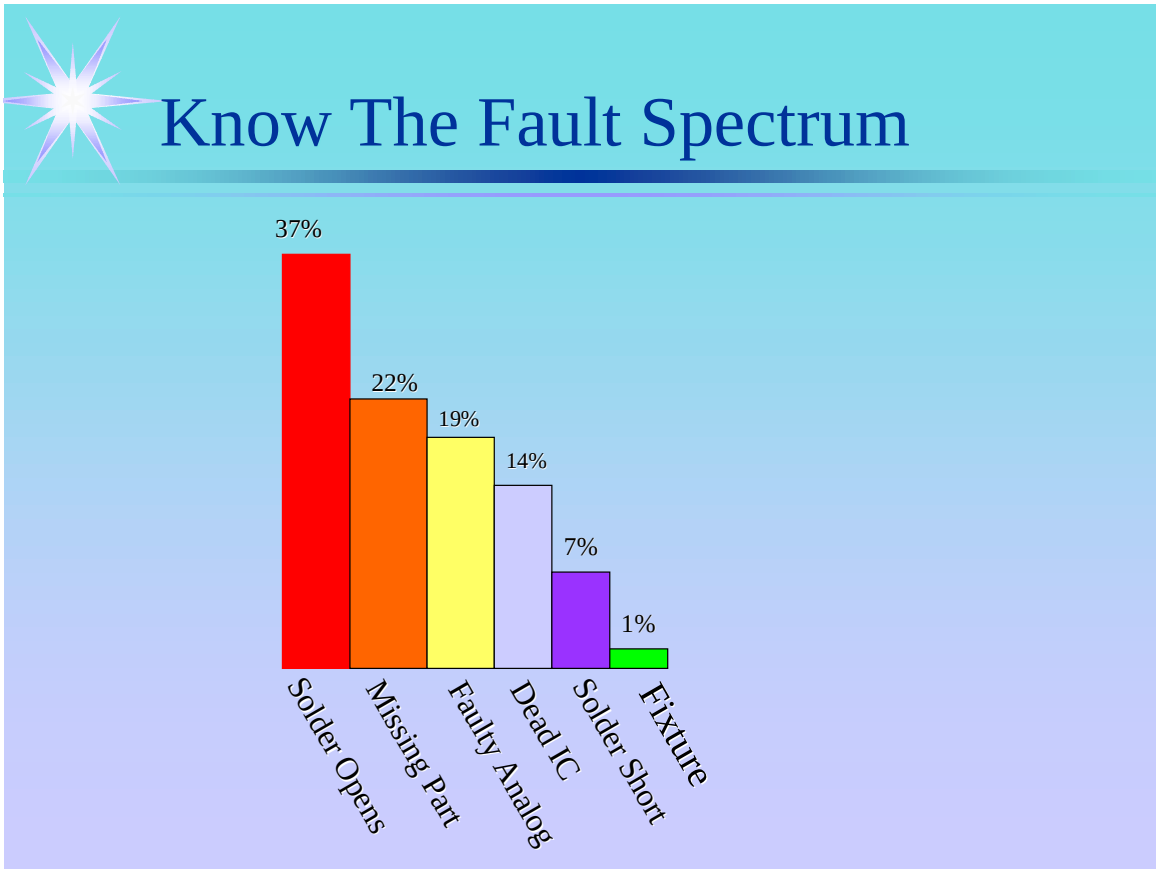


Collaborate From the Start

It should be obvious but deserves to be restated: Keeping up to date on the available test systems and methods, the expectations of manufacturing and the probability of any failure requires vigilance on the part of the both the test engineer and the design engineer. Gone are the days when design, test and production could afford to be isolated entities. Designs cannot be completed to the functional specifications and then *thrown over the wall.* Today, and into the future, cost and time-to-market pressures dictate that a product must involve collaboration between these entities. This collaboration must begin in the earliest stages of the product's conception and be ongoing. Representatives from each of design, test, purchasing, production and support must bring their own experience and knowledge as well as their own goals to the table in order to truly synergize toward a successful product.

Reward Cooperation

Cooperating is hard work. In many corporations there is a cultural barrier between departments. Different managers have different goals because they are graded on different objectives. It is easy to lose site of the corporate goal of creating a profitable product if that is not the level at which individuals are measured or rewarded. Strive to keep the big picture in mind when setting objectives. The idea here is to be proactive and personally go beyond your job description. Actively enlist the help of others and be willing to help other as well. Work to instill an atmosphere of cooperation.

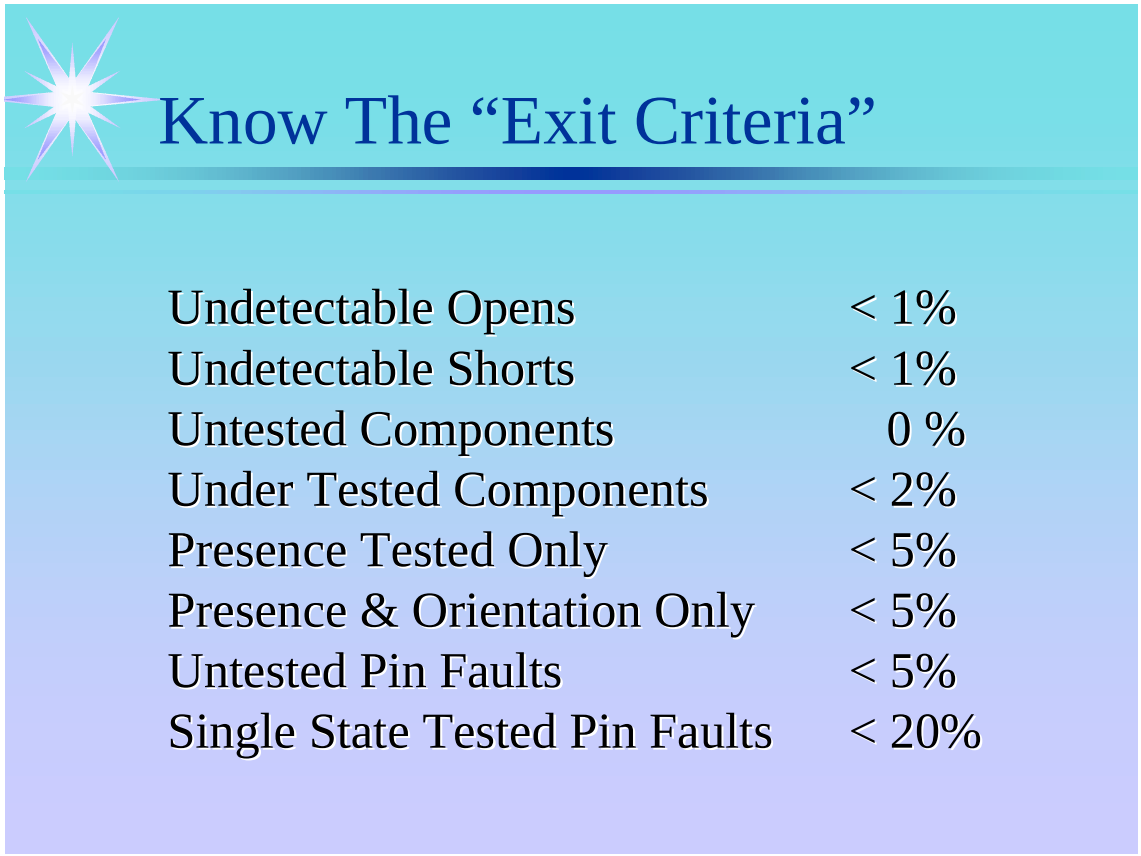


Consider The Fault Spectrum

For the vast majority of boards tested at end-of-line process testing, solder opens and missing or misaligned parts are the number one and number two causes of failure; next come missing, misaligned or wrong parts. Though this is typical, it varies with products and processes. Also, components that have a high probability of failure or are very expensive are usually known in advance, and test visibility can be adjusted accordingly. All departments involved need to be aware of the fault spectrum for the types of products that they design and of the manufacturing processes that are to be employed.

Know The Opportunities for Failure

Every trace, every solder joint, every component and every connector pin presents an opportunity for process failure. Furthermore, board size, routing space, package types, component types, handling etc. all contribute in a good or bad way to probability of failure. Keep this in mind, and try to work with your design department to minimize the opportunities for failures.



Consider The Coverage Criteria

The time that it takes to develop a device model for applying digital patterns to test the logic of an ASIC or large pin count digital device can range from days to weeks. Such factors have lead to the realization that 100% electrical/functional test coverage is no longer feasible where time-to-volume and manufacturing throughput is paramount in achieving profitability.

In recent years, the outsourcing of manufacturing to independent production sites has become an increasing phenomenon. Since the production management is ultimately responsible for the volume and quantity of product shipped, they have pushed back on the test department to quantify the coverage of the testing programs and tester interface fixtures that are provided to them. These coverage metrics are referred to as the *exit criteria* for the test development group. They are generally a compromise between fault coverage and the time required for development. It is important for the design team to be aware of these criteria, and work with the test development group as well as the production entity to assure that the criteria enabling the transition from test to manufacturing can be successfully met.

Consider Your Available Test Arsenal

The methods and systems that can be brought to bear when screening for defects should be taken into consideration when designing and manufacturing an assembly. While each screening method has its own capabilities, each introduced it own restrictions on the designer. Functional test has the ability to test an assembly in the same way that it will be exercised by it users. The test access that is necessary is typically accomplished through the edge fingers or connectors. Unfortunately, this method provides only a go, no-go test with sub-par diagnostics capability. When this is the only test method employed the designer should strive to partition the design modularly. Each module block must be designed with isolation, visibility and control in mind. Enabling, or at least not hampering rework should also be a consideration. Additional hardware designed into the assembly should be considered to provide diagnostic multiplexing for reading signals, out of lock detection and over voltage/over current triggers. Still it is risky to power-up an assembly that is fresh from construction, as the damage potential can be very high.

Because the cost of damage from a pure functional test strategy is potentially high, some sort of screening for electrical shorts and opens is often introduced prior to power-up. Manufacturing defect analyzers (MDA) are a popular form of electrically screening for potentially damaging etching shorts, solder bridges or splashes. Even the least sophisticated of these systems can also detect missing components, etching opens, open solder and raised pins. The more sophisticated of these machines can also test for mis-loaded, including reverse-polarity, wrong or bad passive analog components.

The introduction of an MDA into the testing strategy can impact design severely, since these instruments require probing access to every net of the board that is to be tested. There is also a cost implication since a test fixture is now required; construction of which can delay a products transition to manufacturing.

A giant step up from an MDA is full in-circuit and combinational test. Like an MDA, in-circuit is an electrical test and so it requires a fixture and probing access to PCB. In addition to the shorts/opens and un-powered analog testing, in-circuit test is applicable to powered analog and power digital testing of the mission electronics. Digital in-circuit test utilizes libraries of digital vectors that are sequentially applied to the component to exercise it. In-circuit test has shown itself to be a very cost effective method for screening for both manufacturing and component defects and for providing net, component and even pin level diagnostics with high throughput. For this reason it has become the workhorse of assembly test, and remains such today, having evolved along with device packaging and manufacturing breakthroughs.

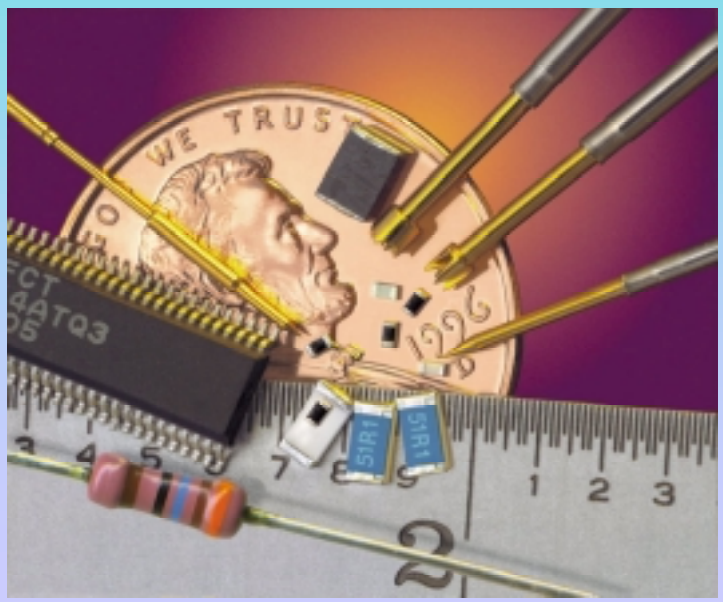
As very fine pitch ball-grid array and flip-chip components become more prevalent and PCB sizes shrink, net access has become increasingly scarce. This has driven the market for non-electrical screening. Where labor is relatively cheap, people are employed to inspect assembled boards, though experience has shown that this is not consistently reliable. The automatic optical inspection (AOI) systems use cameras and imaging algorithms to determining the presence, placement and orientation of components, even before the parts are soldered to the board. AOI is also capable of detecting gross solder problem, including solder splashes and raised pins.

Another non-electrical method, X-ray laminography (AXI), is the currently the fastest growing screening technique. X-ray inspection relies on the x-ray blocking characteristics of the lead content in the solder to assure the integrity of solder joints. They also screen for solder splash and solder flow shorts as well as open joints, even beneath ball-grid array packages. AXI is the only method than can quantitatively, as well as qualitatively assess solder joint integrity. There are three common process faults that are difficult to catch at electrical in-circuit test:

1. Missing/misloaded by-pass capacitors
2. Solder opens on pins that bring power to an IC.
3. Solder opens on pins which provide ground return

These faults can have significant consequences, especially on high-speed microprocessor assemblies. 3-D AXI has the ability to screen for these and other similar manufacturing defects on boards with components mounted to both sides, including multi-chip modules. If any of these structural screening techniques are used, additional design consideration must be given to the viewing angles of the cameras, the spacing between components, and the shadows imposed by taller components or board mechanical hardware. RF shields are also an impediment to manual visual and AOI screening, but perhaps not to AXI.

Limitations of Access



The War Over Real Estate

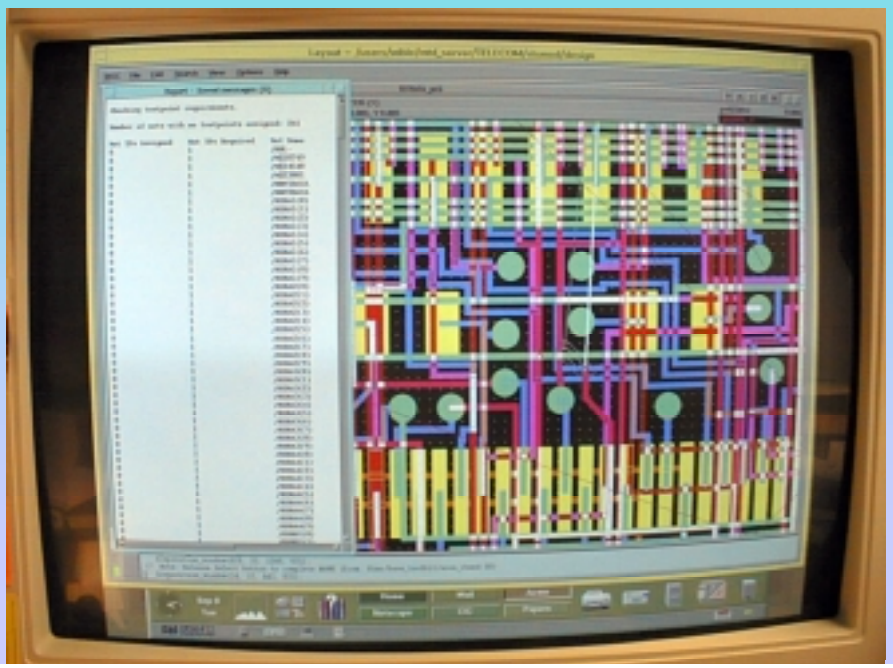
Take a penny from your pocket and look closely at Abraham Lincoln's bow tie. It is about the same size as an 0402 package. In the picture above, notice the comparative size of a test probe tip. It is easy to see that fixturing access for electrical in-circuit takes up the surface real estate that could be used for a number of these components. Take a closer look and compare.

The space that must be allotted to test probe access is becoming more and more significant as a percentage of overall board surface. As the above diagram indicates, using 0.035 pads fully 25% of the surface area of the board in this study had to be dedicated to test probe access. It is unfair to say that test access is an after-thought, but it is almost always secondary to the mission of the electronics of the product.

The Cycle of Integration

It is rare that board size can be increased to accommodate additional test points. With telecom line cards, PC boards, and many hand-held consumer products, it is common that the form factor for the board is set. Competition dictates that more and more functionality must be compacted into this area. This leads to more parts, part modules, and finer pitch parts. This generation of the product will tend to be accessibility challenged. In the next generation, cost will dictate (and time will allow) that many of the part modules will become ASICS and that the glue-logic may go to a LCA. This integration will produce fewer but higher pin count components. As a result there will be some space freed up on the assembly and test access can be enhanced. But at this point, the cycle begins anew and new features are added to fill the available space once again.

Make Use of Design Tools



Use The Design Tools to Gain Access

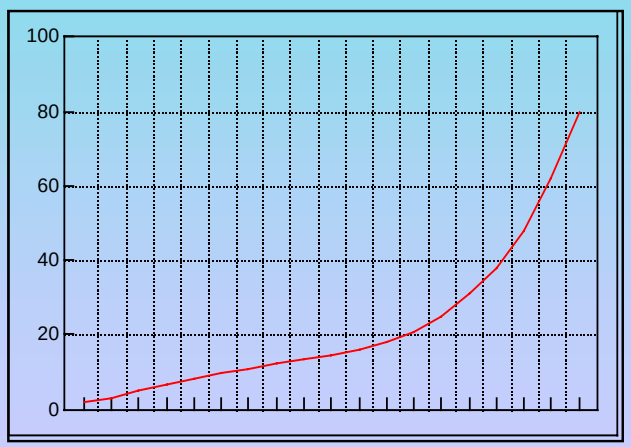
Most modern CAD systems have tools or macros (e.g. Mentor Physical Test Manager ©) that will trade off signal performance for test access. They will first select through-hole leads and then generate vias in the prescribed dimensions and mark them as test points automatically if no other design constraints are violated.

These system tools will also report inaccessible nets for which access must be added manually. Additional care must be taken to ensure that the selected test points are unmasked and not hidden under a component. This also may not be an automatic procedure. Design and layout are notably not conducive to testing since the routing is optimized to the placement of the components, without any ability to move the components for a more optimal routing. Try turning on Force Vectors (if it is available to you) to see if any components really want to move.

At this stage, if the necessary access is still not available, the next step is to add stubs to traces. Some design systems allow the specification of stub lengths for test access, and will provide these and automatically route around them. For other design systems this is a manual process. The same is true for the last resort of ballooning traces out to a test.

How Important is Access?

- What Devices Are On The Net?
  - What is their cost?
  - What is their failure profile
  - What is their rework cost



How Important Is Access - Turning The Question Around

We began by saying that complete test coverage and diagnosis was best achieved when at least 100% net access was provided to electrical in-circuit test. We have briefly looked at ways to maintain full test coverage and diagnostic ability while at the same time requiring less than 100% net access. Unfortunately for test, the question is not being posed, "Where can you do without access?", but is instead being posed "Where do you absolutely need to have access?"

The Economics Of Accessibility

Let us assume that you have done all of the right things as far as working with your cross-functional, new product generation team, and have worked especially with the test engineers and have pared down the access requirements, bringing to bear all of the weapons mentioned above. Still you find that the size and density of your project board is such that you will not have enough real estate to provide all of the test points that are required for a 100% test without spending days or even weeks hand-routing tented vias through layers. How do you judge the tradeoff between the this time and the cost of delaying the release of the design? Further, if you need 60 more test access points and only have enough board surface for 40, what do you do?

The answer to this question involves working closely with not only design, but also production engineering, purchasing and field repair. Given a choice of nets to access, you need to be able to answer the question:
What is the cost of not accessing this net?
And answer it for every net on the PCB.

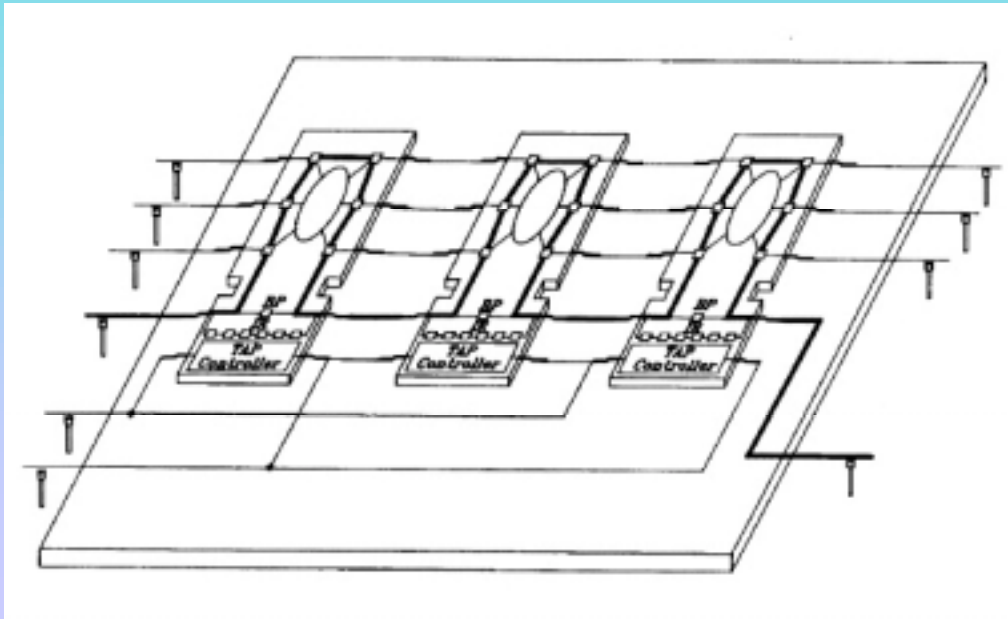
The first step is identifying the components that are connected to the net. Can you get any fault coverage without the missing

access and, if so, what percentage? What is the dollar cost of each of the components? What is the PPM failure rate of each of the components? What are the rework costs, and warranty costs. What is the goodwill costs of not finding the and letting your customer find it?

Ranking of Signal Types

When deciding how much effort to put into providing access to a net there are a few rules of thumb regarding the signal type of the net. Most important is assuring sufficient power injection to the assembly. This is particularly true where microprocessors are involved since their clocking rating is dependent on sufficient current being provided. Ground return access is important not only for powering the assembly, but also for providing sufficient instantaneous current carrying when a large number of digital edges are changing state at the same time. Insufficient ground net access will exacerbate a condition know as “ground bounce” that occurs when these signals are clocked. Next most important are control signals with names such as “ENABLE”, “DISABLE”, “SELECT”, “R/W”, “RESET”, “HALT”, “MODE”, “CLEAR”. Included in these, as we will see later, are the TAP ports that support boundary scan testing. When testing digital components, address lines are more important than data lines since lose of access to a data line will only impact testing a single connection while loss of access to an address line can inhibit testing of many data lines. Of least importance are nets associated only passive analog components and nets with only unused component pins

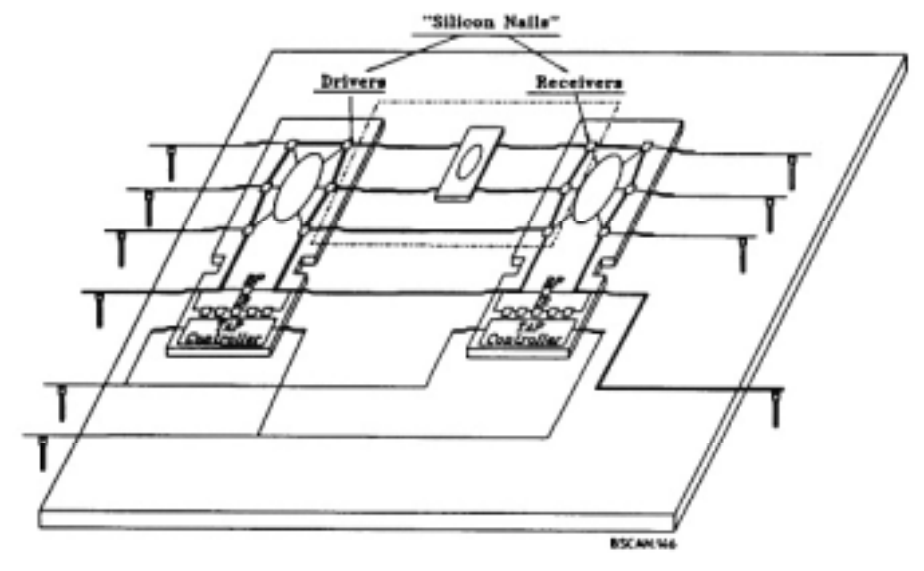
Scan Interconnect Chain



IEEE-1149.1: A Weapon In The Access War

The most promising advances in electrical testability in the decade of the 90s was the definition and adoption of the IEEE-1149.1 Boundary Scan standard. The standard only outlined the addition of a set of 4 (optionally 5) Test Access Port (TAP) pins to the device package and the op-codes for the 16 state machine that allows the observation and control of the device states. Only in recent years have ATE manufacturers begun to wrap the standard in software that is able to quickly generate test coverage for single both single components and chains of IEEE-1149.1 compliant devices. Interconnection Boundary Scan components into chains by tying the output of one component to the input of the next is the real key to decreasing the test access requirements of predominantly digital assemblies.

Scan Cell As Driver & Receiver



There is even more sophisticated software that enables the generation of automatic tests of components that are non-scan compliant, using the boundary scan register instead of tester electronics. This technique further decreases the test access requirements of the board.

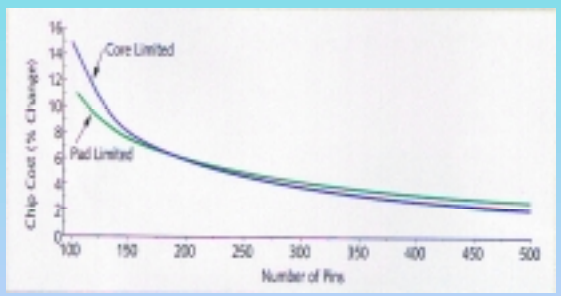
Test Considerations When Using Boundary Scan

There are caveats to be understood when considering this method. Complex dynamic parts cannot be tested at high clock rates. The effective parallel pattern application rate is relatively low since the patterns must be scanned in serially. Also, complex timing cannot be emulated.

IEEE-1149.1 compliant devices should be utilized whenever possible. A significant time advantage can be realized in the testing of these devices because the test engineer can develop a board level test without regard for the device's internal logic. All of the information that most test systems need is contained in the Boundary Scan Description Language (BSDL) file that the manufacturer of the component provides. This assumes that accurate BSDL is available in a timely manner.

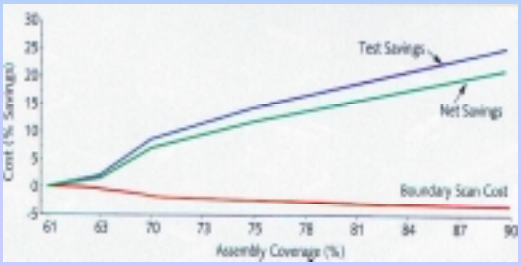
Remember that while there are always development timesavings when IEEE-1149.1 compliant devices are used, reductions in test access are only possible when the components are interconnected in chains. With scan chains all of the Test Clock (TCK) pins are common to a net, and all of the Test Mode Select (TMS) pins common to a net. Make sure that these two nets have test probe access. Also make sure that the Test Data In (TDI) pin of the lead component in the chain has test probe access, and that Test Data Out on the final

Add and Use Boundary Scan



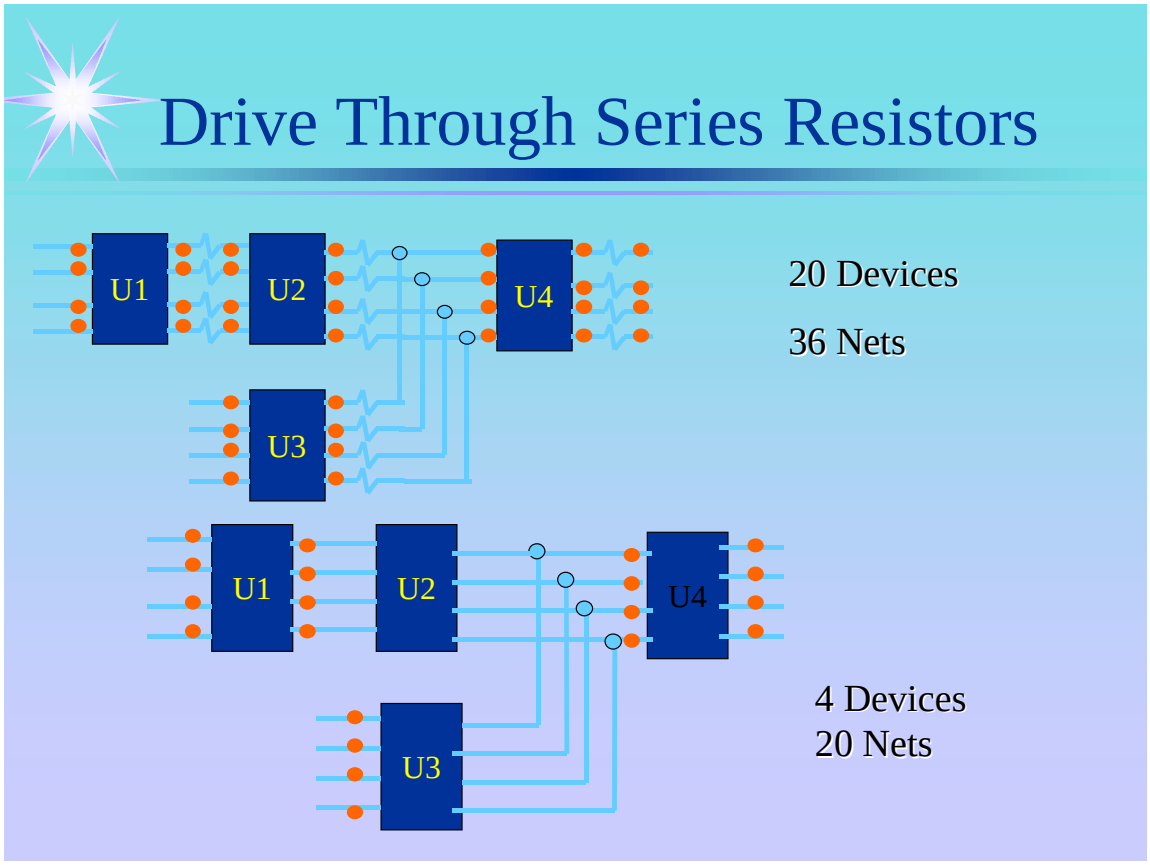
Percentage increase in component cost to add boundary scan

Savings in test development cost as use of boundary scan increases.



component in the chain has test probe access.

If test access is available for the I/O pins and any other pins of the IEEE-1149.1 components, mark these as test points when possible. Just because a component can be tested using boundary scan techniques, don't give up access if it is free. Also, when constructing the component chains, don't make the mistake of thinking that the component designator has any significance. The chain should be constructed by the components proximity to each other.

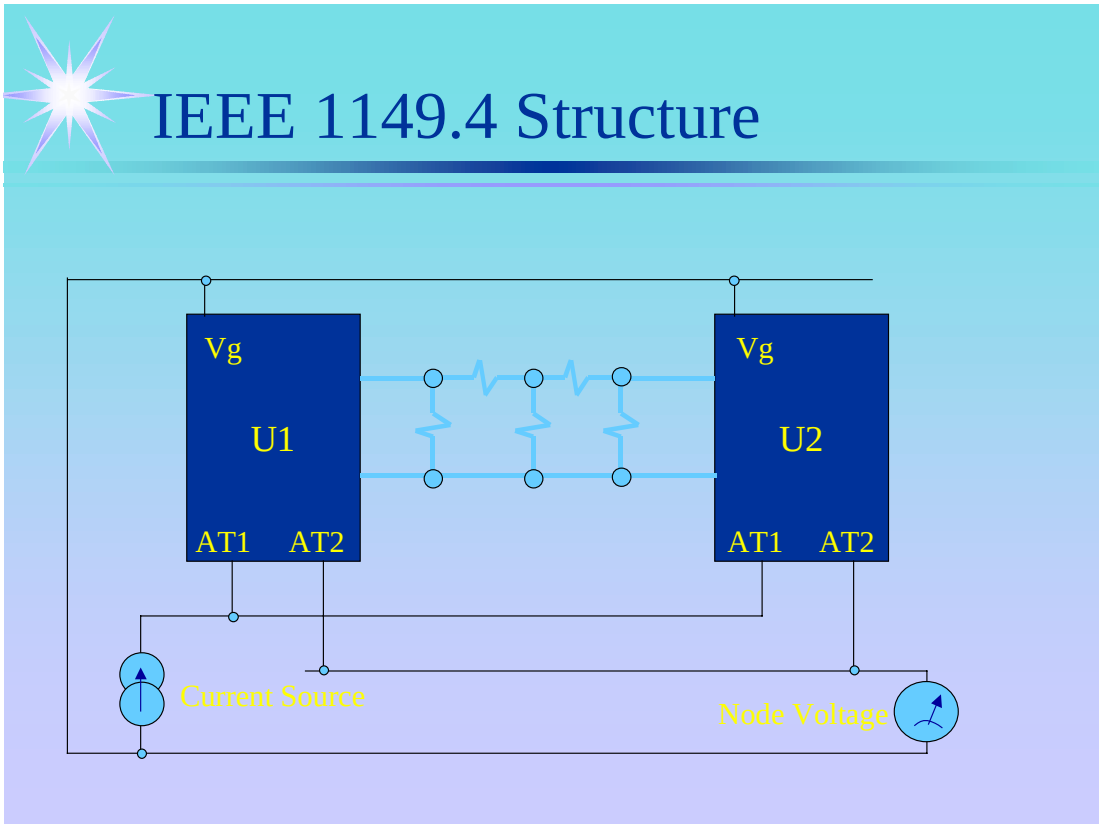


Drive Through Series Resistors

There is another weapon that has the potential of a large test point access savings through the use of software that can analyze the circuit topology to find resistors, capacitors, inductors, jumpers or switches in series with analog or digital ICs. These components and their nets can be factored out of the circuit as far as electrical in-circuit test is concerned. The diagram above is a simple illustration of the access savings that can be realized when this software is applied before the design is released. Shown is a 45% savings in net access and an 80% savings in devices to be tested. Although the results of applying this technique are not as dramatic when Boundary Scan chains are present, this technique is compatible with Boundary Scan and so some additional savings can still be attained.

Leave The Driving To Us

When this level of sophistication is applied DFT analysis is no longer a manual process; software tools must be employed. Of course the type of analysis is of little value if the electrical in-circuit test system does not understand the concepts and is not able to report an adapted diagnosis of failure. For this reason, it is best to use the analysis software as it is made available from your ATE equipment and software provider.



IEEE-1149.4 Help With Analog

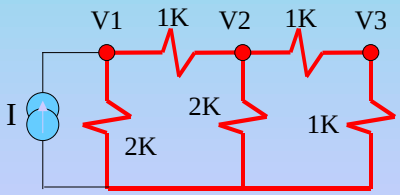
Recent additions to the IEEE-1149 specification have been shown to work in the realm of testing of analog component clusters with reduced test probe access. Note that the standard only outlines a structure in silicon that goes beyond IEEE-1149.1, adding an additional two pins to the digital devices for making interconnecting analog measurements.

Software Selection

This is also a case where DFT is no longer a manual process and software tools must be employed. Work at the University of California at Santa Barbara has provided a software solution that uses the IEEE-1149.4 structure and metrology study to generate the optimal and yet minimum set of test probe locations. Using the recommended access points will provide sufficient observation into the cluster to allow diagnosis to the component level. Unfortunately, this is academic software and does not provide any tests for the analog components. In fact, in this technique, the components are not measured at all. A model of the circuit is made, and extrapolated into a graph of the networks. Multiple measurements are taken at the accessible nodes at the periphery of the cluster. The current to be applied and expected voltages to be measured are calculated using matrix algebra. When those calculations do not match the actual measurements of the network, the adjacent components are indicted.

Full Range Variation

- All components varied over ±99% range



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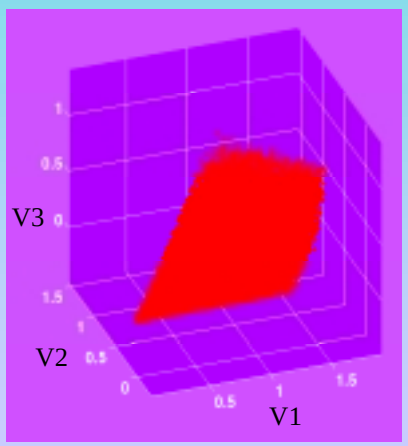


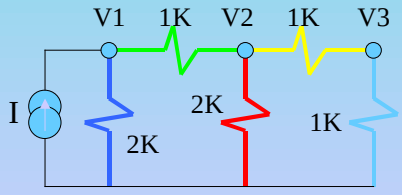
Automatic Access and Test Generation

Only recently has all of this come together.

1. The IEEE-1149.4 structure and command standard
2. The circuit analysis for test probe access
3. The ability to automatically generate the test series and solution set that is required to correctly indict one or multiple failures in both passive and active analog circuitry

A One Fault Example

- Assumes one fault



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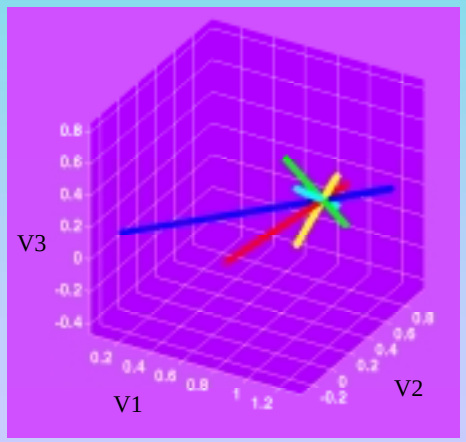


Combining Capabilities
AXI-ICT

Combining Equipment Capabilities

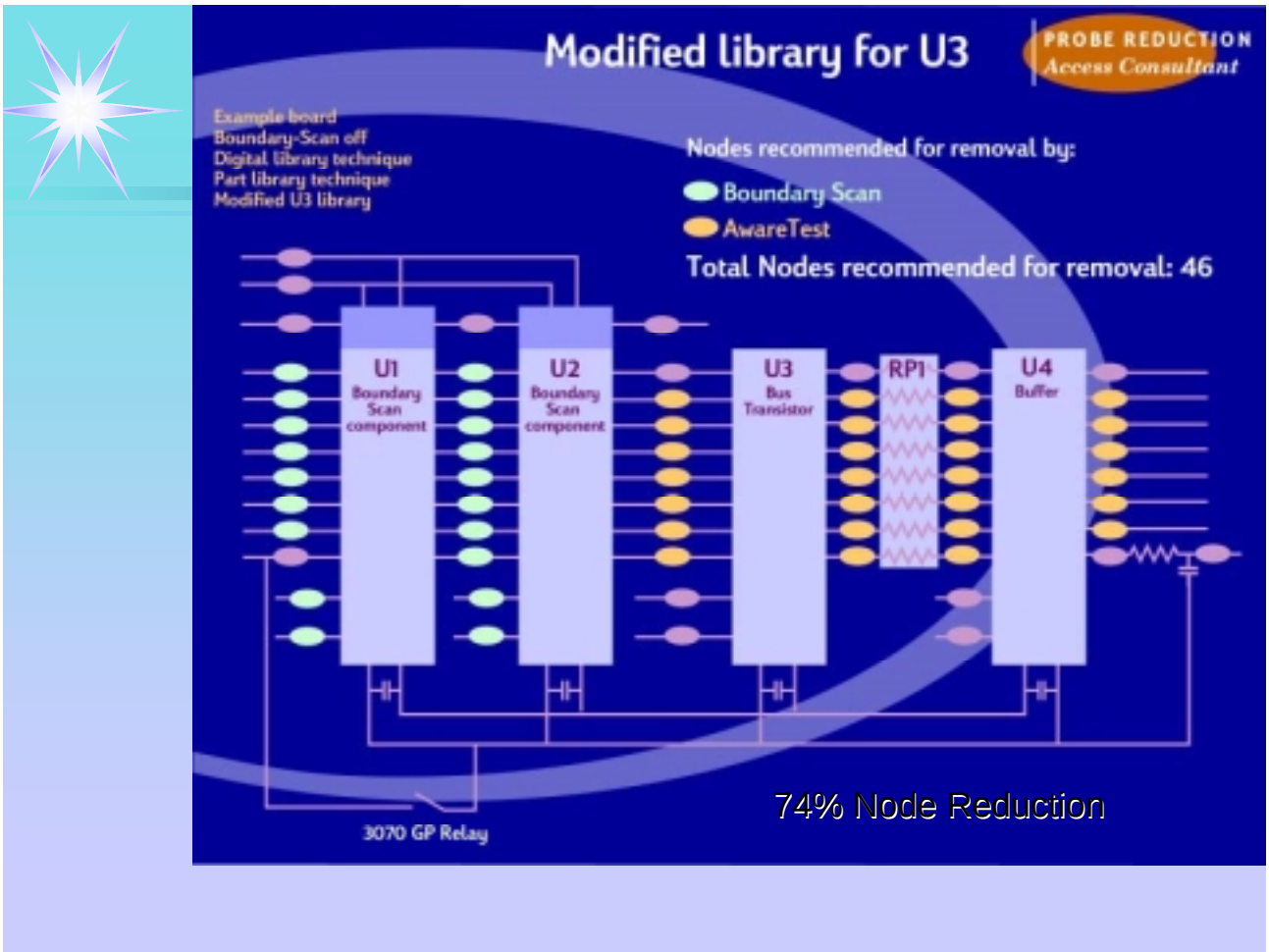
As noted earlier, automatic x-ray inspection systems use the x-ray blocking characteristic of the heavy metals (typically lead) in solder to determine that there is sufficient but not excessive solder at each joint between a component lead and the board, even for BGAs. Since this is not an electrical measurement, no probing access to the board is required. Consider the implications at in-circuit test if it has already been determined that all of the pad patterns have components placed and aligned, and that there are no solder shorts or opens. In-circuit is left to determine only three things:

1. The right component has been placed.
2. A component is oriented correctly.
3. A component is “alive”.

Assuming a functional test step before shipment and the low PPM failure rates of silicon components today, testing for these three is sufficient for in-circuit diagnosis.

This subtractive testing strategy means that boundary scan devices now need probes only the Test Access Port nets. Reading the ID register is sufficient to assure the correct component in the correct orientation and viability. For multi element digital devices only a single gate’s inputs and output (along with power and ground) need to be probed. Even for complex digital components access is required to only a few nets in order for a trivial subset of vectors to toggle an output pin.

Analog “pack” components provide a similar savings in probe access since the correct value of a pack can be determined by testing only one of its elements. Looking below at an example slide from Agilent’s Aware Test xi CBT, it is shown how the probe nodes of a circuit are reduced from sixth-two to sixteen; a reduction of 74%.



Combining AOI and ICT

Combining automated optical inspection with in-circuit can also provide benefit, though not to the scale that x-ray inspection can. AOI is best suited for assuring presence, alignment or polarity of components. Some characteristics of solder joints can also be seen, but not underneath BGAs and surface-mount connectors. Still, the relatively low cost of AOI equipment can make this a good inspection/test strategy for the right products.

Conclusions

Going forward, competitive pressures will make it imperative that product planning, design and testing go hand-in-hand to achieve economic success for the enterprise. As the global economy meets virtual manufacturing, the necessity for close collaboration between functional entities will compete directly with the potential for multi-continent separation of these entities. These will be challenges that must be overcome. When designing to test methodologies is the goal, advances in test methodologies must be tracked. Conversely, as PCB processes and component packaging evolve, test must strive to keep pace.