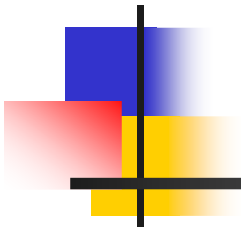

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- Challenges of Testing DDR2's on Agilent 3070
  - OBSERVATIONS
  - SOLUTIONS
  - SUMMARY

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- OBSERVATIONS
  - MULTIPLE VENDORS
  - DIE CHANGES
  - REGISTER MAP
  - INITIALIZATION SEQUENCES
  - DIFFERENTIAL CLOCK
  - LIMITED ACCESS

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- MULTIPLE VENDORS
  - Samsung
  - Micron
  - Hynix
  - Elpida
  - Qimonda

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- DIE CHANGES

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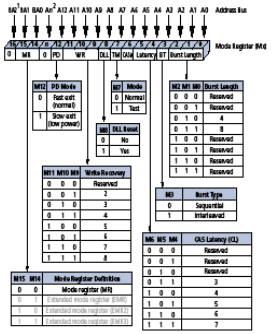
- REGISTER MAP

Burst Length

Burst length is defined by bits M0–M2, as shown in Figure 34 (page 76). Read and write accesses to the DDR2 SDRAM are burst-oriented, with the burst length being programmable to either four or eight. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2–A*i* when BL = 4 and by A3–A*i* when BL = 8 (where A*i* is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

Figure 34: MR Definition



Notes:
1. M16 (BA2) is only applicable for densities 1Gb, reserved for future use, and must be programmed to "0."
2. Mode bits (M*n*) with corresponding address balls (A*n*) greater than M12 (A12) are reserved for future use and must be programmed to "0."
3. Not all listed WR and CL options are supported in any individual speed grade.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved. The burst type is selected via bit M3, as shown in Figure 34 (page 76). The ordering of accesses within a burst is determined by the burst length, the burst type,

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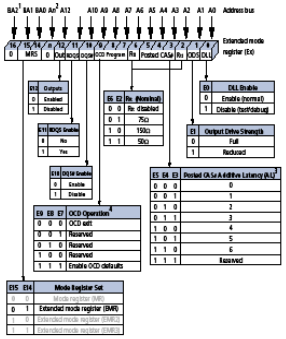
- REGISTER MAP

Extended Mode Register (EMR)

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, on-die termination (ODT), posted AL, off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and output disable/enable. These functions are controlled via the bits shown in Figure 36 (page 81). The EMR is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

The EMR must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in an unspecified operation.

Figure 36: EMR Definition



Notes:
1. E16 (BA2) is only applicable for densities 1Gb, reserved for future use, and must be programmed to "0."
2. Mode bits (En) with corresponding address balls (An) greater than E12 (A12) are reserved for future use and must be programmed to "0."
3. Not all listed AL options are supported in any individual speed grade.
4. As detailed in the Initialization (page 87) section notes, during initialization of the OCD operation, all three bits must be set to "1" for the OCD default state, then set to "0" before initialization is finished.

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- REGISTER MAP

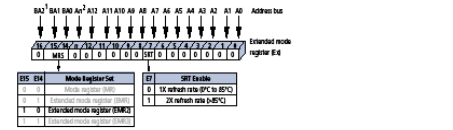
Extended Mode Register 2 (EMR2)

The extended mode register 2 (EMR2) controls functions beyond those controlled by the mode register. Currently all bits in EMR2 are reserved, except for E7, which is used in commercial or high-temperature operations, as shown in Figure 39 (page 85). The EMR2 is programmed via the LM command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

Bit E7 (A7) must be programmed as "1" to provide a faster refresh rate on IT and AT devices if T_C exceeds 85°C.

EMR2 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in an unspecified operation.

Figure 39: EMR2 Definition



Notes:
1. E16 (BA2) is only applicable for densities ≥1Gb, reserved for future use, and must be programmed to "0."
2. Mode bits (E*n*) with corresponding address balls (A*n*) greater than E12 (A12) are reserved for future use and must be programmed to "0."

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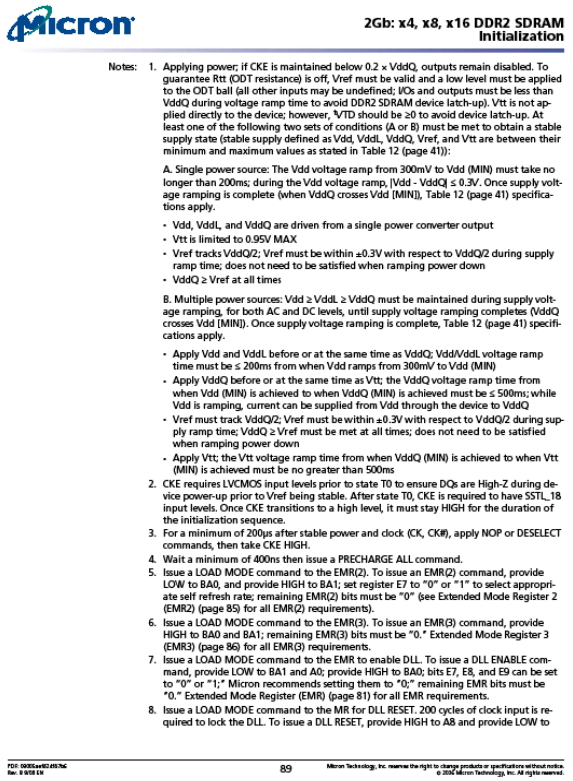
- INITIALIZATION SEQUENCES



Notes:

1. Applying power; if CKE is maintained below 0.2 x VddQ, outputs remain disabled. To guarantee Rtt (ODT resistance) is off, Vref must be valid and a low level must be applied to the ODT ball (all other inputs may be undefined; I/Os and outputs must be less than VddQ during voltage ramp time to avoid DDR2 SDRAM device latch-up). Vtt is not applied directly to the device; however, ^{V}TD should be ≥0 to avoid device latch-up. At least one of the following two sets of conditions (A or B) must be met to obtain a stable supply state (stable supply defined as Vdd, VddL, VddQ, Vref, and Vtt are between their minimum and maximum values as stated in Table 12 (page 41)):

   A. Single power source: The Vdd voltage ramp from 300mV to Vdd (MIN) must take no longer than 200ms; during the Vdd voltage ramp, |Vdd - VddQ| ≤ 0.3V. Once supply voltage ramping is complete (when VddQ crosses Vdd (MIN)), Table 12 (page 41) specifications apply.
   - Vdd, VddL, and VddQ are driven from a single power converter output
   - Vtt is limited to 0.95V MAX
   - Vref tracks VddQ/2; Vref must be within ±0.3V with respect to VddQ/2 during supply ramp time; does not need to be satisfied when ramping power down
   - VddQ ≥ Vref at all times

   B. Multiple power sources: Vdd ≥ VddL ≥ VddQ must be maintained during supply voltage ramping, for both AC and DC levels, until supply voltage ramping completes (VddQ crosses Vdd (MIN)). Once supply voltage ramping is complete, Table 12 (page 41) specifications apply.
   - Apply Vdd and VddL before or at the same time as VddQ; Vdd/VddL voltage ramp time must be ≤ 200ms from when Vdd ramps from 300mV to Vdd (MIN)
   - Apply VddQ before or at the same time as Vtt; the VddQ voltage ramp time from when Vdd (MIN) is achieved to when VddQ (MIN) is achieved must be ≤ 500ms; while Vdd is ramping, current can be supplied from Vdd through the device to VddQ
   - Vref must track VddQ/2; Vref must be within ±0.3V with respect to VddQ/2 during supply ramp time; VddQ ≥ Vref must be met at all times; does not need to be satisfied when ramping power down
   - Apply Vtt; the Vtt voltage ramp time from when VddQ (MIN) is achieved to when Vtt (MIN) is achieved must be no greater than 500ms
2. CKE requires LVCMOS input levels prior to state T0 to ensure DQs are High-Z during device power-up prior to Vref being stable. After state T0, CKE is required to have SSTL_18 input levels. Once CKE transitions to a high level, it must stay HIGH for the duration of the initialization sequence.
3. For a minimum of 200µs after stable power and clock (CK, CK#), apply NOP or DESELECT commands, then take CKE HIGH.
4. Wait a minimum of 400ns then issue a PRECHARGE ALL command.
5. Issue a LOAD MODE command to the EMR(2). To issue an EMR(2) command, provide LOW to BA0, and provide HIGH to BA1; set register E7 to "0" or "1" to select appropriate self refresh rate; remaining EMR(2) bits must be "0" (see Extended Mode Register 2 (EMR2) (page 85) for all EMR(2) requirements).
6. Issue a LOAD MODE command to the EMR(3). To issue an EMR(3) command, provide HIGH to BA0 and BA1; remaining EMR(3) bits must be "0." Extended Mode Register 3 (EMR3) (page 86) for all EMR(3) requirements.
7. Issue a LOAD MODE command to the EMR to enable DLL. To issue a DLL ENABLE command, provide LOW to BA1 and A0; provide HIGH to BA0; bits E7, E8, and E9 can be set to "0" or "1;" Micron recommends setting them to "0;" remaining EMR bits must be "0." Extended Mode Register (EMR) (page 81) for all EMR requirements.
8. Issue a LOAD MODE command to the MR for DLL RESET. 200 cycles of clock input is required to lock the DLL. To issue a DLL RESET, provide HIGH to A8 and provide LOW to

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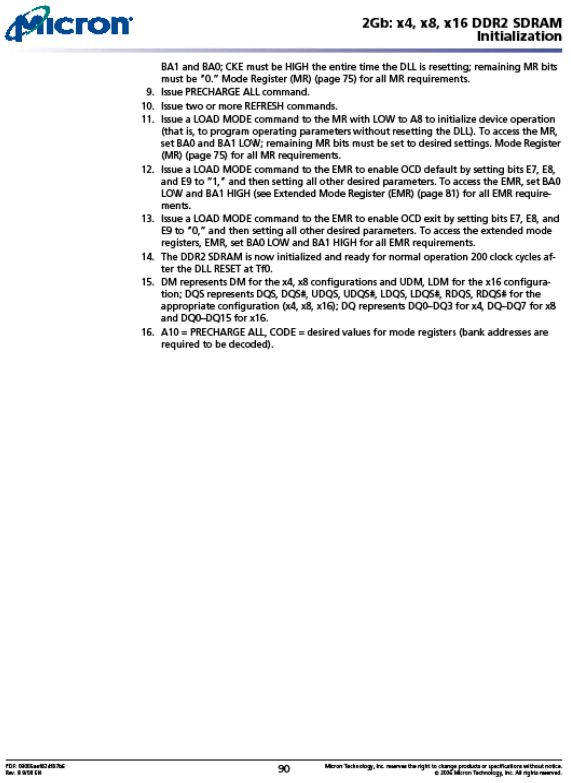
- INITIALIZATION SEQUENCES



BA1 and BA0; CKE must be HIGH the entire time the DLL is resetting; remaining MR bits must be "0." Mode Register (MR) (page 75) for all MR requirements.

9. Issue PRECHARGE ALL command.
10. Issue two or more REFRESH commands.
11. Issue a LOAD MODE command to the MR with LOW to A8 to initialize device operation (that is, to program operating parameters without resetting the DLL). To access the MR, set BA0 and BA1 LOW; remaining MR bits must be set to desired settings. Mode Register (MR) (page 75) for all MR requirements.
12. Issue a LOAD MODE command to the EMR to enable OCD default by setting bits E7, E8, and E9 to "1," and then setting all other desired parameters. To access the EMR, set BA0 LOW and BA1 HIGH (see Extended Mode Register (EMR) (page 81) for all EMR requirements.
13. Issue a LOAD MODE command to the EMR to enable OCD exit by setting bits E7, E8, and E9 to "0," and then setting all other desired parameters. To access the extended mode registers, EMR, set BA0 LOW and BA1 HIGH for all EMR requirements.
14. The DDR2 SDRAM is now initialized and ready for normal operation 200 clock cycles after the DLL RESET at T#0.
15. DM represents DM for the x4, x8 configurations and UDM, LDM for the x16 configuration; DQS represents DQS, DQS#, UDQS, UDQS#, LDQS, LDQS#, RDQS, RDQS# for the appropriate configuration (x4, x8, x16); DQ represents DQ0–DQ3 for x4, DQ–DQ7 for x8 and DQ0–DQ15 for x16.
16. A10 = PRECHARGE ALL, CODE = desired values for mode registers (bank addresses are required to be decoded).

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- DIFFERENTIAL CLOCK

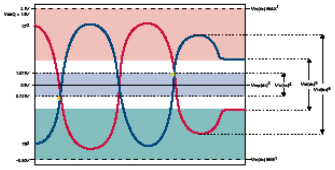
Table 16: Differential Input Logic Levels

All voltages referenced to Vss

Parameter	Symbol	Min	Max	Units	Notes
DC input signal voltage	Vin(DC)	–300	VddQ	mV	1, 6
DC differential input voltage	Vid(DC)	250	VddQ	mV	2, 6
AC differential input voltage	Vid(AC)	500	VddQ	mV	3, 6
AC differential cross-point voltage	Vix(AC)	0.50 x VddQ - 175	0.50 x VddQ + 175	mV	4
Input midpoint voltage	Vmp(DC)	850	950	mV	5

Notes:
1. Vin(DC) specifies the allowable DC execution of each input of differential pair such as CK, CK#, DQS, DQS#, LDQS, LDQS#, UDQS, UDQS#, and RDQS, RDQS#.
2. Vid(DC) specifies the input differential voltage |Vtr - Vcp| required for switching, where Vtr is the true input (such as CK, DQS, LDQS, UDQS) level and Vcp is the complementary input (such as CK#, DQS#, LDQS#, UDQS#) level. The minimum value is equal to Vih(DC) - Vil(DC). Differential input signal levels are shown in Figure 12 (page 44).
3. Vid(AC) specifies the input differential voltage |Vtr - Vcp| required for switching, where Vtr is the true input (such as CK, DQS, LDQS, UDQS, RDQS) level and Vcp is the complementary input (such as CK#, DQS#, LDQS#, UDQS#, RDQS#) level. The minimum value is equal to Vih(AC) - Vil(AC), as shown in Table 15 (page 43).
4. The typical value of Vix(AC) is expected to be about 0.5 x VddQ of the transmitting device and Vix(AC) is expected to track variations in VddQ. Vix(AC) indicates the voltage at which differential input signals must cross, as shown in Figure 12 (page 44).
5. Vmp(DC) specifies the input differential common mode voltage (Vtr + Vcp)/2 where Vtr is the true input (CK, DQS) level and Vcp is the complementary input (CK#, DQS#). Vmp(DC) is expected to be approximately 0.5 x VddQ.
6. VddQ + 300mV allowed provided 1.9V is not exceeded.

Figure 12: Differential Input Signal Levels



Notes:
1. TR and CP may not be more positive than VddQ + 0.3V or more negative than Vss - 0.3V.
2. TR represents the CK, DQS, RDQS, LDQS, and UDQS signals; CP represents CK#, DQS#, RDQS#, LDQS#, and UDQS# signals.
3. This provides a minimum of 850mV to a maximum of 950mV and is expected to be VddQ/2.
4. TR and CP must cross in this region.
5. TR and CP must meet at least Vid(DC) MIN when static and is centered around Vmp(DC).

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- LIMITED ACCESS

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- POSSIBLE SOLUTIONS
  - MINIMIZE NUMBER OF APPROVED SOURCES
  - CAREFUL ATTENTION TO CLOCK SETTINGS
  - CHECK the INITIAL SEQUENCES
  - SILICON NAIL TEST
  - COVERAGE EXTEND??

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- MINIMIZE NUMBER OF APPROVED SOURCES
  - A DIFFERENT TEST MAY NEED TO BE DEVELOPED FOR DIFFERENT VENDORS OR DIE's.

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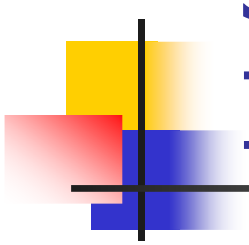

- CAREFUL ATTENTION TO CLOCK SETTINGS
  - PLAY AROUND WITH SLIGHT MODIFICATION TO THE “DH” AND “DL” LEVELS
  - SOURCE CLOCK ON THE OTHER SIDE OF A BUFFER

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- CHECK the INITIAL SEQUENCES
  - A SEQUENCE THAT WORKS WITH ONE VENDOR MAY NOT WORK ON THE OTHER

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- SILICON NAIL TEST
  - GOOD SUCCESS WHEN DDR's ARE CONTROLLED BY A PROCESSOR
  - WATCH OUT WHEN THEY ARE CONTROLLED BY AN "FPGA" OR MULTIPLE BOUNDARY SCAN DEVICES

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- COVERAGE EXTEND
  - IF ALL ELSE FAILS…AGILENT IS WORKING ON THIS AS ANOTHER POSSIBLE SOLUTION
  - CURRENTLY SHIPPING WITH 7.2 SOFTWARE BUT IT'S IN THE EARLY PHASE OF RELEASE

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- SUMMARY
  - DDR's ARE DEFINITELY A CHALLENGE
  - NO "ONE" TEST WORKS ON ALL ASSEMBLIES
  - GRIEF IS TO BE EXPECTED
  - REASONABLE SOLUTIONS ARE OBTAINABLE

THANK YOU!!