

ELECTRICAL IN-CIRCUIT TEST METHODS FOR LIMITED ACCESS BOARDS

*Raymond J. Balzer
Agilent Technologies*

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Introduction

This paper surveys the various electrical test methods and tools available to address testing boards that lack full electrical access. The goal of most of the techniques is to preserve the benefits of in-circuit tests, including automation of test generation, component-level diagnostics and high fault coverage. The alternative test methods will be evaluated in these dimensions and compared to the performance of in-circuit tests. The test methods to be covered include Boundary Scan (IEEE 1149.1), Vectorless test, ICCT (in-circuit cluster test), analog Boundary Scan (IEEE 1149.4) and powered cluster tests. The key support tool covered is the tool to recommend access configuration. Example data will be presented indicating the amount of access reduction available for the various techniques, while maintaining good test coverage.

In-circuit Testing

ICT has been and is the workhorse board-level test technique for many industries. It provides component-level testing and node-oriented shorts testing for virtually all electrical component types. This component-level testing inherently provides component-level diagnosis, thus leading to relatively inexpensive repair, since expensive technician time is not required for diagnosis as compared to many forms of functional testing.

Another key feature of ICT is that test generation is substantially automated. Shorts tests and analog component tests are normally created fully automatically by test generators which, in the best cases, do sophisticated circuit analysis to create the optimal test. These test generators not only create the tests, but also set test limits and decide on sense wire requirements and set guard points, based on surrounding topology. The test generation process can often be optimized by users for tradeoffs of coverage, test speed and fixture complexity, all by setting some up-front options. The resulting tests not only determine component presence, but also value; thus identifying that the correct component has been installed.

Digital test generation originally was virtually entirely based on library tests, usually supplied by the ATE vendor. The program generator automatically adds disabling techniques for surrounding digital parts, backdrive analysis and some test optimization for the topology. The test would normally test all I/O pins at both logic levels and test 3-state as well; this tests for open pins and electrical operation. In addition, this would inherently test at least a fraction of the device's

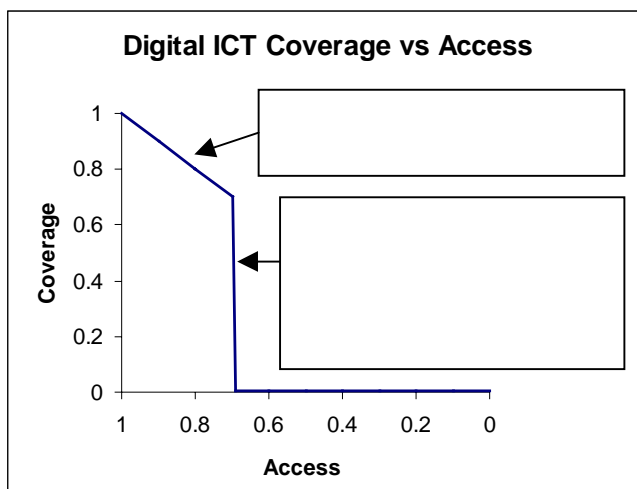
core functionality, which at least partially tests that the correct device is installed. The above combination of tests inherently tests for device orientation, as well. However, complex devices and a quickening pace of IC development have strained library test development. In some cases, it is not practical to develop complete libraries for complex devices such as ASICs and CPLDs. Thus, alternative digital techniques were developed, referred to as vectorless test.

Vectorless test techniques have been developed to reduce the test development effort for complex digital parts. These techniques have also proven applicable to analog ICs. Vectorless techniques typically either use IC pin to lead-frame capacitive measurements or use I/O protection diode measurements. The primary test coverage is for opens and thus, presence, but not correct orientation or the correct device. Diagnostics are provided to pin level, including input pins; this is an improvement over digital library test diagnostics. Test quality and stability varies widely by technique and by the engineering implementation quality by the ATE vendor.

Powered functional tests are the norm for analog and mixed-signal ICs, except where vectorless techniques are used. The better ICT test vendors supply analog and mixed-signal test libraries. Further, their program generators then automatically adapt the libraries for the specific devices and topologies. These device tests typically test each pin's electrical operation, some functional operation and inherently, identify presence and correct device and orientation.

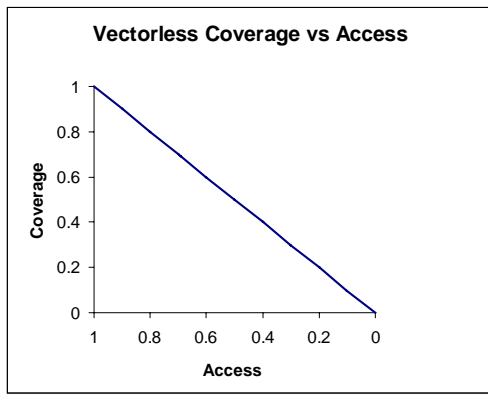
Limited Access Challenges

Excepting for the growing problems with the lack of digital libraries, ICT was and remains successful and dominant in testing boards where the economics of board cost, complexity, volume and quality justify the capital expense of an ICT system. However changes in SMT manufacturing present challenges to the ICT test engineer. Component geometry continued to shrink, as did test pads. Surface mount components loaded on both sides of the board further accelerated the changing board layout. The move to even higher speed operation further drives intra-device spacing to smaller distances and ball grid arrays increase the signal routing problems. The result is that instead of having electrical access to 100% of the nodes, this access is less than 100% and declining. Access varies by industry. Consumer electronics devices are usually squeezed more than industrial equipment.

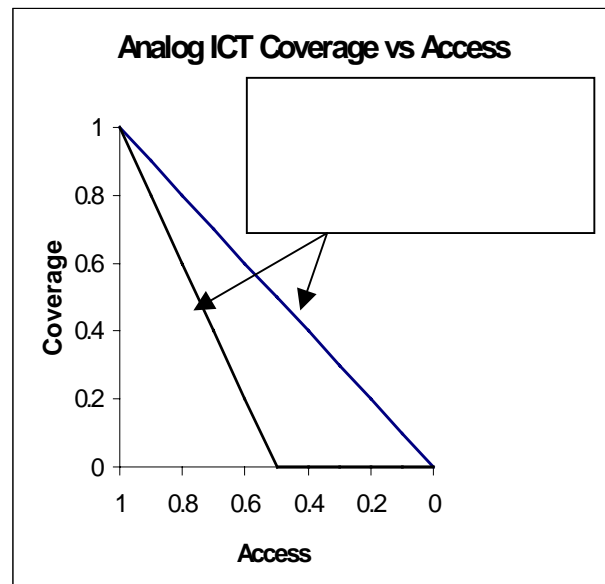


The consequences to ICT can be significant. There is a potential immediate loss of test coverage as access is reduced. The rate of loss of coverage varies, depending on the particular test method. But in general, ICT test methods can lose coverage faster than access is lost. For example, a

board with 90% access may have less than 90% ICT test coverage using traditional test methods, even if the best Design for Test (DFT) procedures for access selection were followed. If DFT practices are not followed, even a slight loss of access at critical points, such as oscillators and disables could result in significant loss of coverage.



Note that in comparison, vectorless techniques are much more linear in loss of coverage. Thus, vectorless test techniques can add value as a method to maintain partial coverage, when digital ICs have a significant loss of access.



Analog ICT tends to lose coverage linearly with loss of access, assuming good DFT decisions. However, the loss of coverage is generally faster than the loss of access.

New ICT Test Methods Maintain Coverage

To address the challenges of testing limited access PCB's, new tools and techniques have been developed. These combined with good DFT preserve the value of ICT and maintain test coverage. These are discussed below.

Handling Digital Parts with Series Terminators

It is increasingly common for high-speed digital logic designs to use series terminators, typically below 40 ohms, for signal quality reasons. This can dramatically increase the board node count and trace density on heavily digital boards. The result, usually is a further loss of ICT electrical access to board nodes.

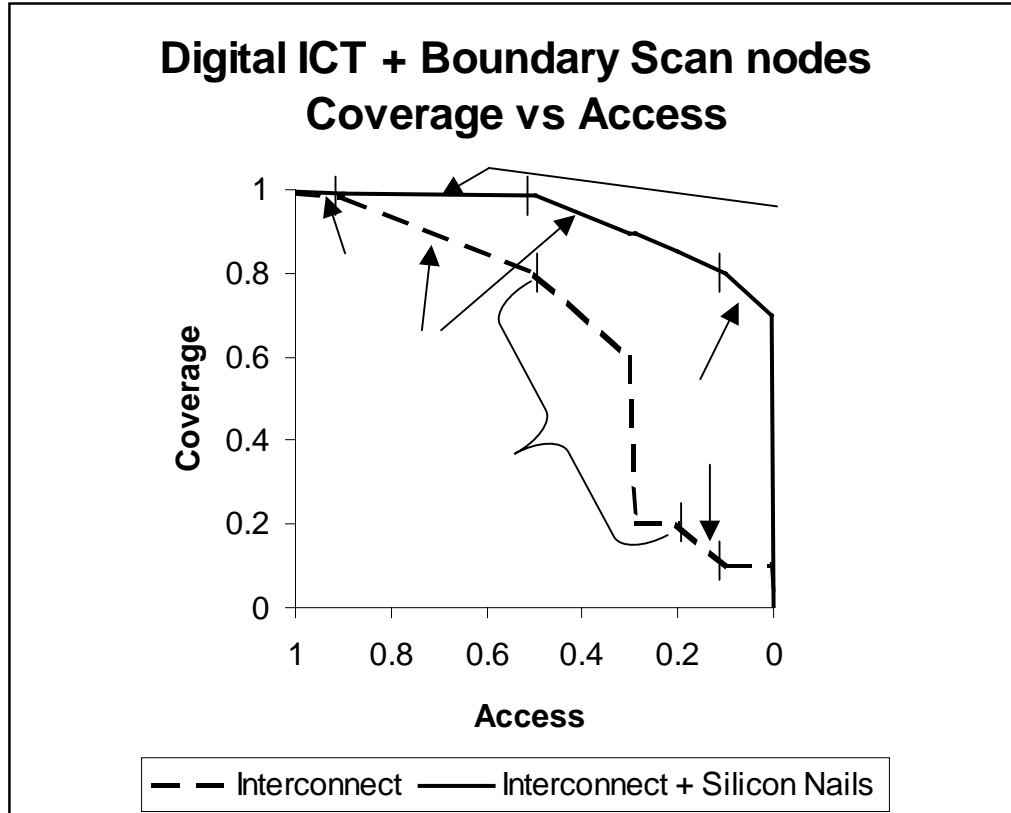
A simple technique is to eliminate access to one side of each series terminator and test or "drive" through it to the adjacent digital IC pin. This technique can be applied to library-based IC tests as well as the lead-frame capacitive vectorless technique because it is an AC measurement and impedances below 20k are relative inconsequential.

This concept maintains test coverage on the more expensive powered digital part, which also has more potential defects. However, there is a loss of coverage on the passive terminator. The testing typically will detect a missing terminator, but not measure the value. Usually, this is a good tradeoff. The value issue is best handled by measuring the first and last placement of the part on the board, confirming the correct part reel was used with the pick and place machine.

Digital Boundary Scan (IEEE 1149.1)

Boundary Scan is a methodology with great limited-access test potential. Implementation begins with ICs being designed with four extra pins to support the TAP test port and extra silicon used at each I/O pin and for a TAP controller to support the various test modes. This implementation can then be augmented at board level through interconnections of multiple Boundary Scan enabled parts, and it can be further extended to system level.

Once multiple devices are on the board and chained together, any nodes that interconnect these devices, and have both drive and receive capability, can be tested without Bed-of-Nails (BON) access. However, before removing access on these nodes, consider any non-scan devices on the nodes because test coverage could be lost for these components. Boundary scan nodes connected to the edge connector can be fully scan tested via edge access and either using a matching scan device or using ATE pin electronics.



Boundary Scan testing will provide node-level shorts testing and pin-level opens testing and diagnostics on scan devices. Since it is a powered test, not only are the I/O pins tested, but their ability to drive and receive are also tested. Orientation is tested. Further, Boundary Scan provides an unmatched ability to test that the correct device is installed using the optional ID code capability.

In summary, Boundary Scan testing provides all the board-level manufacturing fault coverage of digital library tests plus more (e.g. ID code) plus the pin-level diagnostic resolution of the vectorless methods. Further, the test generation is fully automated, based on board topology and a Boundary Scan description (BSDL) of each scan device.

On most boards no more than half of the digital parts, and usually much less, have Boundary Scan. In addition, many of the nodes have pull-up resistors and even analog circuitry driven by the node. Thus, the number of 'pure Boundary Scan nodes' is usually fairly limited, and thus the ability to remove access without loss of coverage at first appears limited.

However, it is possible to test the non-Boundary Scan digital parts by using the drive and receive capability of the Boundary Scan enabled parts connected to the non-scan parts. Frequently, the non-scan part is a memory chip, typically RAM, that is connected solely to a single scan device (e.g. an ASIC). Other times, the non-scan device, typically a bus buffer, is connected to several scan devices. In either case, the device can be tested by using the Boundary Scan drivers and receivers to provide the test stimulus and receive the responses of the non-scan device under test (DUT). This has been called Silicon Nails™ testing, as opposed to testing with physical nails directly attached to ATE pin electronics. It is possible to further extend this conceptual model to test clusters of components.

As seen in the figure, using Boundary Scan to test non-scan devices results in much more test coverage at any level of access. The results are especially dramatic with very low test access.

To facilitate achieving these results, ATE vendors can help by providing automated methods to create the tests for non-scan devices. One such method allows the tests to be created automatically based on the library test description for the non-scan device. The Boundary Scan chains are automatically analyzed for applicability to the DUT and the Boundary Scan resources are selected, disables determined and the parallel test vectors are serialized and fed through the chain.

The prerequisites for developing and utilizing digital Boundary Scan are that the board must be designed with Boundary Scan enabled ICs (and they are not always available), the implementation must be compliant to the standard and the BSDL description file must be accurate. One diagnostic disadvantage is that certain simple topologies result in node-level diagnostics rather than device.pin-level diagnostics more common with full-access ICT methods. Another diagnostic disadvantage can occur if the Boundary Scan chain itself fails to operate; diagnostics are still available, but fault detection could be limited to one fault per test/repair cycle

Analog Boundary Scan (IEEE 1149.4)

As noted above, some Boundary Scan nodes have analog components attached. While digital Boundary Scan permits major reductions in access for testing digital parts, even including non-scan parts, it does nothing for analog parts. That's where the new 1149.4 standard comes into play.

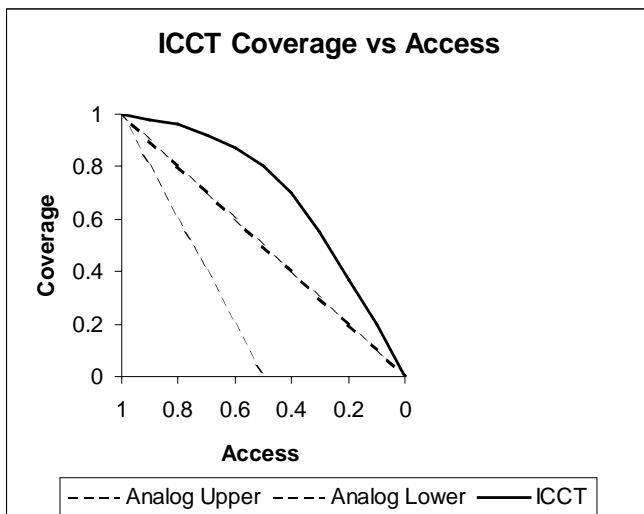
The 1149.4 standard allows for two extra types of test coverage. The first is that analog and mixed signal ICs can conform to the standard and be included in interconnect tests with digital ICs and experience similar test benefits as digital Boundary Scan parts. These benefits include automated test generation that provides powered shorts and opens testing and diagnostics per pin, thus including testing device presence and orientation and that the device is the correct one. The second type of test coverage is analogous to testing non-scan digital parts via scan. In this case, non-scan analog and mixed signal parts can be tested via 1149.4 scan. Provisions are made for test busses that can route signals between instrumentation and the DUT via the 1149.4 components. When this technology matures, it offers the promise of high test coverage with limited nodal access for analog components.

1149.4 issues would be similar to 1149.1, except that 1149.4 is in its infancy and that is its critical disadvantage.

ICCT (Analog In-Circuit Cluster Test)

ICCT is a very recently introduced in-circuit test technology. It is an unpowered test technology that tests clusters of passive analog components, targeting those clusters with limited nodal access. It provides test coverage for shorted and open/missing components, as well as measuring the component value, thus detecting if it is the correct component.

ICCT shares the primary characteristics and features of normal ICT. Test generation is automatic, based on the netlist information; this is automation of cluster identification as well as generation of the stimulus/expected response set. The test generator automatically sets limits, based on the component values and tolerances, as well as the circuit configuration to achieve the goal of identifying wrong components and other manufacturing faults.



ICCT also provides diagnostic analysis and associated repair information automatically like normal ICT. Failures result in diagnostics messages that in the best case report the failing component and its 'measured' value.

On typical clusters, nodal access between 50% and 80% is sufficient to usually achieve close

to 100% coverage of measurable components and circuits.

The key disadvantage of the technique is its relatively low test throughput compared to conventional ICT. Fault coverage in the cluster environment is also very sensitive to the particular topology, which nodes have access in the topology and the tolerances of all of the components. In general, fault coverage will be somewhat lower than conventional analog ICT, but much higher than typical cluster functional tests. Typical analog circuits with limited access today are RF circuits. Unfortunately, typical ICT test frequencies cannot adequately test these circuits and achieve high fault coverage. The fault is not with the ICCT technique, but with today's ATE test hardware limitations.

Powered Cluster Functional Test

The traditional method to test with limited access is edge-connector based test. This concept evolved to testing smaller internal clusters with a BON fixture. These are powered tests and they test the circuit functionally. Functional test has the advantage of providing confidence that the circuit works for the intended application. However, it has serious disadvantages as well.

Digital functional tests are commonly created with the assistance of a computer simulation, both logic and fault, of the circuit to assure through test coverage and to create the data needed for diagnostics. Diagnostics have been done with some combination of backtrace and a fault dictionary. These test methods require high skill and considerable time, because of the lack of full automation provided by ICT. Functional coverage is also limited in some areas, such as verifying the correct values of pullup resistors.

Analog and mixed signal functional tests have usually been limited to testing limited functions, such as gain and frequency response or A to D or D to A conversions. Beyond that, these tests quickly evolve to needed racks of instrumentation with sophisticated synchronization via a test executive. These tests are not for the faint of heart. There usually are no diagnostics, nor fault coverage reporting tools.

For some high volume product areas, commercial test solutions are available that provide the base hardware and the test executive and also help automate test generation, usually with some degree of 'canned' tests. But none of these functional tests come close to providing the level of automation of test generation and diagnosis as ICT.

Access Selection Optimization and Results

There is a considerable potential benefit in selecting the best test points for access. Access selection is a critical part of Design for Testability (DFT). In all of the diagrams showing Coverage versus Access, the curves shown were based on optimal DFT; they can be considered the upper limit of coverage. For many circuits, losing access on a certain few nodes can destroy testability. A typical graph of coverage versus access with bad DFT will show coverage virtually disappearing as even a little access is removed. A simple example would be the

lack of access to the disable of an oscillator then leading to unstable ICT or Boundary Scan tests of all downstream digital parts.

Thus, it is important to strive for good DFT regarding access. Various ATE vendors provide tools to assist in selecting the optimal access points. These tools are best used in partnership with board layout. But even after board layout, such tools can be used to select only a subset of the accessible nodes for actual BON access. This reduction can be simply to reduce fixture cost and complexity, or it can be done when the accessible node count exceeds the available tester resource configuration.

Even with optimal DFT, the amount of access reduction available varies depending on the board design. The following data is categorized according to product/industry. The access reduction is optimized for maximum coverage.

Product	Boundary Scan	ICCT	Terminators	Total Access Reduction
Computer Products ~1200 nodes	6 devices 200 nodes	20 clusters 100 parts 30 nodes	250 resistors 125 nodes	30%
Wireless Products ~700 nodes	2 devices 100 nodes	35 clusters 385 parts 100 nodes	20 resistors 10 nodes	30%
Broadcast Products ~1500 nodes	10 devices 250 nodes	45 clusters 2250 parts 500 nodes	50 resistors 25 nodes	52%
Workstation Products ~5900 nodes	10 devices 400 nodes	50 clusters 1400 parts 300 nodes	400 resistors 200 nodes	15%
Automotive Products ~750 nodes	2 devices 100 nodes	25 clusters 300 parts 75 nodes	10 resistors 5 nodes	25%
Consumer Products ~700 nodes	3 devices 100 nodes	25 clusters 500 parts 120 nodes	50 resistors 25 nodes	35%

- Special thanks to Sid Kramer for this data.

Next, a few selected boards will be displayed.

Board Size			Access Reduction			
Nodes	Components		Boundary Scan*	ICCT	Terminators	Total
	Analog	Digital				
601	759	11	0	15%	10%	25%
4464	2434	45	.04%	.4%	25%	25%
5822	2197	96	0	1.1%	20%	21%
7719	1734	140	1%	.03%	2.5%	3%
9669	625	153	21.9%	.2%	.7%	22%

- Boundary Scan reduction is only based on interconnect tests of Boundary Scan components. Testing non-scan devices via scan would increase scan-based access reduction significantly; access reductions as high as 90% have been seen.
- Special thanks to Joe Kirschling for this data.

Summary

The numerous advantages of in-circuit test have been challenged by the advent of decreasing electrical access. Fortunately, the ATE industry has risen to the challenge and has provided multiple solutions. There are a number of important test techniques that maintain the advantages of ICT, including test development and component-level diagnostics automation, even in a limited access board test environment. These techniques include Boundary Scan and using Boundary Scan to test surrounding non-scan parts, ICCT of passive analog component clusters, and testing 'through' series terminators. DFT techniques to optimize access during board layout serve to maximize coverage.