Design-for-Test Rules for Boundary Scan Test in In-Circuit Test for ODMs

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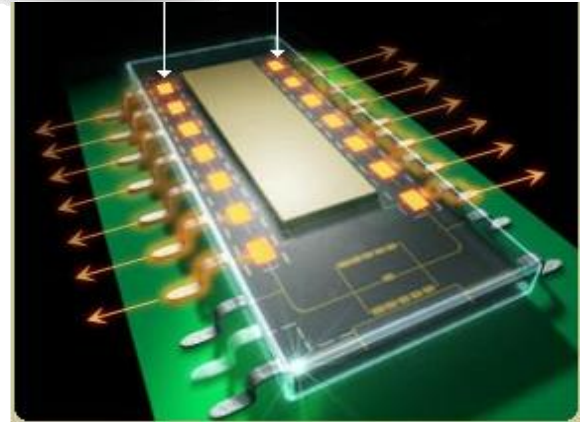

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Before Reading this Material

These Design-for-Test (DFT) rules were made based on our engineers' real-time experience on the production floor.

If some suggestions are not consistent with, or conflict with any current/new silicon technology, we recommend you to consult your silicon vendor first before making any final deployment decision.

If you have any questions, please contact Agilent for further clarification.

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DFT for Boundary Scan Test
Rule #1 TCK Pull-Down, TMS Pull-Up

Rule #1.1: Pull-down R for TCK.

Connect TCK through 100 Ohm resistor to Ground. For low voltage logic (< 1.5 V), the designer may use a 50 Ohm resistor.

Rule #1.2: Pull-Up R for TMS.

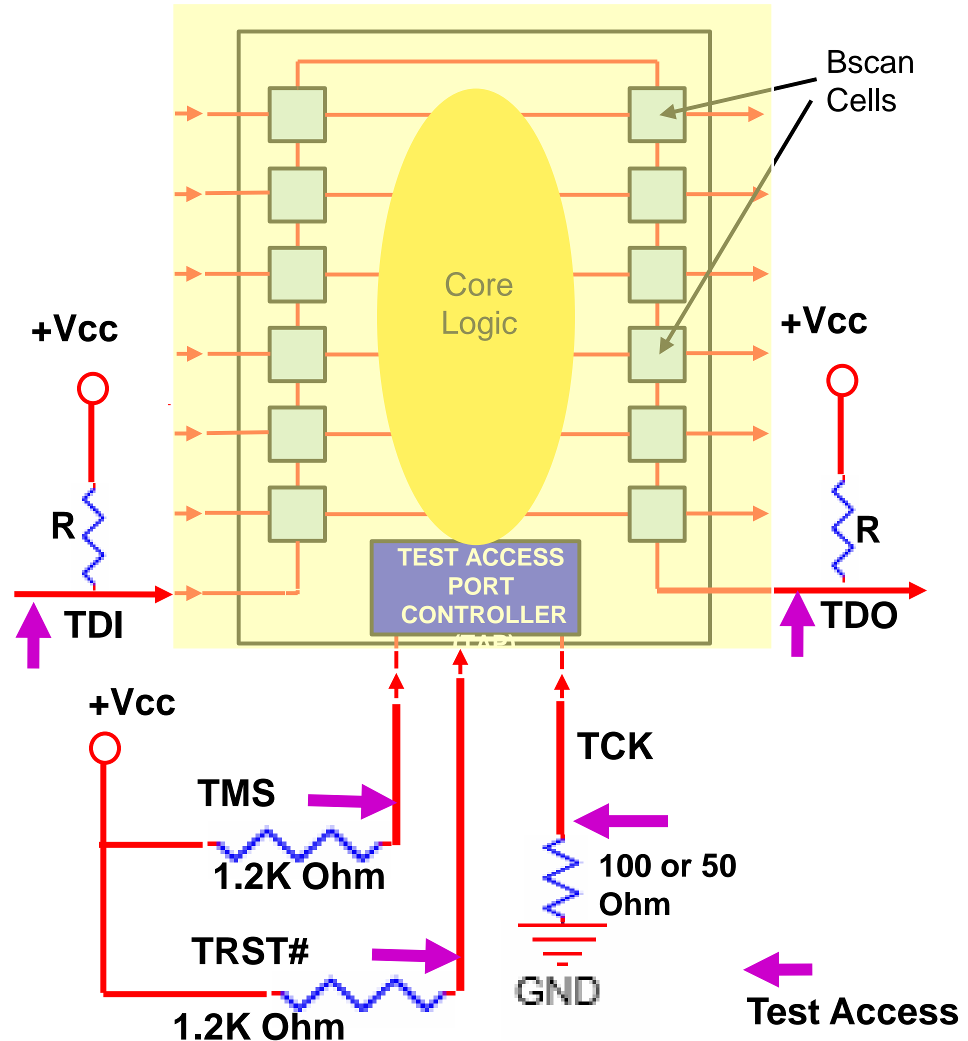
Connect TMS through 1.2K Ohm, pull up resistor to 'high'.

Note1: We also suggest properly pulling up the resistor to Vcc for both the TDI and TDO, so as to have a stable input and output signal. The resistor could be 100 or 50 Ohm as TCK. Other values, like several K Ohms, may apply.

Note 2: If TRST# is used here, a high R (like 1.2K or even higher) to Vcc can be used. Some ICs may require pull-down resistor. In that case, you need to keep the TRST# in high during boundary scan testing.

Note3 : You may reference the IC Design Document to see the exact resistor suggestion from the IC designer. Generally, the pull-up resistor is recommended for many ICs. But some will require a pull-down R instead. Be sure to reference the design-guide document..

Note4: You can consider to change the value of pull-up/down resistor here. The value of resistors may impact the overall power consumption. A lower value resistor requires stronger external driver capability. **Pay attention here when changing test platforms.**



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DFT for Boundary Scan Test
Rule #2 Chain Boundary Scan Devices in Order

Rule #2.1: TDO connects to TDI in serial

Connect the TDO of the 1st Boundary IC TDO to the TDI of the 2nd Boundary IC, 2nd IC's TDO to 3rd IC's TDI…etc.

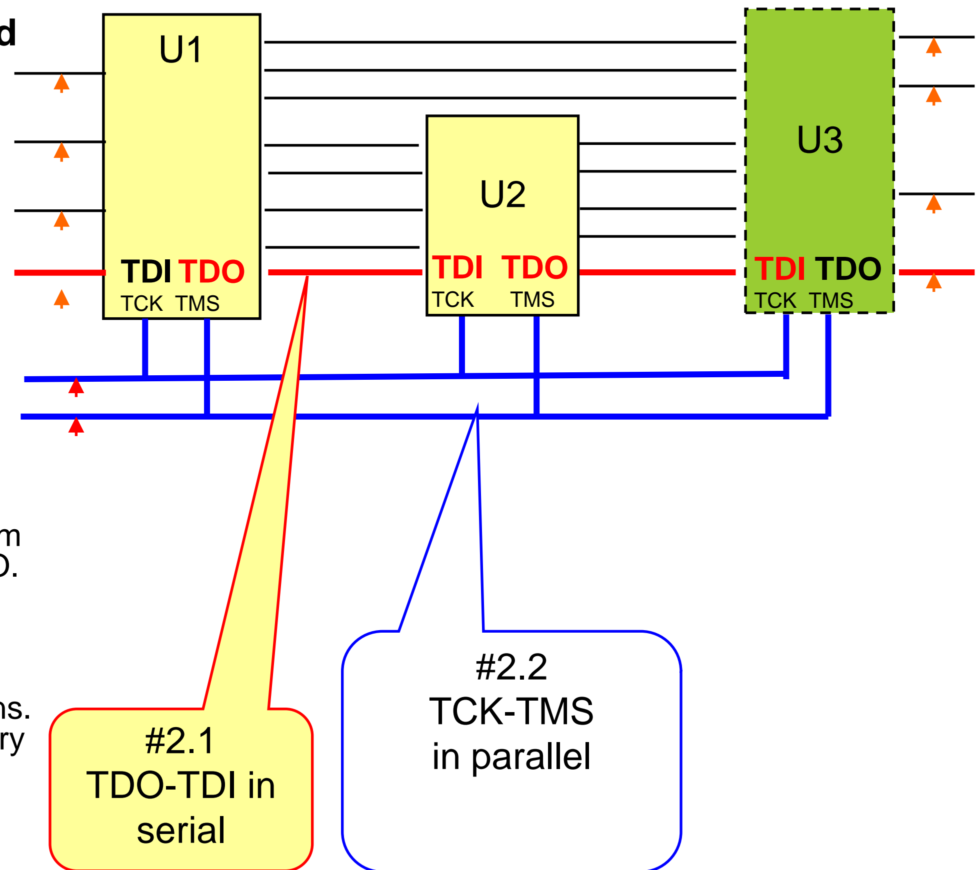
Rule #2.2: TCK , TMS connects in parallel

Connect all TCK and TMS in parallel.

Note1: In some cases, when the board designer has more flexibility in layout arrangement and if there is a new, unverified boundary IC, we suggest putting this IC at the end of the boundary scan chain.

Note2: For any IC, it's a good practice to keep TDI away from TDO to avoid possible "shorts" between the TDI/TDO. Board designers may consider to keep a proper distance under the overall space consideration.

Note3: If there are more ICs in the chain, the TCK and TMS propagation may not be effective as in fewer-IC-chains. In that case, you may consider putting a buffer circuitry for the TCK/TMS, so as to get better TCK/TMS synchronization.



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DFT for Boundary Scan Test
Rule #3 Level Shifter for Different Logic Levels

Rule #3.1: Test Access on EVERY TDI, TDO, TCK, TMS

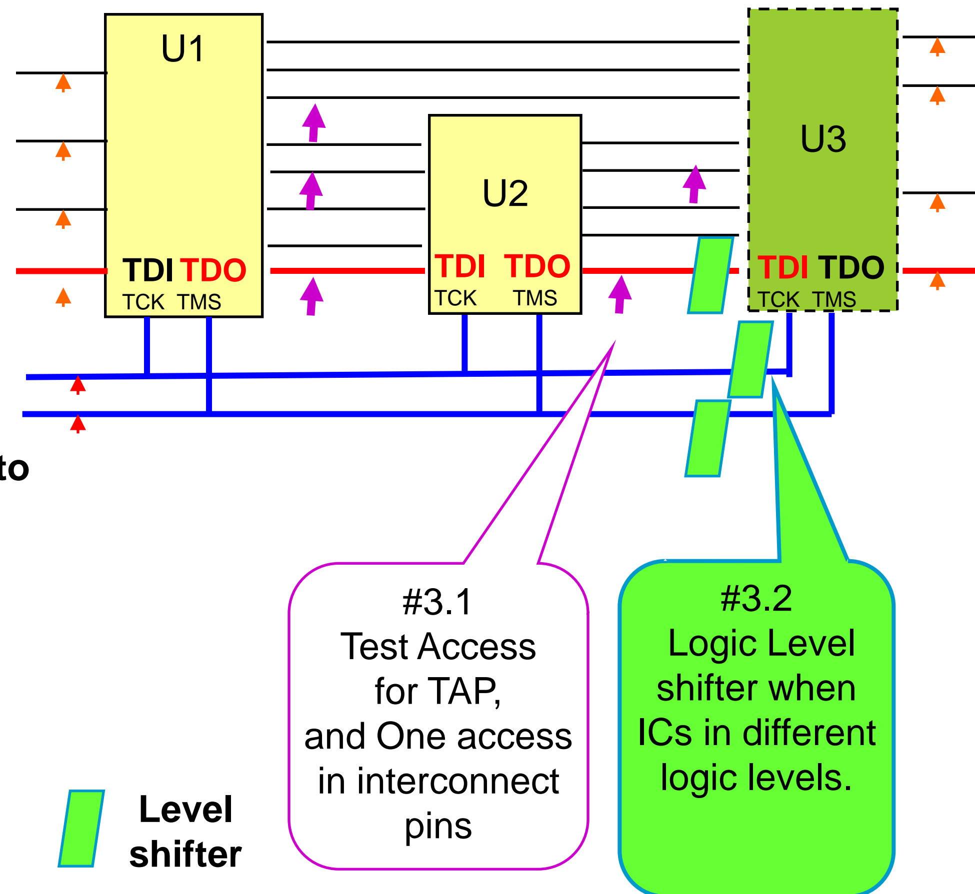
Test access on EVERY TDI, TDO, TCK, TMS and TRST if the IC has a TRST pin.

This is a MUST for debug-purpose.

If possible, set up one access at the interconnect pin. This can help you to understand the output signal situation when debugging the interconnect test.

Rule #3.2 : Check Logic Level of the IC

Put Level Shifter between ICs if the ICs operate at different logic levels. Don't forget to put the TAP (TDI, TDO, TMS, TCK) pins into the logic-level shifter



Note : When you have more than 3 ICs in the chain, you may consider putting jumpers in between the TDI and TDO pins of the ICs. This can help to bypass any non-functioning boundary scan IC, and still make the whole chain work.

If putting a jumper on the board is not allowed, the ICT engineer can put a GP relay or direct wiring inside the fixture to bypass the middle IC.

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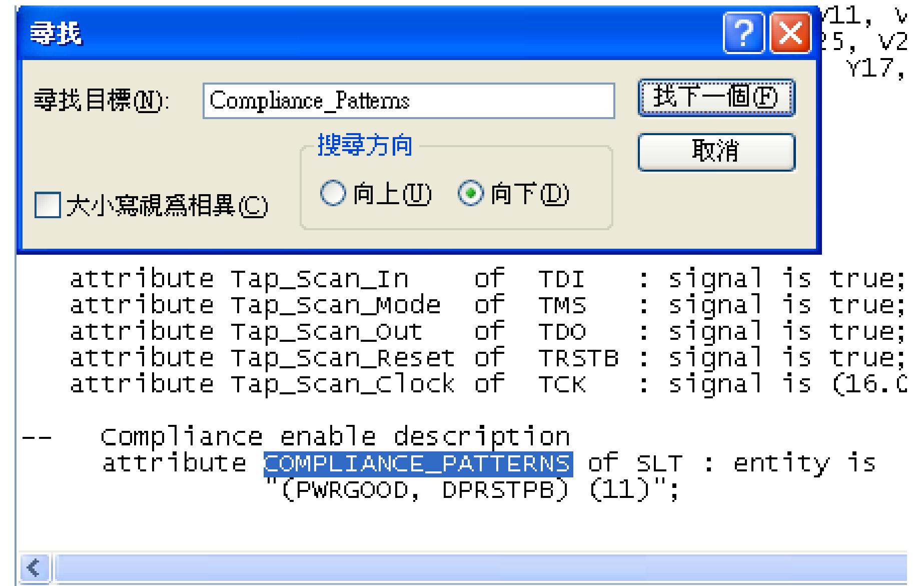
DFT for Boundary Scan Test
Rule #4 Additional Access from BSDL

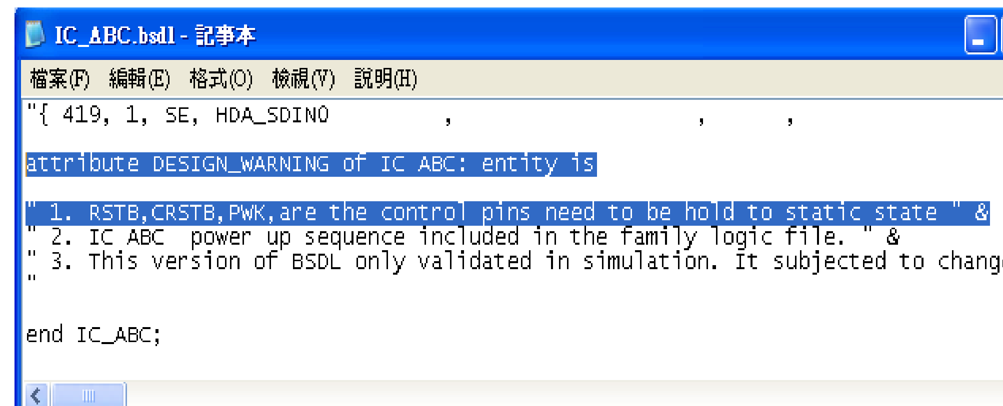


<u>Rule #4.1: Special Access for Compliance_Patterns from BSDL file</u>

Some ICs have special enabling pins, These pins can be found in BSDL file. Search "Compliance_Patterns" to see what pins need to be triggered to smoothly turn on the boundary scan mode.
In this example, The nodes:

PWRGOOD, DPRSTPB,

Need Test Access for keeping "high"



<u>Rule #4.2: Special requirements in DESIGN_WARNING message</u>

1149.1 allows the IC to have special notes in BSDL with DESIGN_WARNING message. You need to check this message to see whether there are special requirements.
In this example, this IC needs 3 pins to be controlled under Bscan mode.
The board designer will need to put test access for RSTB,CRSTB,PWK.

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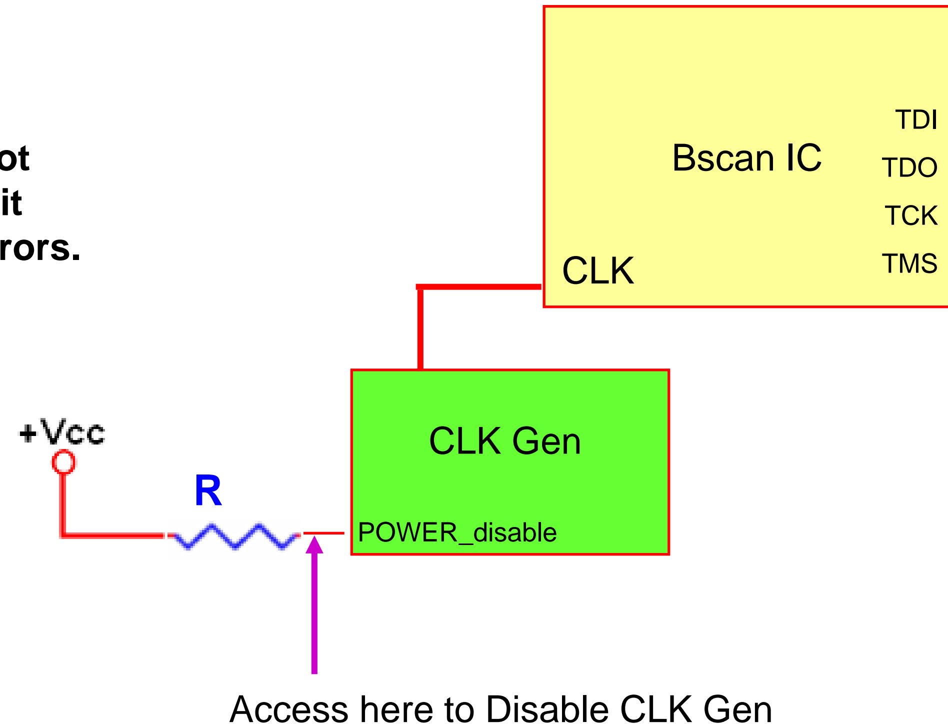
DFT for Boundary Scan Test
Rule #5 Access for Disabling Surrounding Devices

Rule #5: Access for Disabling Surrounding Device

Experience showed: Without disabling the surrounding devices, especially the CLK generator, the boundary IC sometimes cannot function under the boundary scan mode; or it may function with unstable/unpredictable errors.

Therefore, we recommend disabling the surrounding devices, especially the "Clock Generator".

For the disable pin, the designer needs to put a pull-up (or pull-down) resistor and a test access on it.



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DFT for Boundary Scan Test
Rule #6 Boundary Scan Access on Bottom-Side

Rule #6:Pull Boundary Scan Access on Bottom-Side of the Board

Put the TDI, TDO, TCK, TMS, TRST access on Bottom-Side of the board, so that these pins will be probed from the bottom part of the fixture.

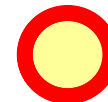
Due to shorter signal paths and not-through transfer-pins, probing from the bottom part of the fixture will have a better signal integrity, and more accurate for the probe to hit the test pad.

Experience showed: Probing TAP pins from bottom side, will result in a more stable boundary scan test.

In exceptional cases, some boundary scan validation "connectors" need to be on top side.

Not Probe from Upper Side

TDI TDO TCK TMS TRST



Probe from Bottom Side

NOTE: TAP access should be done using a test pad, Do NOT enable access through the via hole. Test Pad size should be at least > 30 mils; with 100 mils probe

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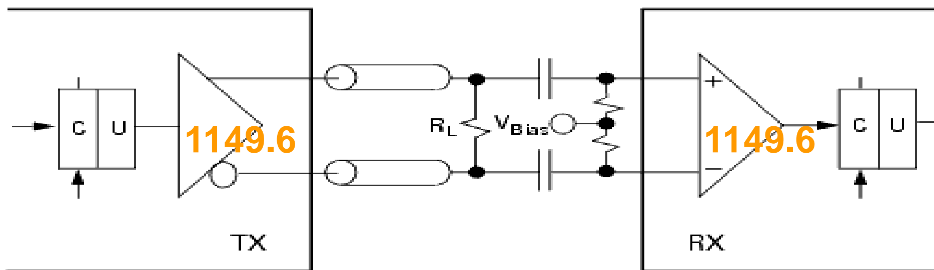
DFT for 1149.6 Boundary Scan Test
Rule#1-2 AC-Differential needs Dot6 at Both Ends

Rule#1 : Follow the previous Bscan DFT Rule#1-6

Rule#2 : When in AC differential Buses, make Sure 1149.6 links to 1149.6

When implementing an AC-differential signal boundary scan test, ensure that the silicon on the board is IEEE 1149.6 compliant, and that the 1149.6 cells link to 1149.6 cells. The boundary scan test will not work if you connect a 1149.1-only cell to a 1149.6 cell. However, if the Bus is DC differential, then, Dot6 to Dot1, or Dot1 to Dot1 can still be tested.

Note : Before developing a 1149.6 test, make sure the silicon and the BSDL file is a 1149.6 compliant device. The 1149.6 BSDL will have new instructions, like the example on the right.




```
use STD_1149_1_2001.all;
use STD_1149_6_2003.all;

attribute COMPONENT_CONFORMANCE of Scan90004 : entity is "STD_1149_1_2001"

attribute PIN_MAP of Scan90004 : entity is PHYSICAL_PIN_MAP;

attribute INSTRUCTION_OPCODE of Scan90004 : entity is

    "EXTEST         (000000010010),"&      --012
    "EXTEST_PULSE   (000000010110),"&      --016
    "EXTEST_TRAIN   (000000011110),"&      --01E
    "BYPASS         (111111111111),"&      --FFF
    "IDCODE         (000000000001),"&      --001
    "PRELOAD        (000000010000),"&      --010
    "SAMPLE         (000000010000),"&      --010
    "HIGHZ          (000000100000),"&      --020
    "CLAMP          (000001100000)";       --060

attribute REGISTER_ACCESS of Scan90004 : entity is
  "BOUNDARY (EXTEST, EXTEST_TRAIN, EXTEST_PULSE, SAMPLE, PRELOAD)," &
  "DEVICE_ID     (IDCODE)," &
  "BYPASS        (CLAMP, HIGHZ, BYPASS)" ;

attribute AIO_COMPONENT_CONFORMANCE of Scan90004 : entity is
  "STD_1149_6_2003";

attribute AIO_Pin_Behavior of Scan90004 : entity is
  "IN3p, IN2p, IN1p, IN0p : LP_time=10.0e-9 HP_time=1.0e-6;"&
  "OUT0p : AC_Select=12;"&
  "OUT1p : AC_Select=11;"&
  "OUT2p : AC_Select=10;"&
  "OUT3p : AC_Select=9";
```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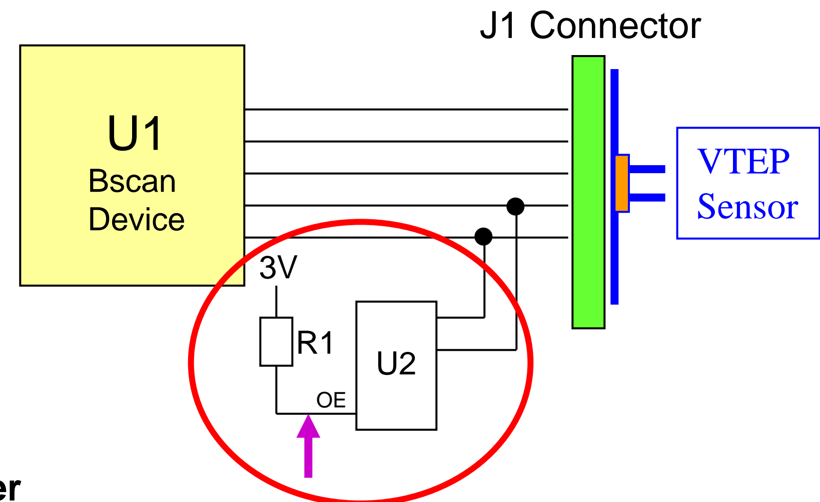
DFT for Cover-Extend Test
Rule#1-3 Ensure Boundary Scan Outputs to Connectors

Rule#1 : Follow the previous boundary scan DFT Rule #1-6

Rule#2: Access to Disable the Device in Between

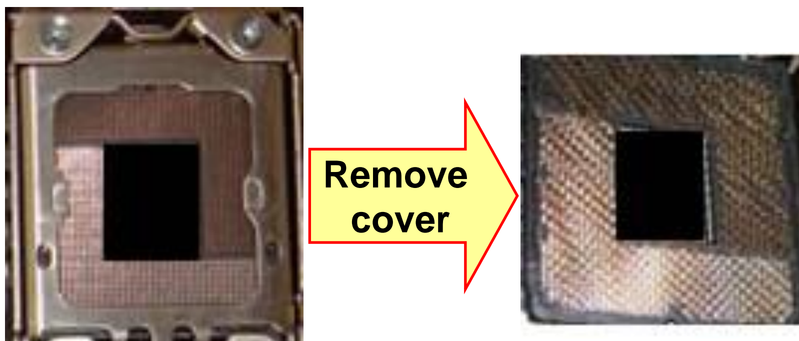
Disabling pins for non-boundary scan devices connected to both target connector and boundary scan device.



Access to disable the device in between

Rule#3: Remove metal cover on a connector

The Connector cannot be shielded with a metal cover



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DFT for Cover-Extend Test
Note: Check BSDL First

Note: Check BSDL

Check the BSDL file, to make sure the connector pins link to boundary scan cells which have output function.

Cover-Extend needs boundary scan cells to output the boundary scan signal to the connector as the VTEP stimulus. If the boundary scan cells are input-only cells, or 'no cell' (linkage), then we cannot perform Cover-Extend for these pins.
By simply checking whether the IC pins are output or input, we cannot tell whether the boundary scan cells are output or input cells. Sometimes, an output IC pin is equipped with an input boundary scan cell. Or an input IC pin equipped with an output boundary scan cell.

BSDL for CET .bsdl - 記事本

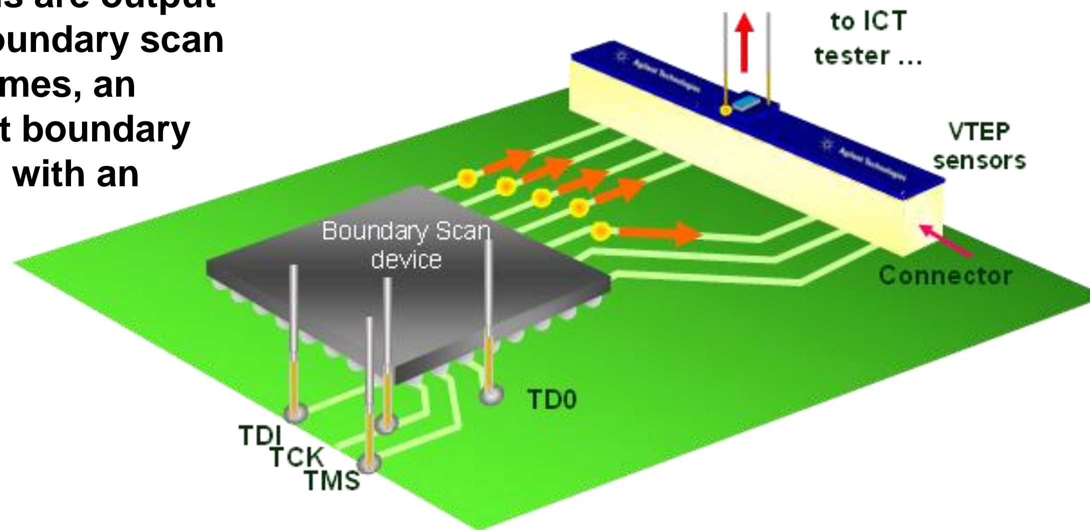
檔案(F) 編輯(E) 格式(O) 檢視(V) 說明(H)

```
h_db_63       : inout    bit;
h_db_62       : inout    bit;
h_db_61       : inout    bit;
h_db_60       : inout    bit;
h_db_59       : inout    bit;
h_db_58       : inout    bit;
h_db_57       : inout    bit;
h_db_56       : inout    bit;
h_dinvb_3     : inout    bit;
h_dstbpb_3    : inout    bit;
h_dstbnb_3    : inout    bit;
h_db_55       : inout    bit;
h_db_54       : inout    bit;
h_db_53       : inout    bit;
h_db_52       : inout    bit;
h_db_51       : inout    bit;
h_db_50       : inout    bit;
h_db_49       : inout    bit;
h_db_48       : inout    bit;
h_db_47       : inout    bit;
h_db_46       : inout    bit;
h_db_45       : inout    bit;
```

BSDL for CET .bsdl - 記事本

檔案(F) 編輯(E) 格式(O) 檢視(V) 說明(H)

```
vcclvds      : linkage
vccsdvo      : linkage
vcchda       : linkage
vcc5ref      : linkage
vccahpll     : linkage
vccdhpll     : linkage
```



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Online Resources

For more information on Agilent's suite of limited access test solutions, please visit the following websites:

www.agilent.com/find/boundaryscan

www.agilent.com/find/limitedaccess

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