Boundary Scan:

Technology Update

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Agilent Boundary Scan User Group Meeting
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Overview

- ASSET InterTech – Driving Embedded Instrumentation
  - Who are we?
- What are the problems with progressing technology?
- How are we trying to address them?
  - IBIST
  - Embedded Instruments
  - IEEE P1687
  - Processor-Controllerd Test
  - ScanWorks Integration to Agilent 3070 / i3070

Questions.
We provide open tools for embedded instrumentation for design validation, test, and debug:

- Boundary Scan (ScanWorks®)
- Processor Controlled Test (JTAG Emulation)
- High-Speed I/O Validation (Intel® IBIST)
- IJTAG (Core Silicon Instrumentation)

Historical roots from Texas Instruments (TI)

Technology leadership in Standards Committees:

- IEEE 1149.1, 1149.6, 1532, JEDEC/STAPL, SVF, SJTAG, PICMG, P1149.7 (MIPI), P1687, iNEMI
JTAG-Based Standards

Boundary Scan = JTAG = 1149.1 = 1149.4 = 1149.6
  • JTAG = Joint Test Action Group
  • .1 = the original (adopted 1990, last additions 2001-1c)
  • .2 = P1149.2 - Extended Digital Serial Subset (died in 1997 – actually Ken Parker says absorbed into .1)
  • .3 = P1149.3 – System Test Bus (died in ?)
  • .4 = Analog - Approved in 1997 but..
  • .5 = MTM – VME backplane - System (died in ?)
  • .6 = AC Extest – Approved in 2004

Compact JTAG IEEE-1149.7 (adopted Jan 2010)

IEEE 1532 = In-System Configuration (.isc files)

BIST – Built in Self Test (device specific)

IBIST – Interconnect BIST (Intel Proprietary)

IJTAG (IEEE-P1687)

SJTAG (Working group only at this time)

Processor - Controlled Test (JTAG, COP, XDP, Debug port)
The Goals of Test

I want the highest test coverage for the least cost!

Huh? Which one of those do you really want?
Interconnect speed advancements

- QuickPath Interconnect (6.4 Gb/s)
- 2nd gen PCI-Express (5-6.25 Gb/s)
  - 6Gb/s SATA III
  - 6.25Gb/s double XAUI
- AdvancedTCA (PICMG 3.x)
- VME320
- XAUI

3.125Gb/s

- RapidIO

2.5Gb/s

- 3GIO, PCI-Express

1.6Gb/s

- HyperTransport

1.5

- Flexbus 4
- POS-PHY L3/L4
- CSIX

1

- CoreConnect
- XAUI

6Gb/s

- PCI-X 66 & 100
- PCI 32/33 & 64/66

10Gb Ethernet

- VXS Backplane (VITA41)
- GigE Backplane (VITA 31.1)
- StarFabric Backplane (PICMG2.17)
- Serial Mesh Backplane (PICMG2.20)

5

- InfiniBand
- Fibre-Channel
- IEEE 1394
- Serial ATA
- USB
- SCSI

2

- CompactPCI
- 1Gb Ethernet

1.5

- VME
- 6.25Gb/s double XAUI

2

- CompactPCI
- 10Gb Ethernet

1
Stacked die – no probe access

Through-Silicon Vias

Die Level 3 - Analog
180 nm technology

Die Level 2 - Memory
65nm technology

Die Level 1 - Microprocessor
32 nm technology

Bond Wire
Benefits of JTAG based Access

Limited Physical Test Access

- High-speed serial I/O links above 5Gbps are not easily tested at the physical level using traditional test tools such as oscilloscopes, logic analyzers, and BERTs.
- Intel foresaw this issue on their next-generation 6.4 Gbps QuickPath Interconnect (QPI) for the Xeon processor 5500 series (codename Nehalem).
- PCIe Gen 2 runs at 5 Gbps
- PCIe Gen 3 runs at 8 Gbps

Using Test probe access can seriously degrade the signal (acting as antenna) in Gigahertz frequency band.
Intel IBIST toolset

- Intel IBIST is embedded IP within the Xeon 5500 platform which allows pattern generation & checking, margining, and BERT to be run via the JTAG / ITP port

- Concurrent testing supported
  - QPI tests can be run on all links in parallel
  - A huge time savings for BERT

- Multiple bus technologies can be tested concurrently (greatly reduces validation time)
  - QPI, PCIe, SMI
**IJTAG P1687 Statement of Scope**

This standard will develop a methodology for access to embedded test and debug features, (but not the features themselves) via the IEEE 1149.1 Test Access Port (TAP) and additional signals that may be required. The elements of the methodology include a description language for the characteristics of the features and for communication with the features, and requirements for interfacing to the features.
Embedded Instruments – examples

- Xilinx
  - ChipScope Pro – Virtual Instrumentation
- Synopsys
  - Embedded Instrument I/P
- Rambus
  - Programmable pseudo-random pattern generation
- Altera
  - Pre-emphasis and Equalization Link Estimator (PELE)
- Vitesse
- LogicVision
  - Embedded Serdes
Embedded Instruments - IEEE P1687

- **1149.1 Test Access Port (w/IJTAG in near future)**
- **Internal Scan Chains**
  - Configure Input Isolators
  - Crosstalk Generation
  - Configure Clock Chop Ratios
  - Configure Scan-In/Scan-Out Ports

- **IO BIST**
  - Bit Error Rate Test
  - Configure Tristate Bus Controllers

- **Logic BIST**
  - Configuration of MISRs and Final Compactors

- **Boundary-Scan Logic (IR, DRs, Controller, etc.)**

- **Memory BIST**
  - Configuration of Memory BISR
  - External Memory BISTs

- **Power Management & Clock Control**
  - Configure Pullup and Pulldown Resistors
  - Configure Input Pin Isolators
  - Configure Input Isolators
  - Configure Tristate Bus Controllers
  - Configure Internal Memory BISTs
  - Configure External Memory BISTs
  - Configuration of Memory BISR
  - Enabling/Disabling Memory Lock
  - IOBIST
  - Crosstalk Generation
  - Bit Error Rate Test

- **Chip Configuration**
  - Configure Access to Test Bus Interface
  - Configure Core Wrappers
  - Configure Scan-In/Scan-Out Ports
  - Configure Scan Dump Modes
  - Configure Core Instrument Interface
  - Configure Access to Test Bus
  - Configure Access to Test Bus

- **Core Wrappers**
  - Reduced Pin Count Modes

- **Current Test**
  - Configure 1500 Wrappers
  - Configure Reduced Pin Count Modes

- **HSIO BIST Engines**
- **Internal Scan Chains**
- **Memory BIST Engines**

- **O-Scope/LA**

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**Processor-Controlled Test**

- A means of controlling a CPU via JTAG / BDM / ITP port (emulation):
- Read/Write to all memory and I/O addresses at speed.
- Download and run test code or program files efficiently.
- Breakpoints and trace for Debug.
Processor-Controlled Test – why?

- Flash Programming is still too slow using boundary scan!
- I need to test all my peripheral device as well i.e. USB, LAN, RS232, Audio, Video.
- My DDR2/DDR3 devices only show real faults running at CPU at-speed.
- I don`t have Scan access to my CPU.
How it all comes together

Board Environment

- 1149.1 and 1149.6 for differential interconnects between devices on a board and to SerDes within a chip.
- BIST and IBIST to utilize built-in device self-test modules.
- Universal debug port for Processor-Controlled Test external to system and within a chip (i.e. ARM, Intel Atom, PPC)
- P1687 to correlate board and chip-level diagnostics at PVTF corners
Externally and Internally Integrated Medalist ICT Solutions – ASSET ScanWorks®

ScanWorks® Pod connects to UUTs

- For Medalist family with UNIX or PC controllers
- PC-based ScanWorks Manufacturing Station
- ScanWorks tests applied under control of Agilent Test Plan
- Simple API calls added to ICT test program

ScanWorks® PCI Card
UNIX linked PC with ScanWorks

Ethernet

Easy to setup and use. Ready for high-volume test.
Fully Integrated Medalist ICT Solution – ASSET ScanWorks®

• For 3070 family with PC controller
• Uses the high-performance ScanWorks PCI-400 controller card with four TAPs
• Seamlessly integrates Test Plan and ScanWorks automation features

Available exclusively from Agilent.
See http://www.home.agilent.com/upload/cmc_upload/All/59889707EN.pdf
One Environment for Embedded Instruments

Test

Validation

Debug

- Processor Controlled Test
- BIST Apps
- Logic Analysis
- Margining
- In-System Yield Loss
- Embedded Diagnostics
- Device Programming
- Shorts & Opens
- ScanWorks

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Questions?