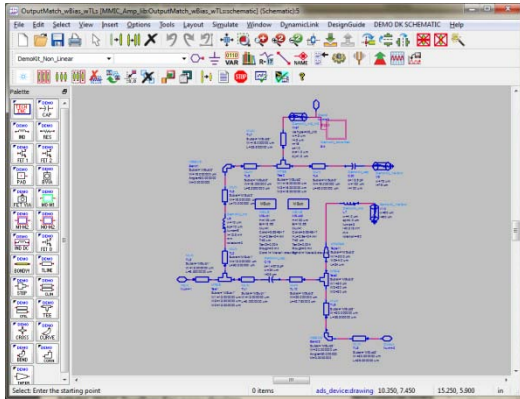
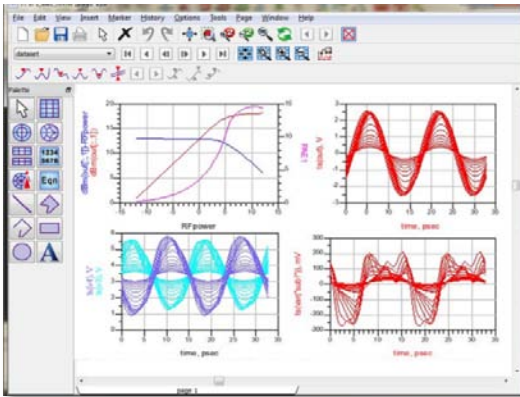


Schematic



Schematic example

Simulation

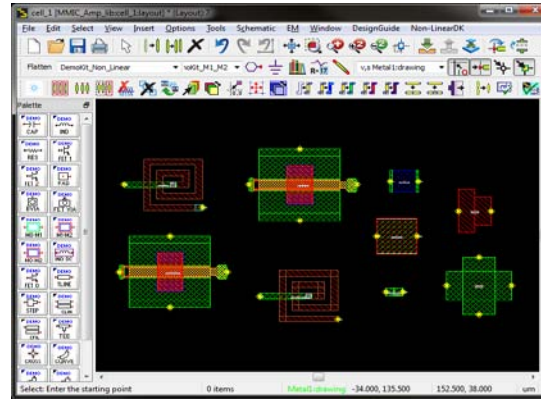


Simulation results

MMIC/RFIC Toolbar for easy design

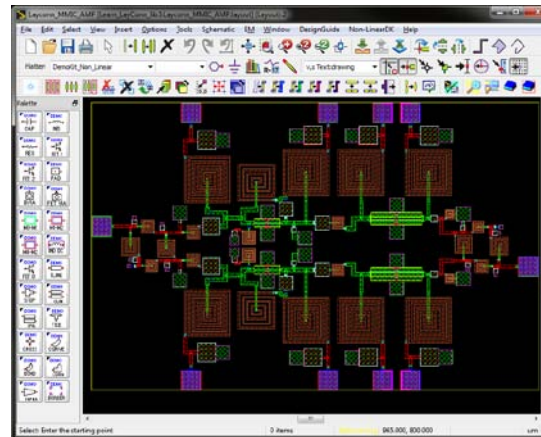


Parametric layout cells



Layout Pcells for CMOS, Passive and bipolar devices

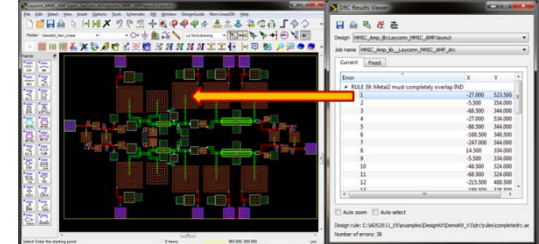
Layout



Microstrip lines

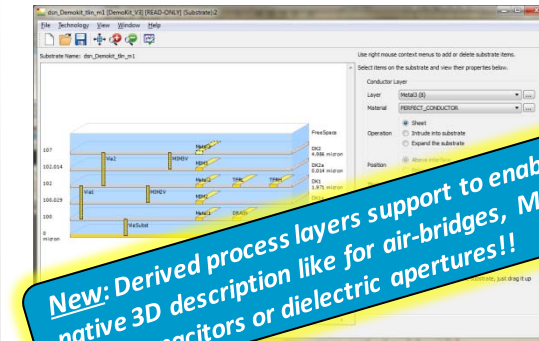


Design Rule Checks



DRC check covering most relevant foundry layout rules

Momentum & FEM stack-up files



New: Derived process layers support to enable native 3D description like for air-bridges, MIM capacitors or dielectric apertures!!

PDK features summary

PDKs enable a complete ADS based flow and typically include the following features:

- Schematic entry
- Simulation
- Momentum EM solver stack-up files
- Layout including PCells
- DRC/LVS Check
- Microstrip lines
- MMIC/RFIC Toolbar for easy design