The Do’s and Don’ts of High Speed Serial Design in FPGAs

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High Speed Digital Design & Validation Seminars 2013
Expanding Programmable Technology Leadership

- Committed to be First to Process Nodes
- Pioneering 3-D IC Technology
- Leading Edge Transceiver Technologies
- Programmable Analog/Mixed Signal
- System to IC Tools & IP to Enable Silicon

From Programmable Logic to Programmable System Integration
Agenda

▶ Overview
  – What are MGTs and where are they used?

▶ MGT architecture
  – PCS/PMA/PLL exposed

▶ Design Do’s and Don’ts
  – Clocking
  – Powering
  – Coupling and de-coupling
  – PCB

▶ Validation and verification options
  – Eye Scan
  – IBIS AMI

▶ Where next?
  – 28GBs and beyond

▶ Summary
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– PCS/PMA/PLL exposed

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Summary
MGTs
Multi Gigabit Transceivers

Multi-gigabit transceiver
From Wikipedia, the free encyclopedia
A Multi-Gigabit Transceiver (MGT) is a SerDes capable of operating at serial bit rates above 1 Gigabit/second. MGTs are used increasingly for data communications because they can run over longer distances, use fewer wires, and thus have lower costs than parallel interfaces with equivalent data throughput

» Primary function of the MGT is to transmit parallel data as stream of serial bits, and convert the serial bits it receives to parallel data.

» MGTs have become the 'data highways' for data processing systems that demand a high in/out raw data input and output

» MGTs must incorporate a number of additional technologies to allow them to operate at high line rates

» Common on FPGA - being especially well fitted for parallel data processing algorithms
7 Series Transceiver Roadmap - 40nm => 28nm

- **GTX**
  - Industry leading 28G with SSI for 100G/400G data path
  - 100GE, SONET/OTU, FC, Aurora, CPRI 19.6G

- **GTH**
  - Low power 13.1G for Wired OTU
  - Advanced DFE for challenging 10G backplanes

- **GTP**
  - High volume, low power, bare die flip chip and wire bond

- **GTZ**
  - Low cost Nx10G, PCIE Gen1/2/3, CPRI 9.8G, 10G Backplanes, 11G OTU/SONET,
Agenda

➤ Overview
  - What are MGTs and where are they used?

➤ MGT architecture
  - PCS/PMA/PLL review

➤ Design Do’s and Don’ts
  - Clocking
  - Powering
  - Coupling and de-coupling
  - PCB

➤ Validation and verification options
  - Eye Scan
  - IBIS AMI

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➤ Summary
7 Series Architecture
Device Layout

Transceivers in Quads
- 4 TX / 4 RX
- PLLs in shielded transceiver quads
- QPLL modelled as a separate block

Layout
- Arranged in columns on one or both sides of the chip.
- Virtex-7: full transceiver columns
- Kintex-7: mix Transceivers and IOs in the same column
- Artix-7: transceivers at top and bottom (wire bond chip)
PLL Structure: 7-GTX/GTH MGTs

- Function is to multiply a local low speed clock to a high speed Serdes clock with high quality

- Ring or LC tanks oscillators normally employed

- Virtex-7/Kintex-7
  - One dedicated Ring PLL per channel, local TX/RX only
  - Shared LC Tank PLL per Quad, drive ANY TX/RX

+ High Flexibility
+ Low Power
+ High Line Rates
– 7-GTH will have the best equalization capability in FPGA industry
  • Compensate reflection in long channels thus support tough 10G backplanes
– 7-GTX equalization is only second to 7-GTH in FPGA industry
  • Fully auto-adaptive DFE for easy link tuning
7 Series TX Driver Structure
With 3 Tap Emphasis

<table>
<thead>
<tr>
<th>7 Series Serdes</th>
<th>GTP</th>
<th>GTX</th>
<th>GTH</th>
<th>GTZ</th>
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<tbody>
<tr>
<td>Main Cursor</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>Post Cursor De-Emphasis</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Pre Cursor De-Emphasis</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<td>10G-KR Backplane TX</td>
<td>NA</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>
TX Emphasis to improve SI – operation review

Transmitted Pulses

Received Pulses

Amplitude

Time

Time
TX Emphasis to improve SI – operation review

Transmitted Pulses

Received Pulses

Amplitude

Time

Cursor
(tap #1)

Page 14

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TX Emphasis to improve SI – operation review

Transmitted Pulses

Received Pulses

Time

Amplitude

Cursor (tap #1)

Degraded Pulse

Time
TX Emphasis to improve SI – operation review

Transmitted Pulses

Received Pulses

Time

Amplitude

Cursor (tap #1)

Pre-cursor (tap #2)

Degraded Pulse
TX Emphasis to improve SI – operation review

Transmitted Pulses

Received Pulses

Amplitude

Time

Cursor (tap #1)

Pre-cursor (tap #2)

Degraded Pulse

Pre-cursor
TX Emphasis to improve SI – operation review

Transmitted Pulses

Received Pulses

Cursor (tap #1)

Degraded Pulse

Pre-cursor (tap #2)

Post-cursor (tap #3)

Pre-cursor
TX Emphasis to improve SI – operation review

Transmitted Pulses

- **Cursor** (tap #1)
- **Pre-cursor** (tap #2)
- **Post-cursor** (tap #3)

Received Pulses

- **Degraded Pulse**
- **Pre-cursor**
- **Post-cursor**
TX Emphasis to improve SI – operation review

Transmitted Pulses

- Cursor (tap #1)
- Cursor (composite)
- Pre-cursor (tap #2)
- Post-cursor (tap #3)

Received Pulses

- Degraded Pulse
- Pre-cursor
- Post-cursor
TX Emphasis to improve SI – operation review

Transmitted Pulses

- Transmitted Pulses
- Pre-cursor (tap #2)
- Cursor (composite)
- Post-cursor (tap #3)
- Cursor (tap #1)

Received Pulses

- Degraded Pulse
- Improved Pulse
- Pre-cursor
- Post-cursor

Amplitude

Time
Decision Feedback Equalization (DFE)

- A nonlinear equalizer that uses previous symbols to eliminate the Inter-Symbol-Interference (ISI) on current symbol.
  - The ISI on current symbol, caused by previous symbols, is subtracted by DFE.

\[
y(t) = u(t) + \sum_{i=1}^{n} w[i] \times y_d(t - i \times UI)
\]
CTLE vs DFE:

- **GTX**
  - Auto-adapting DFE makes difficult links easy to tune

- **GTH:**
  - +2 fixed, +4 sliding taps = better tuning on harder channels
  - Auto-adapting CTLE in DFE path

- **GTP/GTZ**
  - Auto-Adapting CTLE

- **So what? Auto-Adaptation.**
  - Hand tuning a DFE is HARD WORK, takes time and is unreliable.

Continuous Time Linear Equalizer (CTLE) response curve

Decision Feedback Equalizer (DFE) response
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  - Clocking
  - Powering
  - Coupling and de-coupling
  - PCB

- Validation and verification options
  - Eye Scan
  - IBIS AMI

- Where next?
  - 28GBs and beyond

- Summary
Traditionally we worry about ISI – see below

Today we also need to worry about reflections, noise and crosstalk

Signal amplitude at receiver

Receiver threshold

Time (1 bit per tick = 400 ps)

Received Signal (Distorted)
Jitter tolerance and generation

➢ CDR has two components: PLL and data sampler
➢ CDRs PLL produces a clock that tracks the average frequency and phase of the incoming data

Any signal integrity (power/board/clock) will add jitter which may reduce the jitter tolerance of the CDR introducing data errors
Do understand the MGT reference oscillator

MGTs have high speed wide bandwidth PLLs ~ 2 to 40MHz
Noise present on the reference oscillator will be present on the data and CDR
Time domain jitter can be estimated from phase noise – Rj is the ‘area under the curve’

Phase noise specifications

- Are understood by oscillator vendors – dBC/Hz
- Can be converted to rms jitter using conversion programs or spreadsheets
- RMS to peak-peak estimates can be made using an assumption of Gaussian noise distributions ie (10E-12 x14, 10E-15 x16)
- Direct effect on achievable BER

Need to be thinking in terms of ‘low ps’ rms jitter
Do control PSU ripple on MGT analog supplies

- ‘GOOD’ switching supply <5mV pk-pk noise ~ 0.2UI jitter

- ‘BAD’ switching supply ~20mV pk-pk noise >>> 0.32UI jitter
GT power supply options and requirements

GT power supply requirements <10mV pk-pk ripple requirement

- Generally left to user how this is achieved
  - Low noise switching supply (now used on the Xilinx char boards)
  - Traditional LDO scheme, easy but may be less efficient
- GTs generally don’t generate noise extra switching noise (unlike FPGA core and single ended IOs)
  - Have internal decoupling caps on GT rails
Decoupling Capacitors for MGT Power Rails

- On substrate caps significantly reduce requirements on traditional PCB caps

0.75” x 0.75” space of decoupling caps for transceivers per group on printed circuit board

Decoupling capacitors in 7 Series package substrates

AVTT & AVCC Caps
Power Integrity Simulation
XC7V485TFF1761 - Xilinx WP411

MGAVTT Impedance Profile

 Competitor PDN Result

 Virtex-7 with initial PCB Cap Recommendation

 Virtex-7 without PCB caps

Note: Lower is better

Table 2: Case 1 Capacitors

<table>
<thead>
<tr>
<th>QTY per Group</th>
<th>Capacitance (µF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MGTAVCC</td>
<td>MGTAVTT</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
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<tr>
<td>4</td>
<td>4</td>
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<tr>
<td>2</td>
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<tr>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

Table 3: Case 2 Capacitors

<table>
<thead>
<tr>
<th>QTY per Group</th>
<th>Capacitance (µF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MGTAVCC</td>
<td>MGTAVTT</td>
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<tr>
<td>0</td>
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<tr>
<td>0</td>
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</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

28 Caps per Group  ➔  0 Caps
PCB and layout considerations – stack up

- Ideal but can be difficult to achieve
  - Multiple power planes
    - VCCINT, VCCOs
  - Tracking congestion
    - I.e. SE buses DDR
  - Component placements
    - Decoupling and AC coupling caps
  - Data rate considerations
    - Via stubs
    - Stray capacitance

- Take care when routing signals near switching supply planes

Figure 5-11: Stackup for GTX Power and Signal Layers
Physical Description PCB Stackup – 28GB example

- 22 Layers
- HS signal layers: Panasonic Megtron6
- Other layers: ISOLA 370HR - FR4
- For Megtron6 and 370HR interleaved in lower layers for mechanical stability
- For economic reasons other layers are standard FR4 (ISOLA 370HR)
Manufacturability guidelines oppose best layout SI principles
Frequency and rise time review

- Faster edge speed = higher frequency content
- GT edge speeds increasing with each generation

Approximation $BW = \frac{0.34}{T_r}$ for $T_r(10-90)$ or $BW = \frac{0.23}{T_r}$ for $T_r(20-80)$
  - ‘High Speed Digital Design’ Howard Johnson

- Today’s 10Gbs transceivers have ~25ps rise/fall times
  - $BW = \sim 9$GHz

Means all GT transceiver PCB and layout needs considered as a high frequency design
PCB and layout considerations – o/c stubs

- Open circuit stub effects

Less effect for <3GBs
Should be considered for >10Gbs
PCB and layout considerations – differential vias

- **Differential vias**
  - Ground Signal Signal Ground via is good performer

- **Do consider via clearances**
  - PCB design defaults can be too capacitive for MGT data speeds

- **Field solving RL results**
  - L1 to L6 transition
  - L1 to L11 transition
  - > 20dB Sdd11 @ 5GHz
Physical Description Pin/Via Breakout

• Highspeed Signal Pin pad (Backdrilled)

• Standard Signal Pin pad (not Backdrilled)

• Ground Via (Not Backdrilled)

Vias
• 10 mil Drill
• 20 mil pad
• 28 mil anti-pad

Backdrill – 8 mils of target layer +/- 3mils
PCB and layout considerations - coupling

- **Crosstalk**
- **Track and plane proximity**
- **Signal coupling**
  - Near and far end
  - Adjacent tracks
  - Via and connector coupling
  - Use ground screening pins/vias
- **Power plane**
  - Signal contamination
  - High di/dt switching supplies
PCB and layout considerations – SMT pads

- Let's study with a 2D field solver
- Line
  - 5.2 mil wide over 3mil FR4 dielectric
  - L=288nH/m
  - C=116pF/m
  - Zo=50Ω
- Pad
  - 28mil wide over 3mil FR4
  - L=98nH/m
  - C=404pF/m
  - Zo=16Ω
- Pad is low impedance, too little inductance, too much capacitance
- Optimize by removing gnd place under pad
- Pull gnd plane 2.5mils back from either edge of trace
  - L=241nH/m
  - C=89pF/m
  - Zo=52Ω
- Recover 50 ohm by clearing ground plane

50 ohm track
SMT capacitor pad
Pad now 16 ohms Due to excess C
Recover 50 ohm by Clearing ground plane
PCB and layout considerations – SMT pads

- Better than 20dB (10X) improvement in return loss by clearing planes
PCB and layout considerations

➤ P&N length matching
  • Important and easy to maintain using jog outs

➤ Cut out under track
  • Will maintain exact impedance – however not usually needed
PCB and layout considerations – example layout

- P& N via reversal – MGT can reverse back
- Track coupling
- Ground vias moved to fit
- Arc corners nice but not essential
- Congestion due to thru hole
- Continuous ground plane desirable – no split planes
PCB and layout considerations – example

Example layout
Physical Description
PCB Layout – 28GBs breakout
PCB and layout considerations

Summary

– Good practices
  • Differential via construction
  • P&N length matching
  • Observing signal coupling
  • Keep ground plane continuity
  • Component pwr/gnd tracking vs direct connections (excess L)
  • Use suitable material and connectors

– At fast line rates (>10GBs) or where geometries become significant
  • Look at pad capacitance and clearing ground planes (excess C)
  • Consider effect of open circuit stubs on vias and connectors
  • PCB weave and skin loss effects - TBD

– Simulation can be useful
  • IBS-AMI, model extraction, field solving

*In heavily congested boards everything becomes a trade off*
DC vs AC coupling

External AC coupling
More tolerant of different technologies
Used on SFP, XFP, PCIe, SRIO etc….
Needs more work on layout and thought on data traffic to avoid pattern sensitivity (C values)

DC coupling
No DC balance needed
Better for SI – no vias to capacitors
Needs equivalent technology
Good for chip-chip
Needs careful consideration
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  - IBIS AMI /IBERT/Eye Scan

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Xilinx Transceiver IBIS-AMI modeling with ADS
Agilent and Xilinx working together

Simulating FPGA Power Integrity Using S-Parameter Models


The purpose of a Power Distribution Network (PDN) is to provide power to electrical devices in a system. Each device in a system not only has its own power requirements for its internal operation, but also a requirement for the input voltage fluctuation of that power rail. For Xilinx, Kintex-7 and Virtex-7 FPGAs, the analog power rails have an input voltage fluctuation requirement of not more than 10 mV peak-to-peak from the 10 kHz to the 80 MHz frequency range. The self-generated voltage fluctuation on the power rails is a function of frequency and can be described by Ohm’s Law: Voltage (frequency) = Current (frequency) * Self-impedance (frequency).

Thus, if the user determines the self-impedance (frequency) and knows the current (frequency) of the PDN, then the voltage (frequency) can be determined. The self-impedance (frequency) can easily be determined by simulating the frequency domain self-impedance profile of the PDN and is, thus, the subject of this white paper.
28Gb/s De-Embedding and Transceiver Characterization

DesignCon 2013

Tips and Advanced Techniques for Characterizing a 28 Gb/s Transceiver

Jack Carrel, Xilinx
Robert Sleigh, Agilent Technologies
Heidi Barnes, Agilent Technologies
Hoss Hakimi, Xilinx
Mike Resso, Agilent Technologies

Figure 3: DIRECT DUT measurement at the output of the fixture (top) vs. de-embedded signals showing what the 28 Gb/s signal would look like at the ball of the device (three lower waveforms).

<table>
<thead>
<tr>
<th>Description</th>
<th>32 Gb/s</th>
<th>64 Gb/s</th>
<th>Test Structure</th>
<th>Test Structure</th>
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</thead>
<tbody>
<tr>
<td>Rise Time (40-60% Labs)</td>
<td>13.44</td>
<td>13.44</td>
<td>Hybrid (40G)</td>
<td>Hybrid (40G)</td>
</tr>
<tr>
<td>Eye Opening (mV)</td>
<td>815.3</td>
<td>815.3</td>
<td>815.3</td>
<td>815.3</td>
</tr>
<tr>
<td>Eye Openness (dB)</td>
<td>3.19</td>
<td>3.19</td>
<td>3.19</td>
<td>3.19</td>
</tr>
</tbody>
</table>

Table 3: Key parameters as measured directly off of the fixture (top) versus de-embedded signals simulated at the balls of the device (44, 15, 76).
2D Eye Scan

- Parallel scan sampler in PMA
  - Post CTLE and DFE
- Non destructive
  - Full in service BER link margin
- Advanced PCS error measurement
  - Pattern analysis
Xilinx Virtex 13.1G Transceiver – VC7215

7 Series IBERT

* 24” Tyco backplane, prbs31, asynchronous links
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28nm FPGA with GTZ XCVR
7VH580T

VH580T GTZ TX
Eye Diagram: 28.05Gb/s

VH580T GTZ RX Eye Scan: 28.05Gb/s: Thru 12.5dB Trace

7VH580T Demo Video
Stacked Silicon Interconnect leadership

DesignCon 2012

Full System Channel Co-optimization for 28Gb/s SerDes FPGA Applications with Stacked Silicon Interconnect Technology

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Figure 14: The test bench used to test the channel of “TX silicon interposer => LTCC package => Megaroute PCB => LTCC package => RX silicon interposer” with 28 Gb/s data signaled with 3-tap FFE (at Tx side), CTE, and 3-tap DFE (at Rx side).

Figure 15. FPGA slice are bonded to a silicon interposer that provides high-bandwidth, low-latency interconnections through-silicon vias and Cu bumps enable connections to system I/O, power, clocks and other signals through the package substrate.

Figure 18. Simulated eye diagram and measured eye diagram comparison.
2013 OFC
Virtex-7 GTZ – 100GbE with CFP2

- 4x25.78G running **live Ethernet traffic**
- Interconnect with Fujitsu and Finisar Modules, plus Broadcom GearBox
- Another channel to check TX eye diagram
OIF Booth

12km of Fiber

Xilinx V7 H580T & Fujitsu CFP2
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Summary
Summary

- MGT Technology
- Reference oscillators
- Powering
- Layout
- Validation and verification
- Designing with 28GBs and beyond

Merci!

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Xilinx Technology Evolution

Programmable Logic Devices
Enables Programmable ‘Logic’

ALL Programmable Devices
Enables Programmable Systems ‘Integration’