Simulation for 3GPP LTE
From Concept-to-Test
Agenda

Mixed-Signal Design Challenges
Algorithm Design
RF Design
Mixed-Signal System Verification
R&D Hardware Testing
Summary
Mixed-Signal Challenges: System Design Tradeoffs

Mixed-Signal Application Examples:
• PAs (polar loop, DPD)
• Direct conversion receivers and A/D converters

Considerations:
• Sampling Rates
• Bitwidth
• Key Algorithms
• RF Gain, Linearity, NF
• Channel Impairments and Interferers
System Design Tradeoffs- Performance Budgeting

System Design Tradeoffs for EVM & BER/PER

With LTE having such high performance targets every part of the transmit and receive chain becomes critical to the link budget.

So how to decide the optimum balance?

Bits In → Coding Algorithms → D/A → Tx → A/D → Decoding Algorithms → Bits Out

- RF Upconverter/Downconverter
- LOs (Phase Noise)
- PA Nonlinearities
- Baseband HW Bitwidth
- Channel Compensation

With LTE having such high performance targets every part of the transmit and receive chain becomes critical to the link budget.

So how to decide the optimum balance?
System Design Flow Challenges

...several teams, disconnected tools
Agilent ESL Tools for Mixed Signal Design

SystemVue
Algorithm Design
System Architecture
Partition
Refine
Functional Design
Component Firmware Design
Component Verification
System Verification
Integrate
Verify
Prototype Verification
ADS
Production

Wireless Libraries
Agenda

Mixed-Signal Design Challenges

Algorithm Design

RF Design

Mixed-Signal System Verification

R&D Hardware Testing

Summary
SystemVue Algorithm and Fixed-Point Analysis

Evaluate fixed-point resolution on system performance in one summary table.
SystemVue HDL Code Generation

```vhdl
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
library work;
use work.pulse.all;

-- declare Modulator_OFDM entity
entity Modulator_OFDM is
  port
  (    
    Clock : in std_logic;
    In0  : in std_logic_vector(1 downto 0);
    In0Enable : in std_logic;
    Out0  : out std_logic_vector(17 downto 0);
    Out0_Rdy : out std_logic;
    RST : in std_logic
  );

-- end of entity Modulator_OFDM
end Modulator_OFDM;
```

SystemVue Example - LTE IQ Modulator

LTE IQ Data from ADS LTE Wireless Library

Export HDL with HDS

HDL Code

To ADS for HDL Co-Simulation
Agenda

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Summary
Agilent Advanced Design System for RF Design & Verification

**ADS Ptolemy Top Level**

**Simulated and real world signal inputs** → **Simulated and real world analysis**

**RF/Analog Subsystem**

**Transistor-level**

**RF sub-System Designer**

**RF Circuit Designer**

- ESG / MXG
- MXA
- PSA
- Infinium
- Logic Analyzer

**DC Power Analyzer**

**Infiniium Logic Analyzer**
ADS Example: RF Transmitter Design

LTE: Downlink Transmitter Example

Set UE Constellation Types for QPSK, 16QAM, or 64QAM

ADS LTE Downlink Source

ADS LTE Downlink EVM Measurement
Perform System-Level Design Tradeoffs for EVM

Trade-Off for EVM Budgeting:
- Bitwidth of RRC filter
- Phase noise of LO
- 1dB compression point of PA

- Bitwidth of RRC filter
- Phase noise of LO
- 1dB compression point of PA
Initial RF System Performance with Fixed-Pt RRC
LTE Downlink
Initial RF System Performance with Fixed-Pt RRC LTE Uplink

Constellation for First Data Frame

EVM vs SubFrame

<table>
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<tr>
<th>Frame</th>
<th>SubFrame</th>
<th>Data_EVM_Percent</th>
</tr>
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Averaged EVM

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RF Output Spectrum
LTE DL Receiver Design with Swept Phase Noise

Swept SNR

Swept Phase Noise

Parameter Sweep

Parameter Sweep

Sweep1

Sweep2

Sweep1: Start=0

Sweep2: Start=0

Sweep1: Stop=12

Sweep2: Stop=2

Sweep1: Step=4

Sweep2: Step=10

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3GPP LTE from Concept-to-Test

Agilent Restricted

March 2008
LTE DL Receiver Uncoded BER Results
UE 1 Set for QPSK, 16 QAM, and 64 QAM

Phase Noise Swept from -60 dBc/Hz to -80 dBc/Hz @ 10kHz offset

UE1: QPSK
UE1: 16 QAM
UE1: 64 QAM
Comparing Coded LTE BER vs. Uncoded LTE BER

Phase Noise Swept from -60 dBc/Hz to -80 dBc/Hz @ 10kHz offset

Receiver Uncoded vs. Coded BER Simulation Results
Comparing LTE and WiMAX™ BER
(Using same RF Receiver Design)

“WiMAX,” “Mobile WiMAX” and “WiMAX Forum” are trademarks of the WiMAX Forum®
Comparing Coded WiMAX BER to Coded LTE BER

Phase Noise Swept from -60 dBc/Hz to -80 dBc/Hz @ 10kHz offset

Receiver LTE Coded BER vs. WiMAX Coded BER Simulation Results

-60 dBc/Hz

-80 dBc/Hz

-70 dBc/Hz

WiMAX Coded BER (64QAM)

LTE Coded BER (64QAM)
Agenda

Mixed-Signal Design Challenges
Algorithm Design
RF Design
**Mixed-Signal System Verification**
R&D Hardware Testing
Summary
Agilent Advanced Design System for Baseband Verification

ADS Ptolemy Top Level

Simulated and real world signal inputs → Simulated and real world analysis

DSP Floating or Fixed Point

RTL HDL

Design → Verification

ESG / MXG → MXA → PSA → Infiniium → Logic Analyzer

DC Power Analyzer
• Support of leading hardware description languages
• Support for System-C
• Fixed point digital filter synthesis & verification
Conceptual: Using ADS Wireless Libraries for Algorithm Verification

ADS Wireless Libraries as an Independent Algorithm Reference

Reference Data Bits

Custom Algorithm

Compare Vectors at Each Stage Against Independent Reference

Custom Algorithm

Custom Algorithm

ADS Wireless Library 10010110 01110110
m-code 10010110 01110110
HDL code 10010110 01111110

Bit Reversal Detected!
Algorithm Reference Schematic:
Compare ADS CRC to FPGA HDL Code to m-code

ADS LTE Reference Algorithm

HDL Co-Simulation

MATLAB® Co-Simulation

Agilent Technologies
Algorithm Reference Results:
Compare ADS CRC to FPGA HDL Code to m-code

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</tbody>
</table>

No Errors Detected
Mixed-Signal System Verification Example:
LTE HDL Co-Simulation with RF Ckt Co-Simulation

SystemVue IQ Modulator with ADS
LTE IQ Data

HDL Generated with SystemVue HDS3

FPGA HDL Co-Simulation

RF Transmitter with Circuit Co-Simulation

FPGA Target

RF Amplifier
LTE IQ Mod HDL with RF Ckt Co-Sim Results

ADS-VSA Simulation Result
Includes Baseband & RF Impairments
Demo
Agenda

Mixed-Signal Design Challenges
Algorithm Design
RF Design
Mixed-Signal System Verification
R&D Hardware Testing
Summary
**BER: Example System Diagram**

Typical Double Conversion Transceiver

- **Transmitter**:
  - Baseband Coding
  - Modem Modulator
  - IF
  - PA

- **Receiver**:
  - RF
  - IF
  - Demodulator
  - Modem De-Coding

**BER Formula**:

\[
BER = \frac{\text{Errors}}{\text{Bits Sent}}
\]
Where can R&D BER Measurements be Performed?

Simulated Portion of System Design

**Simulated**

- Demodulator
- RF/IF BER
- A/D Converter
- Baseband De-Coding

Where

- MXG, ESG
- ADS, VSA SW
- MXA*, PSA

Step 1:
- Download Signal

Step 2:
- Capture Signal

*Note: Different Analyzer(s) may be used, dependent on required capture depth*
Where can R&D BER Measurements be Performed?

Simulated Portion of System Design

- Demodulator
- A/D Converter
- Baseband De-Coding
- IQ

Step 1: Download Signal
MXG, ESG

Step 2: Capture Signal
ADS, VSA SW

MXA*, PSA

*Note: Different Analyzer(s) may be used, dependent on required capture depth
Where can R&D BER Measurements be Performed?

Simulated Portion of System Design

MXG, ESG

Step 1
Download Signal

Step 2
Capture Signal

ADS, VSA SW

Logic Analyzer

RF/Digital IF BER

Demodulator

A/D Converter

Baseband De-Coding

I
Q

I
Q

I
Q

M(1)
Where can R&D BER Measurements be Performed?

Simulated Portion of System Design

MXG, ESG

Step 1
Download Signal

ADS, VSA SW

Step 2
Capture Signal

Logic Analyzer

RF/Digital IF BER

Baseband Demodulation and De-Coding
Where can R&D BER Measurements be Performed?

- **Baseband Encoding**
  - Simulated
  - Digital/Digital BER
  - ESG + N5102, or Logic Analyzer with Pattern Generator Board

- **Baseband De-Coding**
  - Simulated
  - Digital/Digital BER
  - Logic Analyzers

**Steps:**
1. **Download** Signal
2. **Capture** Signal
Mixed-Signal R&D Testing Example: ADS, ESG, LA, N6705A (Application Example- ADS not shipped with LA)

A/D Converter DUT

16822A Logic Analyzer

N6705 Power Supply

E4438C ESG

ESG
Test Setup Diagram

Download ADS LTE Signal via LAN

Event 1 Marker Out
Trigger In

ESG E4438C

30.72 MHz

ESG

14-Bit A/D
Converter Board (DUT)

16822 Logic
Analysis
System with
ADS SW
installed

USB-GPIB
Converter

N6705A DC Power Analyzer

+ 3.3V

+ 5V

ADS-Arb LTE Signal at 10 MHz IF

LAN Cable

Download ADS LTE Signal via LAN
ADS Schematic in Logic Analyzer
(Application Example- ADS not shipped with LA)

Agilent Technologies LTE Connected Solutions:
LTE Downlink Swept Bias Uncoded BER Measurement

**Work Bench**
- LTE_DL_MXG
  - Download_ADS_LTE_to_MXG
  - LTE_DL_LA_CS1
  - Capture_&_Analyze_LTE_with_LA
  - LTE_Set_N6705A_Bias_Voltage
  - Increment_N6705A_Bias_Voltage

**SEQUENCER**
- Sequeencer
  - Sequeencer1
  - TestBench[1]="Increment_N6705A_Bias_Voltage"
  - TestBench[2]="Download_ADS_LTE_to_MXG"

**PARAMETER SWEEP**
- ParamSweep
  - Sweep1
  - SweepVar="DUT_Bias_Voltage_Volts"
  - Start=4.3
  - Step=5
  - Step=0.7

**Mixe-Signal DUT**
LTE Measurement Results - Uplink

LTE Raw Bit Error Rate Results

<table>
<thead>
<tr>
<th>Index</th>
<th>BER</th>
<th>FER</th>
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<tbody>
<tr>
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<td>0.000</td>
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EVM vs SubFrame

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<th>SubFrame</th>
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Averaged EVM

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<td>5</td>
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LTE Measurement Results - Downlink

LTE Raw Bit Error Rate Results

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<th>FER</th>
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LTE Data Average EVM

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<th>Data_Avg_EVM_Perc</th>
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<tbody>
<tr>
<td>0</td>
<td>4.913</td>
</tr>
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</table>
LTE Measurement Results - Swept Downlink Uncoded BER

- 1% BER at approx. -56 dBm at +5V bias and at approx. -54 dBm at +4.3V bias
FPGA R&D Testing Example: ADS, MXA, LA (Application Example- ADS not shipped with LA or MXA)

*Note: FPGA Implemented with HDL shown in mixed-signal simulation; See appendix for FPGA implementation flow used
Summary

• Performed system-level design trade-offs vs. phase noise, bit width, PA non-linearities
• Compared and contrasted LTE uncoded BER vs. coded BER
• Compared and contrasted LTE DL OFDMA coded BER with WiMAX™ DL OFDMA coded BER
• Showed how to verify existing RF designs for compatibility with both LTE and WiMAX™ by using the ADS Wireless Libraries
• Combined simulation with test equipment to perform measurements on mixed-signal and FPGA hardware for R&D testing
Additional Information

Agilent LTE main site
www.agilent.com/find/lte

Webinar- Concepts of 3GPP LTE
http://www.techonline.com/learning/webinar/201801263

Webinar- Addressing the Design & Verification Challenges of LTE
http://www.techonline.com/learning/webinar/201802528

Webinar- Understanding SC-FDMA –The New LTE Uplink

Advanced Design System:
http://eesof.tm.agilent.com/products/e8895a-new.html
Appendix
FPGA Implementation and Test Flow

Software-Defined Instruments with ADS Installed (Custom Application Example-ADS not Shipped with Equipment)

Logic Analyzer With ADS
MXA Signal Analyzer with ADS
Infinium Scope with ADS
MXG/ESG

FPGA Target
Analogue and/or Digital
Dynamic Probe

HDL Code
Verify HDL Code with ADS + VSA SW
IQ Data

FPGA Synthesis Tool(s)

Run Simulation Inside of Instruments to Create Software-Defined Instruments
RF R&D Testing Example: ADS, MXG, MXA
(Application Example- ADS not shipped with MXA)

* Note: Different DUT than simulated amplifier used in case study
ADS Connected Solutions Schematic in MXA
(Application Example- ADS not shipped with MXA)

Agilent Technologies LTE Connected Solutions:
LTE Uplink EVM & Raw BER Measurement

Work Bench

LTE_UL_MXG
Download_ADS_LTE_to_MXG

Work Bench

LTE_UL_MXA_CS
Capture_&_Analyze_LTE_with_MXA

SEQUENCER

Sequencer
Sequencer1
TestBench[1]="Download_ADS_LTE_to_MXG"
TestBench[2]="Capture_&_Analyze_LTE_with_MXA"

VAR
VAR1
DUT_Input_Power_dBm=-10
DUT_Frequency_MHz=1950

RF
DUT
DUT Test Results: Swept-Power EVM

Error Vector Magnitude (%EVM) vs. RF Input Power (dBm)

- Downlink
- Uplink
DUT Test Results: Swept-Power Uncoded BER

DUT Raw Bit Error Rate (BER) vs. RF Input Power

*Note: Different Analyzer(s) may be used, dependent on required capture depth*
RF- RF/IF Test Equipment Configuration

Simulation
ADS 2008A Update Release 1 with Agilent Ptolemy Simulator (E8823)
ADS 3GPP LTE Wireless Library (E8895) OR
ADS Mobile WiMAX Wireless Library (E8869)

Signal Source
N5182A MXG with options:
- 506 (Freq. range 100kHz to 6 GHz)
- 652 (Internal BB generator 60 MSa/s, 8 MSa), or
- 654 (Internal BB generator 125 MSa/s, 8 MSa)
OR
E4438C ESG with options:
- 506 (6 GHz Freq. range)
- 602 (Internal BB generator 64MSa)

Signal Analyzer
89600 VSA Software (version 8.0 or later) with options:
- 105 (Dynamic link to ADS)
- BHD (LTE modulation analysis) OR
- B7Y (802.16 OFDMA modulation analysis)
N9020A MXA with options
- B25 (25 MHz bandwidth)
- 508 (Freq. range 20 Hz to 3.6 GHz)
OR
E4443A PSA with options
- 140 (40MHz bandwidth digitizer ) OR
- 122 ( 80MHz bandwidth digitizer, 128MSa capture depth)
RF- Baseband Test Equipment Configuration

Simulation
ADS 2008A Update Release 1 with Agilent Ptolemy Simulator (E8823)
ADS 3GPP LTE Wireless Library (E8895) OR
ADS Mobile WiMAX Wireless Library (E8869)

Signal Source
N5182A MXG with options:
- 506 (Freq. range 100kHz to 6 GHz)
- 652 (Internal BB generator 60 MSa/s, 8 MSa), or
- 654 (Internal BB generator 125 MSa/s, 8 MSa)
OR
E4438C ESG with options:
- 506 (6 GHz Freq. range)
- 602 (Internal BB generator 64MSa)

Signal Analyzer
89600 VSA Software (version 8.0 or later) with options:
- 105 (Dynamic link to ADS)
- BHD (LTE modulation analysis) OR
- B7Y (802.16 OFDMA modulation analysis)

16800 Series Logic Analyzer with option 032 (32 MSa capture depth)
OR
16900 Series Logic Analyzer with option 032 (32 MSa capture depth) or option 064 (64 MSa capture depth)