EMI/EMC Analysis for High Speed Digital Designs

HEESOO LEE
3D EM Technical Lead

JONATHAN CHEN
Applications Engineer

Sept 16th, 2014
Agenda

– Introduction to 3DEM
– EMI & EMC
– Solution for EMIC in EMPro
– EMIC Examples in EMPro
– Application Demo
– Examples of Improving Designs for Better EMI/EMC Performance
Introduction to 3D EM
Challenges in High Speed Digital Design

Signal Integrity, Power Integrity, and EMI/EMC

Signal Transmission Issues:
Attenuation, Reflection, Dispersion, Interference, Crosstalk

Power Delivery Issues:
Voltage Drop, Switching Noise, Crosstalk

Electromagnetic Compatibility Issues:
Near Field Coupling, Radiated Emissions

Trends in High Speed Digital Design

– Higher and Higher Bandwidth Requirements
  • 28/32Gbps SERDES
  • 100Gbit Ethernet

– Traditional design methodology starts to break down
  • Analyzing separately simulated PCB, vias, channel, and connectors as cascaded s-parameter blocks becomes questionable for accuracy
  • Need to carefully consider where to chop and what to remove, especially ground planes and vias

– Strong demand on full EM simulations due to design complexity, lack of circuit models, as well as accuracy
Re-cap of EM Technologies for HSD Applications
Common Numerical Analysis Techniques

FDTD (Finite Difference Time Domain)
FEM (Finite Element Method)
MoM (Method of Moment)

- 3D Arbitrary Structures
- Full Wave EM Simulation
- Direct, Iterative Solvers
- Frequency Domain EM
- Multiport simulation at no additional cost
- High Q

3D Planar structures
- Full Wave and Quasi-Static
- Dense & Compressed Solvers
- Frequency Domain
- Multiport simulation at no additional cost
- High Q

3D arbitrary structures
- Full Wave EM simulations
- Handles much larger and complex problems
- Time Domain EM
- Simulate full size cell phone antennas
- EM simulations per each port
- GPU based hardware acceleration
Keysight’s EM Technology Portfolio

**ADS**
- Common Database Integration
- ADS Layout Export

**EMPro**

**Momentum Simulator**
*Method of Moments*

**FEM Simulator**
*Finite Element Method*

**FDTD Simulator**
*Finite Difference Time Domain*
EMI (Electro Magnetic Interference) and EMC (Electro Magnetic Compatibility)
What is EMI and EMC?

- **Power Lines**
- **Signal Lines**

**Conducted**

- Source (Culprit, emitter)
- Transfer (Coupling Path)
- Receptor (Victim, Receiver)

**Radiated**

- Magnetic
- Electric
- Planewave

**Electromagnetic Interference (EMI):** Electromagnetic emissions from a device or system that interfere with the normal operation of another device or system. EMI is also referred to as Radio Frequency Interference (RFI).

**Electromagnetic Compatibility (EMC):** The ability of equipment or system to function satisfactorily in its Electromagnetic Environment (EME) without introducing intolerable electromagnetic disturbance to anything in that environment.

Graphic Source:
Radiation Mechanism

- Source: Near Fields on the device
- Radiation and Coupling Mechanisms
- Far Field Radiation

To have a problem the three following must be present:
- source or generator
- coupling path
- Radiating structure with $>\lambda/4$

Which gives the conclusion:
- Radiation below 300 MHz primarily from cables
- Radiation above 300 MHz is primarily from modules or coupling to cables
Solution for EMIC in EMPro
Types of EMI/EMC Problems Solved in EMPro

- EMI - Estimate emission level at specified distance and compare against EMI compliance (Limit)
- Near Field - Hotspot Analysis
- EMC Characterization (Immunity Test) with Plane Wave Excitation
- Coupling Analysis with S-parameter
Radiated Emission Calculation in EMPro

- Users can plot the radiated emissions at specified distance
  - From 2013.07, it is integrated to standard menu in “Create/Graph”
EMI Calculation with Custom Waveforms

- Emission level depends on the input (noise) sources
- Two ways to configure the inputs for EMI calculation in EMPro

**Standard sources in EMPro**
- Automatic
- Broadband
- Gaussian
- Gaussian Derivative
- Modulated Gaussian
- Sinusoid
- Step
- IEC 61000-4-2 ESD
- User Defined

**Custom (user defined) waveforms**
- Frequency and Time domain waveforms
- Reads CSV (Comma Separated Values) format
  - Measured data and ADS generated waveforms
EMI Overlay Limit in EMPro

EMI Compliances

- **EMI Compliances:** Conformance to the rules that control (un-intended) electromagnetic emissions
  
  - **USA:**
    - Federal Communications Commission (FCC)
    - Emissions only (Radiated & Conducted)
  
  - **Europe:**
    - EMC Directive 2004/108/EC
    - Emissions & Immunity (radiated & conducted)
    - Required for CE mark

- **Supported EMI Limits in EMPro**
  - FCC Part 15 Class A and B
  - CISPR 22 Class A and B
  - MIL-STD 461, ICNIRP
EMI Calculation in EMPro
Option 1* : Post-Processed

- Plot emission level vs. frequencies at discrete frequencies (faster sim)
  - Run broadband s-parameter and far field simulation, no transient far zone
  - Create or read the waveforms to excite sources
  - Run EMI Calculation Add-on and assign ports with corresponding waveforms
  - Plot (post-process) the E-field at the measuring angle with the specified distance such as 3 meters or 10 meters
  - Overlay EMI Limits to the result

* : Both FEM/FDTD Simulation
EMI Calculation in EMPro

Option 2*: Direct EMI Computation

- Plot emission level vs. frequencies like a real measurement (longer sim)
  
  - Create or read the waveforms to excite sources
  - Assign ports with corresponding waveforms
  - Set simulations the simulation for enough periods of excited waveforms with FDTD and enter steady state frequencies (the more the better for the # of frequencies)
  
  - Enable far zone sensors (only for measuring angles) and also set to collect transient far zone

  - Simulate
  - Plot the E-field at the measuring angle with the specified distance such as 3 meters or 10 meters
  - Overlay EMI Limits to the result

* : FDTD Simulation
EMIC Examples in EMPro
Does My Chassis Meet EMI Spec?

EMI/EMC

EMI Calculation: Predict Radiated Emission

E-field @ 2.235GHz

EMC Characterization: Freq dependency on the noise received on power plane

E-field @ 5.68GHz

Rack Mount Chassis with 4-layer PCB
How Much Common Signal Emission from USTP?

USTP (Unshielded Twisted Pair)

Long (~1.2 meter) USTP
Does Slot on Ground Plane Radiate?

Mixed Mode S-Parameters w/Slot and wo Slot

Differential Mode

Without Slot

With Slot

Common Mode

Keysight Technologies
USB 3.0 EMI Emission

Emission level at 3 meters with Both SS channel enabled
Application Demo
Examples of Improving Designs for Better EMI/EMC Performance
What is On-Board Self Jamming?

Modern Mobile Phone

Lots of on-board antennas/wireless modules!!

Source: H. Garbe, Upcoming EMC challenges, EMC Europe 2011, York
Background

- Design of multiple PCB antennas for mobile communications becomes very difficult task due to many sources of noise:
  - Skew, rise-fall time mismatch, delays
  - Reflections
  - Crosstalk
  - Delta-I noise
  - Direct Radiation

- The design task can be easier by adopting simulations early in pre-layout stage of PCB designs
Objectives

– In this example, the following was investigated:
  • What are the main noise sources on a PCB
  • How to reduce the noise coupling
  • How to make the communication link more immune to EMI problems

– Simulation tools that were used:
  • EMPro-FDTD (GPU acceleration!)
  • ADS-Schematic
Challenges in Designing PCB Antenna

- PCB antennas need to:
  - Be small in size
  - Work at multiple frequencies of interest (BT, GSM, GPS,…)
  - Have a high sensitivity because of the low signal levels that need to be successfully received

- PCB antennas rely heavily on ground planes:
  - Shape of ground plane affects antenna performance
  - Size of ground plane affects resonance frequencies

- This has important consequences wrt EMI:
  - ‘Antenna currents’ can spread over total ground plane
  - Unwanted noise coupling caused by overlapping antenna and trace return currents
Self-Jamming: Two-Way Issue!

- When antenna is receiving:
  - Antenna and RF circuitry needs to be able to process very small incoming signals
  - Any noise that is induced at antenna reduces the sensitivity of the receiving circuit
  - Watch out for coupling from digital interfaces to antenna!

- When antenna is transmitting:
  - Output power at antenna can be quite high (e.g. 2 Watt for GSM)
  - This means quite high voltages/currents at the antenna (e.g. 2 Watt ≈ 14 Volt over 50 Ohm)
  - Watch out for coupling from antenna to digital interfaces!
Where to Place Digital Interfaces?

- **Overlap between antenna and return currents is an indication of noise coupling**
- **Easily visualized with full-wave simulation tools**
Where to Place Digital Interfaces?

Coupling between Antenna and Traces

Pos 1: -35 dB
Pos 2: -45 dB
Pos 3: -40 dB
Current Distribution vs Frequency

@ Position 1
Time Domain: Traces to Antenna

Noise Induced at Antenna side due to activity on Digital Interface

Pos 1: 15 mV

Pos 2: 5 mV

Pos 3: 15 mV
Time Domain: Traces to Antenna

Noise Induced at Digital Interface due to transmitting Antenna (Max Power)
Current Distribution on Ground Plane with Slot

Antenna Currents

Return current on traces
Coupling on Ground Plane with Slot

About -20 dB

±15 dB increase in coupling!
Noise Levels on Ground Plane with Slot

Digital interfaces to antenna

Antenna to digital interfaces

>60 mV!
Current Distribution on Ground Plane with Ring

Antenna Currents

Return Current Trace
Coupling on Ground Plane with Ring

On average ±10 dB increase in coupling!

About -22 dB
Simulation on Real PCB

Time domain noise voltage (in V) at antenna port. Traces are excited with a pseudo-random bit sequence of 2Gbit/s
Key Learnings

– Coupling between the traces’ and antenna’s current paths is one of the main contributing factors of noise

– Hence, during the placement stage of components on the PCB, one has to carefully select the location where digital interfaces are placed

– Designs can be simulated and optimized by placing digital interface components outside regions of crowded current distribution and return path discontinuities

– Need to avoid any return current path discontinuities to prevent large current coupling

High Speed Digital Board - Vias

Inspection of Current Distribution indicates “hot-spots” around the area of layer transition

Large Radiation Emission
Antenna Gain is 5.2 dB
Isolating the Problem

Inspection of layout shows lack of GND stitching Vias
Taking Corrective Action

- Add more GND stitching Vias
- Change DP routing to Top layer and avoid Via-to-Via coupling
Improved EMIC Results

Surface Current “hot-spots” are gone with the addition of sufficient GND stitching Vias and Improved layer routing 😊

Much Smaller Radiation Emission
Antenna Gain is -41dB 😊
Typical Routing Mistakes

- Passing over Void
- Serpentine over Void
- Too close to the edge
- Trace ending with small corridor ref-plane and while being on the corridor, pass by two voids
Resources

- EMPro Homepage

- EMPro Application Center
  - http://edocs.soco.agilent.com/display/eesofapps/EM+Applications

- EMPro Forum

- Watch EEsof YouTube Videos:
  - https://www.youtube.com/user/AgilentEEsof